THE DATASHEET OF

OPA653IDBVR

Wideband, Fixed Gain, JFET-Input AMPLIFIER

Check for Samples: OPA653

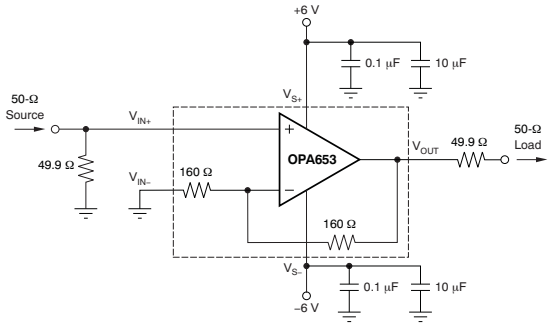
FEATURES

- **HIGH BANDWIDTH: 500 MHz (G = +2 V/V)**
- **HIGH SLEW RATE: 2675 V/µs (4-V Step)**
- **EXCELLENT THD: –71dBc at 10 MHz**
- **LOW INPUT VOLTAGE NOISE: 6.1 nV/√Hz**
- **FAST OVERDRIVE RECOVERY: 8 ns**
- **FAST SETTLING TIME (1% 4-V Step): 7.9 ns**
- **LOW INPUT OFFSET VOLTAGE: ±1 mV**
- **LOW INPUT BIAS CURRENT: ±10 pA**
- **HIGH INPUT IMPEDANCE: 10^{12} Ω||2.5 pF**
- **INTERNAL GAIN SETTING RESISTORS: G = +2 V/V or G = –1 V/V**
- **HIGH OUTPUT CURRENT: 70 mA**

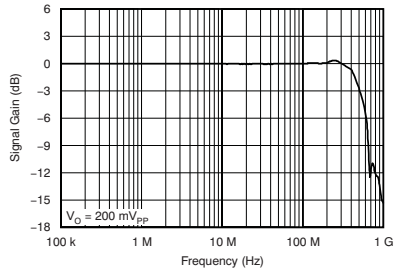
APPLICATIONS

- **TEST AND MEASUREMENT FRONT-END**
- **HIGH-INPUT IMPEDANCE PROBES**
- **DATA ACQUISITION CARDS**
- **OSCILLOSCOPE INPUT**
- **ADC INPUT AMPLIFIER**

NONINVERTING GAIN OF +2 V/V 50-Ω TEST ENVIRONMENT



SMALL-SIGNAL FREQUENCY RESPONSE



DESCRIPTION

The OPA653 combines a very wideband voltage-feedback operational amplifier with a JFET-input stage with internal gain setting resistors to achieve an ultra-high, dynamic-range amplifier for fixed gain of +2-V/V or –1-V/V applications.

The 500-MHz wide gain of +2-V/V bandwidth is complemented by a very high 2675-V/µs slew rate and fast settling time that make it ideal for time-domain and pulse-oriented applications.

Excellent –72-dBc THD distortion performance at 10 MHz makes the OPA653 an excellent choice for frequency-domain and FFT analysis applications.

Additionally, with the low 6.1-nV/√Hz voltage noise, low bias current, and high impedance JFET input, it supports very low noise, wideband, high input impedance applications. Examples include high-impedance probes, data acquisition cards, and oscilloscope front-ends.

RELATED OPERATIONAL AMPLIFIER PRODUCTS

DEVICE	V_S (V)	BW (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPA356	+5	200	300	5.80	Unity-Gain Stable CMOS
OPA656	±5	500	290	7	Unity-Gain Stable JFET-Input
OPA657	±5	350	700	4.8	Gain of +7 Stable JFET-Input
OPA659	±6	650	2550	8.9	Unity-Gain Stable JFET-Input
THS4631	±15	105	900	7	Unity-Gain Stable JFET-Input

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA653	SOT23-5	DBV	–40°C to +85°C	BZW	OPA653IDBVT	Tape and Reel, 250
					OPA653IDBVR	Tape and Reel, 3000
OPA653	VSON-8	DRB	–40°C to +85°C	OBEI	OPA653IDRBT	Tape and Reel, 250
					OPA653IDRBR	Tape and Reel, 3000

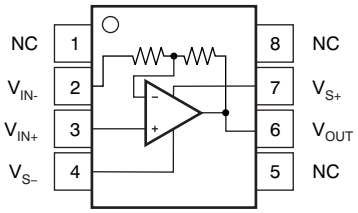
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

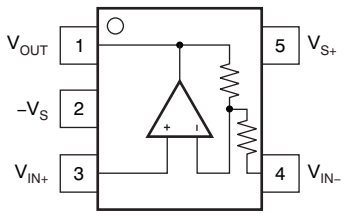
Over operating free-air temperature range (unless otherwise noted).

		OPA653	UNIT
Power Supply Voltage V_{S+} to $V_{S–}$		±6.5	V
Input Voltage		$\pm V_S$	V
Input Current		100	mA
Output Current		100	mA
Continuous Power Dissipation		See Thermal Characteristics	
Operating Free Air Temperature Range, T_A		–40 to +85	°C
Storage Temperature Range		–65 to +150	°C
Maximum Junction Temperature, T_J		+150	°C
Maximum Junction Temperature, T_J (continuous operation for long term reliability)		+125	°C
ESD Rating:	Human Body Model (HBM)	4000	V
	Charge Device Model (CDM)	1000	V
	Machine Model	200	V

DRB PACKAGE
VSON-8
(TOP VIEW)



DRV PACKAGE
SOT23-5
(TOP VIEW)



Note: NC: No connection.

ELECTRICAL CHARACTERISTICS: V_S = ±6 V

At G = +2 V/V, R_L = 100 Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA653 MIN	OPA653 TYP	OPA653 MAX	UNIT	TEST LEVEL (1)
AC PERFORMANCE						
Small-Signal Bandwidth	V_O = 200 mV_{PP}		500		MHz	C
Bandwidth for 0.1-dB Flatness	V_O = 2 V_{PP}		75		MHz	C
Large-Signal Bandwidth	V_O = 2 V_{PP}		475		MHz	B
Slew Rate	V_O = 4-V Step		2675		V/µs	B
Rise and Fall Time	V_O = 4-V Step		1.3		ns	C
Settling Time to 1%	V_O = 4-V Step		7.9		ns	C
Pulse Response Overshoot	V_O = 4-V Step		14		%	C
Harmonic Distortion	f = 10 MHz, V_O = 2 V_{PP}					
2nd harmonic			–72		dBc	C
3rd harmonic			–90		dBc	C
Intermodulation Distortion	V_O = 2-V_{PP} envelope (each tone 1 V_{PP}), f_1 = 10 MHz, f_2 = 11 MHz					
Second-order Intermodulation			–75		dBc	C
Third-order Intermodulation			–96		dBc	C
Input Voltage Noise	f > 100 kHz		6.1		nV/√Hz	C
Input Current Noise	f > 100 kHz		1.8		fA/√Hz	C
DC PERFORMANCE						
Gain Error	T_A = +25°C		±0.5	±1.25	%	A
	T_A = –40° C to +85°C		±0.6	±1.35	%	B
Internal R_F and R_G		140	160	180	Ω	A
Open-Loop Voltage Gain (A_{OL}) (2)			62		dB	C
Input Offset Voltage	T_A = +25°C, V_{CM} = 0 V		±1	±5	mV	A
	T_A = –40°C to +85°C, V_{CM} = 0 V DRB package		±1.5	±7	mV	B
	T_A = –40°C to +85°C, V_{CM} = 0 V DBV package		±1.5	±8.9	mV	B
Average input offset voltage drift	T_A = –40°C to +85°C, V_{CM} = 0 V DRB package		±10	±30	µV/°C	B
	T_A = –40°C to +85°C, V_{CM} = 0 V DBV package		±10	±60	µV/°C	B
Input Bias Current, Noninverting input	T_A = +25°C, V_{CM} = 0 V		±10	±50	pA	A
	T_A = 0°C to + 70°C, V_{CM} = 0 V		±240	±1200	pA	B
	T_A = –40°C to +85°C, V_{CM} = 0 V		±640	±3200	pA	B
Average input bias current drift, noninverting input	T_A = 0°C to +70°C, V_{CM} = 0 V		±5	±26	pA/°C	B
	T_A = –40°C to +85°C, V_{CM} = 0 V		±7	±34	pA/°C	B
INPUT						
Input Voltage Range	V_{IN+} = $V_{IN–}$		±3.5		V	C
Noninverting Input Impedance			10^{12} 2.5		Ω pF	C
OUTPUT						
Output Voltage Swing	T_A = +25°C, No load	±4.35	±4.45		V	A
	T_A = +25°C, R_L = 100 Ω	±3.2	±3.6		V	A
Output Voltage Swing	T_A = –40°C to +85°C, No load	±4.2	±4.3		V	B
	T_A = –40°C to +85°C, R_L = 100 Ω	±3.07	±3.2		V	B
Output Current, Sourcing, Sinking	T_A = +25°C	±60	±70		mA	A
	T_A = –40°C to +85°C	±56	±66		mA	B
Closed-Loop Output Impedance	f = 100 kHz		0.16		Ω	C

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Open loop gain is for informational use only. Open loop gain is from simulation and not measured in a closed-loop amplifier.

ELECTRICAL CHARACTERISTICS: V_S = ±6 V (continued)

At G = +2 V/V, R_L = 100 Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA653			UNIT	TEST LEVEL (1)
		MIN	TYP	MAX		
POWER SUPPLY						
Specified Operating Voltage	T_A = –40°C to +85°C	±3.5	±6	±6.5	V	B
Quiescent Current	T_A = +25°C	30.5	32	33.5	mA	A
	T_A = –40°C to +85°C	28.3		35.7	mA	B
Power-Supply Rejection Ratio	T_A = +25°C, ±V_S = 5.5 V to 6.5 V	62	66		dB	A
	T_A = –40°C to +85°C, ±V_S = 5.5 V to 6.5 V	60	64		dB	B
THERMAL CHARACTERISTICS						
Specified Operating Range DBV and DRB Packages		–40		+85	°C	C
Thermal Resistance, θ_{JA}	Junction-to-ambient					
DBV SOT23-5			105		°C/W	C
DRB VSON-8			55		°C/W	C

TYPICAL CHARACTERISTICS

Table of Graphs

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Input-Referred Voltage and Current Noise Spectral Density		Figure 4
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Inverting Transient Response	0.5-V Step	Figure 6
Harmonic Distortion vs Frequency		Figure 7, Figure 8
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Harmonic Distortion vs Output Voltage		Figure 10
Harmonic Distortion vs ±Supply Voltage		Figure 11
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Output Voltage Swing vs R_{LOAD}		Figure 20

TYPICAL CHARACTERISTICS: V_S = ±6 V

At G = +2 V/V, R_L = 100 Ω, and T_A = +25°C, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE (V_O = 200 mV_{PP})

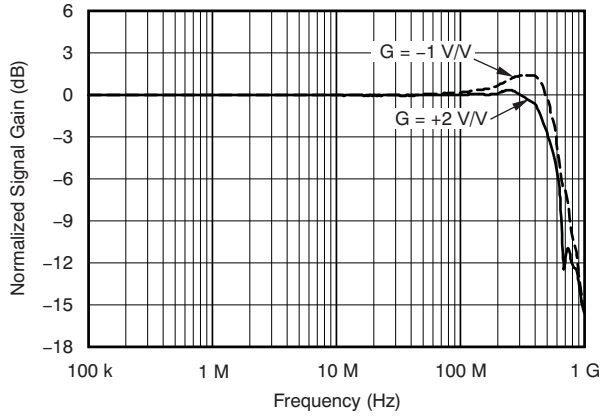

Figure 1.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

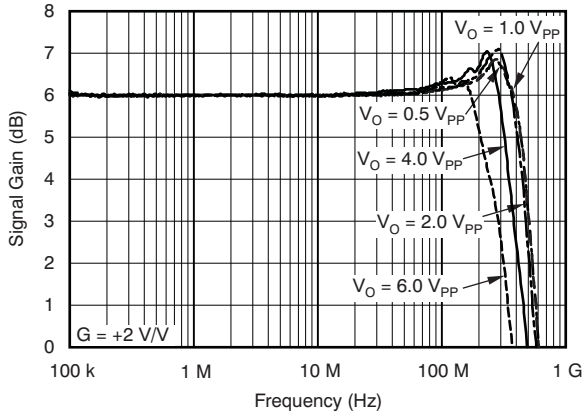

Figure 2.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

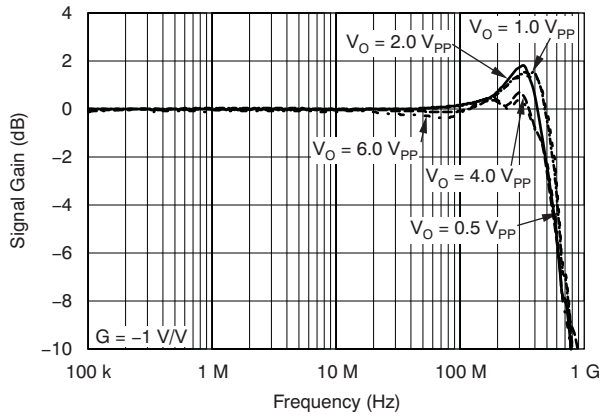

Figure 3.

INPUT-REFERRED VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY

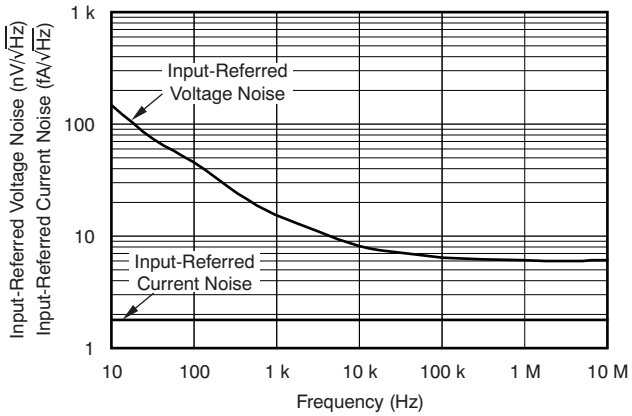

Figure 4.

NONINVERTING TRANSIENT RESPONSE

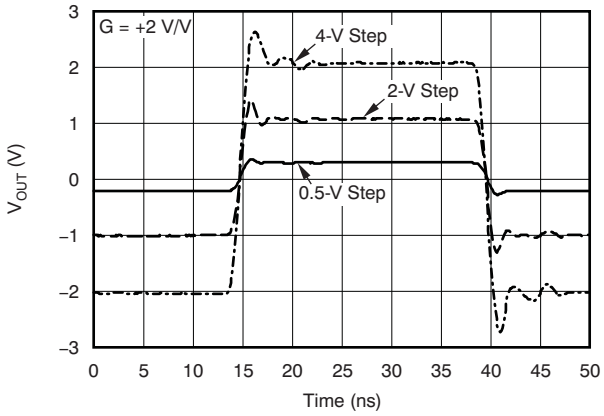

Figure 5.

INVERTING TRANSIENT RESPONSE

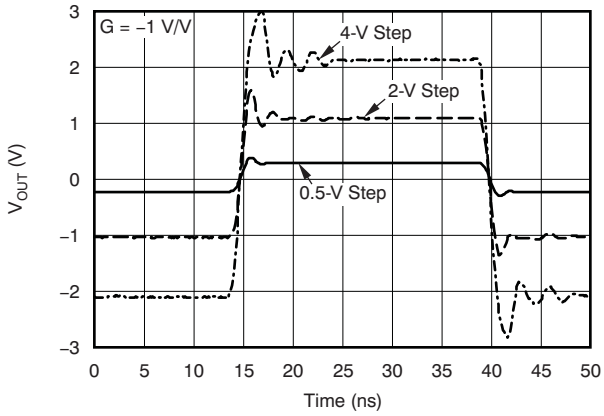

Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±6 V (continued)

At G = +2 V/V, R_L = 100 Ω, and T_A = +25°C, unless otherwise noted.

NONINVERTING HARMONIC DISTORTION vs FREQUENCY

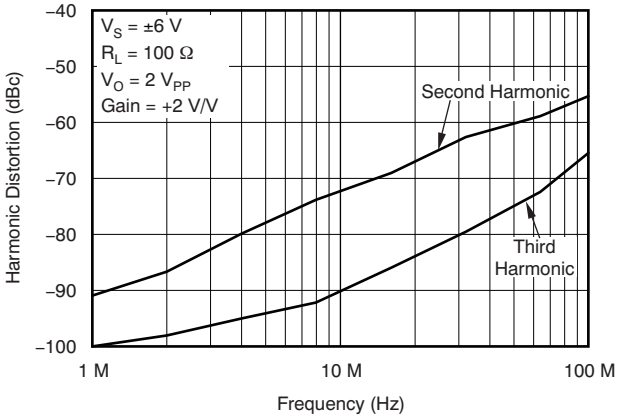

Figure 7.

INVERTING HARMONIC DISTORTION vs FREQUENCY

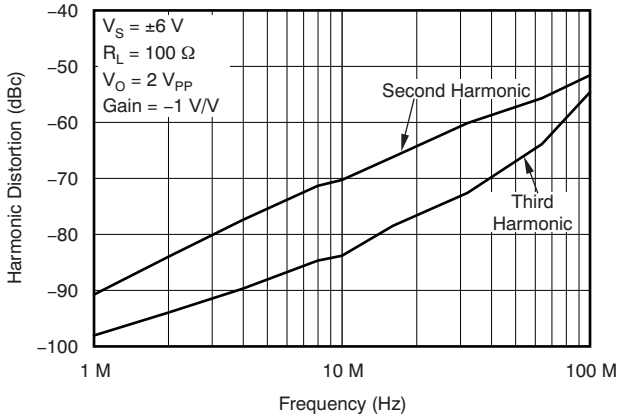

Figure 8.

HARMONIC DISTORTION vs LOAD

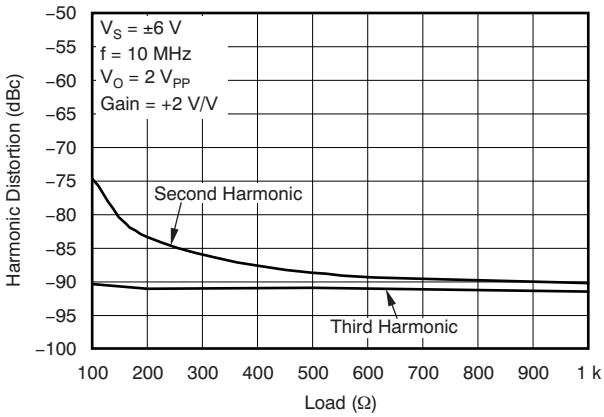

Figure 9.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

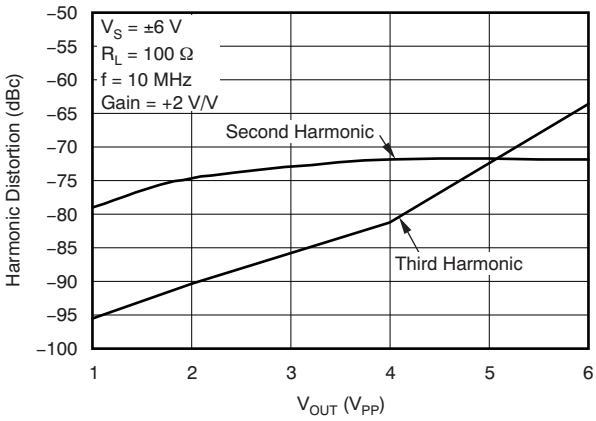

Figure 10.

HARMONIC DISTORTION vs $\pm V_{SUPPLY}$ VOLTAGE

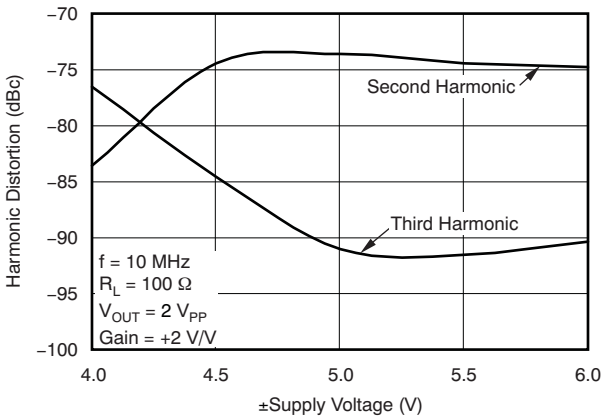

Figure 11.

TWO-TONE INTERMODULATION DISTORTION vs FREQUENCY

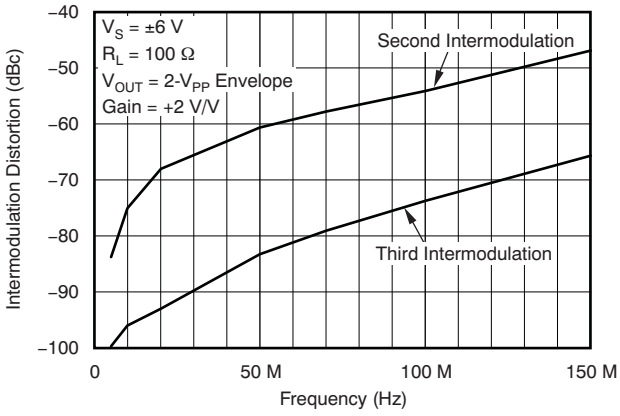

Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±6 V (continued)

At G = +2 V/V, R_L = 100 Ω, and T_A = +25°C, unless otherwise noted.

NONINVERTING OVERDRIVE RECOVERY (GAIN = +2V/V)

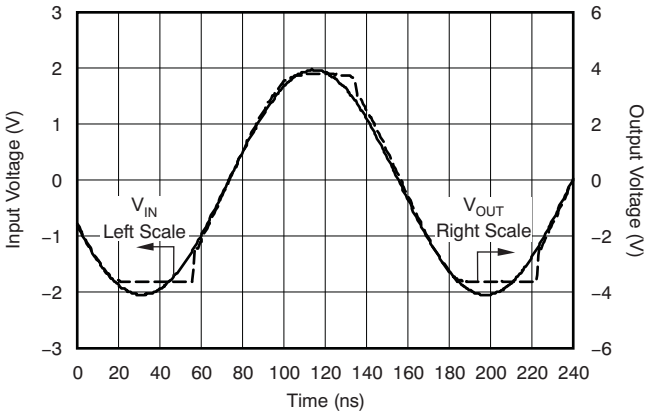

Figure 13.

INVERTING OVERDRIVE RECOVERY (GAIN = –1V/V)

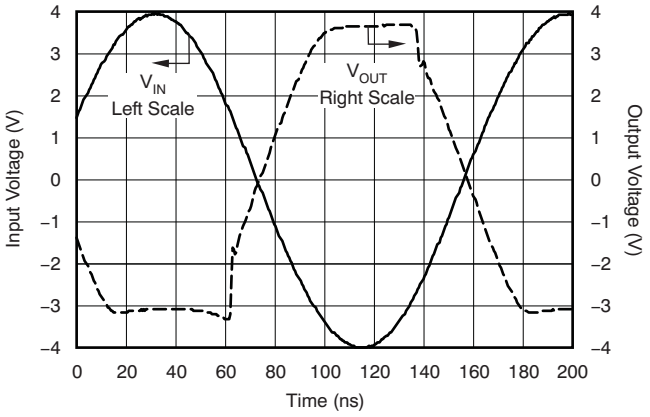

Figure 14.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

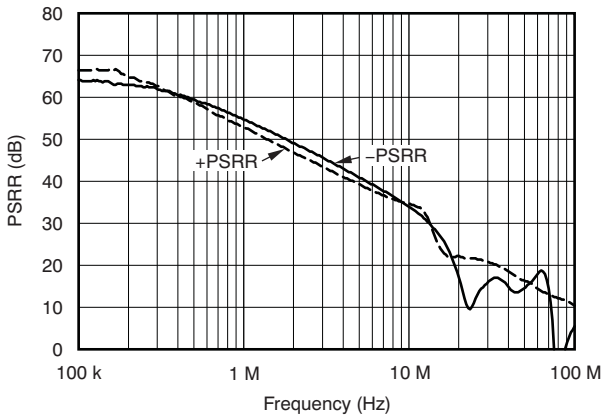

Figure 15.

FREQUENCY RESPONSE vs C_{LOAD} (R_{LOAD} = 1 kΩ)

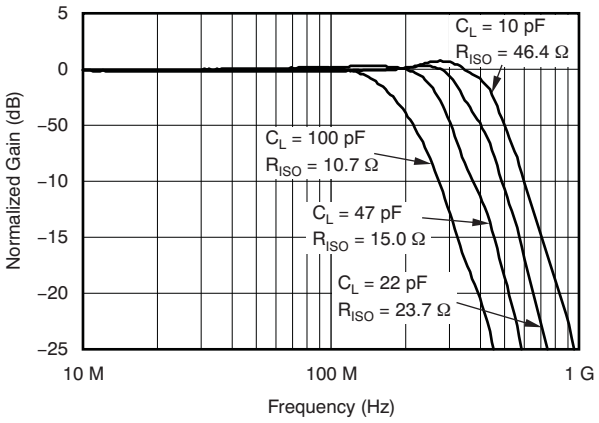

Figure 16.

R_{ISO} vs C_{LOAD} (R_{LOAD} = 1 kΩ)

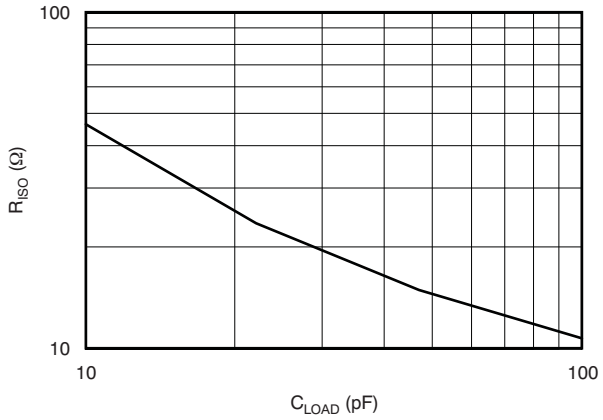

Figure 17.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

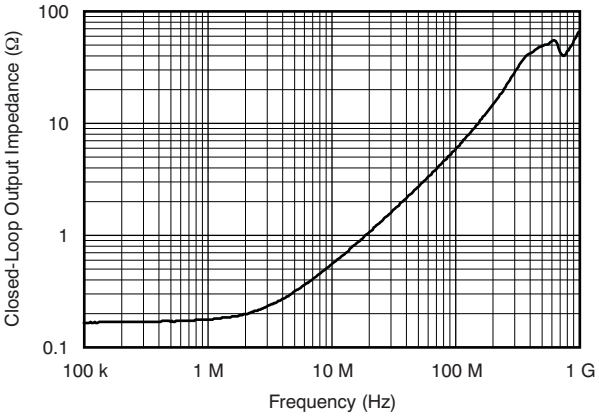

Figure 18.

TYPICAL CHARACTERISTICS: V_S = ±6 V (continued)

At G = +2 V/V, R_L = 100 Ω, and T_A = +25°C, unless otherwise noted.

SLEW RATE vs V_{OUT} STEP

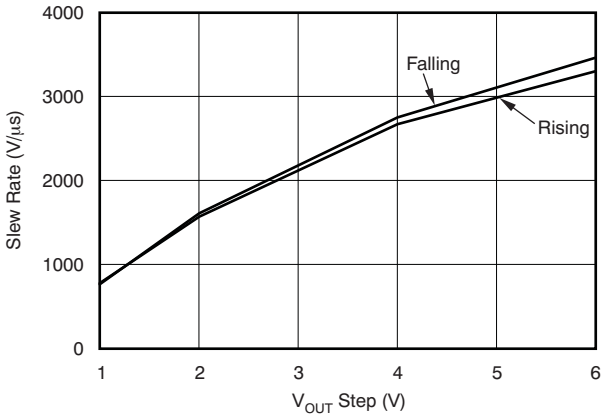

Figure 19.

OUTPUT VOLTAGE SWING vs R_{LOAD}

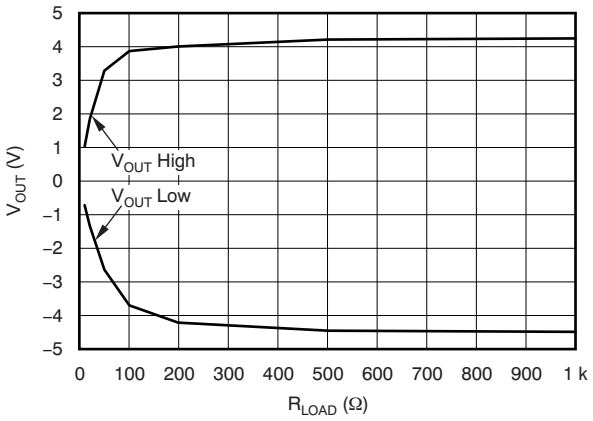

Figure 20.

APPLICATION INFORMATION

Wideband, Noninverting, and Inverting Operation

The OPA653 is a very broadband, voltage-feedback amplifier with internal gain-setting resistors that set a fixed gain of +2 V/V or -1 V/V and a high-impedance JFET-input stage. Its very high bandwidth of 500 MHz can be used to either deliver high signal bandwidths at a gain of +2 V/V or, if driven from a low-impedance source, a gain of –1 V/V . The OPA653 is designed to provide very low noise and accurate pulse response with low overshoot and ringing. To achieve the full performance of the OPA653, careful attention to printed circuit board (PCB) layout and component selection is required as discussed in the remaining sections of this data sheet.

Figure 21 shows the noninverting gain of +2-V/V circuit that is used as the basis for the Typical Characteristics. Most of the curves were characterized using signal sources with 50-Ω driving impedance, and with measurement equipment that presents a 50-Ω load impedance. In Figure 21, the 49.9-Ω shunt resistor to ground at the V_{IN+} input is used to match the source impedance of the test generator and cable, while the 49.9-Ω series output resistor V_{OUT} provides matching impedance for the measurement equipment load and cable. Data sheet voltage swing specifications are taken at the noninverting input pin, V_{IN+}, or the output pin, V_{OUT}, unless otherwise noted.

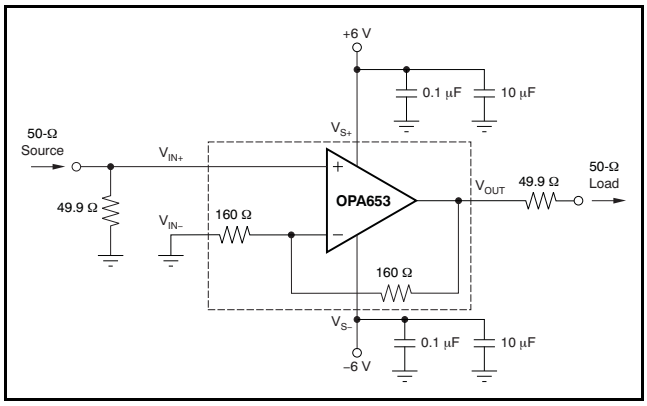

Figure 21. Noninverting Gain of +2 V/V in 50-Ω Test Environment

Figure 22 shows the OPA653 in an inverting gain of –1 V/V configuration in a 50-Ω test environment as was used for testing the Typical Characteristics. The circuit operation is essentially the same as Figure 21 except that a 72.3-Ω termination resistor is now used between the $V_{IN–}$ input and ground, so that together with the gain-setting resistor (R_G = 160 Ω), the input impedance is approximately 50 Ω. The V_{IN+} input is terminated to ground using a 49.9-Ω resistor as a precaution to avoid single transistor oscillations at the input; the value is not critical, but attention should be paid to avoid large values because of the noise contribution as noted below.

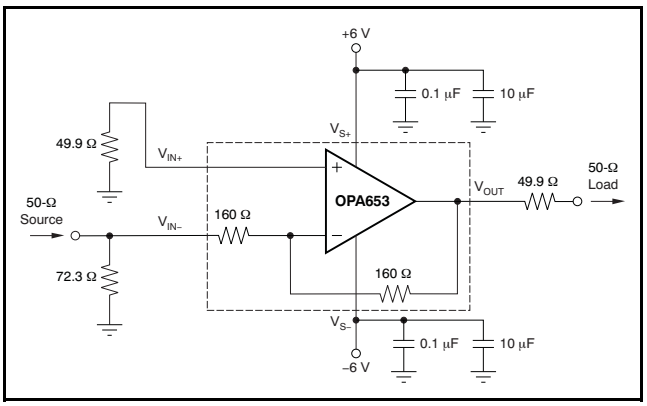

Figure 22. Inverting Gain of –1 V/V in 50-Ω Test Environment

Note that the 72.3-Ω input termination resistor and the 50-Ω source impedance of the test equipment modify the noise gain to +1.84 V/V and the amplifier is compensated for optimal performance with a noise gain of +2 V/V. This compensation reduces the phase margin and results in more peaking in the frequency response and more overshoot/ringing in the pulse response. This effect can be seen by comparing the inverting and noninverting frequency and pulse response graphs in the characteristic data. The amplifier phase margin can be restored in an application that uses an inverting configuration if it is driven from a very low impedance source such as an op amp.

OPERATING SUGGESTIONS

Setting Resistor Values to Minimize Noise

The OPA653 provides a low input noise voltage. Figure 23 shows the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

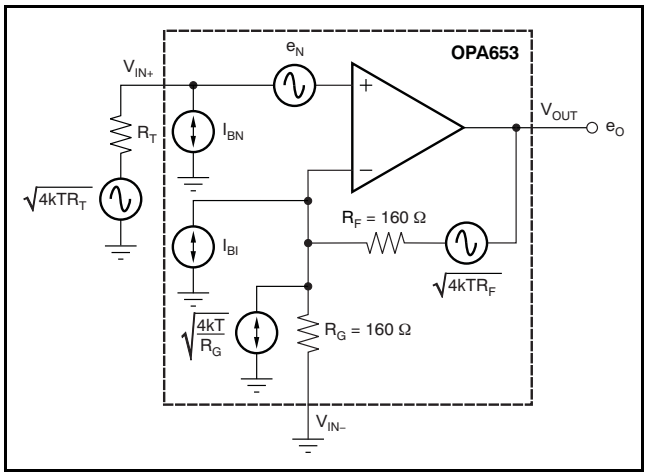

Figure 23. Noise Analysis Circuit

The total output spot noise voltage can be computed as the square root of the squared contributing terms to the output noise voltage. This calculation adds all the contributing noise powers at the output by superposition, then takes the square root to return to a spot noise voltage. Equation 1 shows the general form for this output noise voltage using the terms shown in Figure 23.

$$e_O = \sqrt{\left[4kTR_T + (I_{BN}R_T)^2 + e_N^2\right]\left[1 + \frac{R_F}{R_G}\right]^2 + (I_{BI}R_F)^2 + 4kTR_F\left[1 + \frac{R_F}{R_G}\right]} \quad (1)$$

Dividing this expression by the noise gain = 1 + R_F/R_G gives the equivalent input-referred spot noise voltage at the noninverting input as shown in Equation 2

$$e_{NI} = \sqrt{4kTR_T + (I_{BN}R_T)^2 + e_N^2 + \left[\frac{I_{BI}R_F}{2}\right]^2 + \left[\frac{4kTR_F}{2}\right]} \quad (2)$$

Putting high resistor values into Equation 2 can quickly dominate the total equivalent input-referred noise. Because the gain-setting resistors, R_F and R_G, are internal to the device, the user cannot change this noise contribution, and the noise gain is equal to +2 V/V.

However, attention should be paid to the value of R_T or other source impedance on the noninverting input. High-value resistive impedance on the noninverting input can add significant noise; for example, 2.4 kΩ adds a Johnson voltage noise term equal to the amplifier itself (6.2 nV/√Hz). So while the JFET input of the OPA653 is ideal for high source impedance applications in the noninverting configuration of Figure 21, the overall bandwidth and noise are limited by high source impedances.

Driving Capacitive Loads

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. The OPA653 is very robust, but care should be taken with light loading scenarios so output capacitance does not lead to decreased stability, increased frequency response peaking, overshoot, and ringing. When the amplifier output resistance is considered, capacitive loading introduces an additional pole in the signal path that reduces the phase margin. Several external solutions to this problem have been suggested for standard op amps. Because the OPA653 has internal gain-setting resistors, the only real option is to use a series output resistor. This option is a good solution because when the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, a series output resistor is the simplest and most effective technique. The idea is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor, R_{ISO}, between the amplifier output and the capacitive load as shown in Figure 24 below. In effect, this configuration isolates the phase shift from the loop gain of the amplifier, thus restoring the phase margin and improving stability.

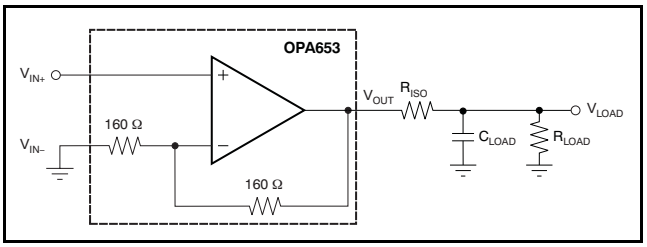

Figure 24. Adding Series Ouput Resistance to Isolate Capacitive Loads

The Typical Characteristics show the recommended R_{ISO} versus Capacitive Load performance (see Figure 17) and the resulting frequency response with a 1-kΩ load. Note that larger R_{ISO} values are required for lower capacitive loading. In this case, a design target of a maximally-flat frequency response was used. Lower values of R_{ISO} may be used if some peaking can be tolerated. Long PCB traces, unmatched cables, and connections to multiple devices can easily degrade the performance of the OPA653. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA653 output pin (see the *Board Layout* section). With heavier loads (for example, the 100-Ω load presented in the test circuits used for testing the Typical Characteristics), the OPA653 is very robust; R_{ISO} can be as low as 10 Ω with capacitive loads less than 5 pF and continue to show a flat frequency response.

Distortion Performance

The OPA653 is capable of delivering low distortion at high frequencies. The distortion plots in the Typical Characteristics show the typical distortion under a wide variety of conditions. Generally, the best distortion performance can be achieved using higher power-supply voltage (±6 V is recommended), lower output voltage swings, and lower loads.

The total load includes the feedback network—in the noninverting configuration, this value is the sum of $R_F + R_G$ = 320 Ω, while in the inverting configuration the total load is only R_F = 160 Ω (see Figure 22).

Power-supply decoupling is critical for harmonic distortion performance. In particular, for optimal second-harmonic performance, the high-frequency, 0.1-µF, power-supply decoupling capacitors should be as close as posible to the positive and negative supply pins and should be brought to a single point ground away from the input pins.

Pulse and Transient Response

To achieve optimum pulse and transient response, the OPA653 should be used in a noise gain of +2 V/V configuration, with minimal capacitance at the output, and high-frequency, 0.1-µF, power-supply decoupling capacitors as close the power pins as possible.

Note: Noise gain of +2 V/V is achieved by tying V_{IN-} to a 0-Ω point. In noninverting gain of +2 V/V applications, V_{IN-} should be grounded, and in inverting gain of –1 V/V applications, V_{IN-} should be driven from a near-0-Ω source such as an op amp.

Board Layout

Achieving optimum performance with a high-frequency amplifier such as the OPA653 requires careful attention to PCB layout parasitics and external component types. Recommendations that can optimize device performance include the following.

a) Minimize parasitic capacitance to any ac ground for all of the signal input/output (I/O) pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional band-limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (less than 0.25 in, or 6,35 mm) from the power-supply pins to the high-frequency, 0.1-µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Use a single point ground, located away from the input pins, for the positive and negative supply high-frequency, 0.1-µF decoupling capacitors. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2-µF to 10-µF) decoupling capacitors, effective at lower frequencies, should also be used on the supply pins. These larger capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components preserves the high-frequency performance of the OPA653. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wirewound-type resistors in a high-frequency application. The inverting input pin is the most sensitive to parasitic capacitance; consequently, always position the feedback resistor as close to the negative input as possible. The output is also sensitive to parasitic capacitance; therefore, position a series output resistor (in this case, R_{ISO}) as close to the output pin as possible.

Other network components, such as noninverting input termination resistors, should also be placed close to the package. Even with a low parasitic capacitance, excessively high resistor values can create significant time constants that can degrade device performance. Good axial metal film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values greater than 1.5 kΩ, this parasitic capacitance can add a pole and/or zero below 500 MHz that can affect circuit operation. Keep resistor values as low as possible. Using values less than 500 Ω automatically holds the resistor noise terms low, and minimizes the effects of parasitic capacitance.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils, or 1,27 cm to 2,54 cm) should be used. Estimate the total capacitive load and set R_{ISO} from the plot of *Recommended R_{ISO} vs Capacitive Load* (Figure 17). Low parasitic capacitive loads (less than 5 pF) may not need an R_{ISO} because the OPA653 is nominally compensated to operate with a 2-pF parasitic load.

Higher parasitic capacitive loads without an R_{ISO} are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and in fact a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA653 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case, and set the series resistor value as shown in the plot of *R_{ISO} vs Capacitive Load* (Figure 17). This configuration does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation as a result of the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part such as the OPA653 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA653 directly onto the board.

Input and ESD Protection

The OPA653 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as Figure 25 shows.

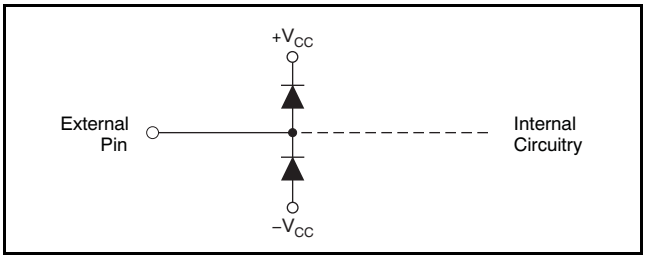

Figure 25. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30-mA continuous current. Where higher currents are possible (for example, in systems with ±12-V supply parts driving into the OPA653), current limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response.

PowerPAD™ Information

The DRB package option is a PowerPAD™ package that includes a thermal pad for increased thermal performance. When using thls package, it is recommended to distribute the negative supply as a power plane, and tie the PowerPAD to this supply wlth multiple vias for proper power dissipation.

For proper operation, the PowerPAD must be tied to the most negative supply voltage. It is recommended to use five evenly-spaced vias under the device as shown in the EVM layer views (see Figure 27).

For more general data and detailed information about the PowerPAD package, refer to the *PowerPAD™ Thermally Enhanced Package* application note (SLMA002).

EVALUATION MODULE

Schematic and PCB Layout

Figure 26 is the OPA653EVM schematic. Layers 1 through 4 of the PCB are shown in Figure 27. It is recommended to follow the layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible.

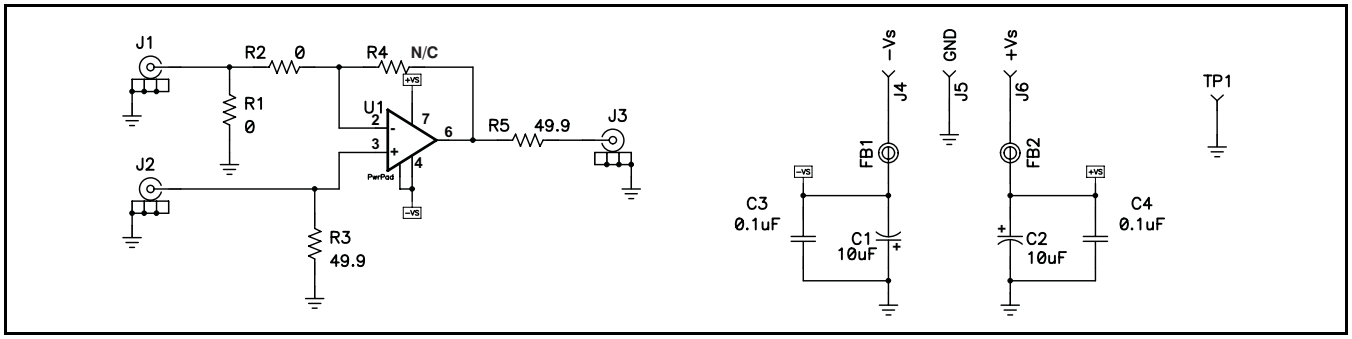

Figure 26. OPA653EVM Schematic

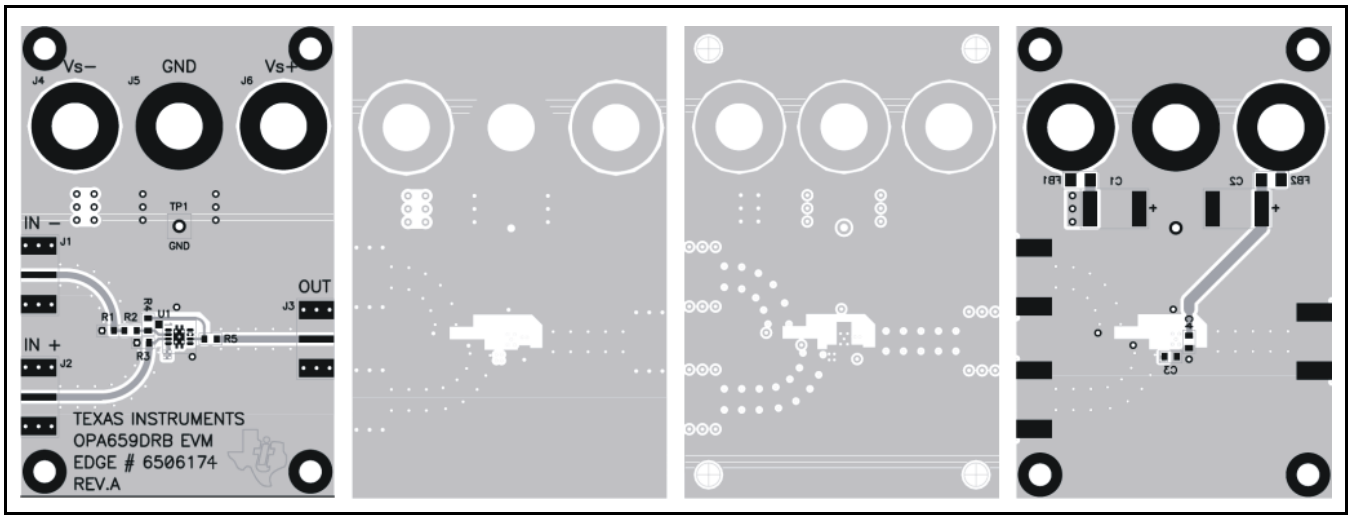

Figure 27. OPA653EVM PCB Layers 1 through 4

Bill of Materials

Table 1 lists the bill of materials for the OPA653EVM as supplied from TI.

Table 1. OPA653EVM Parts List

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	QUANTITY	MANUFACTURER PART NUMBER
1	Cap, 10.0 µF, Tantalum, 10%, 35 V	D	C1, C2	2	(AVX) TAJ106K035R
2	Cap, 0.1 µF, Ceramic, X7R, 16 V	0603	C3, C4	2	(AVX) 0603YC104KAT2A
3	Resistor, 0 Ω	0603	R1, R2	2	(ROHM) MCR03EZPJ000
4	Open	0603	R4	1	
5	Resistor, 49.9 Ω, 1/10W, 1%	0603	R3, R5	2	(ROHM) MCR03EZPFX49R9
6	Jack, Banana Receptance, 0.25-in dia. hole		J4, J5, J8	3	(SPC) 813
7	Connector, Edge, SMA PCB jack		J1, J2, J3	3	(JOHNSON) 142-0701-801
8	Test Point, Black		TP1	1	(KEYSTONE) 5001
9	IC, OPA653		U1	1	(TI) OPA653DRB
10	Standoff, 4-40 Hex, 0.625-in length			4	(KEYSTONE) 1808
11	Screw, Phillips, 4-40, .250 in			4	SHR-0440-016-SN
12	Board, Printed Circuit			1	(TI) EDGE# 6506174
13	Bead, Ferrite, 3 A, 80 Ω	1206	FB1, FB2	2	(STEWARD) HI1206N800R-00

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Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of ±3.5 V to ±6.5 V split-supply and the output voltage range of ±3.5 V to ±6.5 V power-supply voltage; do not exceed ±6.5 V power-supply voltage.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December, 2008) to Revision A **Page**

- Deleted lead temperature specification from *Absolute Maximum Ratings* table 2
- Added *Input offset voltage* specifications for DBV package; noted that existing specifications apply to DRB package 3
- Changed *Input offset voltage* specifications for DRB package to ±1.5 mV from ±3 mV 3
- Changed *Average input offset voltage drift* typical specification for DRB package from ±15μV/°C to ±10μV/°C 3
- Added *PowerPAD™ Information* section 12
- Corrected *Edge number* in Figure 27 13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA653IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZW	Samples
OPA653IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZW	Samples
OPA653IDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OBEI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

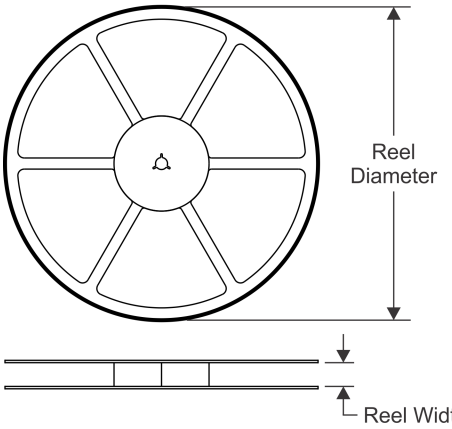
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

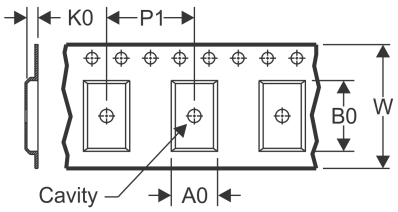
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

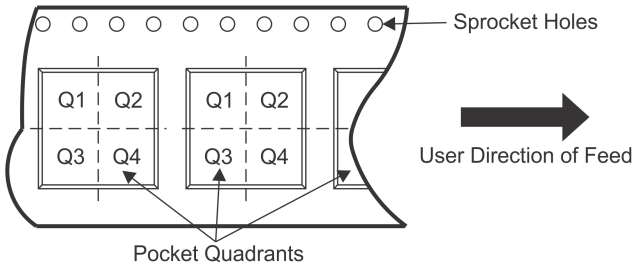


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

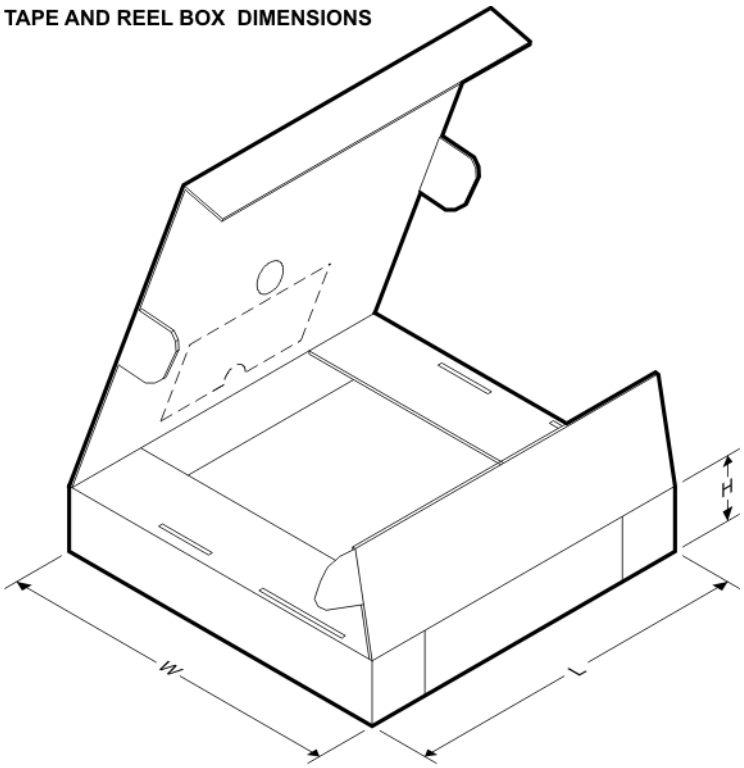
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA653IDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA653IDRBT	SON	DRB	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

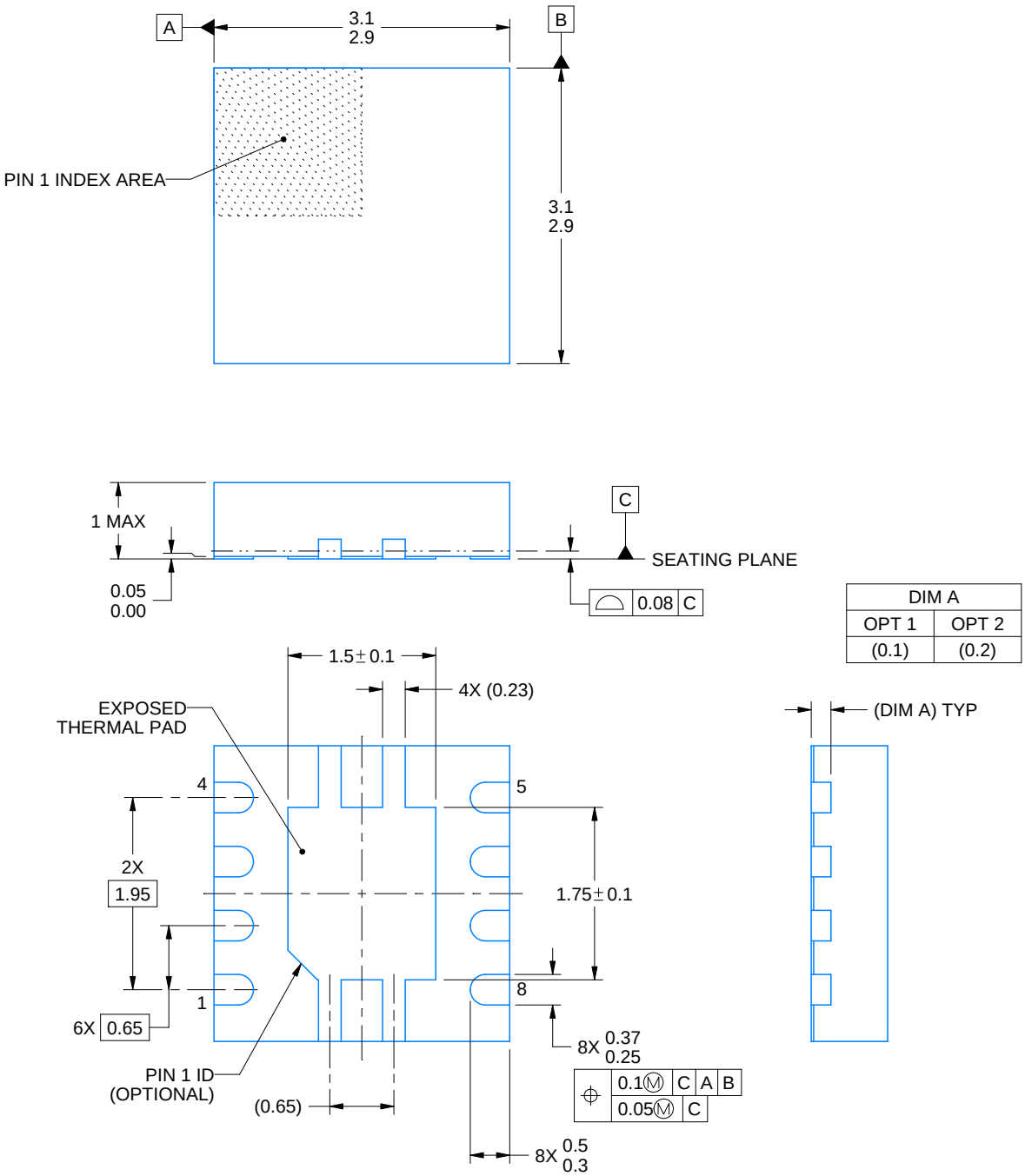
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

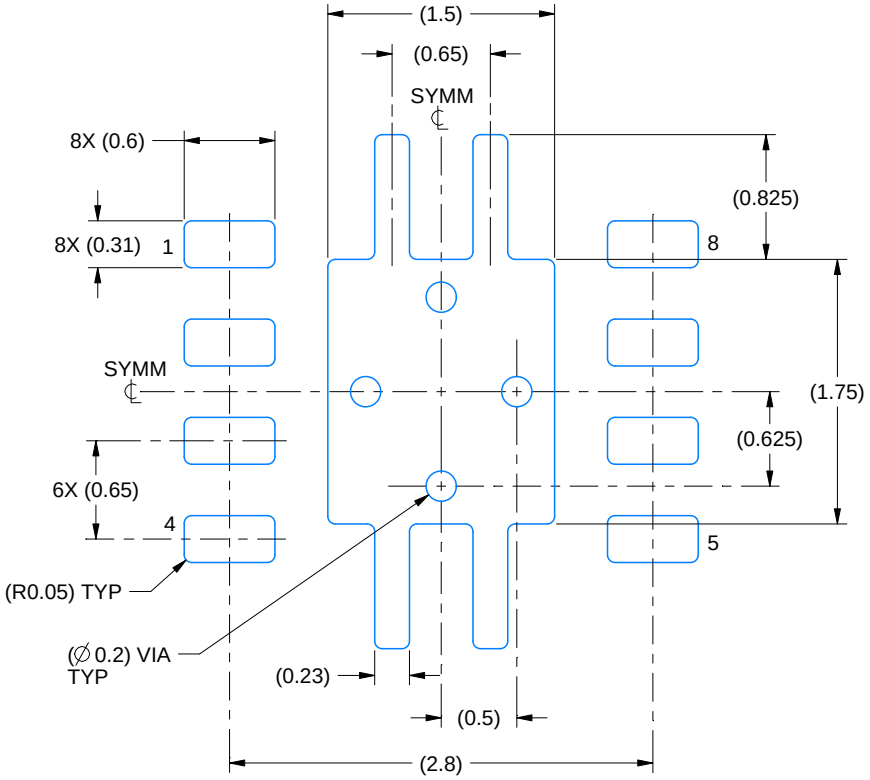
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

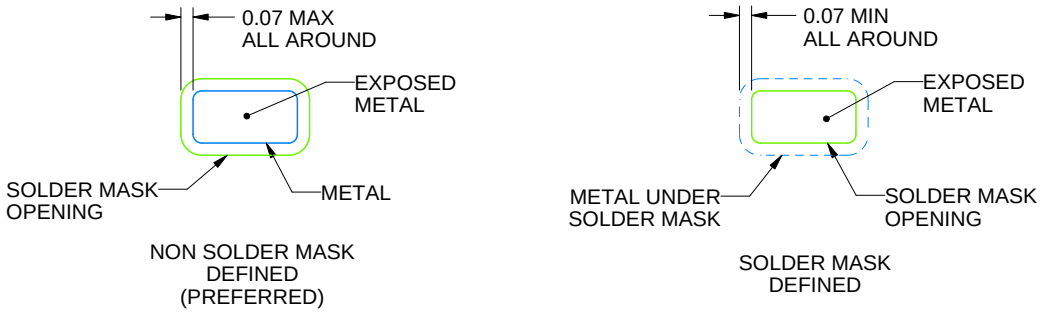
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

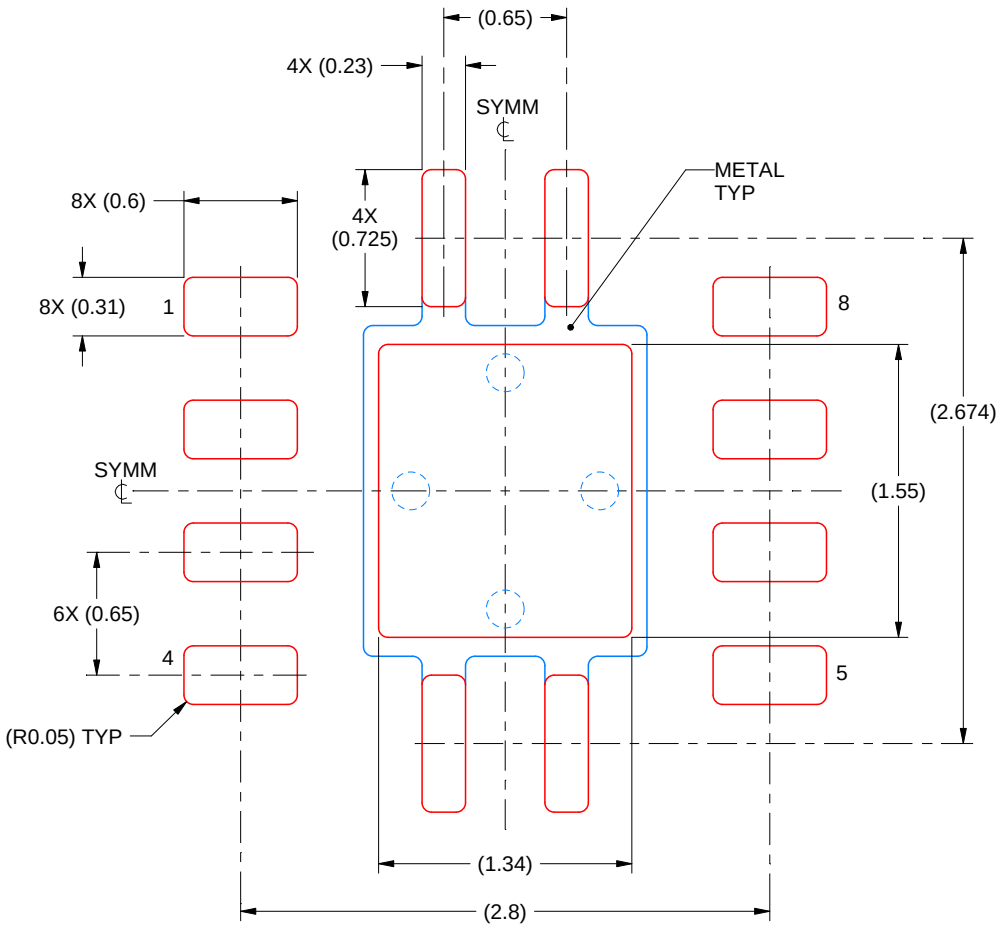


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

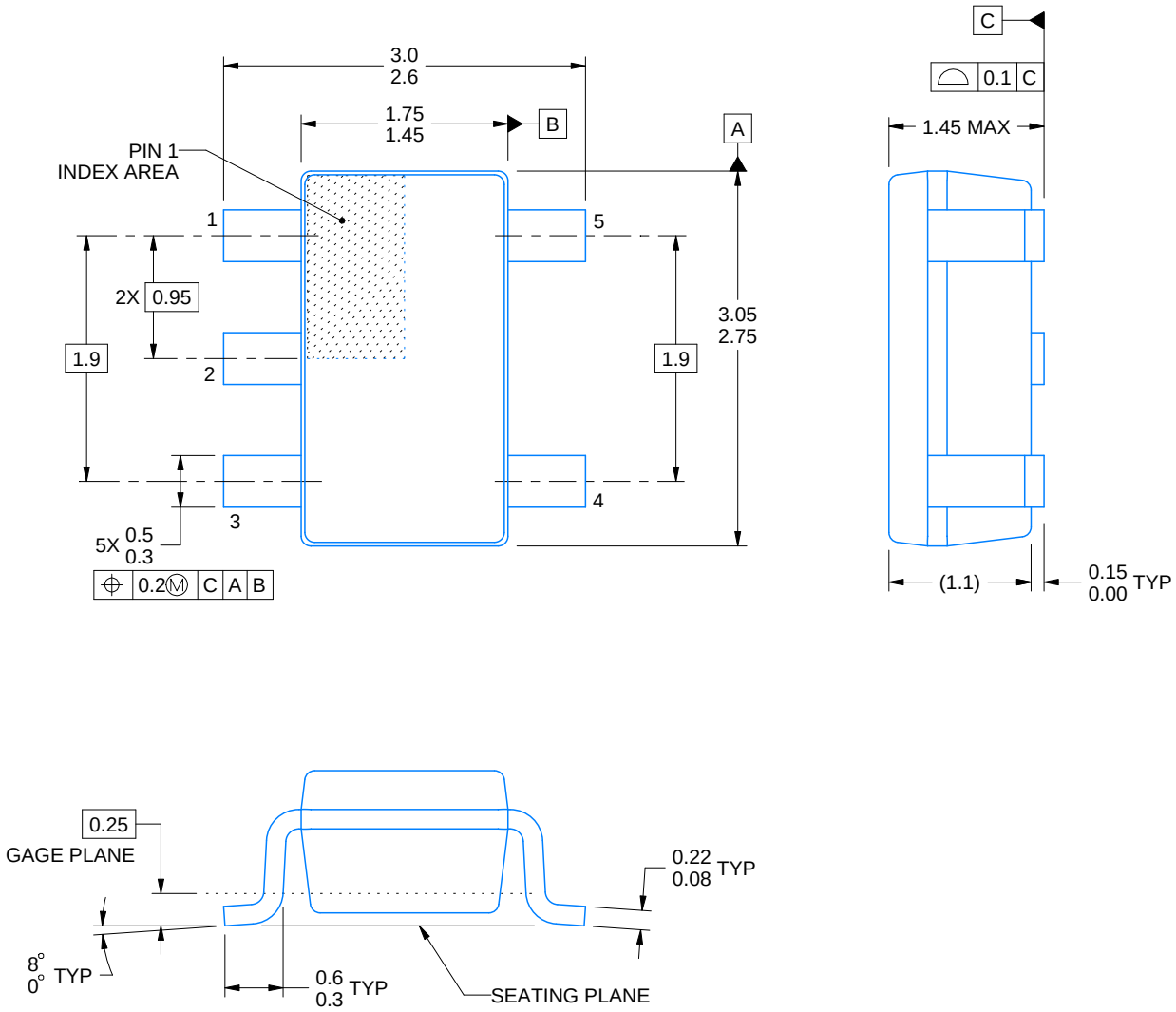
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

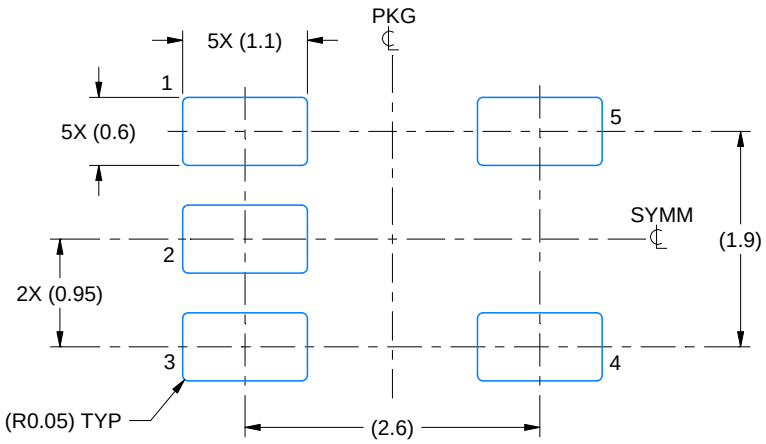
SMALL OUTLINE TRANSISTOR



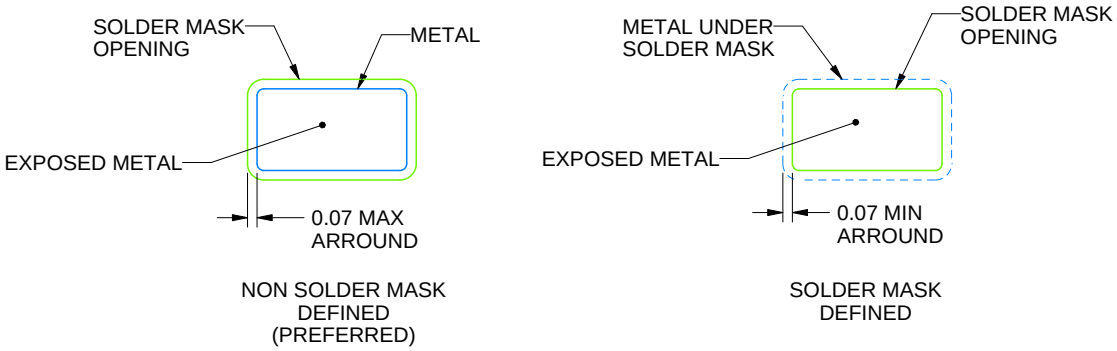
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

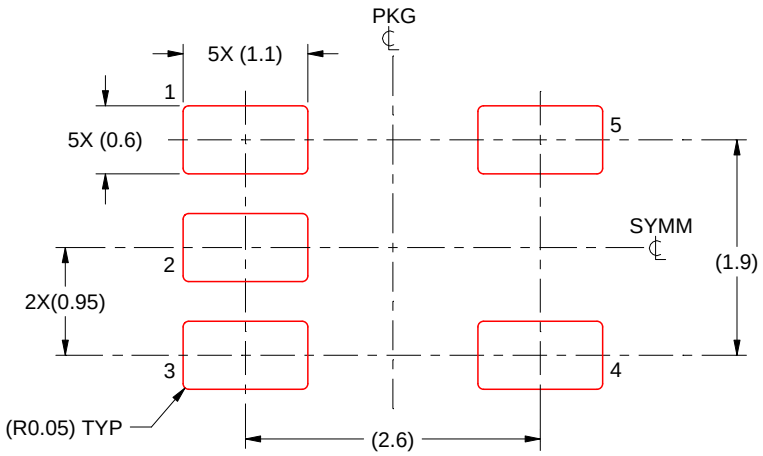


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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