



**THE DATASHEET OF
CSD87335Q3D**



CSD87335Q3D Synchronous Buck NexFET™ Power Block

1 Features

- Half-Bridge Power Block
- Up to 27-V V_{IN}
- 93.5% System Efficiency at 15 A
- Up to 25-A Operation
- High-Frequency Operation (Up to 1.5 MHz)
- High-Density SON 3.3-mm x 3.3-mm Footprint
- Optimized for 5-V Gate Drive
- Low-Switching Losses
- Ultra-Low Inductance Package
- RoHS Compliant
- Halogen Free
- Lead-Free Terminal Plating

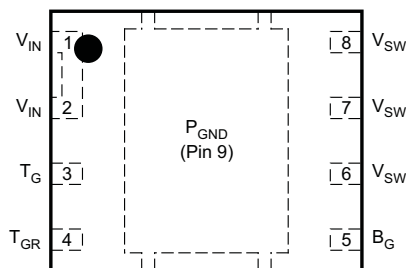
2 Applications

- Synchronous Buck Converters
 - High-Frequency Applications
 - High-Current, Low-Duty Cycle Applications
- Multiphase Synchronous Buck Converters
- POL DC-DC Converters
- IMVP, VRM, and VRD Applications

3 Description

The CSD87335Q3D NexFET™ power block is an optimized design for synchronous buck applications offering high-current, high-efficiency, and high-frequency capability in a small 3.3-mm x 3.3-mm outline. Optimized for 5-V gate drive applications, this product offers a flexible solution capable of offering a high-density power supply when paired with any 5-V gate drive from an external controller or driver.

Top View



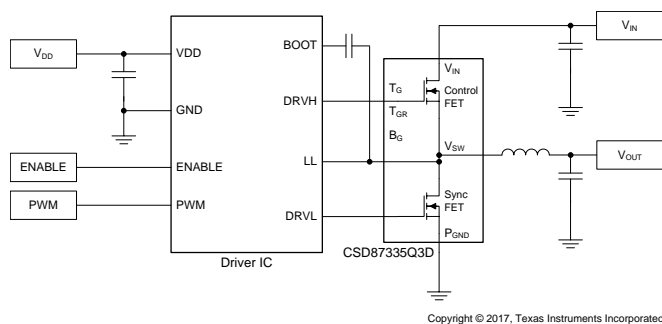
P0116-01

Device Information⁽¹⁾

DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD87335Q3D	13-Inch Reel	2500	SON	Tape and Reel
CSD87335Q3DT	7-Inch Reel	250	3.30-mm x 3.30-mm Plastic Package	Tape and Reel

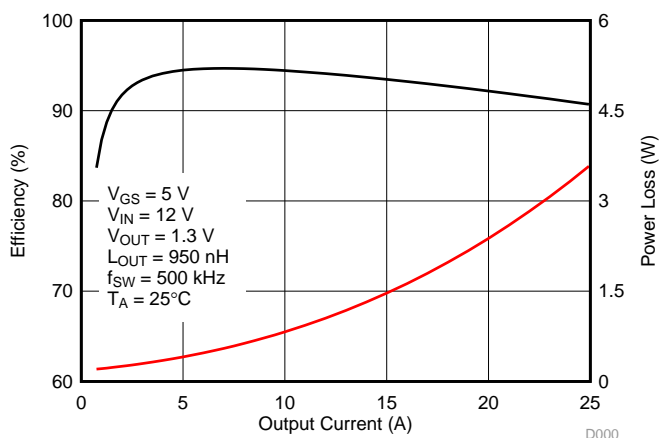
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Circuit



Copyright © 2017, Texas Instruments Incorporated

Typical Power Block Efficiency and Power Loss



D000



Table of Contents

1 Features	1	6.5 Calculating Power Loss and SOA	13
2 Applications	1	7 Recommended PCB Design Overview	15
3 Description	1	7.1 Electrical Performance	15
4 Revision History	2	7.2 Thermal Performance	16
5 Specifications	3	8 Device and Documentation Support	17
5.1 Absolute Maximum Ratings	3	8.1 Receiving Notification of Documentation Updates..	17
5.2 Recommended Operating Conditions	3	8.2 Community Resources	17
5.3 Thermal Information	3	8.3 Trademarks	17
5.4 Power Block Performance	3	8.4 Electrostatic Discharge Caution	17
5.5 Electrical Characteristics	4	8.5 Glossary	17
5.6 Typical Power Block Device Characteristics	5	9 Mechanical, Packaging, and Orderable	
5.7 Typical Power Block MOSFET Characteristics	7	Information	18
6 Applications and Implementation	10	9.1 Q3D Package Dimensions	18
6.1 Application Information	10	9.2 Land Pattern Recommendation	19
6.2 Power Loss Curves	12	9.3 Stencil Recommendation	19
6.3 Safe Operating Curves (SOA)	12	9.4 Q3D Tape and Reel Information	20
6.4 Normalized Curves	12	9.5 Pin Configuration	20

4 Revision History

Changes from Revision A (October 2017) to Revision B Page

- Updated [Figure 33](#) top layer showing pins 1 and 2 connected. 16

Changes from Original (February 2016) to Revision A Page

- Corrected X & Y axis labels on [Figure 29](#)
- Corrected X & Y axis labels on [Figure 30](#)

5 Specifications

5.1 Absolute Maximum Ratings

 $T_A = 25^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	V_{IN} to P_{GND}		30	V
	V_{SW} to P_{GND}		30	
	V_{SW} to P_{GND} (10 ns)		32	
	T_G to T_{GR}	-8	10	
	B_G to P_{GND}	-8	10	
Pulsed current rating, I_{DM} ⁽²⁾			70	A
Power dissipation, P_D			6	W
Avalanche energy, E_{AS}	Sync FET, $I_D = 51$ A, $L = 0.1$ mH		130	mJ
	Control FET, $I_D = 33$ A, $L = 0.1$ mH		54	
Operating junction and storage temperature, T_J , T_{STG}		-55	150	$^\circ\text{C}$

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Pulse duration ≤ 50 μs , duty cycle $\leq 1\%$.

5.2 Recommended Operating Conditions

 $T_A = 25^\circ\text{C}$ (unless otherwise noted)

		MIN	MAX	UNIT
V_{GS}	Gate drive voltage	4.5	8	V
V_{IN}	Input supply voltage		27	V
f_{SW}	Switching frequency	$C_{BST} = 0.1$ μF (min)	1500	kHz
	Operating current		25	A
T_J	Operating temperature		125	$^\circ\text{C}$

5.3 Thermal Information

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu) ⁽¹⁾			135	$^\circ\text{C}/\text{W}$
	Junction-to-ambient thermal resistance (max Cu) ⁽¹⁾⁽²⁾			73	
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package) ⁽¹⁾			29	$^\circ\text{C}/\text{W}$
	Junction-to-case thermal resistance (P_{GND} pin) ⁽¹⁾			2.5	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu pad on a 1.5-in \times 1.5-in (3.81-cm \times 3.81-cm), 0.06-in (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1-in² (6.45-cm²) Cu.

5.4 Power Block Performance⁽¹⁾

 $T_A = 25^\circ\text{C}$ (unless otherwise noted)

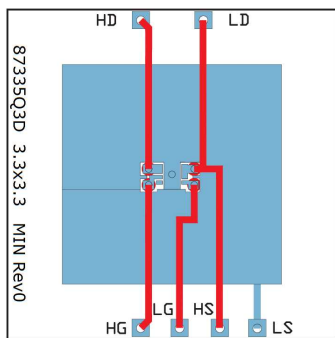
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}	Power loss ⁽¹⁾		1.5		W
I_{QVIN}	V_{IN} quiescent current	T_G to $T_{GR} = 0$ V, B_G to $P_{GND} = 0$ V	10		μA

(1) Measurement made with six 10- μF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high-current 5-V driver IC.

5.5 Electrical Characteristics

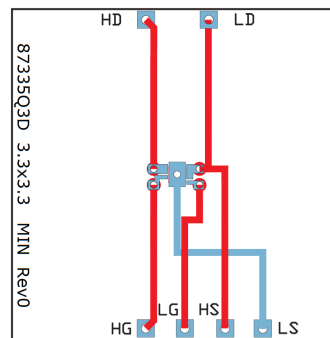
 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER	TEST CONDITIONS	Q1 Control FET			Q2 Sync FET			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
STATIC CHARACTERISTICS									
BV_{DSS}	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$			30			V	
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1			μA	
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = +10\text{ V} / -8\text{ V}$			100			nA	
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$			1.0 1.9			V	
$Z_{DS(on)}$	Effective AC on-impedance	$V_{IN} = 12\text{ V}, V_{GS} = 5\text{ V}, V_{OUT} = 1.3\text{ V}, I_{OUT} = 15\text{ A}, f_{SW} = 500\text{ kHz}, L_{OUT} = 950\text{ nH}$			6.7 1.9			$\text{m}\Omega$	
g_{fs}	Transconductance	$V_{DS} = 3\text{ V}, I_{DS} = 15\text{ A}$			59 107			S	
DYNAMIC CHARACTERISTICS									
C_{ISS}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$			805 1050		1620 2100		pF
C_{OSS}	Output capacitance				412 536		783 1020		pF
C_{RSS}	Reverse transfer capacitance				15 20		28 36		pF
R_G	Series gate resistance	$V_{DS} = 15\text{ V}, I_{DS} = 15\text{ A}$			1.2 2.4		0.6 1.2		Ω
Q_g	Gate charge total (4.5 V)				5.7 7.4		10.7 14.0		nC
Q_{gd}	Gate charge – gate-to-drain				1.1		1.7		nC
Q_{gs}	Gate charge – gate-to-source				2.1		2.8		nC
$Q_{g(th)}$	Gate charge at V_{th}				1.1		1.4		nC
Q_{OSS}	Output charge	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$			11 19		nC		
$t_{d(on)}$	Turnon delay time	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_{DS} = 15\text{ A}, R_G = 2\ \Omega$			8		8		ns
t_r	Rise time				29		27		ns
$t_{d(off)}$	Turnoff delay time				13		17		ns
t_f	Fall time				4		5		ns
DIODE CHARACTERISTICS									
V_{SD}	Diode forward voltage	$I_{DS} = 15\text{ A}, V_{GS} = 0\text{ V}$			0.8 1.0		0.8 1.0		V
Q_{rr}	Reverse recovery charge	$V_{DS} = 15\text{ V}, I_F = 15\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$			24		40		nC
t_{rr}	Reverse recovery time				17		22		ns



M0205-01

Max $R_{\theta JA} = 73^\circ\text{C}/\text{W}$
 when mounted on 1 in²
 (6.45 cm²) of 2-oz
 (0.071-mm) thick Cu.

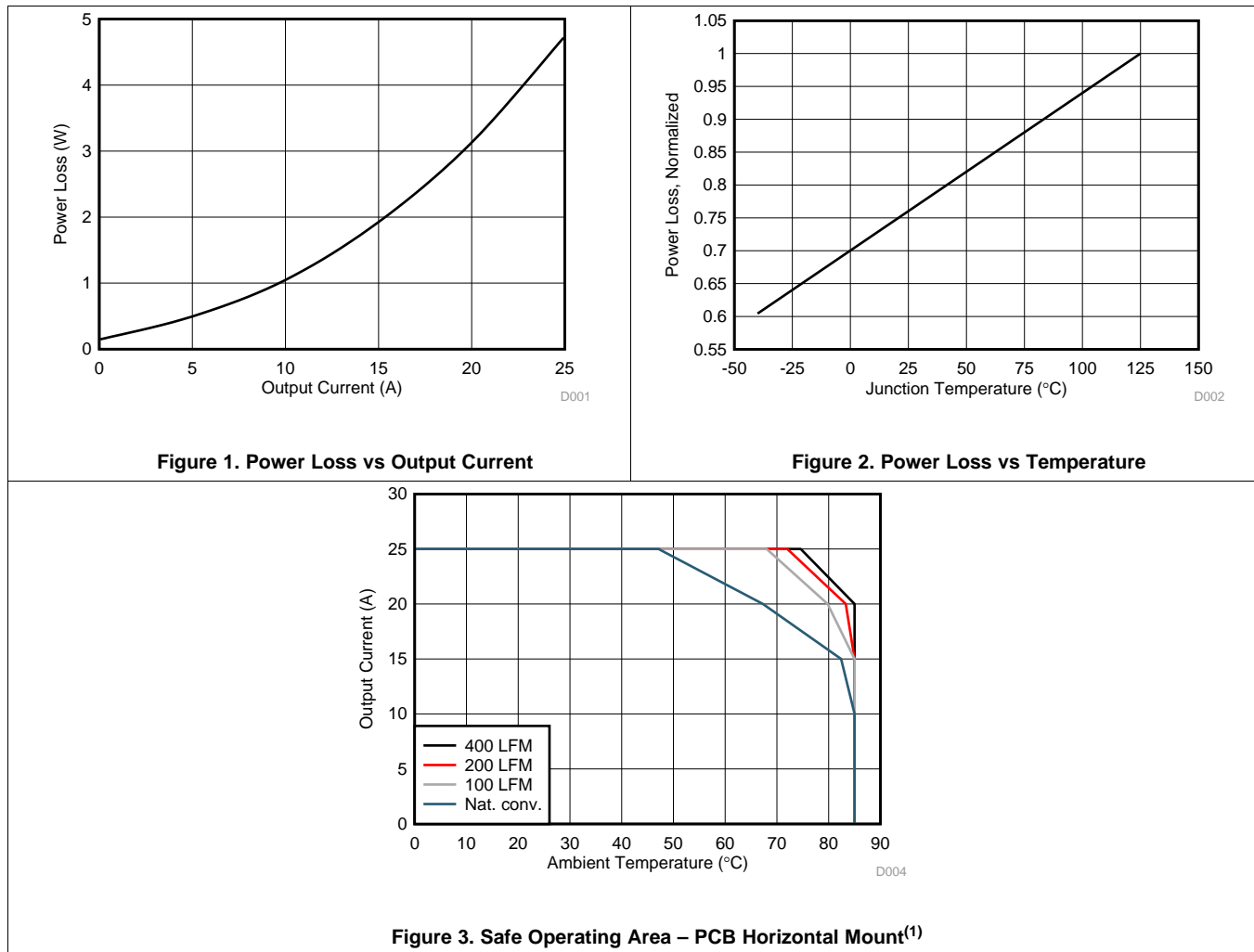


M0205-01

Max $R_{\theta JA} = 135^\circ\text{C}/\text{W}$
 when mounted on
 minimum pad area of
 2-oz. (0.071-mm) thick
 Cu.

5.6 Typical Power Block Device Characteristics

Test conditions: $V_{IN} = 12\text{ V}$, $V_{DD} = 5\text{ V}$, $f_{SW} = 500\text{ kHz}$, $V_{OUT} = 1.3\text{ V}$, $L_{OUT} = 950\text{ nH}$, $I_{OUT} = 25\text{ A}$, $T_J = 125^\circ\text{C}$, unless stated otherwise.



(1) The Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4 in (W) x 3.5 in (L) x 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See [Applications and Implementation](#) section for detailed explanation.

Typical Power Block Device Characteristics (continued)

Test conditions: $V_{IN} = 12\text{ V}$, $V_{DD} = 5\text{ V}$, $f_{SW} = 500\text{ kHz}$, $V_{OUT} = 1.3\text{ V}$, $L_{OUT} = 950\text{ nH}$, $I_{OUT} = 25\text{ A}$, $T_J = 125^\circ\text{C}$, unless stated otherwise.

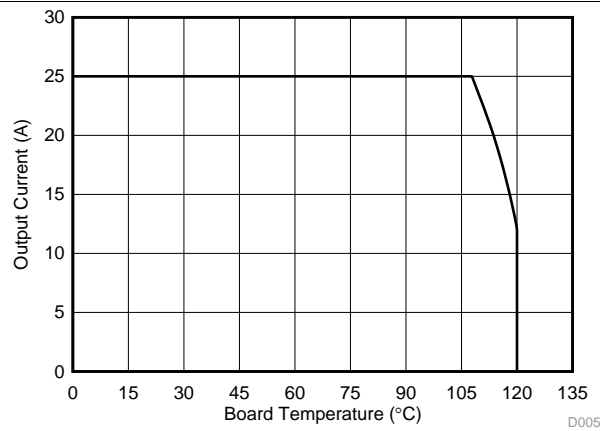


Figure 4. Typical Safe Operating Area⁽¹⁾

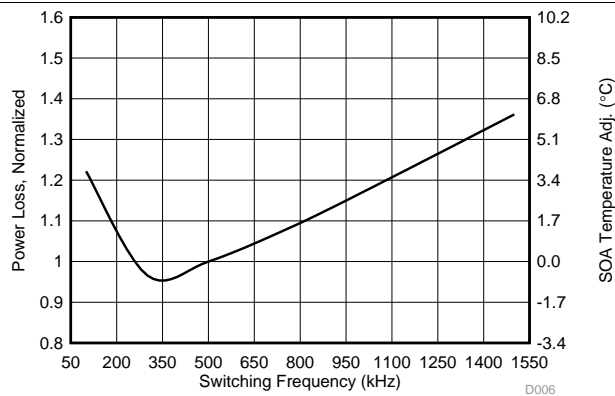


Figure 5. Normalized Power Loss vs Switching Frequency

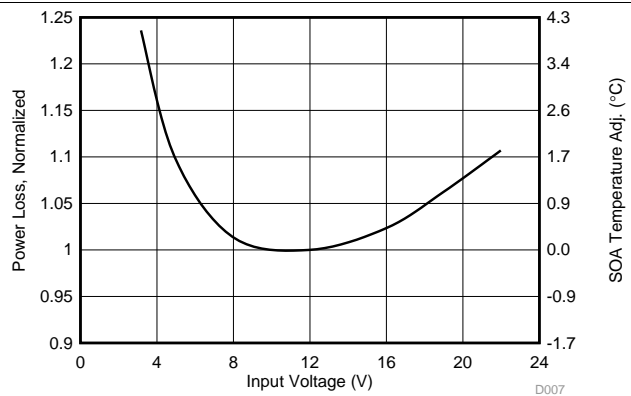


Figure 6. Normalized Power Loss vs Input Voltage

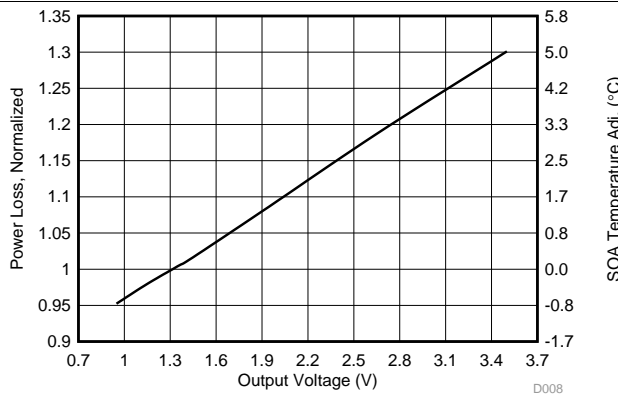


Figure 7. Normalized Power Loss vs Output Voltage

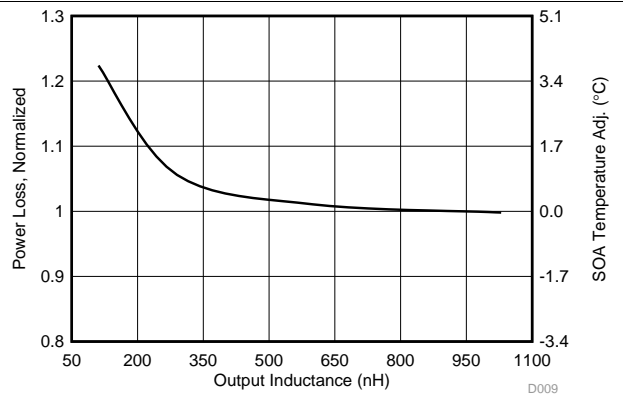


Figure 8. Normalized Power Loss vs Output Inductance

5.7 Typical Power Block MOSFET Characteristics

$T_A = 25^\circ\text{C}$, unless stated otherwise.

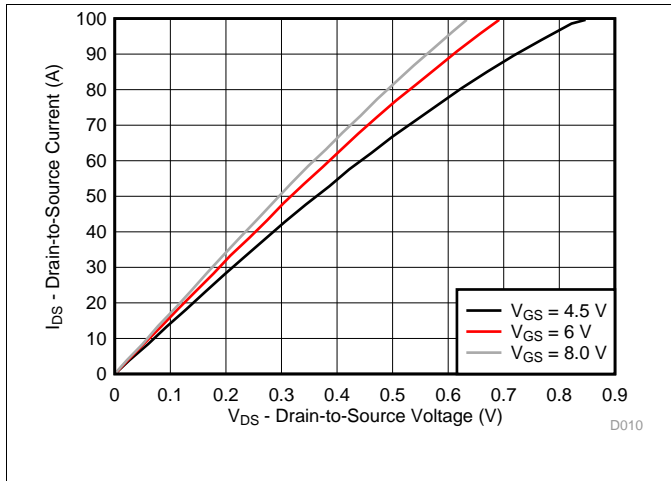


Figure 9. Control MOSFET Saturation

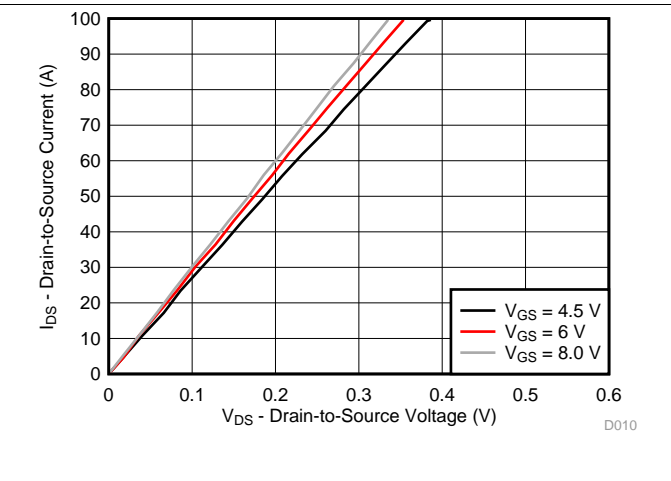


Figure 10. Sync MOSFET Saturation

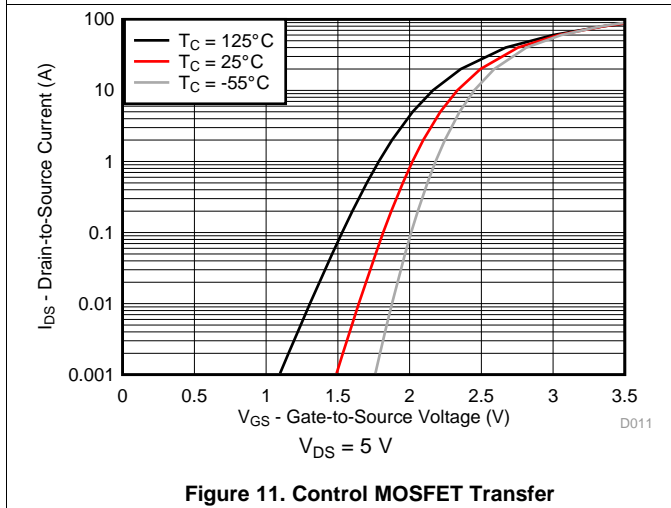


Figure 11. Control MOSFET Transfer

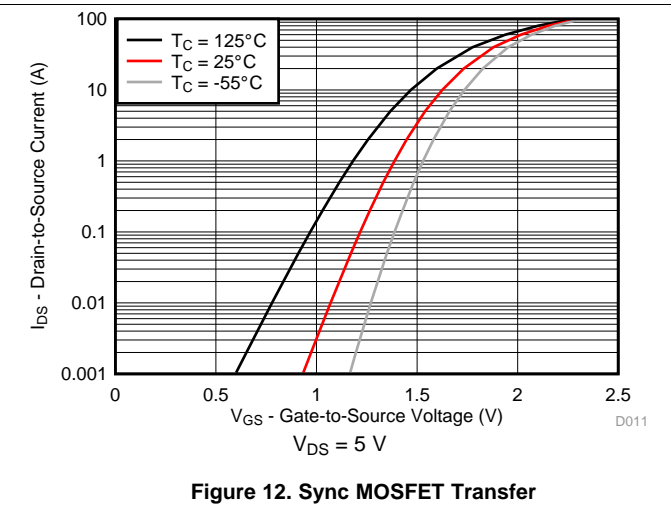


Figure 12. Sync MOSFET Transfer

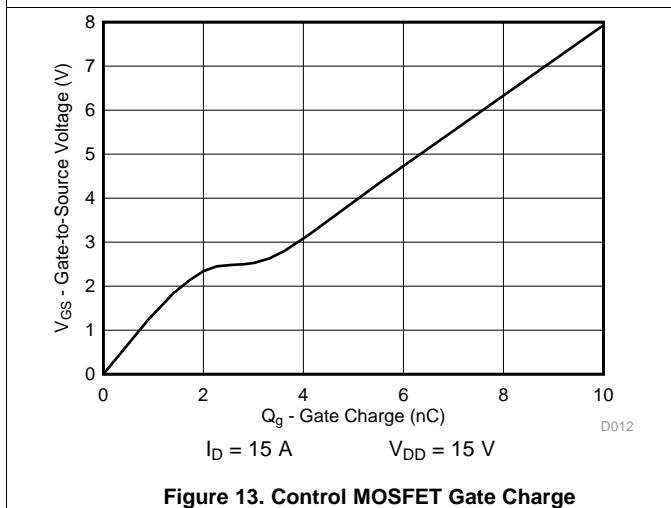


Figure 13. Control MOSFET Gate Charge

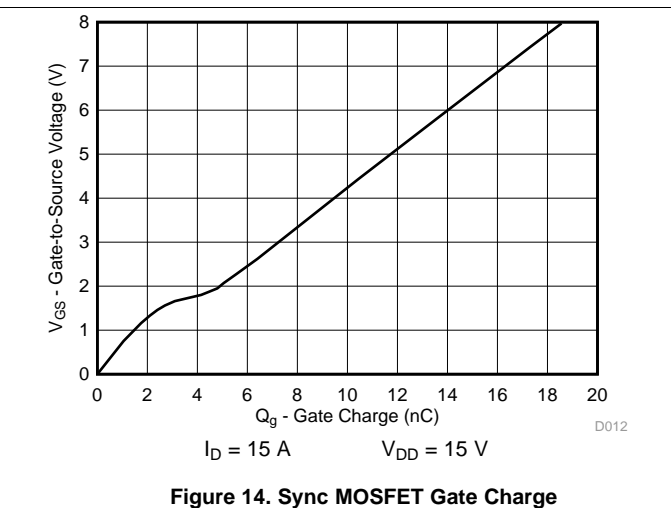
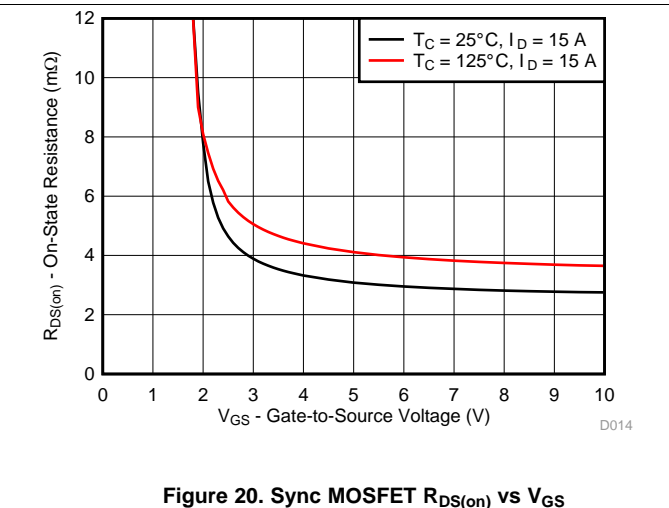
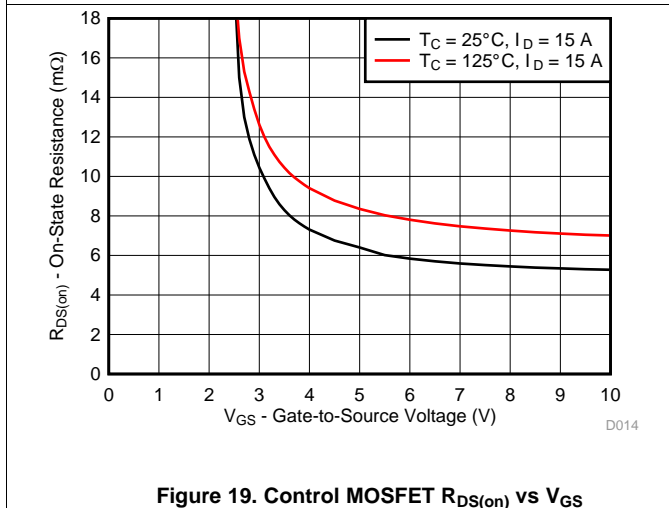
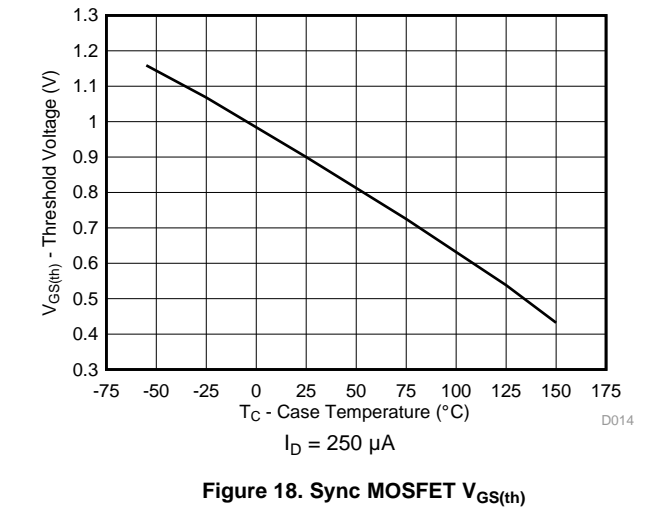
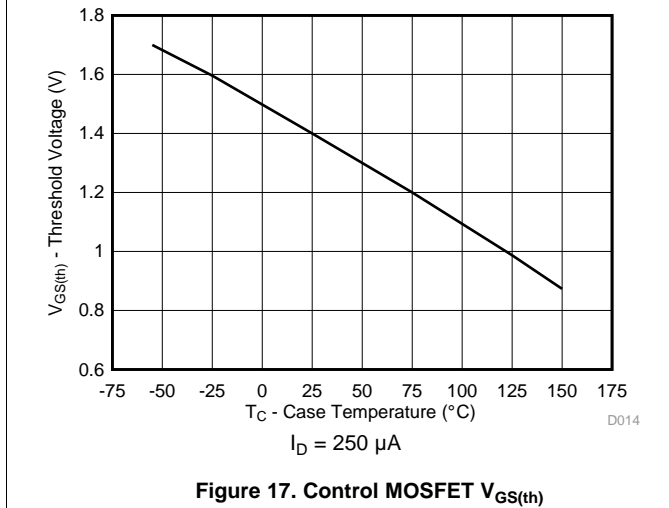
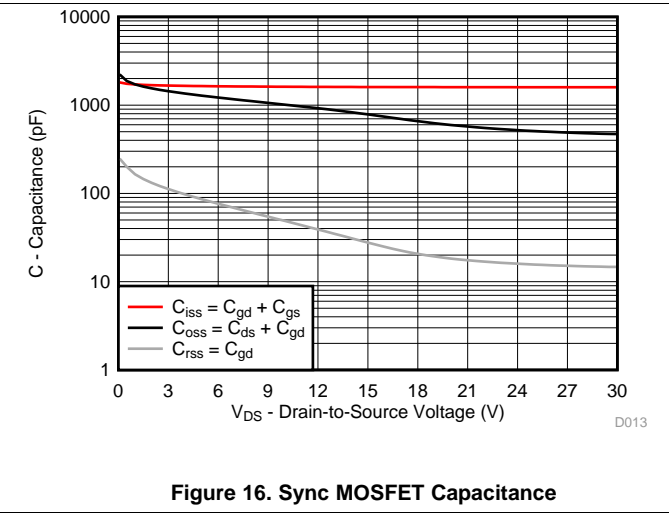
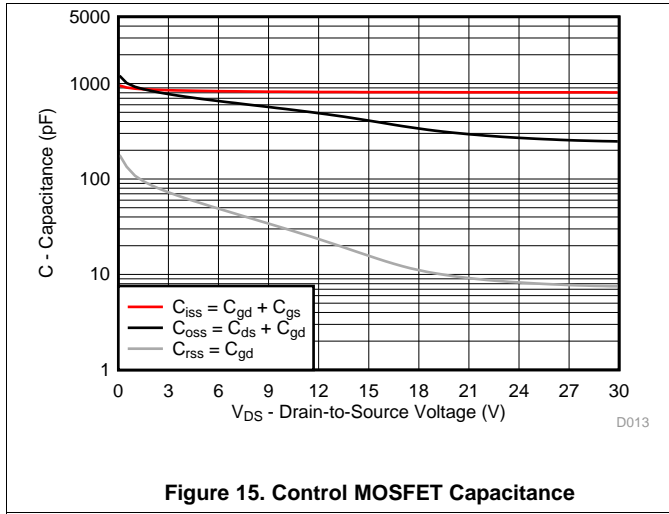


Figure 14. Sync MOSFET Gate Charge

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.



Typical Power Block MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$, unless stated otherwise.

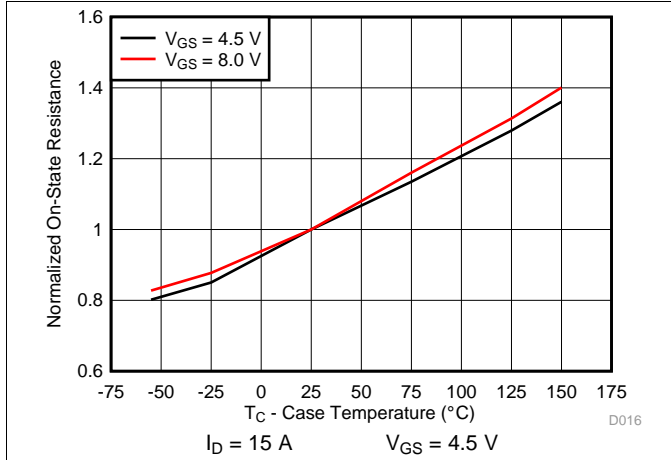


Figure 21. Control MOSFET Normalized $R_{DS(on)}$

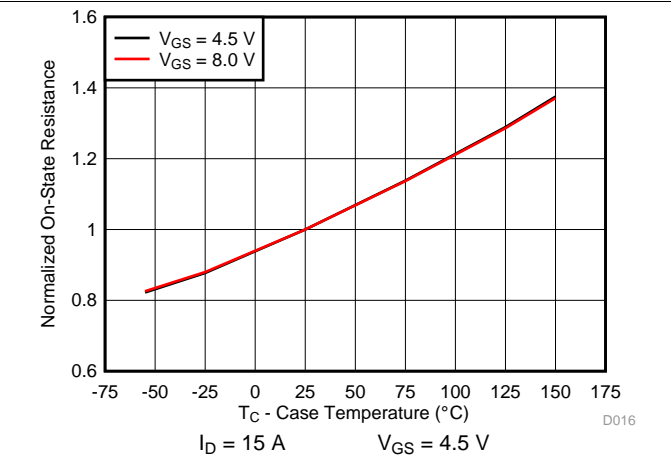


Figure 22. Sync MOSFET Normalized $R_{DS(on)}$

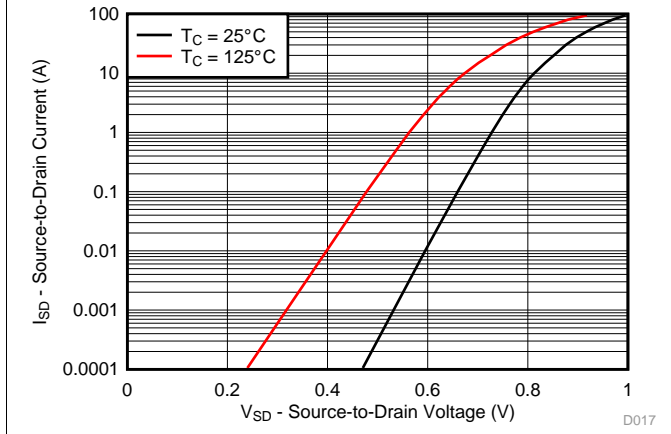


Figure 23. Control MOSFET Body Diode

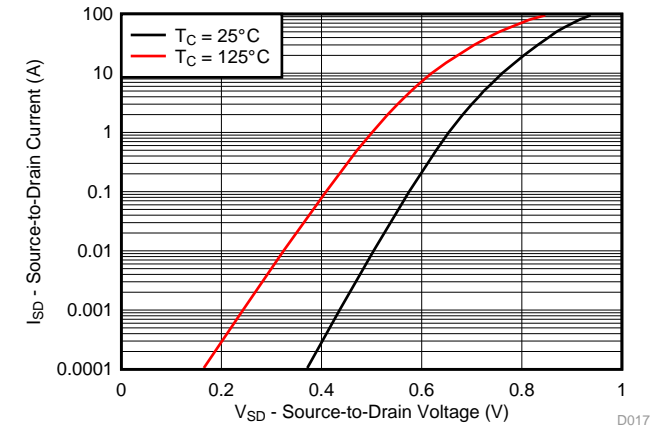


Figure 24. Sync MOSFET Body Diode

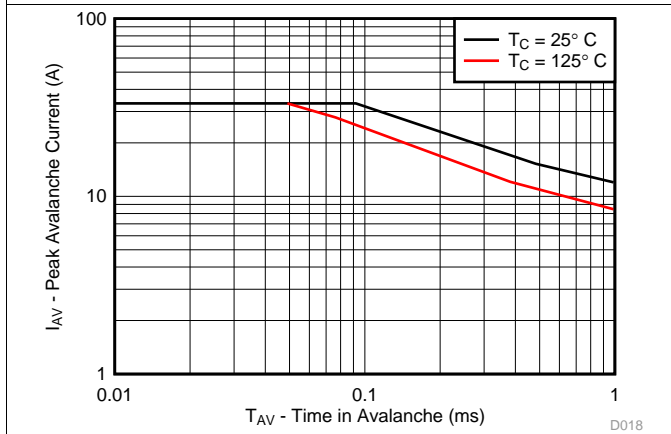


Figure 25. Control MOSFET Unclamped Inductive Switching

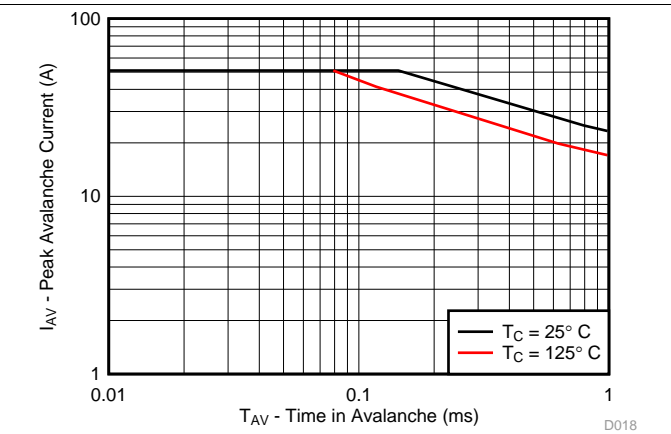


Figure 26. Sync MOSFET Unclamped Inductive Switching

6 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

6.1.1 Equivalent System Performance

Many of today's high-performance computing systems require low-power consumption in an effort to reduce system operating temperatures and improve overall system efficiency. This has created a major emphasis on improving the conversion efficiency of today's synchronous buck topology. In particular, there has been an emphasis in improving the performance of the critical power semiconductor in the power stage of this application (see [Figure 27](#)). As such, optimization of the power semiconductors in these applications, needs to go beyond simply reducing $R_{DS(ON)}$.

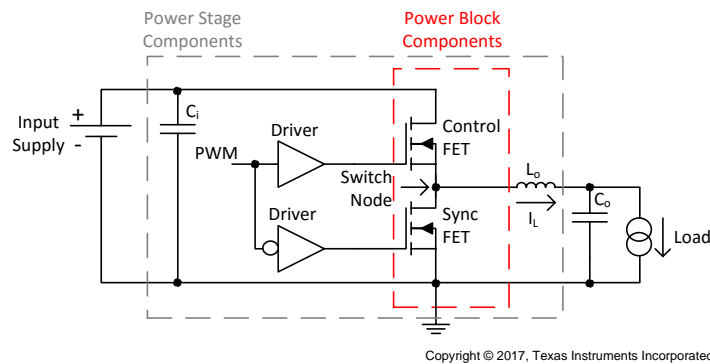


Figure 27. Equivalent System Schematic

The CSD87335Q3D is part of TI's power block product family which is a highly optimized product for use in a synchronous buck topology requiring high current, high efficiency, and high frequency. It incorporates TI's latest generation silicon which has been optimized for switching performance, as well as minimizing losses associated with Q_{GD} , Q_{GS} , and Q_{RR} . Furthermore, TI's patented packaging technology has minimized losses by nearly eliminating parasitic elements between the control FET and sync FET connections (see [Figure 28](#)). A key challenge solved by TI's patented packaging technology is the system level impact of Common Source Inductance (CSI). CSI greatly impedes the switching characteristics of any MOSFET which in turn increases switching losses and reduces system efficiency. As a result, the effects of CSI need to be considered during the MOSFET selection process. In addition, standard MOSFET switching loss equations used to predict system efficiency need to be modified in order to account for the effects of CSI. Further details behind the effects of CSI and modification of switching loss equations are outlined in [Power Loss Calculation With Common Source Inductance Consideration for Synchronous Buck Converters](#) (SLPA009).

Application Information (continued)

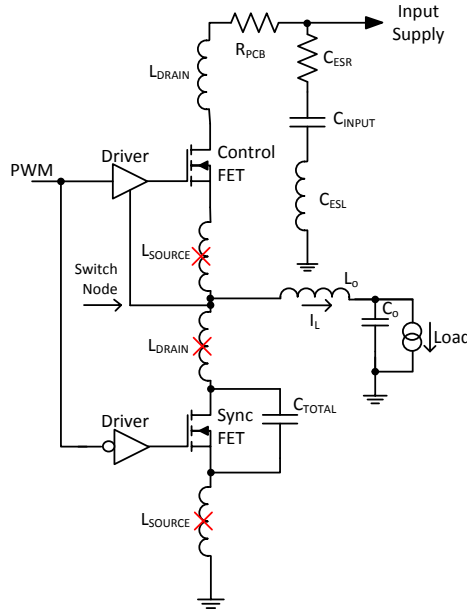


Figure 28. Elimination of Parasitic Inductances

The combination of TI's latest generation silicon and optimized packaging technology has created a benchmarking solution that outperforms industry standard MOSFET chipsets of similar $R_{DS(ON)}$ and MOSFET chipsets with lower $R_{DS(ON)}$. Figure 29 and Figure 30 compare the efficiency and power loss performance of the CSD87335Q3D versus industry standard MOSFET chipsets commonly used in this type of application. This comparison purely focuses on the efficiency and generated loss of the power semiconductors only. The performance of CSD87335Q3D clearly highlights the importance of considering the effective AC on-impedance ($Z_{DS(ON)}$) during the MOSFET selection process of any new design. Simply normalizing to traditional MOSFET $R_{DS(ON)}$ specifications is not an indicator of the actual in-circuit performance when using TI's power block technology.

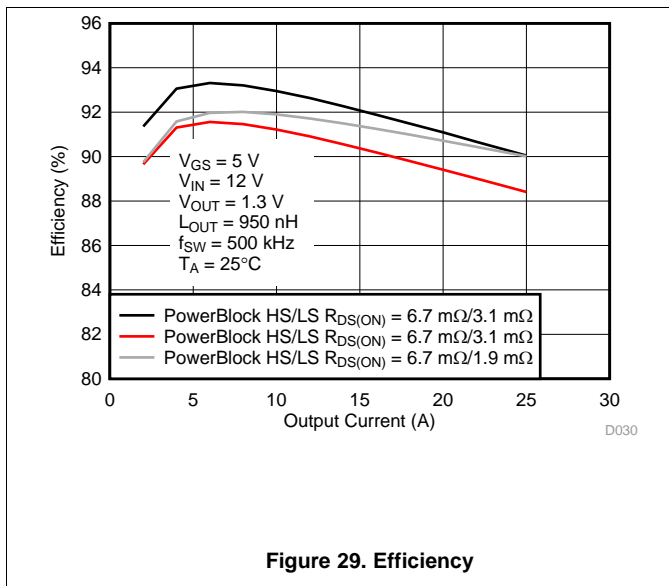


Figure 29. Efficiency

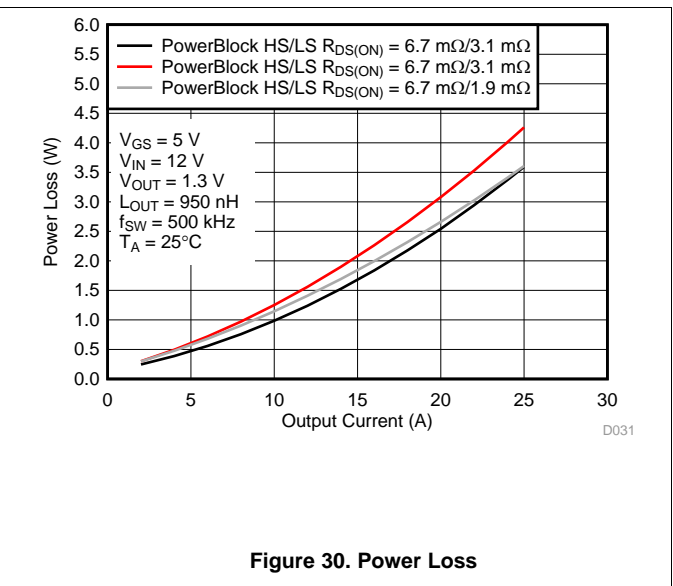


Figure 30. Power Loss

Application Information (continued)

Table 1 compares the traditional DC measured $R_{DS(ON)}$ of CSD87335Q3D versus its $Z_{DS(ON)}$. This comparison takes into account the improved efficiency associated with TI's patented packaging technology. As such, when comparing TI's power block products to individually packaged discrete MOSFETs or dual MOSFETs in a standard package, the in-circuit switching performance of the solution must be considered. In this example, individually packaged discrete MOSFETs or dual MOSFETs in a standard package would need to have DC measured $R_{DS(ON)}$ values that are equivalent to CSD87335Q3D's $Z_{DS(ON)}$ value in order to have the same efficiency performance at full load. Mid to light-load efficiency will still be lower with individually packaged discrete MOSFETs or dual MOSFETs in a standard package.

Table 1. Comparison of $R_{DS(ON)}$ vs. $Z_{DS(ON)}$

PARAMETER	HS		LS	
	TYP	MAX	TYP	MAX
Effective AC on-impedance $Z_{DS(ON)}$ ($V_{GS} = 5\text{ V}$)	6.7	—	1.9	—
DC measured $R_{DS(ON)}$ ($V_{GS} = 4.5\text{ V}$)	6.7	8.1	3.1	3.9

The CSD87335Q3D NexFET™ power block is an optimized design for synchronous buck applications using 5-V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems-centric environment. System-level performance curves such as power loss, Safe Operating Area (SOA), and normalized graphs allow engineers to predict the product performance in the actual application.

6.2 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. **Figure 1** plots the power loss of the CSD87335Q3D as a function of load current. This curve is measured by configuring and running the CSD87335Q3D as it would be in the final application (see **Figure 31**). The measured power loss is the CSD87335Q3D loss and consists of both input conversion loss and gate drive loss. **Equation 1** is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW_AVG} \times I_{OUT}) = \text{Power loss} \quad (1)$$

The power loss curve in **Figure 1** is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

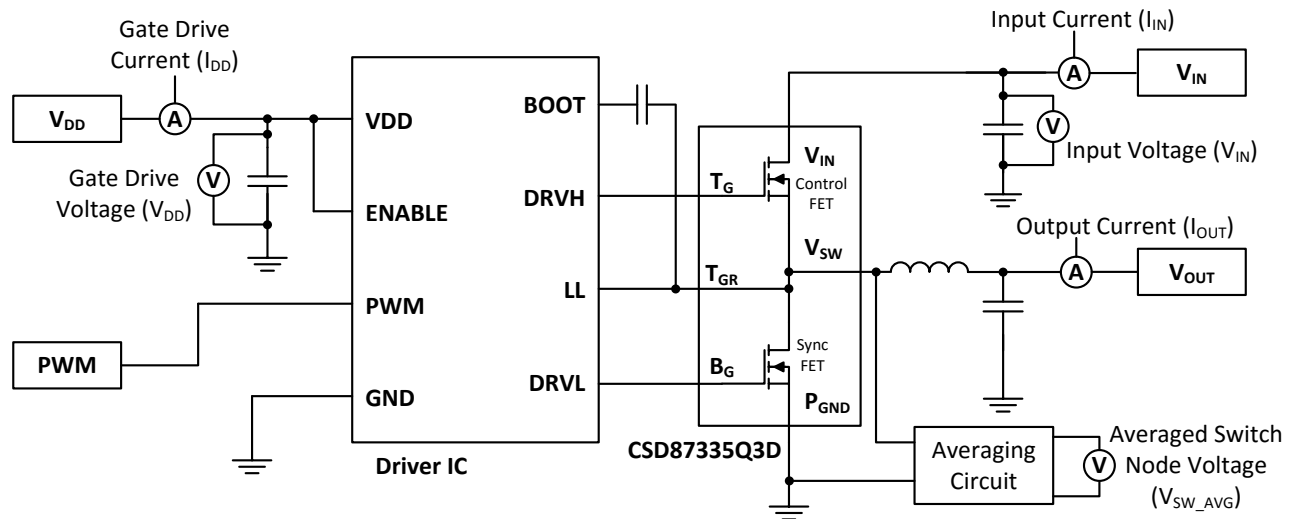
6.3 Safe Operating Curves (SOA)

The SOA curves in the CSD87335Q3D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. **Figure 4** outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (T) and 6 copper layers of 1-oz copper thickness.

6.4 Normalized Curves

The normalized curves in the CSD87335Q3D data sheet provides guidance on the power loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change in system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the power loss curve and the change in temperature is subtracted from the SOA curve.

Normalized Curves (continued)



Copyright © 2017, Texas Instruments Incorporated

Figure 31. Typical Application

6.5 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see [Design Example](#) section). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

6.5.1 Design Example

Operating conditions:

- Output current = 15 A
- Input voltage = 14 V
- Output voltage = 1.4 V
- Switching frequency = 750 kHz
- Inductor = 600 nH

6.5.2 Calculating Power Loss

- Power loss at 15 A = 1.92 W ([Figure 1](#))
- Normalized power loss for input voltage ≈ 1.01 ([Figure 6](#))
- Normalized power loss for output voltage ≈ 1.01 ([Figure 7](#))
- Normalized power loss for switching frequency ≈ 1.08 ([Figure 5](#))
- Normalized power loss for output inductor ≈ 1.01 ([Figure 8](#))
- **Final calculated power loss = $1.92 \text{ W} \times 1.01 \times 1.01 \times 1.08 \times 1.01 \approx 2.14 \text{ W}$**

6.5.3 Calculating SOA Adjustments

- SOA adjustment for input voltage $\approx 0.14^\circ\text{C}$ ([Figure 6](#))
- SOA adjustment for output voltage $\approx 0.17^\circ\text{C}$ ([Figure 7](#))
- SOA adjustment for switching frequency $\approx 1.32^\circ\text{C}$ ([Figure 5](#))
- SOA adjustment for output inductor $\approx 0.18^\circ\text{C}$ ([Figure 8](#))
- **Final calculated SOA adjustment = $0.14 + 0.17 + 1.32 + 0.18 \approx 1.81^\circ\text{C}$**

Calculating Power Loss and SOA (continued)

In the design example above, the estimated power loss of the CSD87335Q3D would increase to 2.14 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 1.81°C. [Figure 32](#) graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 1.81°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

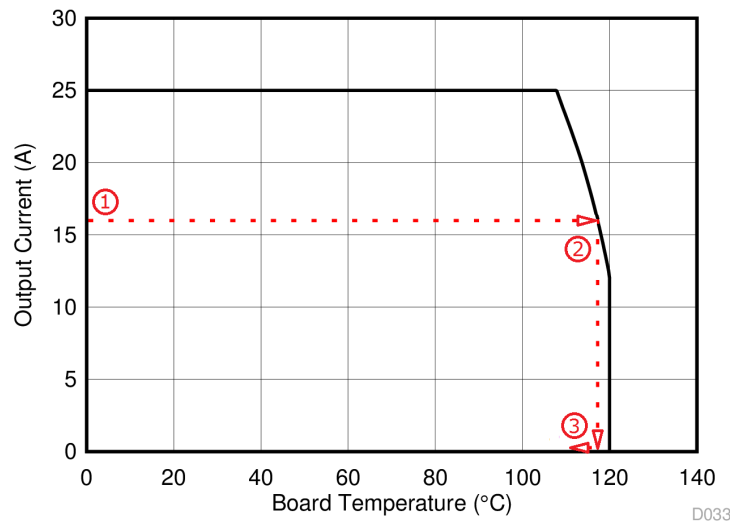


Figure 32. Power Block SOA

7 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. A brief description on how to address each parameter is provided.

7.1 Electrical Performance

The power block has the ability to switch voltages at rates greater than 10 kV/μs. Special care must be then taken with the PCB layout design and placement of the input capacitors, driver IC, and output inductor.

- The placement of the input capacitors relative to the power block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see [Figure 33](#)). The example in [Figure 33](#) uses 6 × 10-μF ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the power block, C5, C7, C19, and C8 should follow in order.
 - The driver IC should be placed relatively close to the power block gate pins. T_G and B_G should connect to the outputs of the driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the phase pin of the IC (sometimes called LX, LL, SW, PH, etc.). The bootstrap capacitor for the driver IC will also connect to this pin.
 - The switching node of the output inductor should be placed relatively close to the power block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a boost resistor or RC snubber can be an effective way to easily reduce the peak ring level. The recommended boost resistor value will range between 1 Ω to 4.7 Ω depending on the output characteristics of driver IC used in conjunction with the power block. The RC snubber values can range from 0.5 Ω to 2.2 Ω for the R and 330 pF to 2200 pF for the C. Please refer to [Snubber Circuits: Theory, Design and Application](#) (SLUP100) for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the Vsw node and PGND (see [Figure 33](#)).⁽¹⁾
- (1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

7.2 Thermal Performance

The power block has the ability to utilize the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in [Figure 33](#) uses vias with a 10-mil drill hole and a 16-mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

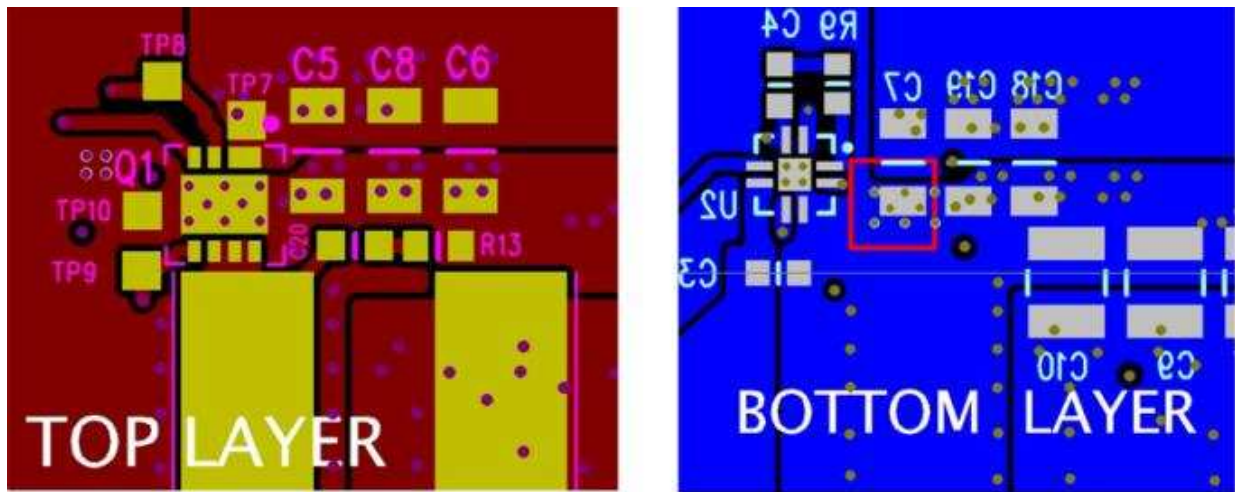


Figure 33. Recommended PCB Layout (Top Down)

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.5 Glossary

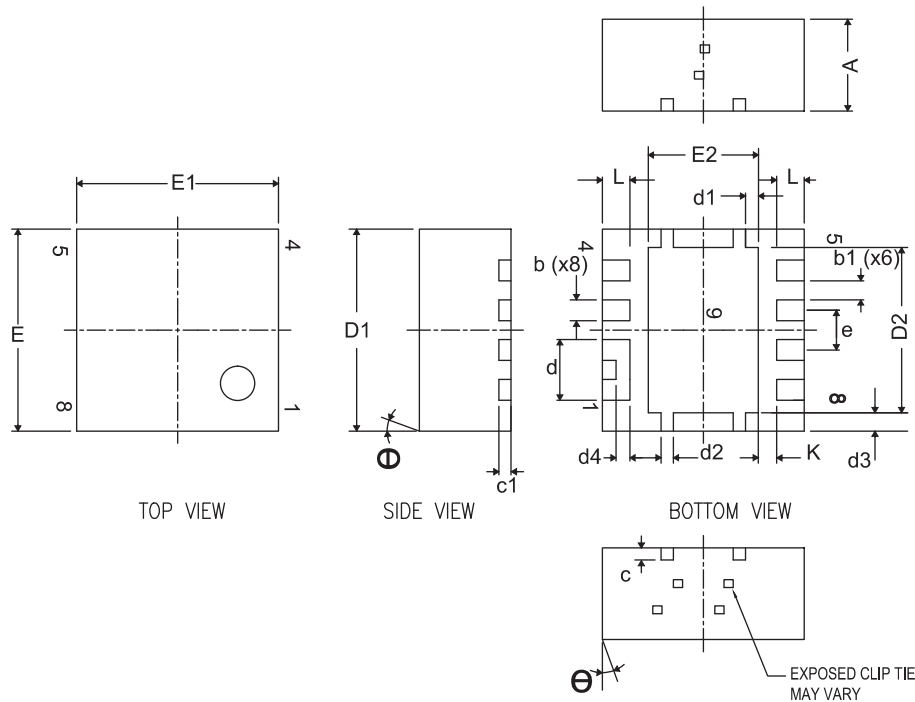
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

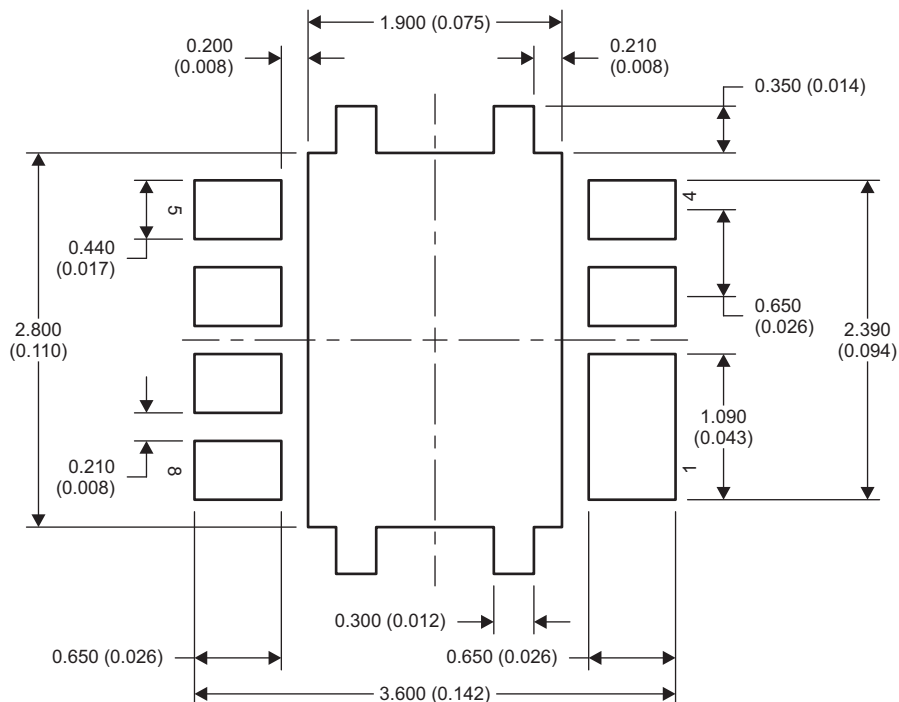
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Q3D Package Dimensions



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.400	1.500	0.055	0.059
b	0.280	0.400	0.011	0.016
b1	0.310 NOM		0.012 NOM	
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
d	0.940	1.040	0.037	0.041
d1	0.160	0.260	0.006	0.010
d2	0.150	0.250	0.006	0.010
d3	0.250	0.350	0.010	0.014
d4	0.175	0.275	0.007	0.011
D1	3.200	3.400	0.126	0.134
D2	2.650	2.750	0.104	0.108
E	3.200	3.400	0.126	0.134
E1	3.200	3.400	0.126	0.134
E2	1.750	1.850	0.069	0.073
e	0.650 TYP		0.026 TYP	
L	0.400	0.500	0.016	0.020
θ	0.00	—	—	—
K	0.300 TYP		0.012 TYP	

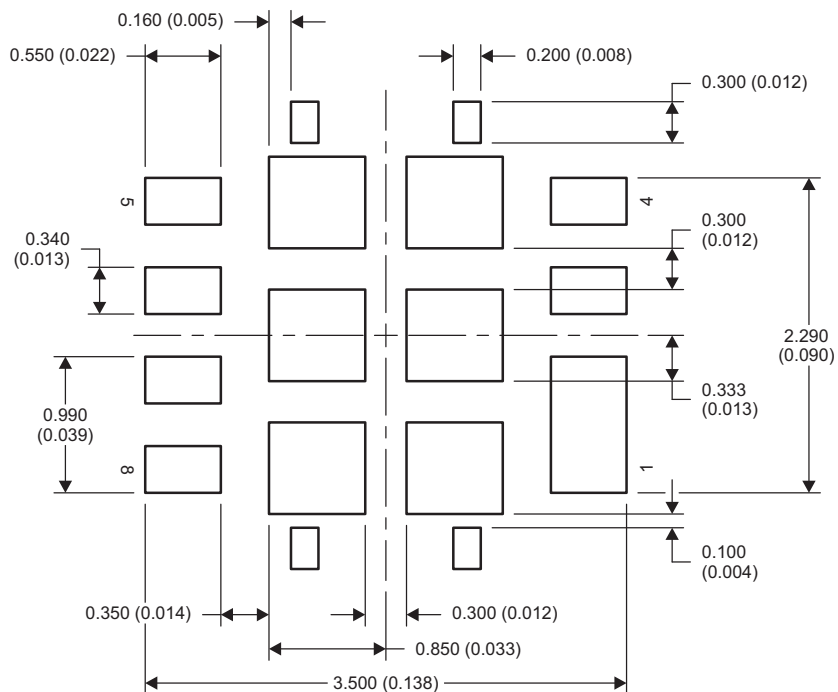
9.2 Land Pattern Recommendation



M0193-01

NOTE: Dimensions are in mm (inches).

9.3 Stencil Recommendation

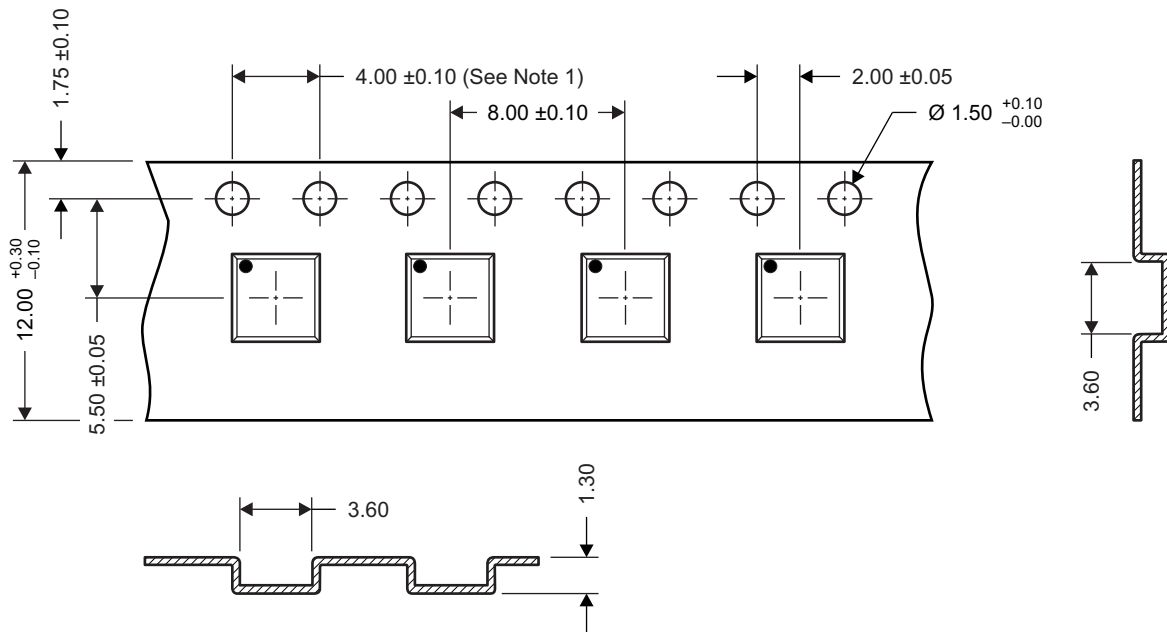


M0207-01

NOTE: Dimensions are in mm (inches).

For recommended circuit layout for PCB designs, see [Reducing Ringing Through PCB Layout Techniques \(SLPA005\)](#).

9.4 Q3D Tape and Reel Information



- NOTES: 1. 10-sprocket hole-pitch cumulative tolerance ± 0.2 .
 2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
 3. Material: black static-dissipative polystyrene.
 4. All dimensions are in mm, unless otherwise specified.
 5. Thickness: 0.3 ± 0.05 mm.
 6. MSL1 260°C (IR and convection) PbF reflow compatible.

M0144-01

9.5 Pin Configuration

POSITION	DESIGNATION
Pin 1	V_{IN}
Pin 2	V_{IN}
Pin 3	T_G
Pin 4	T_{GR}
Pin 5	B_G
Pin 6	V_{SW}
Pin 7	V_{SW}
Pin 8	V_{SW}
Pin 9	P_{GND}

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87335Q3D	ACTIVE	LSON-CLIP	DQZ	8	2500	Pb-Free (RoHS Exempt)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 150	87335D	Samples
CSD87335Q3DT	ACTIVE	LSON-CLIP	DQZ	8	250	Pb-Free (RoHS Exempt)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 150	87335D	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View CSD87335Q3D on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management