



**THE DATASHEET OF  
SN65LVEL11DGKR**



## 3.3 V ECL 1:2 Fanout Buffer

### FEATURES

- 1:2 ECL Fanout Buffer
- Operating Range
  - PECL  $V_{CC} = 3.0\text{ V to }3.8\text{ V}$  With  $V_{EE} = 0\text{ V}$
  - NECL:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0$  to  $-3.8\text{ V}$
- 5 ps Skew Between Outputs
- Support for Clock Frequencies > 2.0 GHz
- 265 ps Typical Propagation Delay
- Deterministic Output Value for Open Input Conditions or When Inputs =  $V_{EE}$
- Built-in Temperature Compensation
- Drop in Compatible to MC10LVEL11, MC100LVEL11
- Built-In Input Pull Down Resistors

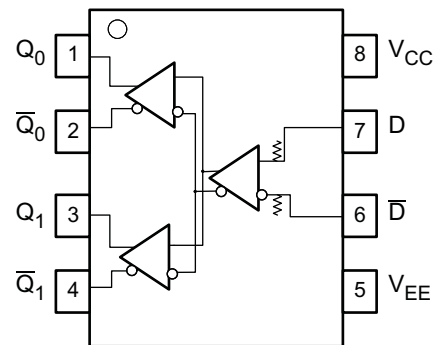
### APPLICATIONS

- Data and Clock Transmission Over Backplane
- Signaling Level Conversion

### DESCRIPTION

The SN65LVEL11 is a fully differential 1:2 ECL fanout buffer. The device includes circuitry to maintain a known logic level when inputs are in open condition. The SN65LVEL11 is functionally equivalent to SN65EL11 with improved performance. The SN65LVEL11 is housed in an industry standard SOIC-8 package and is also available in the TSSOP-8 package option.

### PINOUT ASSIGNMENT



**Table 1. Pin Description**

PIN	FUNCTION
D, $\bar{D}$	PECL/ECL data inputs
$Q_0, \bar{Q}_0, Q_1, \bar{Q}_1$	PECL/ECL outputs
$V_{CC}$	Positive supply
$V_{EE}$	Negative supply

### ORDERING INFORMATION<sup>(1)</sup>

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65LVEL11D	SN65LVEL11	SOIC	NiPdAu
SN65LVEL11DGK	SN65LVEL11	SOIC-TSSOP	NiPdAu

(1) Leaded device options not initially available. Contact TI sales representative for further details.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

PARAMETER	CONDITION	VALUE	UNIT
Absolute PECL mode supply voltage, $V_{CC}$	$V_{EE} = 0\text{ V}$	6	V
Absolute NECL mode power supply, $V_{EE}$	$V_{CC} = 0\text{ V}$	–6	V
PECL mode input voltage	$V_{EE} = 0\text{ V}; V_I \leq V_{CC}$	6	V
NECL mode input voltage	$V_{CC} = 0\text{ V}; V_I \geq V_{EE}$	–6	V
Output current	Continuous	50	mA
	Surge	100	
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING $T_A < 25^\circ\text{C}$ (mW)	THERMAL RESISTANCE, JUNCTION TO AMBIENT NO AIRFLOW	DERATING FACTOR $T_A > 25^\circ\text{C}$ (mW/°C)	POWER RATING $T_A = 85^\circ\text{C}$ (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

## THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
$\theta_{JB}$	Junction-to Board Thermal Resistance	SOIC	79	°C/W
		SOIC-TSSOP	120	
$\theta_{JC}$	Junction-to Case Thermal Resistance	SOIC	98	°C/W
		SOIC-TSSOP	74	

## KEY ATTRIBUTES

CHARACTERISTICS	VALUE
Internal input pull down resistor	75 k $\Omega$
Moisture sensitivity level	Level 1
Flammability rating (Oxygen Index: 28 to 34)	UL 94 V-0 at 0.125 in
ESD-HBM	4 kV
ESD-machine model	200 V
ESD-charge device model	2 kV
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test	

**LVPECL DC CHARACTERISTICS<sup>(1)</sup> ( $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0.0\text{ V}$ )<sup>(2)</sup>**

CHARACTERISTICS		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$I_{CC}$	Power Supply Current		20	25		20	25		21	25	mA
$V_{OH}$	Output HIGH Voltage <sup>(3)</sup>	2215		2420	2215	2286	2420	2215		2420	mV
$V_{OL}$	Output LOW Voltage <sup>(3)</sup>	1470		1680	1470	1584	1680	1470		1680	mV
$V_{IH}$	Input High Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
$V_{IHCMR}$	Input HIGH voltage common mode range (Differential) <sup>(4)</sup>										V
		$V_{pp} < 500\text{ mV}$	1.2	3.1	1.1		3.1	1.1		3.1	
		$V_{pp} > 500\text{ mV}$	1.4	3.1	1.3		3.1	1.3		3.1	
$I_{IH}$	Input HIGH Current			150			150			150	μA
$I_{IL}$	Input LOW current										μA
		D	0.5		0.5			0.5			
		$\bar{D}$	–600		–600			–600			

- (1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$
- (3) Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
- (4)  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PP}$  min and 1 V.

**LVPNECL DC CHARACTERISTICS<sup>(1)</sup> ( $V_{EE} = -3.3\text{ V}$ ;  $V_{CC} = 0.0\text{ V}$ ;) <sup>(2)</sup>**

CHARACTERISTICS		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$I_{EE}$	Power supply current		20	25		20	25		21	25	mA
$V_{OH}$	Output HIGH voltage <sup>(3)</sup>	–1085		–880	–1085	–1013	–880	–1085		–880	mV
$V_{OL}$	Output LOW voltage <sup>(3)</sup>	–1830		–1620	–1830	–1722	–1620	–1830		–1620	mV
$V_{IH}$	Input high voltage (Single-Ended)	–1165		–880	–1165		–880	–1165		–880	mV
$V_{IL}$	Input LOW voltage (Single-Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
$V_{IHCMR}$	Input HIGH voltage common mode range (Differential) <sup>(4)</sup>										V
		$V_{pp} < 500\text{ mV}$	–2.1	–0.2	–2.2		–0.2	–2.2		–0.2	
		$V_{pp} > 500\text{ mV}$	–1.9	–0.2	–2.0		–0.2	–2.0		–0.2	
$I_{IH}$	Input HIGH current			150			150			150	μA
$I_{IL}$	Input LOW current										μA
		D	0.5		0.5			0.5			
		$\bar{D}$	–600		–600			–600			

- (1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
- (3) Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
- (4)  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PP}$  min and 1 V.

**AC CHARACTERISTICS** <sup>(1)</sup>( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$ )<sup>(2)</sup>

CHARACTERISTIC		-40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$f_{MAX}$	Max switching frequency <sup>(3)</sup> See Figure 6	2.9			2.7			2.4			GHz
$t_{PLH}/t_{PHL}$	Propagation delay to output	235		350	235		350	235		350	ps
$t_{SKEW}$	Within device skew <sup>(4)</sup>	10 18			10 18			10 18			ps
	Device to device skew <sup>(5)</sup>	10 25			10 25			10 25			ps
	Duty cycle skew <sup>(6)</sup>	5 15			5 15			5 15			ps
$t_{JITTER}$	Random clock jitter (RMS)	0.2			0.2			0.2			ps
$V_{PP}$	Input swing <sup>(7)</sup>	200		1000	200		1000	200		1000	mV
$t_r/t_f$	Output rise/fall times Q (20%–80%)	150		300	150		300	150		300	ps

- (1) Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2)  $V_{EE}$  can vary  $\pm 0.3\text{ V}$
- (3) Maximum switching frequency measured at output amplitude of 300 mVpp.
- (4) Within-device skew is defined as identical transitions on similar paths through a device.
- (5) Device-Device Skew is defined as identical transitions at identical Vcc levels.
- (6) Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.
- (7)  $V_{PP(min)}$  is the minimum input swing for which AC parameters are assured.

**Typical Termination for Output Driver**

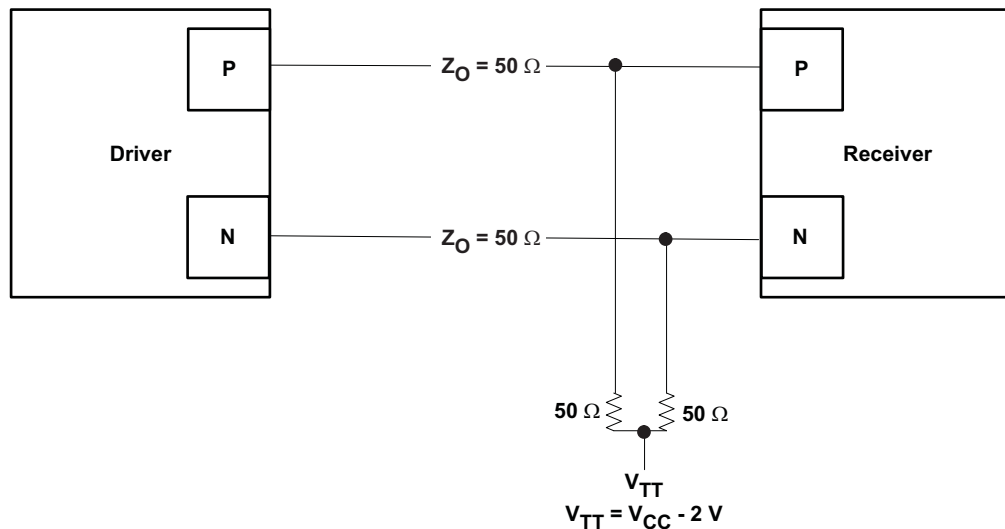


Figure 1. Termination for Output Driver

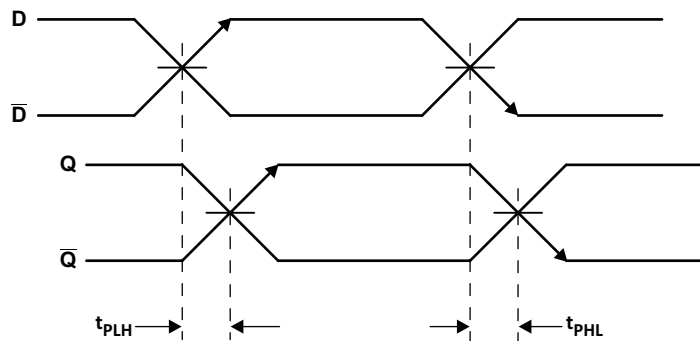


Figure 2. Propagation Delay

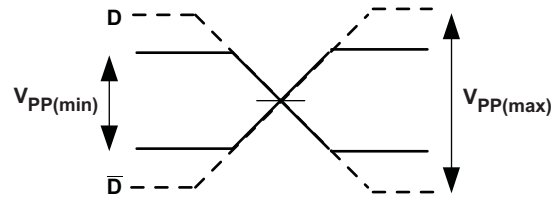


Figure 3. Input Voltage Swing

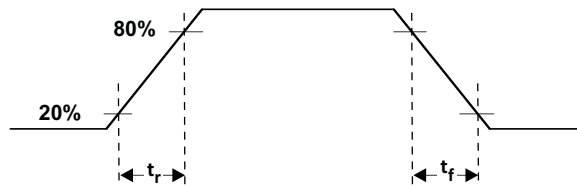


Figure 4. Output Rise and Fall Times

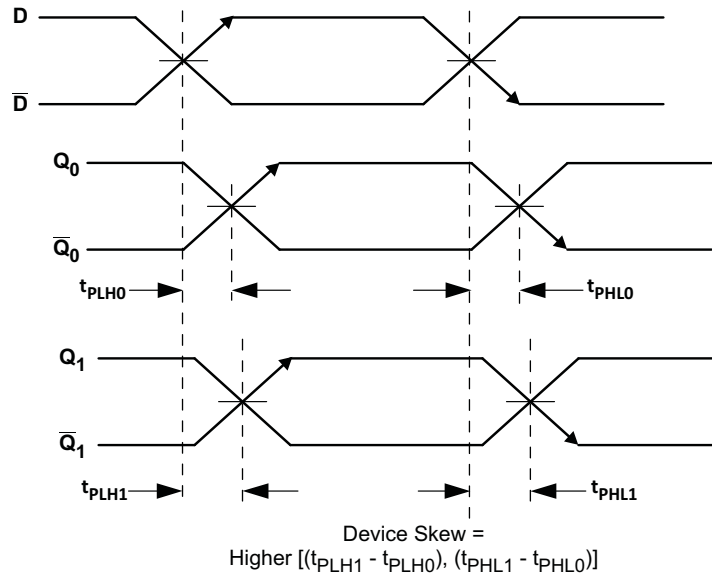


Figure 5. Device Skew

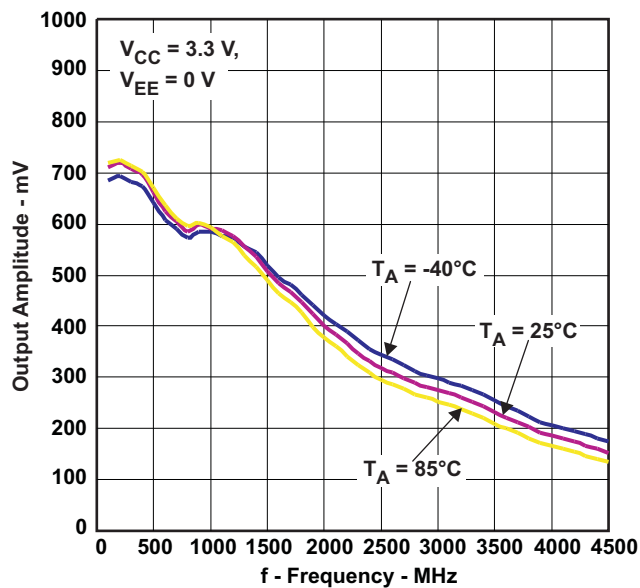


Figure 6. Output Amplitude vs Frequency

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVEL11D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL11	<a href="#">Samples</a>
SN65LVEL11DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SINI	<a href="#">Samples</a>
SN65LVEL11DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   Call TI	Level-1-260C-UNLIM	-40 to 85	SINI	<a href="#">Samples</a>
SN65LVEL11DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL11	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVEL11DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVEL11DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVEL11DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
SN65LVEL11DR	SOIC	D	8	2500	367.0	367.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

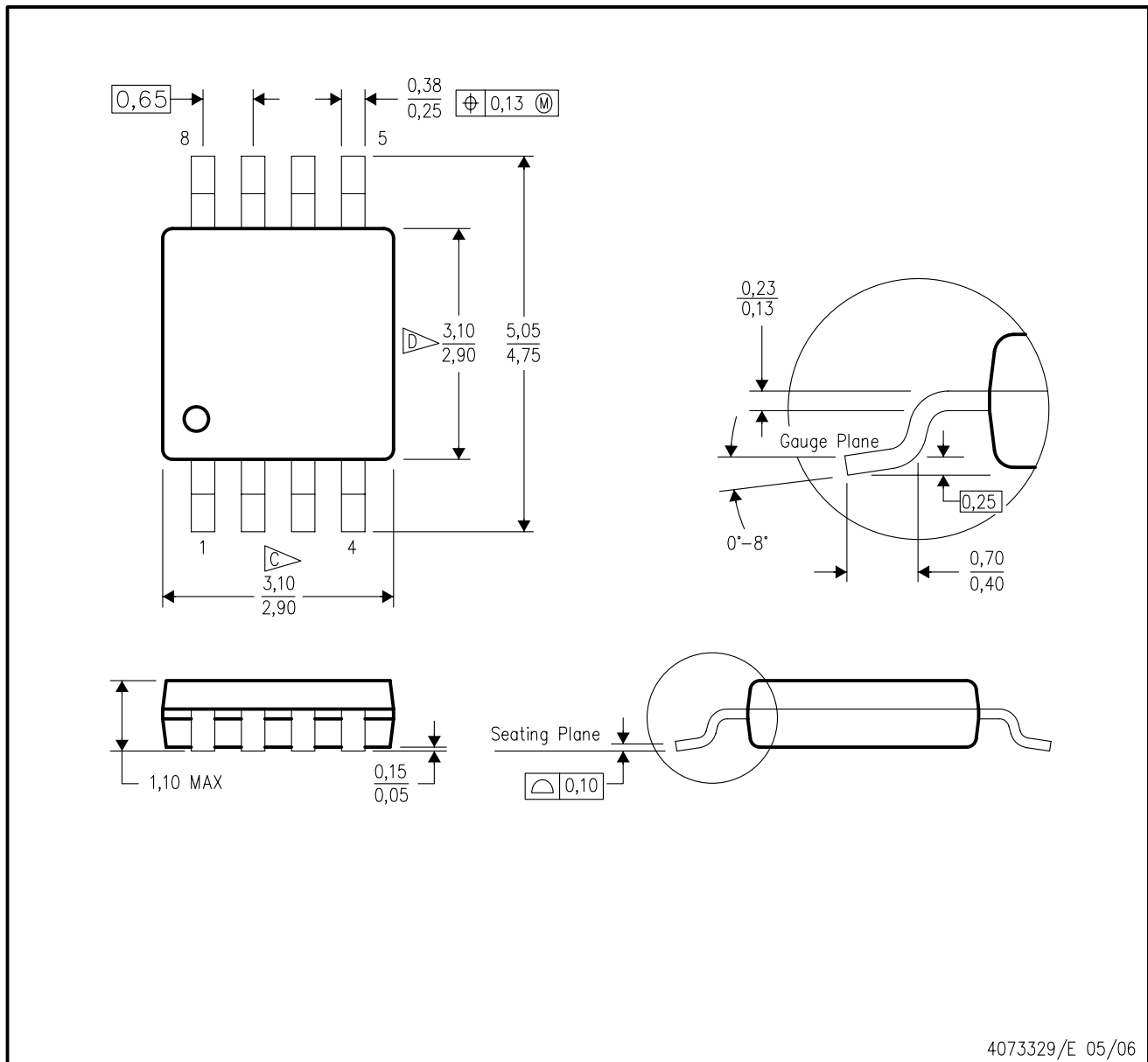
4214825/C 02/2019

NOTES: (continued)

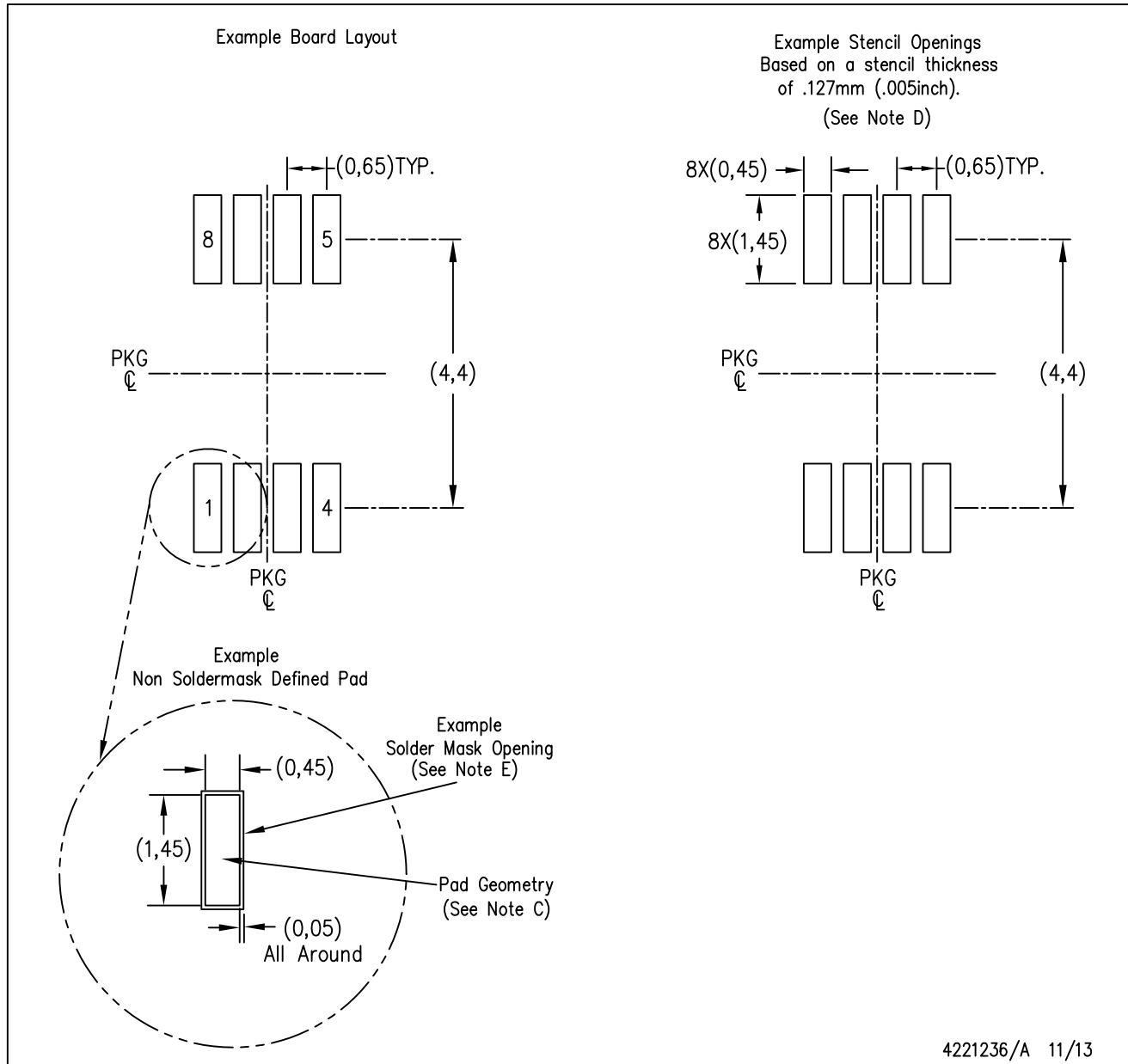
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2019, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View SN65LVEL11DGKR on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management