



# THE DATASHEET OF STP5N105K5



## N-channel 1050 V, 2.9 $\Omega$ typ., 3 A MDmesh™ K5 Power MOSFET in a TO-220 package

Datasheet - production data

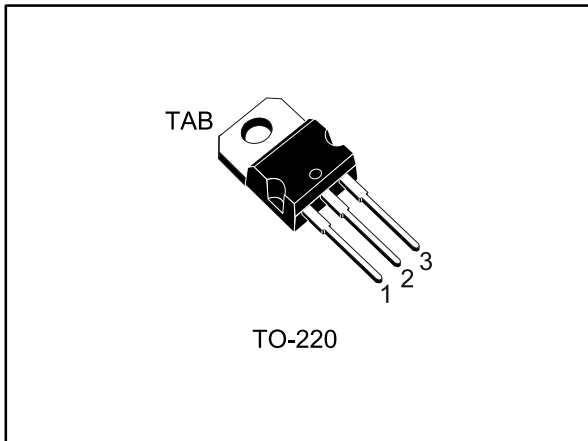
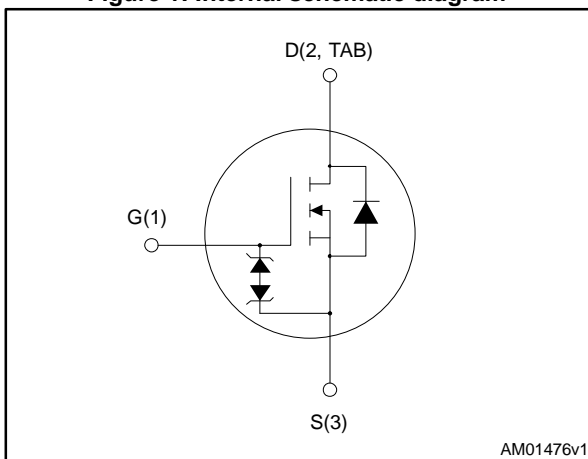


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STP5N105K5	1050 V	3.5 $\Omega$	3 A	85 W

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This N-channel Zener-protected Power MOSFET is designed using ST's revolutionary avalanche-rugged very high voltage MDmesh™ K5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STP5N105K5	5N105K5	TO-220	Tube

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>GS</sub>	Gate- source voltage	± 30	V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	3	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	2	A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	12	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	85	W
I <sub>AR</sub>	Max current during repetitive or single pulse avalanche	1	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>J</sub> = 25 °C, I <sub>D</sub> =I <sub>AS</sub> , V <sub>DD</sub> = 50 V)	85	mJ
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	4.5	V/ns
dv/dt <sup>(3)</sup>	MOSFET dv/dt ruggedness	50	V/ns
T <sub>j</sub>	Operating junction temperature	- 55 to 150	°C
T <sub>stg</sub>	Storage temperature		

**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area

<sup>(2)</sup>I<sub>SD</sub> ≤ 3 A, di/dt ≤ 100 A/μs, V<sub>DS(peak)</sub> ≤ V<sub>(BR)DSS</sub>

<sup>(3)</sup>V<sub>DS</sub> ≤ 840 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case max	1.47	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-amb max	62.5	°C/W

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified).

**Table 4: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0, I <sub>D</sub> = 1 mA	1050			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0, V <sub>DS</sub> = 1050 V			1	μA
		V <sub>GS</sub> = 0, V <sub>DS</sub> = 1050 V, T <sub>C</sub> = 125 °C			50	μA
I <sub>GSS</sub>	Gate body leakage current	V <sub>DS</sub> = 0, V <sub>GS</sub> = ± 20 V			±10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100 μA	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.5 A		2.9	3.5	Ω

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iSS</sub>	Input capacitance	V <sub>DS</sub> = 100 V, f = 1 MHz, V <sub>GS</sub> = 0	-	210	-	pF
C <sub>oSS</sub>	Output capacitance		-	16	-	pF
C <sub>rSS</sub>	Reverse transfer capacitance		-	0.5	-	pF
C <sub>o(tr)</sub> <sup>(1)</sup>	Equivalent capacitance time related	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0 to 840 V	-	26	-	pF
C <sub>o(er)</sub> <sup>(2)</sup>	Equivalent capacitance energy related		-	10	-	pF
R <sub>G</sub>	Intrinsic gate resistance	f = 1MHz open drain	-	9	-	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 840 V, I <sub>D</sub> = 3 A	-	12.5	-	nC
Q <sub>gs</sub>	Gate-source charge	V <sub>GS</sub> = 10 V	-	2	-	nC
Q <sub>gd</sub>	Gate-drain charge	Figure 16: "Gate charge test circuit"	-	9.5	-	nC

**Notes:**

<sup>(1)</sup>Time related is defined as a constant equivalent capacitance giving the same charging time as C<sub>oSS</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

<sup>(2)</sup>Energy related is defined as a constant equivalent capacitance giving the same stored energy as C<sub>oSS</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 525V, I <sub>D</sub> = 1.5 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V Figure 18: "Unclamped inductive load test circuit"	-	15.5	-	ns
t <sub>r</sub>	Rise time		-	8.5	-	ns
t <sub>d(off)</sub>	Turn-off delay time		-	31	-	ns
t <sub>f</sub>	Fall time		-	24	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		3	A
$I_{SDM}$	Source-drain current (pulsed)				12	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 3\text{ A}, V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 3\text{ A}, V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , <i>Figure 17: " Test circuit for inductive load switching and diode recovery times"</i>	-	400		ns
$Q_{rr}$	Reverse recovery charge		-	2.3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	12		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 3\text{ A}, V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , $T_j = 150\text{ }^\circ\text{C}$ <i>Figure 17: " Test circuit for inductive load switching and diode recovery times"</i>	-	560		ns
$Q_{rr}$	Reverse recovery charge		-	3.1		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	11		A

**Notes:**

<sup>(1)</sup>Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}, I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

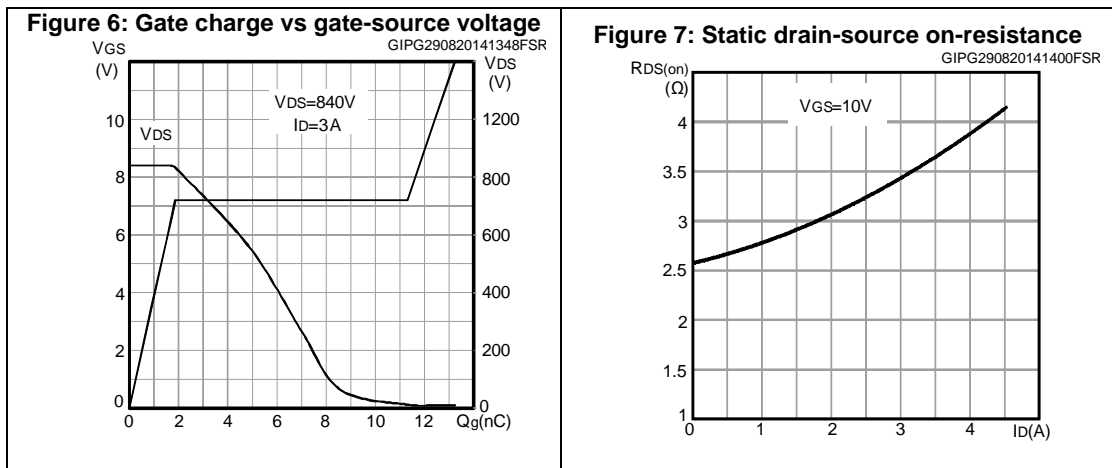
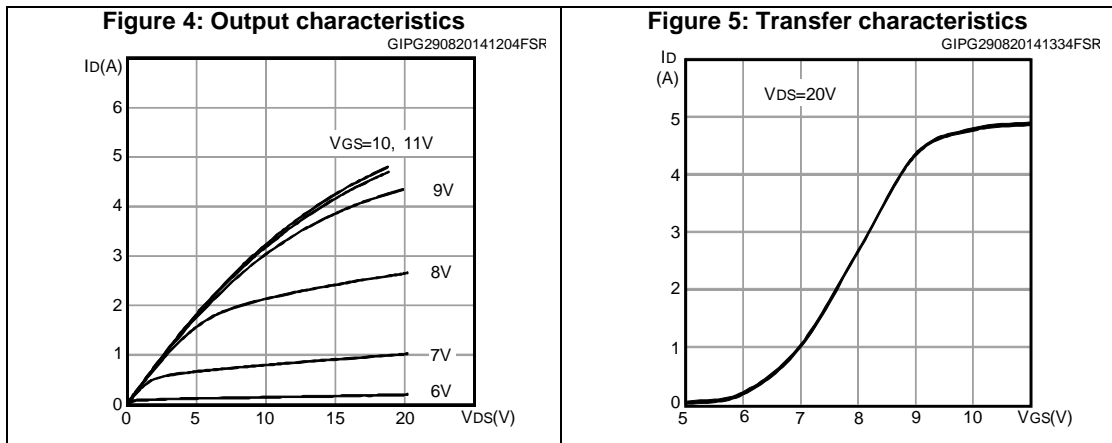
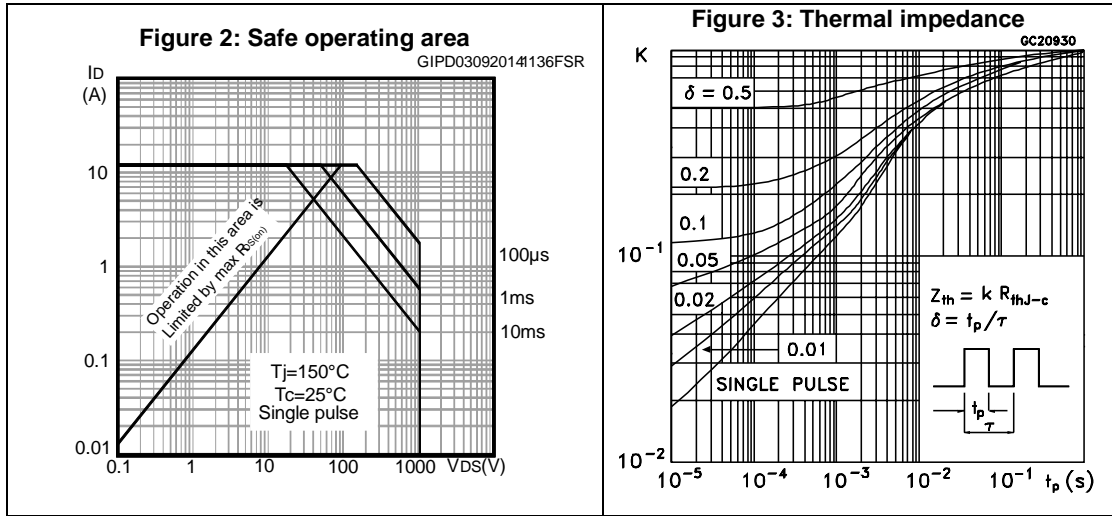


Figure 8: Capacitance variations

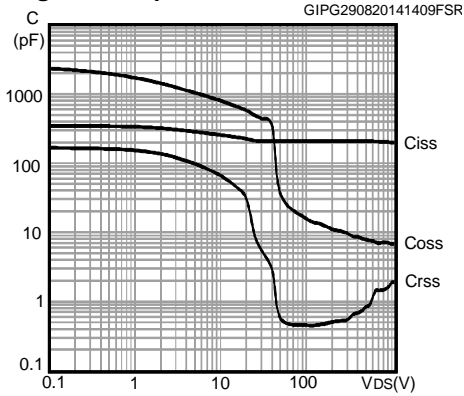


Figure 9: Source-drain diode forward characteristics

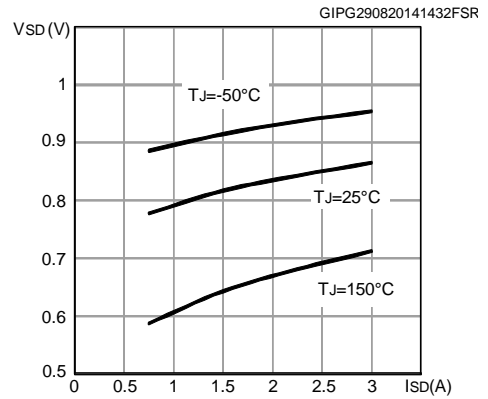


Figure 10: Normalized gate threshold voltage vs temperature

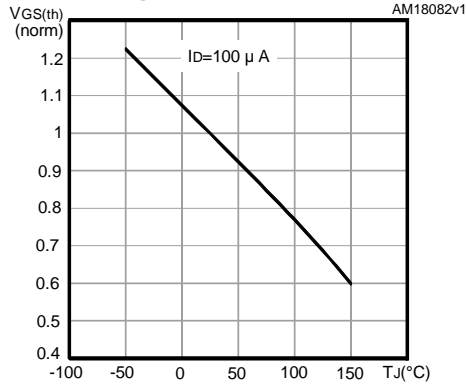


Figure 11: Normalized on-resistance vs temperature

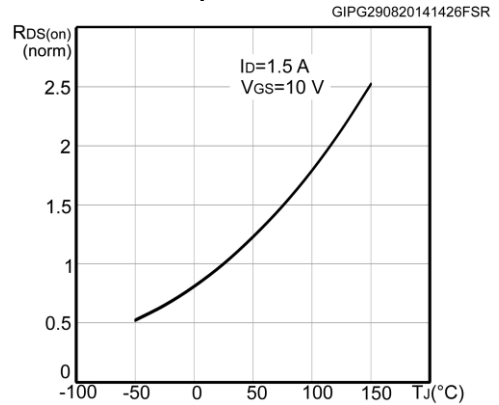


Figure 12: Normalized V(BR)DSS vs temperature

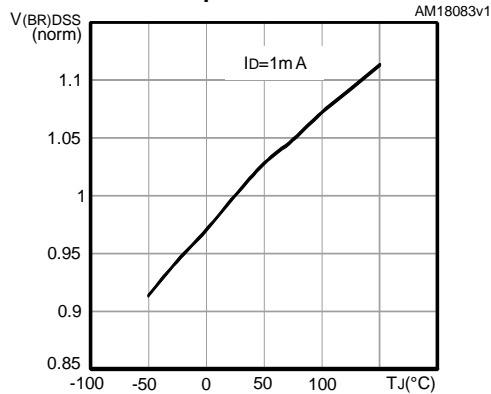


Figure 13: Maximum avalanche energy

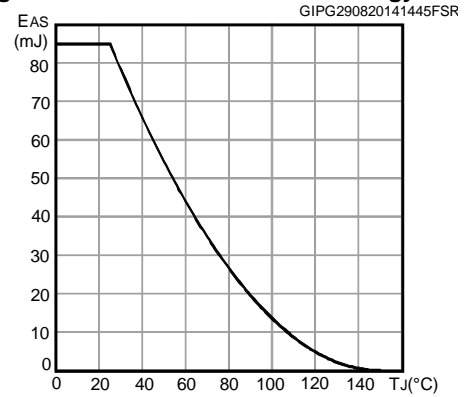
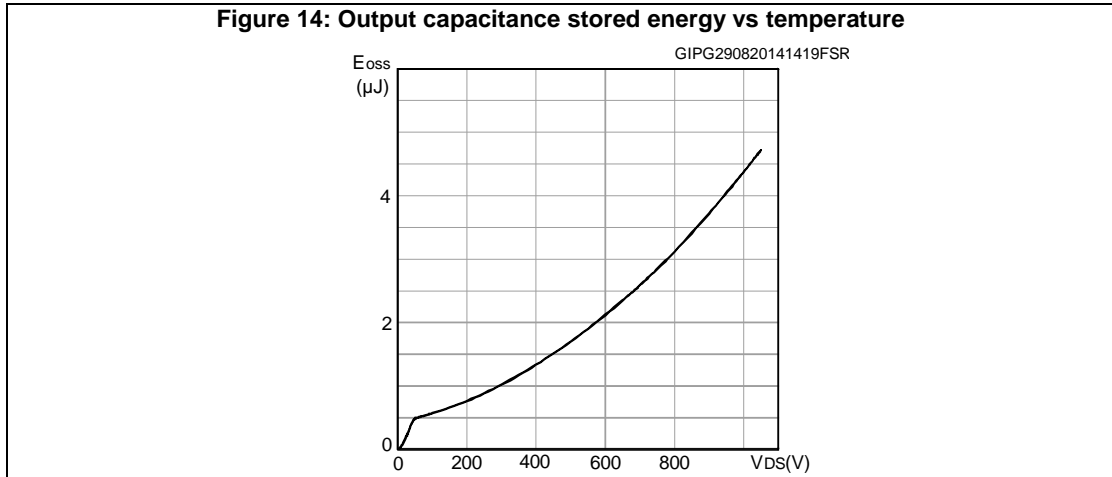
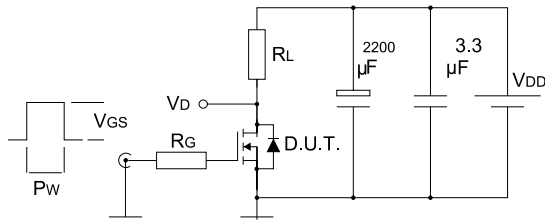


Figure 14: Output capacitance stored energy vs temperature



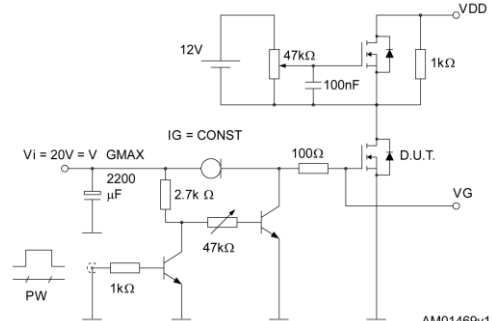
### 3 Test circuits

**Figure 15: Switching times test circuit for resistive load**



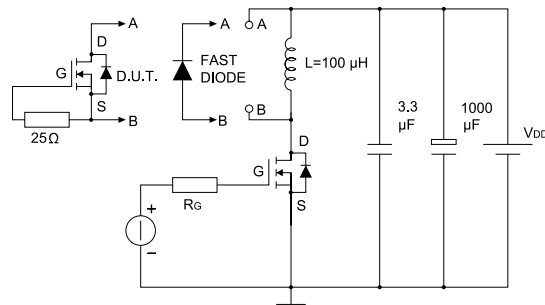
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**Figure 16: Gate charge test circuit**



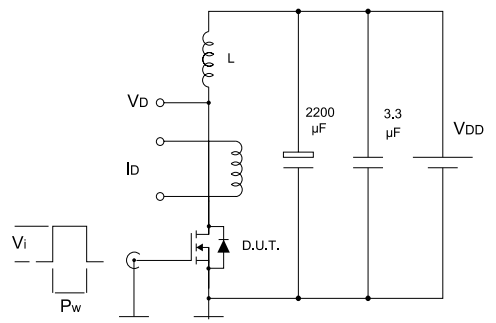
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**Figure 17: Test circuit for inductive load switching and diode recovery times**



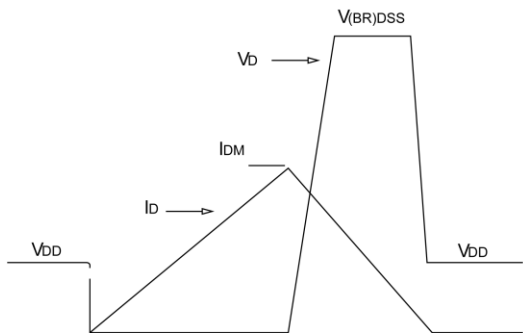
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**Figure 18: Unclamped inductive load test circuit**



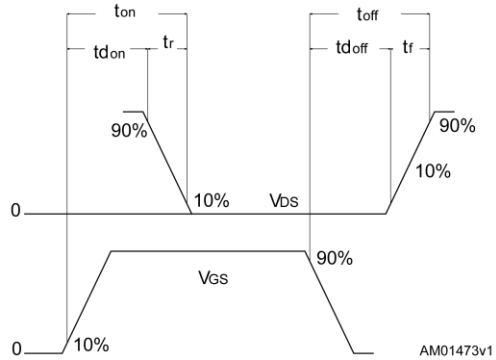
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**Figure 19: Unclamped inductive waveform**



AM01472v1

**Figure 20: Switching time waveform**



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-220 package mechanical data

Figure 21: TO-220 type A package outline

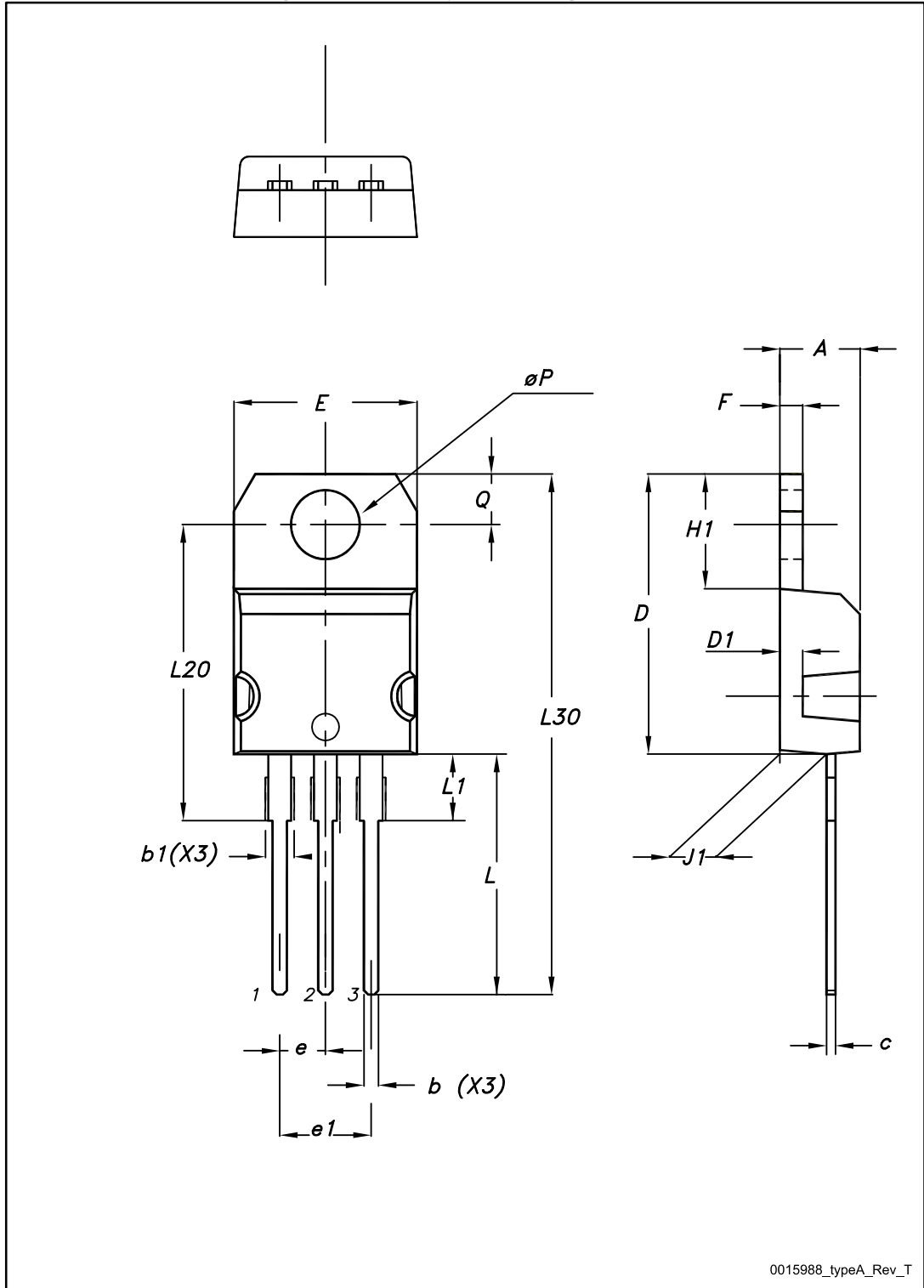


Table 9: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ÆP	3.75		3.85
Q	2.65		2.95

## 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
17-Jul-2014	1	First release.
03-Sep-2014	2	Document status promoted from preliminary to production data. Added <i>Section 3.1: "Electrical characteristics (curves)"</i> Minor text changes.
15-Oct-2014	3	Updated <i>Figure 6: "Gate charge vs gate-source voltage"</i> and <i>Figure 8: "Capacitance variations"</i>

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