



# THE DATASHEET OF MSP430F2330TRHAT



## MIXED SIGNAL MICROCONTROLLER

### FEATURES

- **Low Supply Voltage Range: 1.8 V to 3.6 V**
- **Ultra-Low Power Consumption**
  - Active Mode: 270  $\mu$ A at 1 MHz, 2.2 V
  - Standby Mode: 0.7  $\mu$ A
  - Off Mode (RAM Retention): 0.1  $\mu$ A
- **Ultra-Fast Wake-Up From Standby Mode in Less Than 1  $\mu$ s**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Basic Clock Module Configurations**
  - Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to  $\pm 1\%$
  - Internal Very-Low-Power Low-Frequency (LF) Oscillator
  - 32-kHz Crystal
  - High-Frequency (HF) Crystal up to 16 MHz
  - Resonator
  - External Digital Clock Source
  - External Resistor
- **16-Bit Timer\_A With Three Capture/Compare Registers**
- **16-Bit Timer\_B With Three Capture/Compare Registers**
- **On-Chip Comparator for Analog Signal Compare Function or Slope Analog-to-Digital (A/D) Conversion**
- **Universal Serial Communication Interface**
  - Enhanced UART Supporting Auto Baudrate Detection (LIN)
  - IrDA Encoder and Decoder
  - Synchronous SPI
  - I<sup>2</sup>C™
- **Brownout Detector**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **Bootstrap Loader**
- **On-Chip Emulation Module**
- **Family Members Include:**
  - **MSP430F2330**
    - 8KB + 256B Flash Memory
    - 1KB RAM
  - **MSP430F2350**
    - 16KB + 256B Flash Memory
    - 2KB RAM
  - **MSP430F2370**
    - 32KB + 256B Flash Memory
    - 2KB RAM
- **Available in 40-Pin QFN Package and 49-Pin Die-Sized BGA Package (See [Table 1](#))**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide (SLAU144)***

### DESCRIPTION

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1  $\mu$ s.

The MSP430F23x0 series is an ultra-low-power microcontroller with two built-in 16-bit timers, one universal serial communication interface (USCI), a versatile analog comparator, and 32 I/O pins.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**Table 1. Available Options**

| T <sub>A</sub> | PACKAGED DEVICES <sup>(1)(2)</sup> |                          |
|----------------|------------------------------------|--------------------------|
|                | PLASTIC 49-PIN DSBGA (YFF)         | PLASTIC 40-PIN QFN (RHA) |
| -40°C to 85°C  | MSP430F2330IYFF                    | MSP430F2330IRHA          |
|                | MSP430F2350IYFF                    | MSP430F2350IRHA          |
|                | MSP430F2370IYFF                    | MSP430F2370IRHA          |
| -40°C to 105°C | -                                  | MSP430F2330TRHA          |
|                | -                                  | MSP430F2350TRHA          |
|                | -                                  | MSP430F2370TRHA          |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

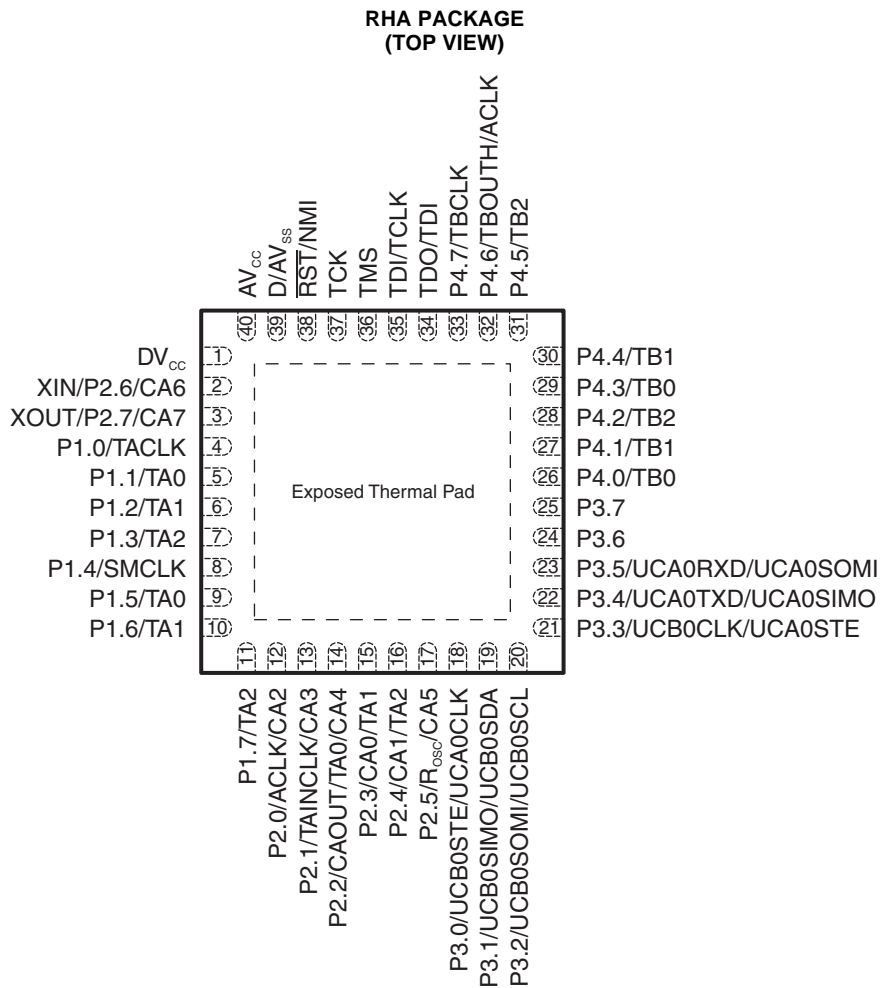
(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

## Development Tool Support

All MSP430 microcontrollers include an Embedded Emulation Module (EEM) that allows advanced debugging and programming through easy-to-use development tools. Recommended hardware options include:

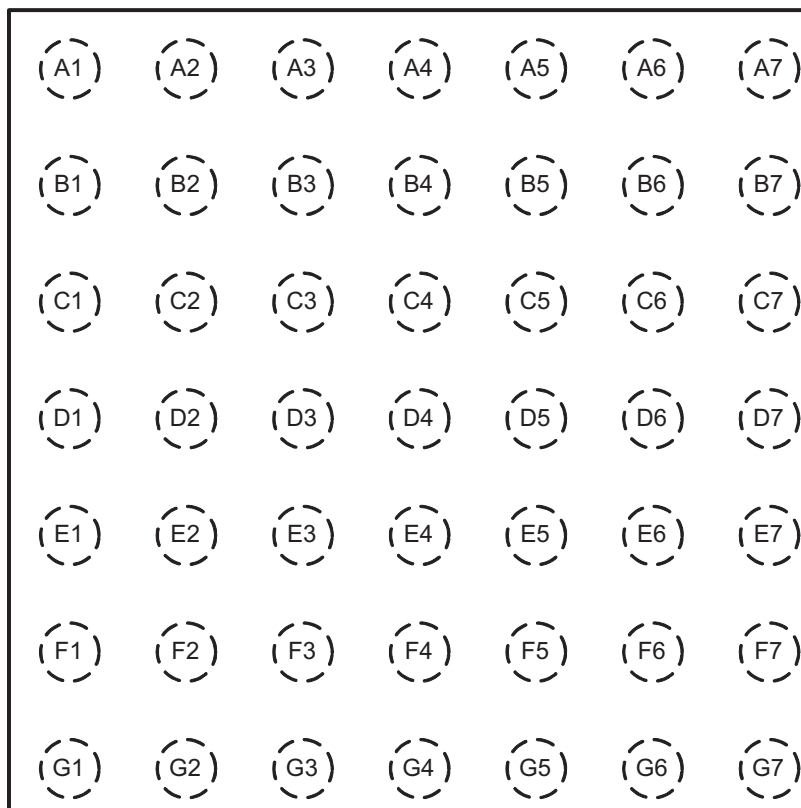
- Debugging and Programming Interface with Target Board
  - MSP-FET430U23X0 (RHA package)
- Debugging and Programming Interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (Parallel Port)
- Target Board
  - MSP-TS430QFN23X0 (RHA package)
- Production Programmer
  - MSP-GANG430

Device Pinout, RHA Package



## Device Pinout, YFF Package

**YFF PACKAGE  
(TOP VIEW)**



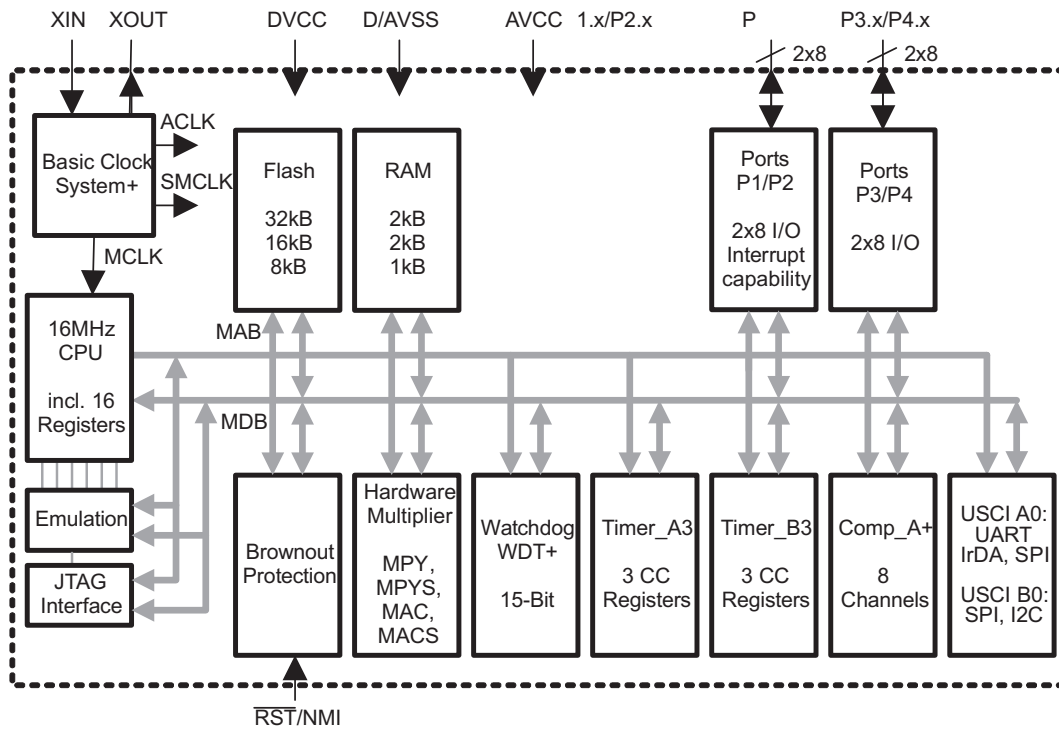
### Package Dimensions

The package dimensions for this YFF package are shown in the following table. See the package drawing at the end of this data sheet for more details.

**Table 2. YFF Package Dimensions**

| PACKAGED DEVICES                                      | D              | E              |
|---|----------------|----------------|
| MSP430F2370IYFF<br>MSP430F2350IYFF<br>MSP430F2330IYFF | 3.20 ± 0.05 mm | 3.20 ± 0.05 mm |

Functional Block Diagram



**Table 3. Terminal Functions**

| TERMINAL<br>NAME             | YFF | RHA | I/O | DESCRIPTION   |
|------------------------------|-----|-----|-----|---|
| DV <sub>CC</sub>             | B3  | 1   |     | Digital supply voltage, positive terminal. Supplies all digital parts.  |
| XIN/P2.6/CA6                 | A2  | 2   | I/O | Input terminal of crystal oscillator/general-purpose digital I/O pin/Comparator_A input                             |
| XOUT/P2.7/CA7                | A3  | 3   | I/O | Output terminal of crystal oscillator/general-purpose digital I/O pin/Comparator_A input                            |
| P1.0/TACLK                   | B4  | 4   | I/O | General-purpose digital I/O pin/Timer_A, clock signal TACLK input   |
| P1.1/TA0                     | C4  | 5   | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output                                 |
| P1.2/TA1                     | A5  | 6   | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output                                 |
| P1.3/TA2                     | B5  | 7   | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output                                 |
| P1.4/SMCLK                   | A6  | 8   | I/O | General-purpose digital I/O pin/SMCLK signal output   |
| P1.5/TA0                     | B6  | 9   | I/O | General-purpose digital I/O pin/Timer_A, compare: Out0 output   |
| P1.6/TA1                     | A7  | 10  | I/O | General-purpose digital I/O pin/Timer_A, compare: Out1 output   |
| P1.7/TA2                     | B7  | 11  | I/O | General-purpose digital I/O pin/Timer_A, compare: Out2 output   |
| P2.0/ACLK/CA2                | C5  | 12  | I/O | General-purpose digital I/O pin/ACLK output/Comparator_A input  |
| P2.1/TAINCLK/CA3             | C7  | 13  | I/O | General-purpose digital I/O pin/Timer_A, clock signal at INCLK/Comparator_A input                                   |
| P2.2/CAOUT/TA0/CA4           | C6  | 14  | I/O | General-purpose digital I/O pin/Comparator_A output/Timer_A, capture: CCI0B input/Comparator_A input                |
| P2.3/CA0/TA1                 | D7  | 15  | I/O | General-purpose digital I/O pin/Comparator_A input/Timer_A, compare: Out1 output                                    |
| P2.4/CA1/TA2                 | D6  | 16  | I/O | General-purpose digital I/O pin/Comparator_A input/Timer_A, compare: Out2 output                                    |
| P2.5/R <sub>OSC</sub> /CA5   | E7  | 17  | I/O | General-purpose digital I/O pin/input for external resistor defining the DCO nominal frequency/Comparator_A input   |
| P3.0/UCB0STE/<br>UCA0CLK     | E6  | 18  | I/O | General-purpose digital I/O pin/USCIB0 slave transmit enable/USCIA clock input/output                               |
| P3.1/UCB0SIMO/<br>UCB0SDA    | F7  | 19  | I/O | General-purpose digital I/O pin/USCIB0 slave in/master out in SPI mode, SDA I2C data in I2C mode                    |
| P3.2/UCB0SOMI/<br>UCB0SCL    | F6  | 20  | I/O | General-purpose digital I/O pin/USCIB0 slave out/master in in SPI mode, SCL I2C clock in I2C mode                   |
| P3.3/UCB0CLK/<br>UCA0STE     | G7  | 21  | I/O | General-purpose digital I/O/USCIB0 clock input/output, USCIA0 slave transmit enable                                 |
| P3.4/UCA0TXD/<br>UCA0SIMO    | G6  | 22  | I/O | General-purpose digital I/O pin/USCIA0 transmit data output in UART mode, slave data in/master out in SPI mode      |
| P3.5/UCA0RXD/<br>UCA0SOMI    | G5  | 23  | I/O | General-purpose digital I/O pin/USCIA0 receive data input in UART mode, slave data out/master in in SPI mode        |
| P3.6                         | F5  | 24  | I/O | General-purpose digital I/O pin   |
| P3.7                         | G4  | 25  | I/O | General-purpose digital I/O pin   |
| P4.0/TB0                     | F4  | 26  | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI0A input, compare: Out0 output                                 |
| P4.1/TB1                     | G3  | 27  | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI1A input, compare: Out1 output                                 |
| P4.2/TB2                     | G2  | 28  | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI2A input, compare: Out2 output                                 |
| P4.3/TB0                     | F3  | 29  | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI0B input, compare: Out0 output                                 |
| P4.4/TB1                     | G1  | 30  | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI1B input, compare: Out1 output                                 |
| P4.5/TB2                     | F1  | 31  | I/O | General-purpose digital I/O pin/Timer_B, compare: Out2 output   |
| P4.6/TBOUTH/ACLK             | F2  | 32  | I/O | General-purpose digital I/O pin/switch all PWM digital outputs to high impedance - Timer_B3: TB0 to TB2/ACLK output |
| P4.7/TBCLK                   | E2  | 33  | I/O | General-purpose digital I/O pin/input clock TBCLK - Timer_B3  |
| TDO/TDI                      | E1  | 34  | I/O | Test data output port. TDO/TDI data output or programming data input terminal                                       |
| TDI/TCLK                     | D1  | 35  | I   | Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.                           |
| TMS                          | D2  | 36  | I   | Test mode select. TMS is used as an input port for device programming and test.                                     |
| TCK                          | C1  | 37  | I   | Test clock. TCK is the clock input port for device programming and test.  |
| $\overline{\text{RST}}$ /NMI | C2  | 38  | I   | Reset input, nonmaskable interrupt input port.  |
| D/AV <sub>SS</sub>           | B1  | 39  |     | Digital/analog supply voltage, negative terminal  |

**Table 3. Terminal Functions (continued)**

| TERMINAL         |   |     |     | DESCRIPTION   |
|------------------|---|-----|-----|---|
| NAME             | YFF   | RHA | I/O |   |
| AV <sub>CC</sub> | A1  | 40  |     | Analog supply voltage, positive terminal  |
| QFN Pad          | -   | NA  | NA  | QFN package pad. Connection to D/AV <sub>SS</sub> recommended.                          |
| Reserved         | A4,<br>B2,<br>C3,<br>D3,<br>D4,<br>D5,<br>E3,<br>E4, E5 | -   | NA  | BGA package GND balls. Connection to DV <sub>SS</sub> /AV <sub>SS</sub> is recommended. |

## SHORT-FORM DESCRIPTION

### CPU

The MSP430™ CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.

### Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. [Table 4](#) shows examples of the three types of instruction formats; [Table 5](#) shows the address modes.

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC/R0     |
| Stack Pointer            | SP/R1     |
| Status Register          | SR/CG1/R2 |
| Constant Generator       | CG2/R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

**Table 4. Instruction Word Formats**

| INSTRUCTION FORMAT                       | EXAMPLE   | OPERATION             |
|--|-----------|-----------------------|
| Dual operands, source-destination        | ADD R4,R5 | R4 + R5 → R5          |
| Single operands, destination only        | CALL R8   | PC → (TOS), R8 → PC   |
| Relative jump, unconditional/conditional | JNE       | Jump-on-equal bit = 0 |

**Table 5. Address Mode Descriptions**

| ADDRESS MODE           | S <sup>(1)</sup> | D <sup>(2)</sup> | SYNTAX          | EXAMPLE          | OPERATION                     |
|------------------------|------------------|------------------|-----------------|------------------|-------------------------------|
| Register               | ✓                | ✓                | MOV Rs,Rd       | MOV R10,R11      | R10 → R11                     |
| Indexed                | ✓                | ✓                | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6)  | M(2+R5) → M(6+R6)             |
| Symbolic (PC relative) | ✓                | ✓                | MOV EDE,TONI    |                  | M(EDE) → M(TONI)              |
| Absolute               | ✓                | ✓                | MOV &MEM,&TCDAT |                  | M(MEM) → M(TCDAT)             |
| Indirect               | ✓                |                  | MOV @Rn,Y(Rm)   | MOV @R10,Tab(R6) | M(R10) → M(Tab+R6)            |
| Indirect autoincrement | ✓                |                  | MOV @Rn+,Rm     | MOV @R10+,R11    | M(R10) → R11<br>R10 + 2 → R10 |
| Immediate              | ✓                |                  | MOV #X,TONI     | MOV #45,TONI     | #45 → M(TONI)                 |

(1) S = source

(2) D = destination

## Operating Modes

The MSP430 microcontrollers have one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled.
  - ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 1 (LPM1)
  - CPU is disabled ACLK and SMCLK remain active. MCLK is disabled.
  - DCO dc-generator is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator remains enabled.
  - ACLK remains active.
- Low-power mode 3 (LPM3)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator is disabled.
  - ACLK remains active.
- Low-power mode 4 (LPM4)
  - CPU is disabled.
  - ACLK is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator is disabled.
  - Crystal oscillator is stopped.

## Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0xFFFF to 0xFFC0. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0xFFFFE) contains 0xFFFF (for example, if flash is not programmed), the CPU goes into LPM4 immediately after power up.

**Table 6. Interrupt Vector Addresses**

| INTERRUPT SOURCE  | INTERRUPT FLAG  | SYSTEM INTERRUPT                                   | WORD ADDRESS     | PRIORITY        |
|---|---|--|------------------|-----------------|
| Power-up<br>External Reset<br>Watchdog<br>Flash key violation<br>PC out of range <sup>(1)</sup> | PORIFG<br>RSTIFG<br>WDTIFG<br>KEYV<br>(2)                 | Reset  | 0xFFFFE          | 31, highest     |
| NMI<br>Oscillator Fault<br>Flash memory access violation  | NMIIFG<br>OFIFG<br>ACCVIFG <sup>(2)(3)</sup>              | (non)–maskable<br>(non)–maskable<br>(non)–maskable | 0xFFFFC          | 30              |
| Timer_B3  | TBCCR0 CCIFG <sup>(4)</sup>                               | maskable   | 0xFFFFA          | 29              |
| Timer_B3  | TBCCR1 and TBCCR2,<br>CCIFGs, TBIFG <sup>(2)(4)</sup>     | maskable   | 0xFFFF8          | 28              |
| Comparator_A+   | CAIFG   | maskable   | 0xFFFF6          | 27              |
| Watchdog timer  | WDTIFG  | maskable   | 0xFFFF4          | 26              |
| Timer_A3  | TACCR0 CCIFG <sup>(4)</sup>                               | maskable   | 0xFFFF2          | 25              |
| Timer_A3  | TACCR1 CCIFG,<br>TACCR2 CCIFG,<br>TAIFG <sup>(2)(4)</sup> | maskable   | 0xFFFF0          | 24              |
| USCI_A0/USCI_B0 Receive<br>USCI_B0 I2C Status   | UCA0RXIFG,<br>UCB0RXIFG <sup>(2)(5)</sup>                 | maskable   | 0xFFEE           | 23              |
| USCI_A0/USCI_B0 Transmit<br>USCI_B0 I2C Receive/Transmit  | UCA0TXIFG,<br>UCB0TXIFG <sup>(2)(6)</sup>                 | maskable   | 0xFFEC           | 22              |
|   |   |  | 0xFFEA           | 21              |
|   |   |  | 0xFFE8           | 20              |
| I/O port P2 (eight flags)   | P2IFG.0 to P2IFG.7 <sup>(2)(3)</sup>                      | maskable   | 0xFFE6           | 19              |
| I/O port P1 (eight flags)   | P1IFG.0 to P1IFG.7 <sup>(2)(3)</sup>                      | maskable   | 0xFFE4           | 18              |
|   |   |  | 0xFFE2           | 17              |
|   |   |  | 0xFFE0           | 16              |
| See <sup>(7)</sup>  |   |  | 0xFFDE           | 15              |
| See <sup>(8)</sup>  |   |  | 0xFFDC to 0xFFC0 | 14 to 0, lowest |

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0x0000 to 0x01FF) or from within unused address range.

(2) Multiple source flags

(3) (non)–maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot. Nonmaskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.

(4) Interrupt flags are located in the module.

(5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG

(6) In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG

(7) This location is used as bootstrap loader security key (BSLSKEY).

A 0xAA55 at this location disables the BSL completely.


A zero (0x0) disables the erasure of the flash if an invalid password is supplied.

(8) The interrupt vectors at addresses 0xFFDC to 0xFFC0 are not used in this device and can be used for regular program code if necessary.





## Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

### Legend





|   |   |
|---|---|
| rw  | Bit can be read and written.                            |
| rw-0, 1   | Bit can be read and written. It is Reset or Set by PUC. |
| rw-(0), (1)   | Bit can be read and written. It is Reset or Set by POR. |
|  | SFR bit is not present in device.                       |

**Table 7. Interrupt Enable 1**

| Address | 7   | 6   | 5      | 4     | 3  | 2   | 1    | 0     |
|---------|---|---|--------|-------|--|---|------|-------|
| 00h     |  |  | ACCVIE | NMIIE |  |  | OFIE | WDTIE |
|         |   |   | rw-0   | rw-0  |  |   | rw-0 | rw-0  |




|        |  |
|--------|--|
| WDTIE  | Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode. |
| OFIE   | Oscillator fault interrupt enable  |
| NMIIE  | (Non)maskable interrupt enable   |
| ACCVIE | Flash access violation interrupt enable  |

**Table 8. Interrupt Enable 2**

| Address | 7   | 6   | 5   | 4   | 3        | 2        | 1        | 0        |
|---------|---|---|---|---|----------|----------|----------|----------|
| 01h     |  |  |  |  | UCB0TXIE | UCB0RXIE | UCA0TXIE | UCA0RXIE |
|         |   |   |   |   | rw-0     | rw-0     | rw-0     | rw-0     |





|          |                                   |
|----------|-----------------------------------|
| UCA0RXIE | USCI_A0 receive-interrupt enable  |
| UCA0TXIE | USCI_A0 transmit-interrupt enable |
| UCB0RXIE | USCI_B0 receive-interrupt enable  |
| UCB0TXIE | USCI_B0 transmit-interrupt enable |

**Table 9. Interrupt Flag Register 1**

| Address | 7   | 6   | 5   | 4      | 3      | 2      | 1     | 0      |
|---------|---|---|---|--------|--------|--------|-------|--------|
| 02h     |  |  |  | NMIIFG | RSTIFG | PORIFG | OFIFG | WDTIFG |
|         |   |   |   | rw-0   | rw-(0) | rw-(1) | rw-1  | rw-(0) |

|        |  |
|--------|--|
| WDTIFG | Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V <sub>CC</sub> power-up or a reset condition at $\overline{RST}/NMI$ pin in reset mode. |
| OFIFG  | Flag set on oscillator fault   |
| RSTIFG | External reset interrupt flag. Set on a reset condition at $\overline{RST}/NMI$ pin in reset mode. Reset on V <sub>CC</sub> power up.  |
| PORIFG | Power-on reset interrupt flag. Set on V <sub>CC</sub> power up.  |
| NMIIFG | Set via $\overline{RST}/NMI$ pin   |

**Table 10. Interrupt Flag Register 2**

| Address | 7   | 6   | 5   | 4   | 3         | 2         | 1         | 0         |
|---------|---|---|---|---|-----------|-----------|-----------|-----------|
| 03h     |  |  |  |  | UCB0TXIFG | UCB0RXIFG | UCA0TXIFG | UCA0RXIFG |
|         |   |   |   |   | rw-0      | rw-0      | rw-0      | rw-0      |

|           |                                 |
|-----------|---------------------------------|
| UCA0RXIFG | USCI_A0 receive-interrupt flag  |
| UCA0TXIFG | USCI_A0 transmit-interrupt flag |
| UCB0RXIFG | USCI_B0 receive-interrupt flag  |
| UCB0TXIFG | USCI_B0 transmit-interrupt flag |

## Memory Organization

**Table 11. Memory Organization**

|                        |           | <b>MSP430F2330</b> | <b>MSP430F2350</b> | <b>MSP430F2370</b> |
|------------------------|-----------|--------------------|--------------------|--------------------|
| Memory                 | Size      | 8KB Flash          | 16KB Flash         | 32KB               |
| Main: interrupt vector | Flash     | 0xFFFF - 0xFFC0    | 0xFFFF - 0xFFC0    | 0xFFFF - 0xFFC0    |
| Main: code memory      | Flash     | 0xFFFF - 0xE000    | 0xFFFF - 0xC000    | 0xFFFF - 0x8000    |
| Information memory     | Size      | 256 Byte           | 256 Byte           | 256 Byte           |
|                        | Flash     | 0x10FF - 0x1000    | 0x10FF - 0x1000    | 0x10FF - 0x1000    |
| Boot memory            | Size      | 1KB                | 1KB                | 1KB                |
|                        | ROM       | 0x0FFF - 0x0C00    | 0x0FFF - 0x0C00    | 0x0FFF - 0x0C00    |
| RAM                    | Size      | 1KB                | 2KB                | 2KB                |
|                        |           | 0x5FF - 0x0200     | 0x9FF - 0x0200     | 0x09FF - 0x0200    |
| Peripherals            | 16-bit    | 0x01FF - 0x0100    | 0x01FF - 0x0100    | 0x01FF - 0x0100    |
|                        | 8-bit     | 0x00FF - 0x0010    | 0x00FF - 0x0010    | 0x00FF - 0x0010    |
|                        | 8-bit SFR | 0x000F - 0x0000    | 0x000F - 0x0000    | 0x000F - 0x0000    |

## Bootstrap Loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide*, literature number [SLAU319](#).

**Table 12. BSL Function Pins**

| <b>BSL FUNCTION</b> | <b>YFF PACKAGE PINS</b> | <b>RHA PACKAGE PINS</b> |
|---------------------|-------------------------|-------------------------|
| Data transmit       | C4 - P1.1               | 5 - P1.1                |
| Data receive        | C6 - P2.2               | 14 - P2.2               |

## Flash Memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset, segment A is protected against programming and erasing. It can be unlocked, but care should be taken not to erase this segment if the device-specific calibration data is required.

## Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide (SLAU144)*.

## Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator, an internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1  $\mu$ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal, or the internal very-low-power LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

**Table 13. DCO Calibration Data, Provided From Factory In Flash Info Memory Segment A**

| DCO FREQUENCY | CALIBRATION REGISTER | SIZE | ADDRESS |
|---------------|----------------------|------|---------|
| 1 MHz         | CALBC1_1MHZ          | byte | 0x10FF  |
|               | CALBC0_1MHZ          | byte | 0x10FE  |
| 8 MHz         | CALBC1_8MHZ          | byte | 0x10FD  |
|               | CALBC0_8MHZ          | byte | 0x10FC  |
| 12 MHz        | CALBC1_12MHZ         | byte | 0x10FB  |
|               | CALBC0_12MHZ         | byte | 0x10FA  |
| 16 MHz        | CALBC1_16MHZ         | byte | 0x10F9  |
|               | CALBC0_16MHZ         | byte | 0x10F8  |

## Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

## Digital I/O

There are four 8-bit I/O ports implemented—ports P1, P2, P3, and P4:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all eight bits of port P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

The MSP430F23x0 devices provide 32 total port I/O pins available externally. See the device pinout for more information.

## Watchdog Timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

## Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16, 16×8, 8×16, and 8×8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

## Comparator\_A+

The primary function of the comparator\_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

## Timer\_A3

Timer\_A3 is a 16-bit timer/counter with three capture/compare registers. Timer\_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 14. Timer\_A3 Signal Connections**

| INPUT PIN NUMBER |           | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |           |
|------------------|-----------|---------------------|-------------------|--------------|----------------------|-------------------|-----------|
| YFF              | RHA       |                     |                   |              |                      | YFF               | RHA       |
| B4 – P1.0        | 4 – P1.0  | TACLK               | TACLK             | Timer        | NA                   |                   |           |
|                  |           | ACLK                | ACLK              |              |                      |                   |           |
|                  |           | SMCLK               | SMCLK             |              |                      |                   |           |
| C7 – P2.1        | 13 – P2.1 | TAINCLK             | INCLK             |              |                      |                   |           |
| C4 – P1.1        | 5 – P1.1  | TA0                 | CCI0A             | CCR0         | TA0                  | C4 – P1.1         | 5 – P1.1  |
| C6 – P2.2        | 14 – P2.2 | TA0                 | CCI0B             |              |                      | B6 – P1.5         | 9 – P1.5  |
|                  |           | V <sub>SS</sub>     | GND               |              |                      |                   |           |
|                  |           | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |           |
| A5 – P1.2        | 6 – P1.2  | TA1                 | CCI1A             | CCR1         | TA1                  | A5 – P1.2         | 6 – P1.2  |
|                  |           | CAOUT (internal)    | CCI1B             |              |                      | A7 – P1.6         | 10 – P1.6 |
|                  |           | V <sub>SS</sub>     | GND               |              |                      | D7 – P2.3         | 15 – P2.3 |
|                  |           | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |           |
| B5 – P1.3        | 7 – P1.3  | TA2                 | CCI2A             | CCR2         | TA2                  | B5 – P1.3         | 7 – P1.3  |
|                  |           | ACLK (internal)     | CCI2B             |              |                      | B7 – P1.7         | 11 – P1.7 |
|                  |           | V <sub>SS</sub>     | GND               |              |                      | D6 – P2.4         | 16 – P2.4 |
|                  |           | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |           |

## Timer\_B3

Timer\_B3 is a 16-bit timer/counter with three capture/compare registers. Timer\_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 15. Timer\_B3 Signal Connections**

| INPUT PIN NUMBER |           | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |           |
|------------------|-----------|---------------------|-------------------|--------------|----------------------|-------------------|-----------|
| YFF              | RHA       |                     |                   |              |                      | YFF               | RHA       |
| E2 – P4.7        | 33 – P4.7 | TBCLK               | TACLK             | Timer        | NA                   |                   |           |
|                  |           | ACLK                | ACLK              |              |                      |                   |           |
|                  |           | SMCLK               | SMCLK             |              |                      |                   |           |
|                  |           | TBCLK               | INCLK             |              |                      |                   |           |
| F4 – P4.0        | 26 – P4.0 | TB0                 | CCI0A             | CCR0         | TB0                  | F4 – P4.0         | 26 – P4.0 |
| F3 – P4.3        | 29 – P4.3 | TB0                 | CCI0B             |              |                      | F3 – P4.3         | 29 – P4.3 |
|                  |           | V <sub>SS</sub>     | GND               |              |                      |                   |           |
|                  |           | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |           |
| G3 – P4.1        | 27 – P4.1 | TA1                 | CCI1A             | CCR1         | TB1                  | G3 – P4.1         | 27 – P4.1 |
| G1 – P4.4        | 30 – P4.4 | TB1                 | CCI1B             |              |                      | G1 – P4.4         | 30 – P4.4 |
|                  |           | V <sub>SS</sub>     | GND               |              |                      |                   |           |
|                  |           | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |           |
| G2 – P4.2        | 28 – P4.2 | TB2                 | CCI2A             | CCR2         | TB2                  | G2 – P4.2         | 28 – P4.2 |
|                  |           | ACLK (internal)     | CCI2B             |              |                      | F1 – P4.5         | 31 – P4.5 |
|                  |           | V <sub>SS</sub>     | GND               |              |                      |                   |           |
|                  |           | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |           |

## Universal Serial Communications Interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I2C and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI\_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

USCI\_B0 provides support for SPI (3 or 4 pin) and I2C.

## Peripheral File Map

### Table 16. Peripherals With Word Access

| MODULE                     | REGISTER NAME                        | SHORT NAME | ADDRESS OFFSET |
|----------------------------|--------------------------------------|------------|----------------|
| <b>Timer_B3</b>            | Capture/compare register             | TBCCR2     | 0x0196         |
|                            | Capture/compare register             | TBCCR1     | 0x0194         |
|                            | Capture/compare register             | TBCCR0     | 0x0192         |
|                            | Timer_B register                     | TBR        | 0x0190         |
|                            | Capture/compare control              | TBCCTL2    | 0x0186         |
|                            | Capture/compare control              | TBCCTL1    | 0x0184         |
|                            | Capture/compare control              | TBCCTL0    | 0x0182         |
|                            | Timer_B control                      | TBCTL      | 0x0180         |
|                            | Timer_B interrupt vector             | TBIV       | 0x011E         |
| <b>Timer_A3</b>            | Capture/compare register             | TACCR2     | 0x0176         |
|                            | Capture/compare register             | TACCR1     | 0x0174         |
|                            | Capture/compare register             | TACCR0     | 0x0172         |
|                            | Timer_A register                     | TAR        | 0x0170         |
|                            | Capture/compare control              | TACCTL2    | 0x0166         |
|                            | Capture/compare control              | TACCTL1    | 0x0164         |
|                            | Capture/compare control              | TACCTL0    | 0x0162         |
|                            | Timer_A control                      | TACTL      | 0x0160         |
|                            | Timer_A interrupt vector             | TAIV       | 0x012E         |
| <b>Flash Memory</b>        | Flash control 3                      | FCTL3      | 0x012C         |
|                            | Flash control 2                      | FCTL2      | 0x012A         |
|                            | Flash control 1                      | FCTL1      | 0x0128         |
| <b>Hardware Multiplier</b> | Sum extend                           | SUMEXT     | 0x013E         |
|                            | Result high word                     | RESHI      | 0x013C         |
|                            | Result low word                      | RESLO      | 0x013A         |
|                            | Second operand                       | OP2        | 0x0138         |
|                            | Multiply signed +accumulate/operand1 | MACS       | 0x0136         |
|                            | Multiply+accumulate/operand1         | MAC        | 0x0134         |
|                            | Multiply signed/operand1             | MPYS       | 0x0132         |
|                            | Multiply unsigned/operand1           | MPY        | 0x0130         |
| <b>Watchdog Timer+</b>     | Watchdog/timer control               | WDTCTL     | 0x0120         |

### Table 17. Peripherals With Byte Access

| MODULE         | REGISTER NAME              | SHORT NAME | ADDRESS OFFSET |
|----------------|----------------------------|------------|----------------|
| <b>USCI_B0</b> | USCI_B0 transmit buffer    | UCB0TXBUF  | 0x06F          |
|                | USCI_B0 receive buffer     | UCB0RXBUF  | 0x06E          |
|                | USCI_B0 status             | UCB0STAT   | 0x06D          |
|                | USCI_B0 bit rate control 1 | UCB0BR1    | 0x06B          |
|                | USCI_B0 bit rate control 0 | UCB0BR0    | 0x06A          |
|                | USCI_B0 control 1          | UCB0CTL1   | 0x069          |
|                | USCI_B0 control 0          | UCB0CTL0   | 0x068          |
|                | USCI_B0 I2C slave address  | UCB0SA     | 0x011A         |
|                | USCI_B0 I2C own address    | UCB0OA     | 0x0118         |

**Table 17. Peripherals With Byte Access (continued)**

| MODULE                     | REGISTER NAME                  | SHORT NAME | ADDRESS OFFSET |
|----------------------------|--------------------------------|------------|----------------|
| <b>USCI_A0</b>             | USCI_A0 transmit buffer        | UCA0TXBUF  | 0x0067         |
|                            | USCI_A0 receive buffer         | UCA0RXBUF  | 0x0066         |
|                            | USCI_A0 status                 | UCA0STAT   | 0x0065         |
|                            | USCI_A0 modulation control     | UCA0MCTL   | 0x0064         |
|                            | USCI_A0 baud rate control 1    | UCA0BR1    | 0x0063         |
|                            | USCI_A0 baud rate control 0    | UCA0BR0    | 0x0062         |
|                            | USCI_A0 control 1              | UCA0CTL1   | 0x0061         |
|                            | USCI_A0 control 0              | UCA0CTL0   | 0x0060         |
|                            | USCI_A0 IrDA receive control   | UCA0IRRCTL | 0x005F         |
|                            | USCI_A0 IrDA transmit control  | UCA0IRTCTL | 0x005E         |
|                            | USCI_A0 auto baud rate control | UCA0ABCTL  | 0x005D         |
| <b>Basic Clock System+</b> | Basic clock system control 3   | BCSCTL3    | 0x0053         |
|                            | Basic clock system control 2   | BCSCTL2    | 0x0058         |
|                            | Basic clock system control 1   | BCSCTL1    | 0x0057         |
|                            | DCO clock frequency control    | DCOCTL     | 0x0056         |
| <b>Port P4</b>             | Port P4 resistor enable        | P4REN      | 0x0011         |
|                            | Port P4 selection              | P4SEL      | 0x001F         |
|                            | Port P4 direction              | P4DIR      | 0x001E         |
|                            | Port P4 output                 | P4OUT      | 0x001D         |
|                            | Port P4 input                  | P4IN       | 0x001C         |
| <b>Port P3</b>             | Port P3 resistor enable        | P3REN      | 0x0010         |
|                            | Port P3 selection              | P3SEL      | 0x001B         |
|                            | Port P3 direction              | P3DIR      | 0x001A         |
|                            | Port P3 output                 | P3OUT      | 0x0019         |
|                            | Port P3 input                  | P3IN       | 0x0018         |
| <b>Port P2</b>             | Port P2 resistor enable        | P2REN      | 0x002F         |
|                            | Port P2 selection              | P2SEL      | 0x002E         |
|                            | Port P2 interrupt enable       | P2IE       | 0x002D         |
|                            | Port P2 interrupt edge select  | P2IES      | 0x002C         |
|                            | Port P2 interrupt flag         | P2IFG      | 0x002B         |
|                            | Port P2 direction              | P2DIR      | 0x002A         |
|                            | Port P2 output                 | P2OUT      | 0x0029         |
|                            | Port P2 input                  | P2IN       | 0x0028         |
| <b>Port P1</b>             | Port P1 resistor enable        | P1REN      | 0x0027         |
|                            | Port P1 selection              | P1SEL      | 0x0026         |
|                            | Port P1 interrupt enable       | P1IE       | 0x0025         |
|                            | Port P1 interrupt edge select  | P1IES      | 0x0024         |
|                            | Port P1 interrupt flag         | P1IFG      | 0x0023         |
|                            | Port P1 direction              | P1DIR      | 0x0022         |
|                            | Port P1 output                 | P1OUT      | 0x0021         |
|                            | Port P1 input                  | P1IN       | 0x0020         |
| <b>Special Function</b>    | SFR interrupt flag 2           | IFG2       | 0x0003         |
|                            | SFR interrupt flag 1           | IFG1       | 0x0002         |
|                            | SFR interrupt enable 2         | IE2        | 0x0001         |
|                            | SFR interrupt enable 1         | IE1        | 0x0000         |

**Absolute Maximum Ratings<sup>(1)</sup>**

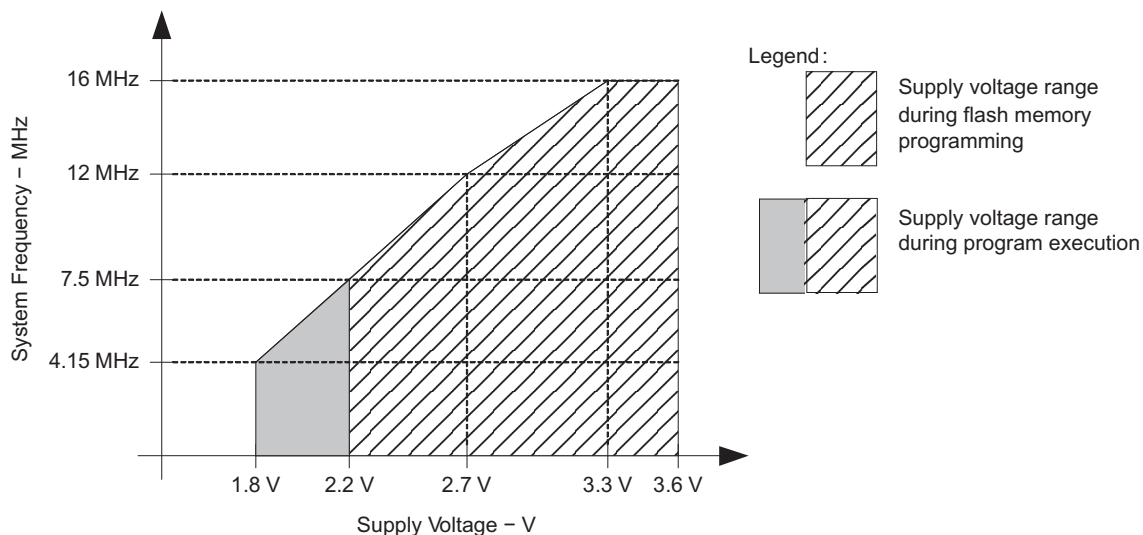
|   |                     |                               |
|---|---------------------|-------------------------------|
| Voltage applied at $V_{CC}$ to $V_{SS}$       |                     | -0.3 V to 4.1 V               |
| Voltage applied to any pin <sup>(2)</sup>     |                     | -0.3 V to ( $V_{CC} + 0.3$ V) |
| Diode current at any device terminal          |                     | ±2 mA                         |
| Storage temperature, $T_{stg}$ <sup>(3)</sup> | Unprogrammed device | -55°C to 150°C                |
|   | Programmed device   | -55°C to 150°C                |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to  $V_{SS}$ . The JTAG fuse-blow voltage,  $V_{FB}$ , is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
- (3) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

**Recommended Operating Conditions<sup>(1)</sup>**

|              |  | MIN  | MAX  | UNIT |    |
|--------------|--|--|------|------|----|
| $V_{CC}$     | Supply voltage <sup>(2)</sup> , $AV_{CC} = DV_{CC} = V_{CC}$                     | During program execution                   |      | V    |    |
|              |  | 1.8  | 3.6  |      |    |
| $V_{SS}$     | Supply voltage, $AV_{SS} = DV_{SS} = V_{SS}$                                     | During flash memory programming            |      | V    |    |
|              |  | 2.2  | 3.6  |      |    |
| $T_A$        | Operating free-air temperature   | I version                                  |      | °C   |    |
|              |  | -40  | 85   |      |    |
| $T_A$        | Operating free-air temperature   | T version                                  |      | °C   |    |
|              |  | -40  | 105  |      |    |
| $f_{SYSTEM}$ | Processor frequency (maximum MCLK frequency) <sup>(1)(3)</sup><br>(see Figure 1) | $V_{CC} = 1.8$ V, Duty cycle = 50% ±10%    |      | MHz  |    |
|              |  | dc   | 4.15 |      |    |
|              |  | $V_{CC} = 2.7$ V, Duty cycle = 50% ±10%    |      |      | dc |
|              |  | $V_{CC} \geq 3.3$ V, Duty cycle = 50% ±10% |      | dc   | 16 |

- (1) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.
- (2) It is recommended to power  $AV_{CC}$  and  $DV_{CC}$  from the same source. A maximum difference of 0.3 V between  $AV_{CC}$  and  $DV_{CC}$  can be tolerated during power-up.
- (3) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum  $V_{CC}$  of 2.2 V.

**Figure 1. Operating Area**

### Active Mode Supply Current (Into DV<sub>CC</sub> + AV<sub>CC</sub>) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)(2)</sup>

| PARAMETER   | TEST CONDITIONS   | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|---|---|----------------|-----------------|-----|-----|-----|------|
| I <sub>AM,1MHz</sub> Active mode (AM) current (1 MHz)     | f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 1 MHz, f <sub>ACLK</sub> = 32768 Hz, Program executes in flash, BCSCCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0                  |                | 2.2 V           |     | 270 | 370 | μA   |
|   |   |                | 3 V             |     | 390 | 550 |      |
| I <sub>AM,1MHz</sub> Active mode (AM) current (1 MHz)     | f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 1 MHz, f <sub>ACLK</sub> = 32768 Hz, Program executes in RAM, BCSCCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0                    |                | 2.2 V           |     | 226 |     | μA   |
|   |   |                | 3 V             |     | 318 |     |      |
| I <sub>AM,4kHz</sub> Active mode (AM) current (4 kHz)     | f <sub>MCLK</sub> = f <sub>SMCLK</sub> = f <sub>ACLK</sub> = 32768 Hz / 8 = 4096 Hz, f <sub>DCO</sub> = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0 | -40°C to 85°C  | 2.2 V           |     | 2   | 6   | μA   |
|   |   | 105°C          |                 |     | 14  |     |      |
|   |   | -40°C to 85°C  | 3 V             |     | 3   | 9   |      |
|   |   | 105°C          |                 |     | 17  |     |      |
| I <sub>AM,100kHz</sub> Active mode (AM) current (100 kHz) | f <sub>MCLK</sub> = f <sub>SMCLK</sub> = f <sub>DCO(0,0)</sub> ≈ 100 kHz, f <sub>ACLK</sub> = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1  | -40°C to 85°C  | 2.2 V           |     | 60  | 85  | μA   |
|   |   | 105°C          |                 |     | 95  |     |      |
|   |   | -40°C to 85°C  | 3 V             |     | 72  | 95  |      |
|   |   | 105°C          |                 |     | 105 |     |      |

- (1) All inputs are tied to 0 V or V<sub>CC</sub>. Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

### Typical Characteristics - Active-Mode Supply Current (Into DV<sub>CC</sub> + AV<sub>CC</sub>)

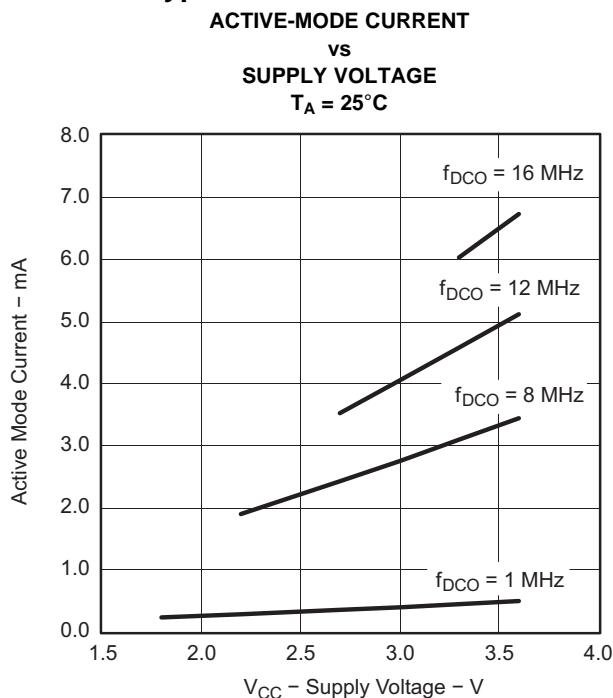


Figure 2.

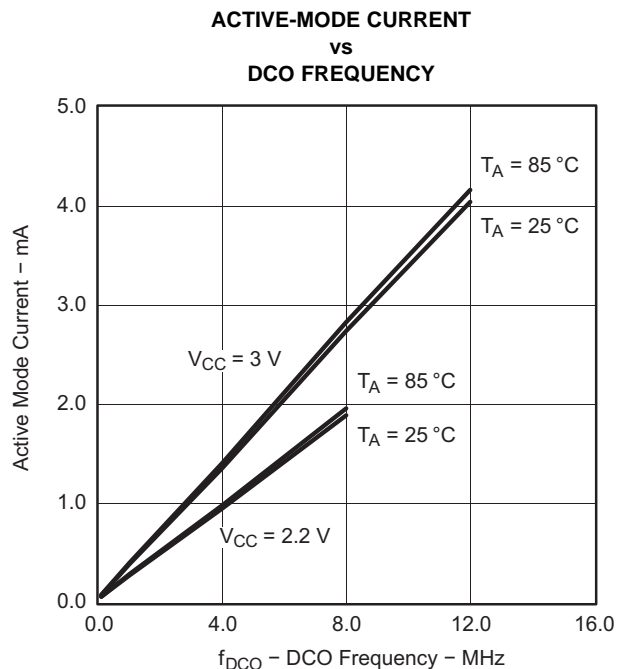


Figure 3.

**Low-Power-Mode Supply Currents (Into  $V_{CC}$ ) Excluding External Current <sup>(1)(2)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS   | $T_A$         | $V_{CC}$ | MIN  | TYP | MAX     | UNIT |
|---|---|---------------|----------|------|-----|---------|------|
|   |   |               |          |      |     |         |      |
| $I_{LPM0, 1MHz}$ Low-power mode 0 (LPM0) current <sup>(3)</sup>   | $f_{MCLK} = 0$ MHz,<br>$f_{SMCLK} = f_{DCO} = 1$ MHz,<br>$f_{ACLK} = 32768$ Hz,<br>BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>CPUOFF = 1, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 0 | -40°C to 85°C | 2.2 V    | 68   | 84  | $\mu$ A |      |
|   |   | 105°C         |          | 90   |     |         |      |
|   |   | -40°C to 85°C | 3 V      | 88   | 110 |         |      |
|   |   | 105°C         |          | 115  |     |         |      |
| $I_{LPM0, 100kHz}$ Low-power mode 0 (LPM0) current <sup>(3)</sup> | $f_{MCLK} = 0$ MHz,<br>$f_{SMCLK} = f_{DCO}(0, 0) \approx 100$ kHz,<br>$f_{ACLK} = 0$ Hz,<br>RSELX = 0, DCOx = 0,<br>CPUOFF = 1, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 1                  | -40°C to 85°C | 2.2 V    | 36   | 45  | $\mu$ A |      |
|   |   | 105°C         |          | 50   |     |         |      |
|   |   | -40°C to 85°C | 3 V      | 40   | 50  |         |      |
|   |   | 105°C         |          | 54   |     |         |      |
| $I_{LPM2}$ Low-power mode 2 (LPM2) current <sup>(4)</sup>         | $f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{DCO} = 1$ MHz,<br>$f_{ACLK} = 32768$ Hz,<br>BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>CPUOFF = 1, SCG0 = 0, SCG1 = 1,<br>OSCOFF = 0 | -40°C to 85°C | 2.2 V    | 20   | 28  | $\mu$ A |      |
|   |   | 105°C         |          | 32   |     |         |      |
|   |   | -40°C to 85°C | 3 V      | 23   | 32  |         |      |
|   |   | 105°C         |          | 37   |     |         |      |
| $I_{LPM3, LFXT1}$ Low-power mode 3 (LPM3) current <sup>(4)</sup>  | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{ACLK} = 32768$ Hz,<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 0  | -40°C to 25°C | 2.2 V    | 0.7  | 1   | $\mu$ A |      |
|   |   | 85°C          |          | 3.3  |     |         |      |
|   |   | 105°C         |          | 10   |     |         |      |
|   |   | -40°C to 25°C | 3 V      | 0.85 | 1.2 |         |      |
|   |   | 85°C          |          | 3.8  |     |         |      |
|   |   | 105°C         |          | 12   |     |         |      |
| $I_{LPM3, VLO}$ Low-power mode 3 current, (LPM3) <sup>(4)</sup>   | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{ACLK}$ from internal LF oscillator (VLO),<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 0   | -40°C to 25°C | 2.2 V    | 0.25 | 0.8 | $\mu$ A |      |
|   |   | 85°C          |          | 2.9  |     |         |      |
|   |   | 105°C         |          | 9    |     |         |      |
|   |   | -40°C to 25°C | 3 V      | 0.35 | 1   |         |      |
|   |   | 85°C          |          | 3.5  |     |         |      |
|   |   | 105°C         |          | 11   |     |         |      |
| $I_{LPM4}$ Low-power mode 4 (LPM4) current <sup>(5)</sup>         | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{ACLK} = 0$ Hz,<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 1  | -40°C         | 2.2 V    | 0.5  | 0.5 | $\mu$ A |      |
|   |   | 25°C          |          | 0.5  |     |         |      |
|   |   | 85°C          |          | 1.7  | 2.7 |         |      |
|   |   | 105°C         | 3 V      | 8.6  |     |         |      |
|   |   | -40°C         |          | 0.5  |     |         |      |
|   |   | 25°C          |          | 0.5  |     |         |      |
|   |   | 85°C          |          | 1.9  | 3   |         |      |
|   |   | 105°C         |          | 9    |     |         |      |

(1) All inputs are tied to 0 V or  $V_{CC}$ . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

(3) Current for brownout and WDT clocked by SMCLK included.

(4) Current for brownout and WDT clocked by ACLK included.

(5) Current for brownout included.

### Schmitt-Trigger Inputs (Ports P1, P2, P3, P4, JTAG, $\overline{\text{RST/NMI}}$ , XIN<sup>(1)</sup>)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER         |   | TEST CONDITIONS  | V <sub>CC</sub> | MIN                  | TYP  | MAX                  | UNIT |
|-------------------|---|--|-----------------|----------------------|------|----------------------|------|
| V <sub>IT+</sub>  | Positive-going input threshold voltage                          |  |                 | 0.45 V <sub>CC</sub> |      | 0.75 V <sub>CC</sub> | V    |
|                   |   |  | 2.2 V           | 1                    | 1.65 |                      |      |
|                   |   |  | 3 V             | 1.35                 | 2.25 |                      |      |
| V <sub>IT-</sub>  | Negative-going input threshold voltage                          |  |                 | 0.25 V <sub>CC</sub> |      | 0.55 V <sub>CC</sub> | V    |
|                   |   |  | 2.2 V           | 0.55                 | 1.20 |                      |      |
|                   |   |  | 3 V             | 0.75                 | 1.65 |                      |      |
| V <sub>hys</sub>  | Input voltage hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> ) |  | 2.2 V           | 0.2                  |      | 1                    | V    |
|                   |   |  | 3 V             | 0.3                  |      | 1                    |      |
| R <sub>Pull</sub> | Pullup/pulldown resistor  | For pullup: V <sub>IN</sub> = V <sub>SS</sub> ,<br>For pulldown: V <sub>IN</sub> = V <sub>CC</sub> |                 | 20                   | 35   | 50                   | kΩ   |
| C <sub>I</sub>    | Input capacitance   | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>   |                 |                      | 5    |                      | pF   |

(1) XIN only in bypass mode

### Inputs (Ports P1, P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER          |                           | TEST CONDITIONS  | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|--------------------|---------------------------|--|-----------------|-----|-----|-----|------|
| t <sub>(int)</sub> | External interrupt timing | Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag <sup>(1)</sup> | 2.2 V/3 V       | 20  |     |     | ns   |

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse width t<sub>(int)</sub> is met. It may be set with trigger signals shorter than t<sub>(int)</sub>.

### Leakage Current (Ports P1, P2, P3, P4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              |                                | TEST CONDITIONS | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|------------------------|--------------------------------|-----------------|-----------------|-----|-----|-----|------|
| I <sub>lkg(Px.y)</sub> | High-impedance leakage current | (1) (2)         | 2.2 V/3 V       |     |     | ±50 | nA   |

(1) The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pin(s), unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

## Outputs (Ports P1, P2, P3, P4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER       |                           | TEST CONDITIONS                               | V <sub>CC</sub> | MIN                    | MAX                    | UNIT |
|-----------------|---------------------------|---|-----------------|------------------------|------------------------|------|
| V <sub>OH</sub> | High-level output voltage | I <sub>OH(max)</sub> = -1.5 mA <sup>(1)</sup> | 2.2 V           | V <sub>CC</sub> - 0.25 | V <sub>CC</sub>        | V    |
|                 |                           | I <sub>OH(max)</sub> = -6 mA <sup>(2)</sup>   |                 | V <sub>CC</sub> - 0.6  | V <sub>CC</sub>        |      |
|                 |                           | I <sub>OH(max)</sub> = -1.5 mA <sup>(1)</sup> | 3 V             | V <sub>CC</sub> - 0.25 | V <sub>CC</sub>        |      |
|                 |                           | I <sub>OH(max)</sub> = -6 mA <sup>(2)</sup>   |                 | V <sub>CC</sub> - 0.6  | V <sub>CC</sub>        |      |
| V <sub>OL</sub> | Low-level output voltage  | I <sub>OL(max)</sub> = 1.5 mA <sup>(1)</sup>  | 2.2 V           | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 | V    |
|                 |                           | I <sub>OL(max)</sub> = 6 mA <sup>(2)</sup>    |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.6  |      |
|                 |                           | I <sub>OL(max)</sub> = 1.5 mA <sup>(1)</sup>  | 3 V             | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 |      |
|                 |                           | I <sub>OL(max)</sub> = 6 mA <sup>(2)</sup>    |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.6  |      |

- (1) The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

## Output Frequency (Ports P1, P2, P3, P4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER             |                                   | TEST CONDITIONS   | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-----------------------|-----------------------------------|---|-----------------|-----|-----|-----|------|
| f <sub>Px,y</sub>     | Port output frequency (with load) | P1.4/SMCLK, C <sub>L</sub> = 20 pF, R <sub>L</sub> = 1 kΩ <sup>(1)(2)</sup> | 2.2 V           |     |     | 7.5 | MHz  |
|                       |                                   |   | 3 V             |     |     | 12  |      |
| f <sub>Port*CLK</sub> | Clock output frequency            | P2.0/ACLK, P1.4/SMCLK, C <sub>L</sub> = 20 pF <sup>(2)</sup>                | 2.2 V           |     |     | 7.5 | MHz  |
|                       |                                   |   | 3 V             |     |     | 16  |      |

- (1) A resistive divider with two 0.5-kΩ resistors between V<sub>CC</sub> and V<sub>SS</sub> is used as load. The output is connected to the center tap of the divider.
- (2) The output voltage reaches at least 10% and 90% V<sub>CC</sub> at the specified toggle frequency.

### Typical Characteristics - Outputs

One output loaded at a time.

**TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE**

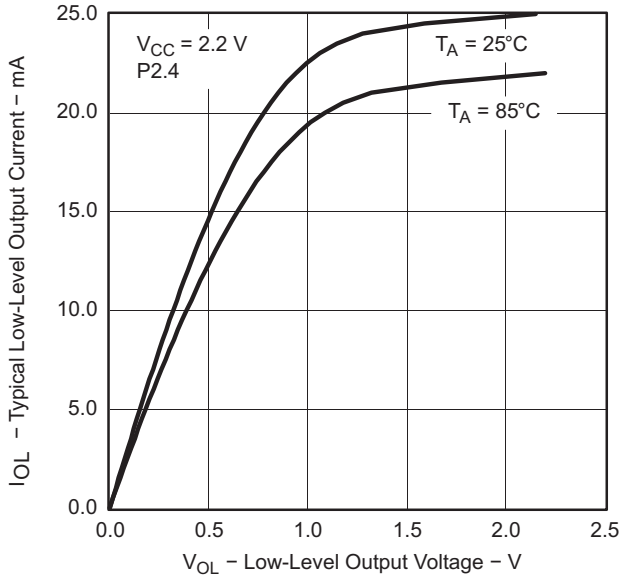


Figure 4.

**TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE**

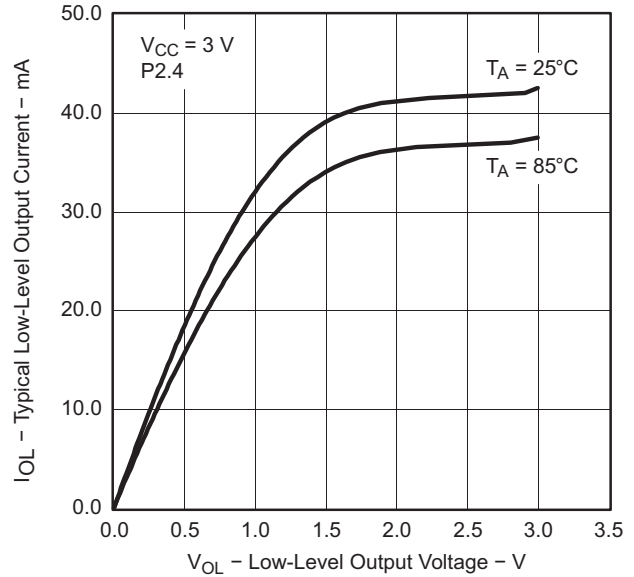


Figure 5.

**TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE**

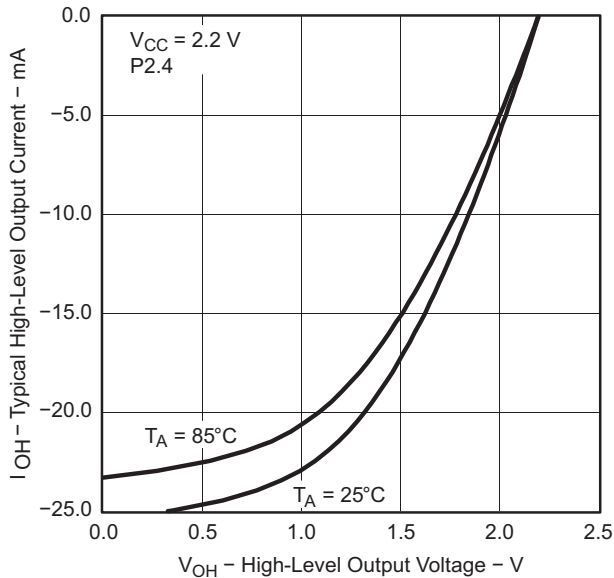


Figure 6.

**TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE**

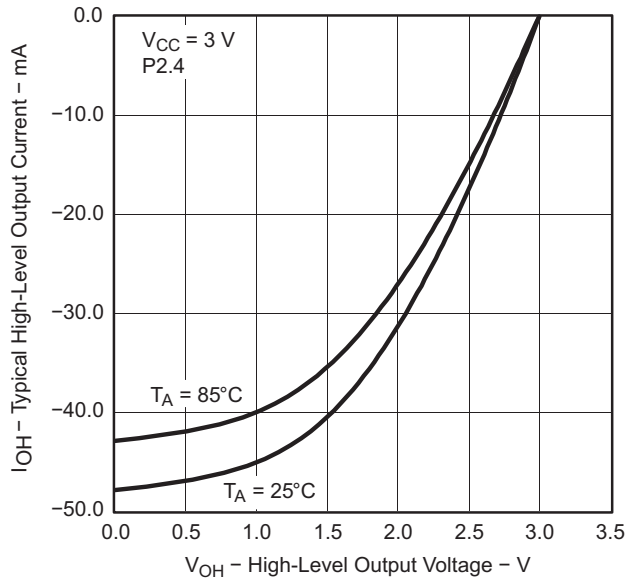


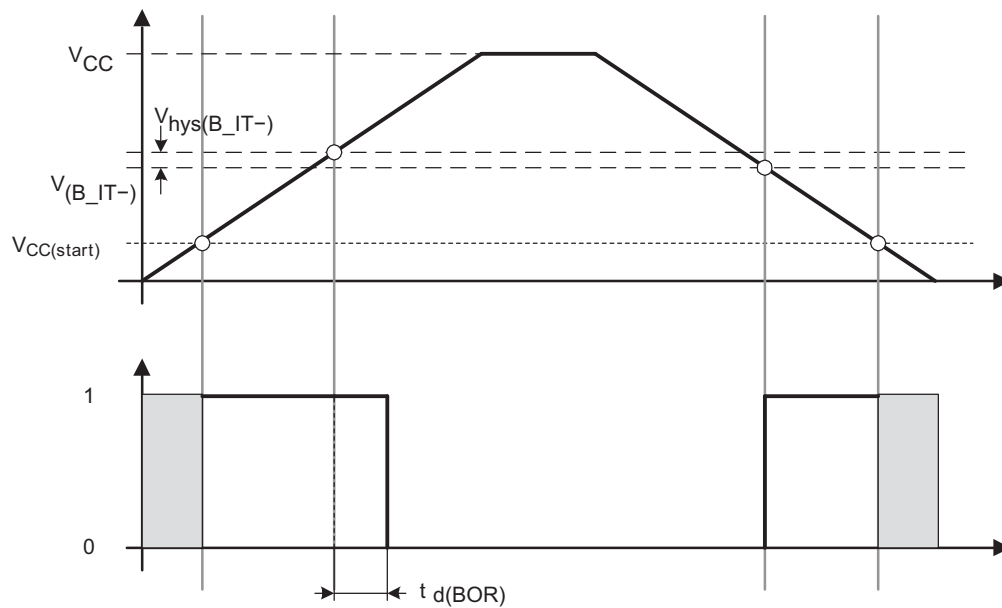
Figure 7.

**POR/Brownout Reset (BOR)<sup>(1)(2)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS  | V <sub>CC</sub>              | MIN | TYP                        | MAX  | UNIT |
|-------------------------|--|------------------------------|-----|----------------------------|------|------|
| V <sub>CC(start)</sub>  | See Figure 8   | dV <sub>CC</sub> /dt ≤ 3 V/s |     | 0.7 × V <sub>(B_IT-)</sub> |      | V    |
| V <sub>(B_IT-)</sub>    | See Figure 8 through Figure 10   | dV <sub>CC</sub> /dt ≤ 3 V/s |     |                            | 1.71 | V    |
| V <sub>hys(B_IT-)</sub> | See Figure 8   | dV <sub>CC</sub> /dt ≤ 3 V/s | 70  | 130                        | 210  | mV   |
| t <sub>d(BOR)</sub>     | See Figure 8   |                              |     |                            | 2000 | μs   |
| t <sub>(reset)</sub>    | Pulse length needed at $\overline{\text{RST}}/\text{NMI}$ pin to accepted reset internally | 2.2 V/3 V                    | 2   |                            |      | μs   |

- (1) The current consumption of the brownout module is already included in the I<sub>CC</sub> current consumption data. The voltage level V<sub>(B\_IT-)</sub> + V<sub>hys(B\_IT-)</sub> is ≤ 1.8 V.
- (2) During power up, the CPU begins code execution following a period of t<sub>d(BOR)</sub> after V<sub>CC</sub> = V<sub>(B\_IT-)</sub> + V<sub>hys(B\_IT-)</sub>. The default DCO settings must not be changed until V<sub>CC</sub> ≥ V<sub>CC(min)</sub>, where V<sub>CC(min)</sub> is the minimum supply voltage for the desired operating frequency.



**Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage**

Typical Characteristics - POR/Brownout Reset (BOR)

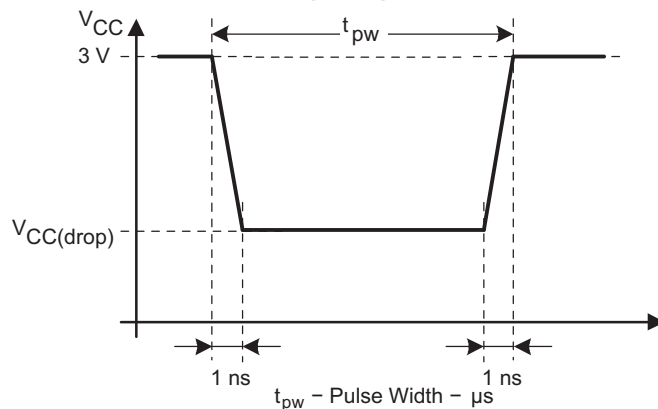
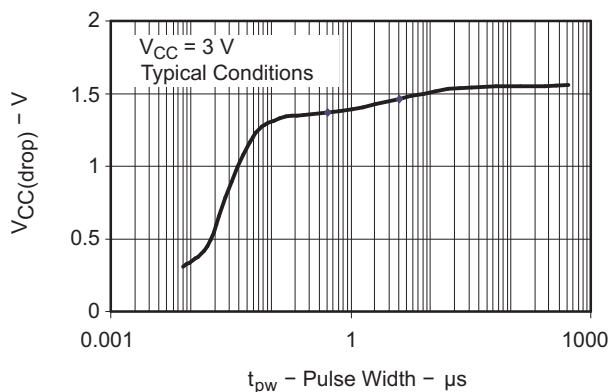


Figure 9. V<sub>CC(drop)</sub> Level With a Square Voltage Drop to Generate a POR/Brownout Signal

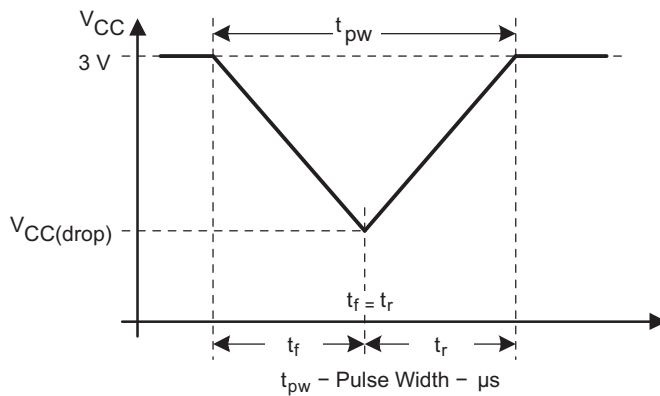
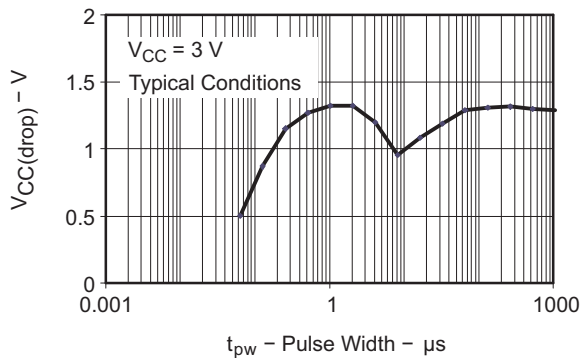


Figure 10. V<sub>CC(drop)</sub> Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

## Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S<sub>DCO</sub>.
- Modulation control bits MODx select how often f<sub>DCO(RSEL,DCO+1)</sub> is used within the period of 32 DCOCLK cycles. The frequency f<sub>DCO(RSEL,DCO)</sub> is used for the remaining cycles. The frequency is an average equal to:

$$f_{\text{average}} = \frac{32 \times f_{\text{DCO(RSEL,DCO)}} \times f_{\text{DCO(RSEL,DCO+1)}}}{\text{MOD} \times f_{\text{DCO(RSEL,DCO)}} + (32 - \text{MOD}) \times f_{\text{DCO(RSEL,DCO+1)}}}$$

## DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              |  | TEST CONDITIONS   | V <sub>CC</sub> | MIN  | TYP  | MAX  | UNIT  |
|------------------------|--|---|-----------------|------|------|------|-------|
| V <sub>CC</sub>        | Supply voltage range                         | RSELx < 14  |                 | 1.8  |      | 3.6  | V     |
|                        |  | RSELx = 14  |                 | 2.2  |      | 3.6  |       |
|                        |  | RSELx = 15  |                 | 3.0  |      | 3.6  |       |
| f <sub>DCO(0,0)</sub>  | DCO frequency (0, 0)                         | RSELx = 0, DCOx = 0, MODx = 0   | 2.2 V/3 V       | 0.06 |      | 0.14 | MHz   |
| f <sub>DCO(0,3)</sub>  | DCO frequency (0, 3)                         | RSELx = 0, DCOx = 3, MODx = 0   | 2.2 V/3 V       | 0.07 |      | 0.17 | MHz   |
| f <sub>DCO(1,3)</sub>  | DCO frequency (1, 3)                         | RSELx = 1, DCOx = 3, MODx = 0   | 2.2 V/3 V       | 0.10 |      | 0.20 | MHz   |
| f <sub>DCO(2,3)</sub>  | DCO frequency (2, 3)                         | RSELx = 2, DCOx = 3, MODx = 0   | 2.2 V/3 V       | 0.14 |      | 0.28 | MHz   |
| f <sub>DCO(3,3)</sub>  | DCO frequency (3, 3)                         | RSELx = 3, DCOx = 3, MODx = 0   | 2.2 V/3 V       | 0.20 |      | 0.40 | MHz   |
| f <sub>DCO(4,3)</sub>  | DCO frequency (4, 3)                         | RSELx = 4, DCOx = 3, MODx = 0   | 2.2 V/3 V       | 0.28 |      | 0.54 | MHz   |
| f <sub>DCO(5,3)</sub>  | DCO frequency (5, 3)                         | RSELx = 5, DCOx = 3, MODx = 0   | 2.2 V/3 V       | 0.39 |      | 0.77 | MHz   |
| f <sub>DCO(6,3)</sub>  | DCO frequency (6, 3)                         | RSELx = 6, DCOx = 3, MODx = 0   | 2.2 V/3 V       | 0.54 |      | 1.06 | MHz   |
| f <sub>DCO(7,3)</sub>  | DCO frequency (7, 3)                         | RSELx = 7, DCOx = 3, MODx = 0   | 2.2 V/3 V       | 0.80 |      | 1.50 | MHz   |
| f <sub>DCO(8,3)</sub>  | DCO frequency (8, 3)                         | RSELx = 8, DCOx = 3, MODx = 0   | 2.2 V/3 V       | 1.10 |      | 2.10 | MHz   |
| f <sub>DCO(9,3)</sub>  | DCO frequency (9, 3)                         | RSELx = 9, DCOx = 3, MODx = 0   | 2.2 V/3 V       | 1.60 |      | 3.00 | MHz   |
| f <sub>DCO(10,3)</sub> | DCO frequency (10, 3)                        | RSELx = 10, DCOx = 3, MODx = 0  | 2.2 V/3 V       | 2.50 |      | 4.30 | MHz   |
| f <sub>DCO(11,3)</sub> | DCO frequency (11, 3)                        | RSELx = 11, DCOx = 3, MODx = 0  | 2.2 V/3 V       | 3.00 |      | 5.50 | MHz   |
| f <sub>DCO(12,3)</sub> | DCO frequency (12, 3)                        | RSELx = 12, DCOx = 3, MODx = 0  | 2.2 V/3 V       | 4.30 |      | 7.30 | MHz   |
| f <sub>DCO(13,3)</sub> | DCO frequency (13, 3)                        | RSELx = 13, DCOx = 3, MODx = 0  | 2.2 V/3 V       | 6.00 |      | 9.60 | MHz   |
| f <sub>DCO(14,3)</sub> | DCO frequency (14, 3)                        | RSELx = 14, DCOx = 3, MODx = 0  | 2.2 V/3 V       | 8.60 |      | 13.9 | MHz   |
| f <sub>DCO(15,3)</sub> | DCO frequency (15, 3)                        | RSELx = 15, DCOx = 3, MODx = 0  | 3 V             | 12.0 |      | 18.5 | MHz   |
| f <sub>DCO(15,7)</sub> | DCO frequency (15, 7)                        | RSELx = 15, DCOx = 7, MODx = 0  | 3 V             | 16.0 |      | 26.0 | MHz   |
| S <sub>RSEL</sub>      | Frequency step between range RSEL and RSEL+1 | S <sub>RSEL</sub> = f <sub>DCO(RSEL+1,DCO)</sub> / f <sub>DCO(RSEL,DCO)</sub> | 2.2 V/3 V       |      |      | 1.55 | ratio |
| S <sub>DCO</sub>       | Frequency step between tap DCO and DCO+1     | S <sub>DCO</sub> = f <sub>DCO(RSEL,DCO+1)</sub> / f <sub>DCO(RSEL,DCO)</sub>  | 2.2 V/3 V       | 1.05 | 1.08 | 1.12 | ratio |
|                        | Duty cycle                                   | Measured at P1.4/SMCLK  | 2.2 V/3 V       | 40   | 50   | 60   | %     |

### Calibrated DCO Frequencies - Tolerance at Calibration

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS  | T <sub>A</sub> | V <sub>CC</sub> | MIN   | TYP  | MAX   | UNIT |
|--|--|----------------|-----------------|-------|------|-------|------|
| Frequency tolerance at calibration               |  | 25°C           | 3 V             | -1    | ±0.2 | +1    | %    |
| f <sub>CAL(1MHz)</sub> 1-MHz calibration value   | BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>Gating time: 5 ms   | 25°C           | 3 V             | 0.990 | 1    | 1.010 | MHz  |
| f <sub>CAL(8MHz)</sub> 8-MHz calibration value   | BCSCTL1 = CALBC1_8MHZ,<br>DCOCTL = CALDCO_8MHZ,<br>Gating time: 5 ms   | 25°C           | 3 V             | 7.920 | 8    | 8.080 | MHz  |
| f <sub>CAL(12MHz)</sub> 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ,<br>DCOCTL = CALDCO_12MHZ,<br>Gating time: 5 ms | 25°C           | 3 V             | 11.88 | 12   | 12.12 | MHz  |
| f <sub>CAL(16MHz)</sub> 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ,<br>DCOCTL = CALDCO_16MHZ,<br>Gating time: 2 ms | 25°C           | 3 V             | 15.84 | 16   | 16.16 | MHz  |

### Calibrated DCO Frequencies - Tolerance Over Temperature 0°C to 85°C

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS  | T <sub>A</sub> | V <sub>CC</sub> | MIN   | TYP  | MAX   | UNIT |
|--|--|----------------|-----------------|-------|------|-------|------|
| 1-MHz tolerance over temperature                 |  | 0°C to 85°C    | 3 V             | -2.5  | ±0.5 | +2.5  | %    |
| 8-MHz tolerance over temperature                 |  | 0°C to 85°C    | 3 V             | -2.5  | ±1   | +2.5  | %    |
| 12-MHz tolerance over temperature                |  | 0°C to 85°C    | 3 V             | -2.5  | ±1   | +2.5  | %    |
| 16-MHz tolerance over temperature                |  | 0°C to 85°C    | 3 V             | -3    | ±2   | +3    | %    |
| f <sub>CAL(1MHz)</sub> 1-MHz calibration value   | BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>Gating time: 5 ms   | 0°C to 85°C    | 2.2 V           | 0.97  | 1    | 1.03  | MHz  |
|  |  |                | 3 V             | 0.975 | 1    | 1.025 |      |
|  |  |                | 3.6 V           | 0.97  | 1    | 1.03  |      |
| f <sub>CAL(8MHz)</sub> 8-MHz calibration value   | BCSCTL1 = CALBC1_8MHZ,<br>DCOCTL = CALDCO_8MHZ,<br>Gating time: 5 ms   | 0°C to 85°C    | 2.2 V           | 7.76  | 8    | 8.4   | MHz  |
|  |  |                | 3 V             | 7.8   | 8    | 8.2   |      |
|  |  |                | 3.6 V           | 7.6   | 8    | 8.24  |      |
| f <sub>CAL(12MHz)</sub> 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ,<br>DCOCTL = CALDCO_12MHZ,<br>Gating time: 5 ms | 0°C to 85°C    | 2.2 V           | 11.64 | 12   | 12.36 | MHz  |
|  |  |                | 3 V             | 11.64 | 12   | 12.36 |      |
|  |  |                | 3.6 V           | 11.64 | 12   | 12.36 |      |
| f <sub>CAL(16MHz)</sub> 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ,<br>DCOCTL = CALDCO_16MHZ,<br>Gating time: 2 ms | 0°C to 85°C    | 3 V             | 15.52 | 16   | 16.48 | MHz  |
|  |  |                | 3.6 V           | 15    | 16   | 16.48 |      |

### Calibrated DCO Frequencies - Tolerance Over Supply Voltage $V_{CC}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

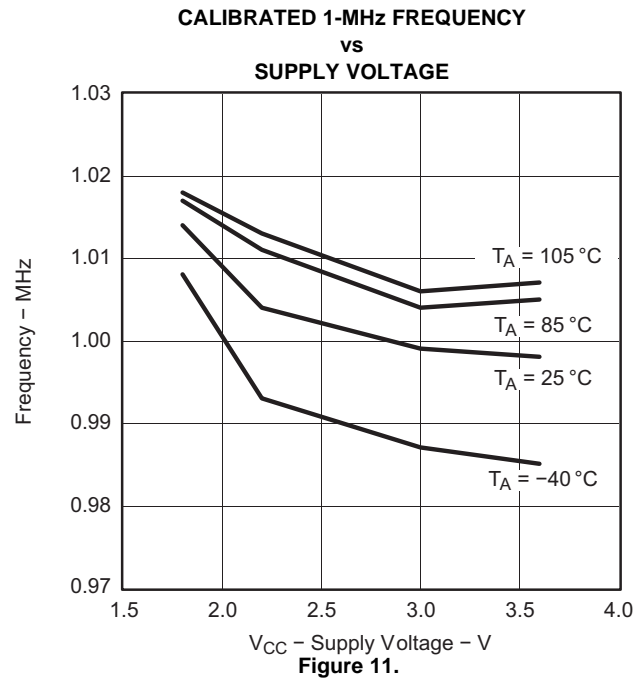
| PARAMETER                                 | TEST CONDITIONS  | $T_A$ | $V_{CC}$       | MIN   | TYP | MAX   | UNIT |
|---|--|-------|----------------|-------|-----|-------|------|
| 1-MHz tolerance over $V_{CC}$             |  | 25°C  | 1.8 V to 3.6 V | -3    | ±2  | +3    | %    |
| 8-MHz tolerance over $V_{CC}$             |  | 25°C  | 1.8 V to 3.6 V | -3    | ±2  | +3    | %    |
| 12-MHz tolerance over $V_{CC}$            |  | 25°C  | 2.2 V to 3.6 V | -3    | ±2  | +3    | %    |
| 16-MHz tolerance over $V_{CC}$            |  | 25°C  | 3 V to 3.6 V   | -6    | ±2  | +3    | %    |
| $f_{CAL(1MHz)}$ 1-MHz calibration value   | BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>Gating time: 5 ms   | 25°C  | 1.8 V to 3.6 V | 0.97  | 1   | 1.03  | MHz  |
| $f_{CAL(8MHz)}$ 8-MHz calibration value   | BCSCTL1 = CALBC1_8MHZ,<br>DCOCTL = CALDCO_8MHZ,<br>Gating time: 5 ms   | 25°C  | 1.8 V to 3.6 V | 7.76  | 8   | 8.24  | MHz  |
| $f_{CAL(12MHz)}$ 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ,<br>DCOCTL = CALDCO_12MHZ,<br>Gating time: 5 ms | 25°C  | 2.2 V to 3.6 V | 11.64 | 12  | 12.36 | MHz  |
| $f_{CAL(16MHz)}$ 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ,<br>DCOCTL = CALDCO_16MHZ,<br>Gating time: 2 ms | 25°C  | 3 V to 3.6 V   | 15    | 16  | 16.48 | MHz  |

### Calibrated DCO Frequencies - Overall Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS  | $T_A$          | $V_{CC}$       | MIN  | TYP | MAX  | UNIT |
|---|--|----------------|----------------|------|-----|------|------|
| 1-MHz tolerance overall                   |  | -40°C to 105°C | 1.8 V to 3.6 V | -5   | ±2  | +5   | %    |
| 8-MHz tolerance overall                   |  | -40°C to 105°C | 1.8 V to 3.6 V | -5   | ±2  | +5   | %    |
| 12-MHz tolerance overall                  |  | -40°C to 105°C | 2.2 V to 3.6 V | -5   | ±2  | +5   | %    |
| 16-MHz tolerance overall                  |  | -40°C to 105°C | 3 V to 3.6 V   | -6   | ±3  | +6   | %    |
| $f_{CAL(1MHz)}$ 1-MHz calibration value   | BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>Gating time: 5 ms   | -40°C to 105°C | 1.8 V to 3.6 V | 0.95 | 1   | 1.05 | MHz  |
| $f_{CAL(8MHz)}$ 8-MHz calibration value   | BCSCTL1 = CALBC1_8MHZ,<br>DCOCTL = CALDCO_8MHZ,<br>Gating time: 5 ms   | -40°C to 105°C | 1.8 V to 3.6 V | 7.6  | 8   | 8.4  | MHz  |
| $f_{CAL(12MHz)}$ 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ,<br>DCOCTL = CALDCO_12MHZ,<br>Gating time: 5 ms | -40°C to 105°C | 2.2 V to 3.6 V | 11.4 | 12  | 12.6 | MHz  |
| $f_{CAL(16MHz)}$ 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ,<br>DCOCTL = CALDCO_16MHZ,<br>Gating time: 2 ms | -40°C to 105°C | 3 V to 3.6 V   | 15   | 16  | 17   | MHz  |

**Typical Characteristics - Calibrated 1-MHz DCO Frequency**



### Wake-Up From Lower-Power Modes (LPM3/4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS                                  | V <sub>CC</sub> | MIN | TYP   | MAX | UNIT |
|--|--|-----------------|-----|---|-----|------|
| t <sub>DCO,LPM3/4</sub><br>DCO clock wake-up time from LPM3/4 <sup>(1)</sup> | BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ   | 2.2 V/3 V       |     |   | 2   | μs   |
|  | BCSCTL1 = CALBC1_8MHZ,<br>DCOCTL = CALDCO_8MHZ   |                 |     | 1.5   |     |      |
|  | BCSCTL1 = CALBC1_12MHZ,<br>DCOCTL = CALDCO_12MHZ |                 |     | 1   |     |      |
|  | BCSCTL1 = CALBC1_16MHZ,<br>DCOCTL = CALDCO_16MHZ | 3 V             |     | 1   |     |      |
| t <sub>CPU,LPM3/4</sub><br>CPU wake-up time from LPM3/4 <sup>(2)</sup>       |  |                 |     | 1 / f <sub>MCLK</sub> + t <sub>clock,LPM3/4</sub> |     |      |

- (1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, a port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
- (2) Parameter applicable only if DCOCLK is used for MCLK.

### Typical Characteristics - DCO Clock Wake-Up Time From LPM3/4

CLOCK WAKE-UP TIME FROM LPM3  
vs  
DCO FREQUENCY

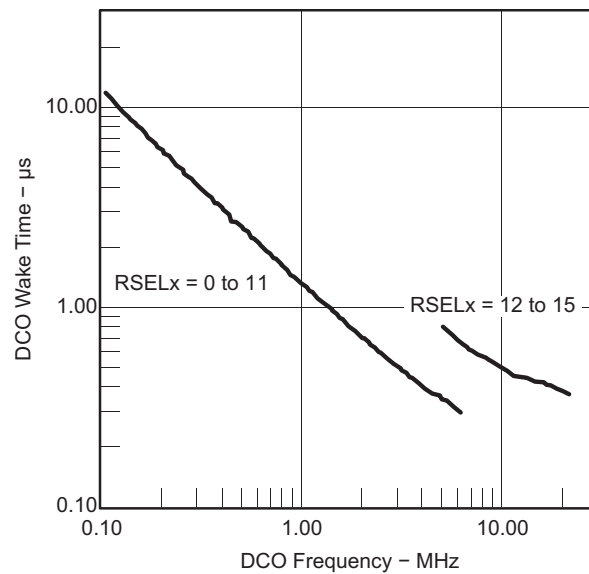


Figure 12.

### DCO With External Resistor $R_{OSC}$ <sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS   | $V_{CC}$  | MIN | TYP       | MAX | UNIT          |
|--|---|-----------|-----|-----------|-----|---------------|
| $f_{DCO,ROSC}$ DCO output frequency with $R_{OSC}$ | DCOR = 1,<br>RSELx = 4, DCOx = 3, MODx = 0,<br>$T_A = 25^\circ C$ | 2.2 V     |     | 1.8       |     | MHz           |
|  |   | 3 V       |     | 1.95      |     |               |
| $D_T$ Temperature drift                            | DCOR = 1,<br>RSELx = 4, DCOx = 3, MODx = 0                        | 2.2 V/3 V |     | $\pm 0.1$ |     | %/ $^\circ C$ |
| $D_V$ Drift with $V_{CC}$                          | DCOR = 1,<br>RSELx = 4, DCOx = 3, MODx = 0                        | 2.2 V/3 V |     | 10        |     | %/V           |

(1)  $R_{OSC} = 100\text{ k}\Omega$ . Metal film resistor, type 0257, 0.6 W with 1% tolerance and  $T_K = \pm 50\text{ ppm}/^\circ C$ .

### Typical Characteristics - DCO With External Resistor $R_{OSC}$

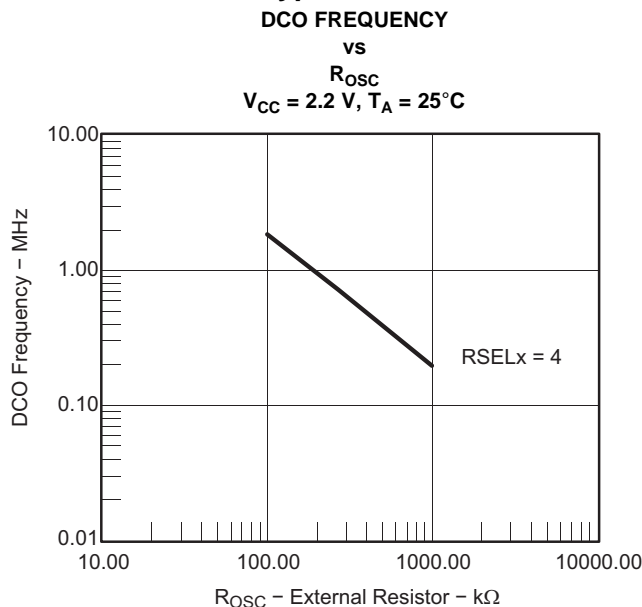


Figure 13.

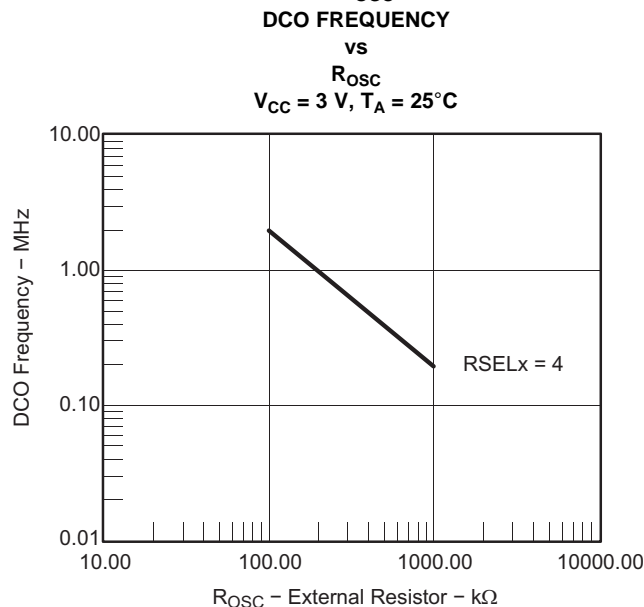


Figure 14.

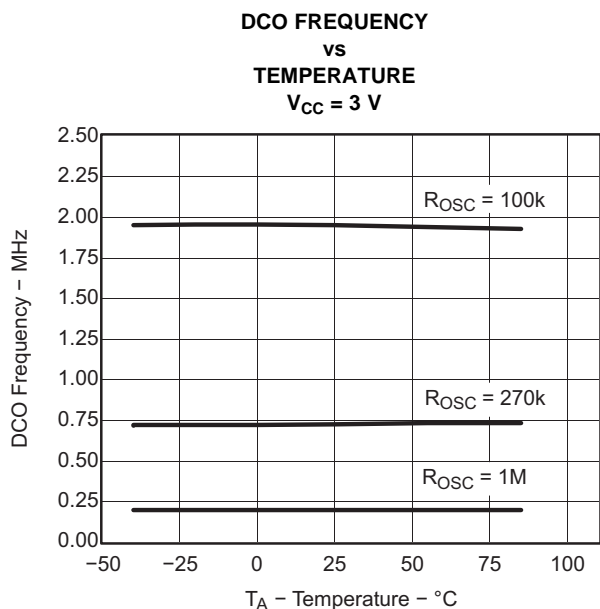


Figure 15.

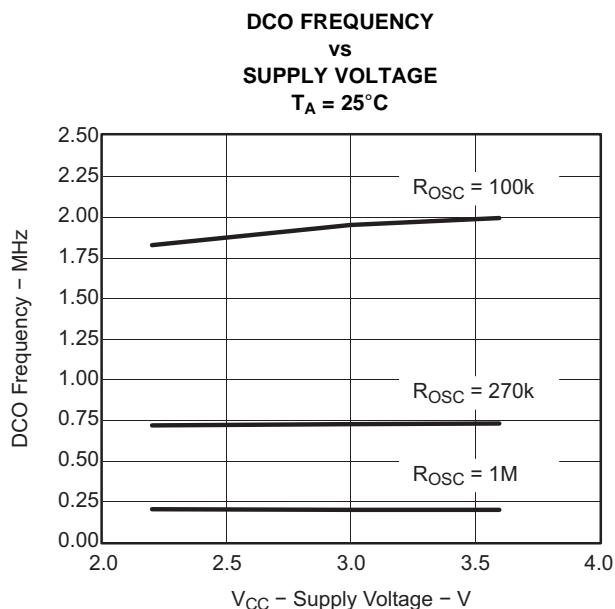


Figure 16.

## Crystal Oscillator LFXT1, Low-Frequency Mode<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                   |   | TEST CONDITIONS  | V <sub>CC</sub> | MIN   | TYP   | MAX   | UNIT |
|-----------------------------|---|--|-----------------|-------|-------|-------|------|
| f <sub>LFXT1,LF</sub>       | LFXT1 oscillator crystal frequency, LF mode 0, 1                  | XTS = 0, LFXT1Sx = 0 or 1  | 1.8 V to 3.6 V  |       | 32768 |       | Hz   |
| f <sub>LFXT1,LF,logic</sub> | LFXT1 oscillator logic level square wave input frequency, LF mode | XTS = 0, XCAPx = 0, LFXT1Sx = 3  | 1.8 V to 3.6 V  | 10000 | 32768 | 50000 | Hz   |
| O <sub>A,LF</sub>           | Oscillation allowance for LF crystals                             | XTS = 0, LFXT1Sx = 0, f <sub>LFXT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 6 pF  |                 |       | 500   |       | kΩ   |
|                             |   | XTS = 0, LFXT1Sx = 0, f <sub>LFXT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 12 pF |                 |       | 200   |       |      |
| C <sub>L,eff</sub>          | Integrated effective load capacitance, LF mode <sup>(2)</sup>     | XTS = 0, XCAPx = 0   |                 |       | 1     |       | pF   |
|                             |   | XTS = 0, XCAPx = 1   |                 |       | 5.5   |       |      |
|                             |   | XTS = 0, XCAPx = 2   |                 |       | 8.5   |       |      |
|                             |   | XTS = 0, XCAPx = 3   |                 |       | 11    |       |      |
|                             | Duty cycle, LF mode   | XTS = 0, Measured at P2.0/ACLK, f <sub>LFXT1,LF</sub> = 32768 Hz                   | 2.2 V/3 V       | 30    | 50    | 70    | %    |
| f <sub>Fault,LF</sub>       | Oscillator fault frequency, LF mode <sup>(3)</sup>                | XTS = 0, XCAPx = 0, LFXT1Sx = 3 <sup>(4)</sup>                                     | 2.2 V/3 V       | 10    |       | 10000 | Hz   |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
  - (a) Keep the trace between the device and the crystal as short as possible.
  - (b) Design a good ground plane around the oscillator pins.
  - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  - (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
  - (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).  
Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the crystal that is used.
- (3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (4) Measured with logic-level input frequency but also applies to operation with crystals.

## Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                           |   | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|-----------------|-----|-----|-----|------|
| f <sub>VLO</sub>                    | VLO frequency                                     | 2.2 V/3 V       | 4   | 12  | 20  | kHz  |
| df <sub>VLO</sub> /dT               | VLO frequency temperature drift <sup>(1)</sup>    | 2.2 V/3 V       |     | 0.5 |     | %/°C |
| df <sub>VLO</sub> /dV <sub>CC</sub> | VLO frequency supply voltage drift <sup>(2)</sup> | 1.8 V to 3.6 V  |     | 4   |     | %/V  |

- (1) Calculated using the box method:  
I version: [MAX(-40...85°C) - MIN(-40...85°C)]/MIN(-40...85°C)/[85°C - (-40°C)]  
T version: [MAX(-40...105°C) - MIN(-40...105°C)]/MIN(-40...105°C)/[105°C - (-40°C)]
- (2) Calculated using the box method: [MAX(1.8...3.6 V) - MIN(1.8...3.6 V)]/MIN(1.8...3.6 V)/(3.6 V - 1.8 V)

**Crystal Oscillator LFXT1, High-Frequency Mode<sup>(1)</sup>**

| PARAMETER                   |   | TEST CONDITIONS   | V <sub>CC</sub> | MIN  | TYP | MAX | UNIT |
|-----------------------------|---|---|-----------------|------|-----|-----|------|
| f <sub>LFXT1,HF0</sub>      | LFXT1 oscillator crystal frequency, HF mode 0                       | XTS = 1, XCAPx = 0, LFXT1Sx = 0   | 1.8 V to 3.6 V  | 0.4  |     | 1   | MHz  |
| f <sub>LFXT1,HF1</sub>      | LFXT1 oscillator crystal frequency, HF mode 1                       | XTS = 1, XCAPx = 0, LFXT1Sx = 1   | 1.8 V to 3.6 V  | 1    |     | 4   | MHz  |
| f <sub>LFXT1,HF2</sub>      | LFXT1 oscillator crystal frequency, HF mode 2                       | XTS = 1, XCAPx = 0, LFXT1Sx = 2   | 1.8 V to 3.6 V  | 2    |     | 10  | MHz  |
|                             |   |   | 2.2 V to 3.6 V  | 2    |     | 12  |      |
|                             |   |   | 3 V to 3.6 V    | 2    |     | 16  |      |
| f <sub>LFXT1,HF,logic</sub> | LFXT1 oscillator logic-level square-wave input frequency, HF mode   | XTS = 1, XCAPx = 0, LFXT1Sx = 3   | 1.8 V to 3.6 V  | 0.4  |     | 10  | MHz  |
|                             |   |   | 2.2 V to 3.6 V  | 0.4  |     | 12  |      |
|                             |   |   | 3 V to 3.6 V    | 0.4  |     | 16  |      |
| O <sub>AHF</sub>            | Oscillation allowance for HF crystals (see Figure 17 and Figure 18) | XTS = 1, XCAPx = 0, LFXT1Sx = 0, f <sub>LFXT1,HF</sub> = 1 MHz, C <sub>L,eff</sub> = 15 pF  |                 | 2700 |     |     | Ω    |
|                             |   | XTS = 1, XCAPx = 0, LFXT1Sx = 1, f <sub>LFXT1,HF</sub> = 4 MHz, C <sub>L,eff</sub> = 15 pF  |                 | 800  |     |     |      |
|                             |   | XTS = 1, XCAPx = 0, LFXT1Sx = 2, f <sub>LFXT1,HF</sub> = 16 MHz, C <sub>L,eff</sub> = 15 pF |                 | 300  |     |     |      |
| C <sub>L,eff</sub>          | Integrated effective load capacitance, HF mode <sup>(2)</sup>       | XTS = 1, XCAPx = 0 <sup>(3)</sup>   |                 | 1    |     |     | pF   |
|                             | Duty cycle, HF mode   | XTS = 1, XCAPx = 0, Measured at P2.0/ACLK, f <sub>LFXT1,HF</sub> = 10 MHz                   | 2.2 V/3 V       | 40   | 50  | 60  | %    |
|                             |   | XTS = 1, XCAPx = 0, Measured at P2.0/ACLK, f <sub>LFXT1,HF</sub> = 16 MHz                   |                 | 40   | 50  | 60  |      |
| f <sub>Fault,HF</sub>       | Oscillator fault frequency <sup>(4)</sup>                           | XTS = 1, XCAPx = 0, LFXT1Sx = 3 <sup>(5)</sup>  | 2.2 V/3 V       | 30   |     | 300 | kHz  |

- (1) To improve EMI on the XT2 oscillator the following guidelines should be observed:
  - (a) Keep the trace between the device and the crystal as short as possible.
  - (b) Design a good ground plane around the oscillator pins.
  - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  - (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
  - (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
- (5) Measured with logic-level input frequency, but also applies to operation with crystals.

**Typical Characteristics - LFXT1 Oscillator in HF Mode (XTS = 1)**  
**OSCILLATION ALLOWANCE**  
 vs  
**CRYSTAL FREQUENCY**  
 $C_{L,eff} = 15 \text{ pF}, T_A = 25^\circ\text{C}$

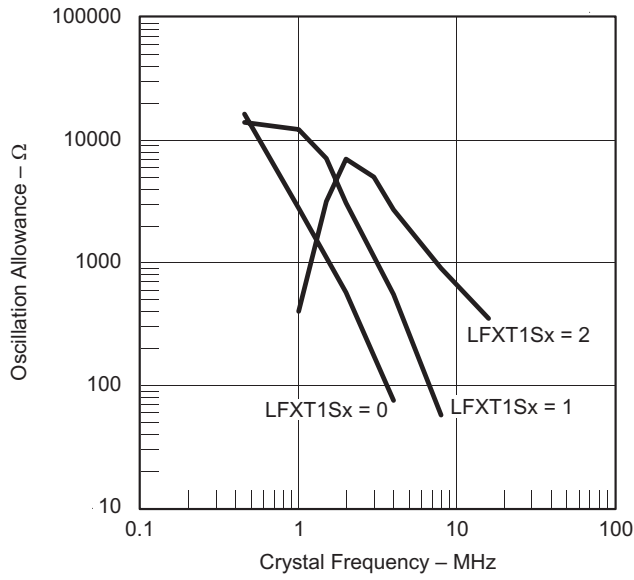


Figure 17.

**OSCILLATOR SUPPLY CURRENT**  
 vs  
**CRYSTAL FREQUENCY**  
 $C_{L,eff} = 15 \text{ pF}, T_A = 25^\circ\text{C}$

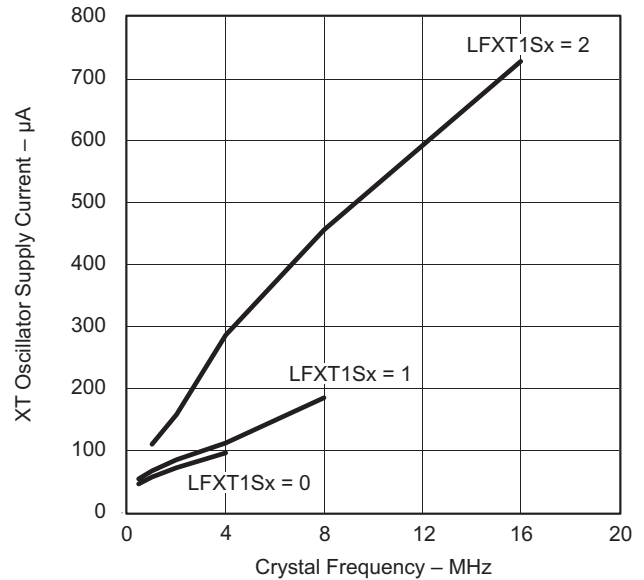


Figure 18.

### Timer\_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |                         | TEST CONDITIONS   | V <sub>CC</sub> | MIN | MAX | UNIT |
|---------------------|-------------------------|---|-----------------|-----|-----|------|
| f <sub>TA</sub>     | Timer_A clock frequency | Internal: SMCLK, ACLK<br>External: TACLK, INCLK<br>Duty cycle = 50% ± 10% | 2.2 V           |     | 10  | MHz  |
|                     |                         |   | 3 V             |     | 16  |      |
| t <sub>TA,cap</sub> | Timer_A capture timing  | TA0, TA1, TA2   | 2.2 V/3 V       | 20  |     | ns   |

### Timer\_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |                         | TEST CONDITIONS   | V <sub>CC</sub> | MIN | MAX | UNIT |
|---------------------|-------------------------|---|-----------------|-----|-----|------|
| f <sub>TB</sub>     | Timer_B clock frequency | Internal: SMCLK, ACLK<br>External: TACLK, INCLK<br>Duty cycle = 50% ± 10% | 2.2 V           |     | 10  | MHz  |
|                     |                         |   | 3 V             |     | 16  |      |
| t <sub>TB,cap</sub> | Timer_B capture timing  | TB0, TB1, TB2   | 2.2 V/3 V       | 20  |     | ns   |

## USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER               |   | CONDITIONS  | V <sub>CC</sub> | MIN | TYP | MAX                 | UNIT |
|-------------------------|---|---|-----------------|-----|-----|---------------------|------|
| f <sub>USCI</sub>       | USCI input clock frequency  | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ± 10% |                 |     |     | f <sub>SYSTEM</sub> | MHz  |
| f <sub>max,BITCLK</sub> | Maximum BITCLK clock frequency (equals baud rate in Mbaud) <sup>(1)</sup> |   | 2.2 V/3 V       | 2   |     |                     | MHz  |
| t <sub>r</sub>          | UART receive deglitch time <sup>(2)</sup>                                 |   | 2.2 V           | 50  | 150 |                     | ns   |
|                         |   |   | 3 V             | 50  | 100 |                     |      |

(1) The DCO wake-up time must be considered in LPM3/4 for baudrates above 1 MHz.

(2) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

## USCI (SPI Master Mode)<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see [Figure 19](#) and [Figure 20](#))

| PARAMETER             |                             | TEST CONDITIONS                                    | V <sub>CC</sub> | MIN | TYP | MAX                 | UNIT |
|-----------------------|-----------------------------|--|-----------------|-----|-----|---------------------|------|
| f <sub>USCI</sub>     | USCI input clock frequency  | SMCLK, ACLK<br>Duty cycle = 50% ± 10%              |                 |     |     | f <sub>SYSTEM</sub> | MHz  |
| t <sub>SU,MI</sub>    | SOMI input data setup time  |  | 2.2 V           | 110 |     |                     | ns   |
|                       |                             |  | 3 V             | 75  |     |                     |      |
| t <sub>HD,MI</sub>    | SOMI input data hold time   |  | 2.2 V           | 0   |     |                     | ns   |
|                       |                             |  | 3 V             | 0   |     |                     |      |
| t <sub>VALID,MO</sub> | SIMO output data valid time | UCLK edge to SIMO valid,<br>C <sub>L</sub> = 20 pF | 2.2 V           |     |     | 30                  | ns   |
|                       |                             |  | 3 V             |     |     | 20                  |      |

(1)  $f_{UCxCLK} = 1/2t_{LO/HI}$  with  $t_{LO/HI} \geq \max(t_{VALID,MO}(USCI) + t_{SU,SI}(Slave), t_{SU,MI}(USCI) + t_{VALID,SO}(Slave))$ .  
For the slave's parameters  $t_{SU,SI}(Slave)$  and  $t_{VALID,SO}(Slave)$ , see the SPI parameters of the attached slave.

## USCI (SPI Slave Mode)<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see [Figure 21](#) and [Figure 22](#))

| PARAMETER             |   | TEST CONDITIONS                                    | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|-----------------|-----|-----|-----|------|
| t <sub>STE,LEAD</sub> | STE lead time, STE low to clock                   |  | 2.2 V/3 V       |     | 50  |     | ns   |
| t <sub>STE,LAG</sub>  | STE lag time, Last clock to STE high              |  | 2.2 V/3 V       | 10  |     |     | ns   |
| t <sub>STE,ACC</sub>  | STE access time, STE low to SOMI data out         |  | 2.2 V/3 V       |     | 50  |     | ns   |
| t <sub>STE,DIS</sub>  | STE disable time, STE high to SOMI high impedance |  | 2.2 V/3 V       |     | 50  |     | ns   |
| t <sub>SU,SI</sub>    | SIMO input data setup time                        |  | 2.2 V           | 20  |     |     | ns   |
|                       |   |  | 3 V             | 15  |     |     |      |
| t <sub>HD,SI</sub>    | SIMO input data hold time                         |  | 2.2 V           | 10  |     |     | ns   |
|                       |   |  | 3 V             | 10  |     |     |      |
| t <sub>VALID,SO</sub> | SOMI output data valid time                       | UCLK edge to SOMI valid,<br>C <sub>L</sub> = 20 pF | 2.2 V           |     | 75  | 110 | ns   |
|                       |   |  | 3 V             |     | 50  | 75  |      |

(1)  $f_{UCxCLK} = 1/2t_{LO/HI}$  with  $t_{LO/HI} \geq \max(t_{VALID,MO}(Master) + t_{SU,SI}(USCI), t_{SU,MI}(Master) + t_{VALID,SO}(USCI))$ .  
For the master's parameters  $t_{SU,MI}(Master)$  and  $t_{VALID,MO}(Master)$  refer to the SPI parameters of the attached slave.

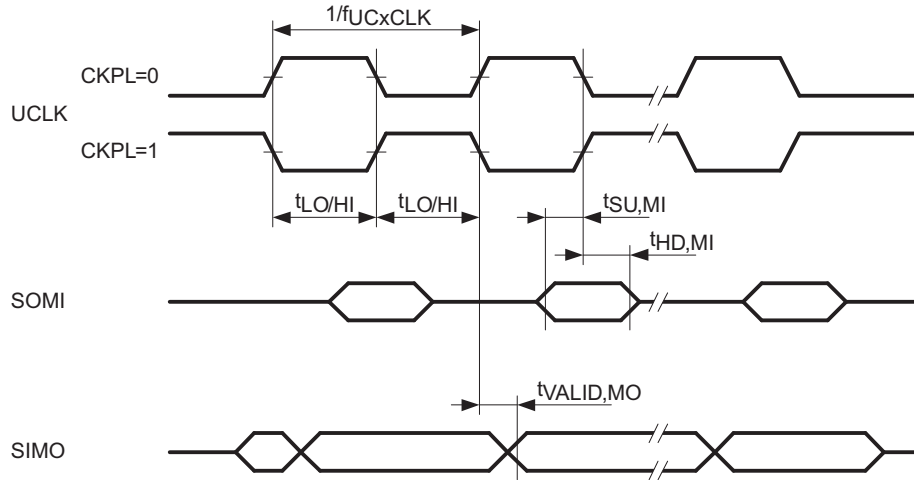


Figure 19. SPI Master Mode, CKPH = 0

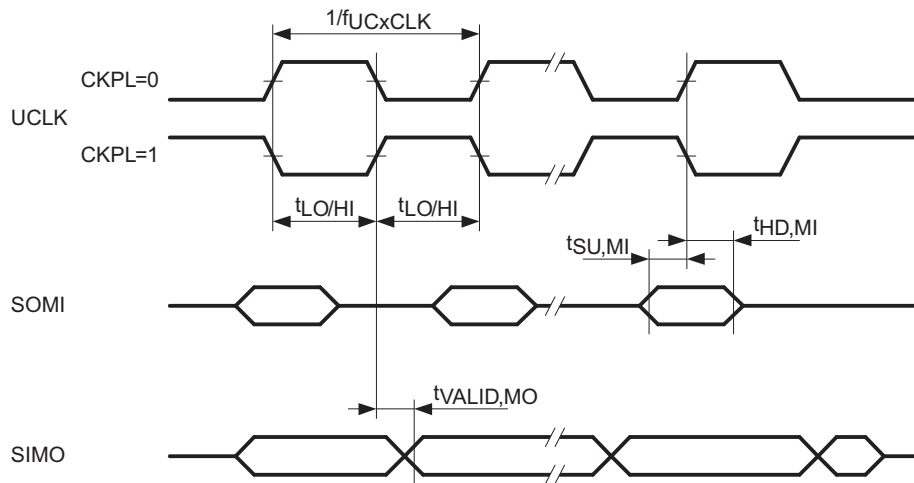


Figure 20. SPI Master Mode, CKPH = 1

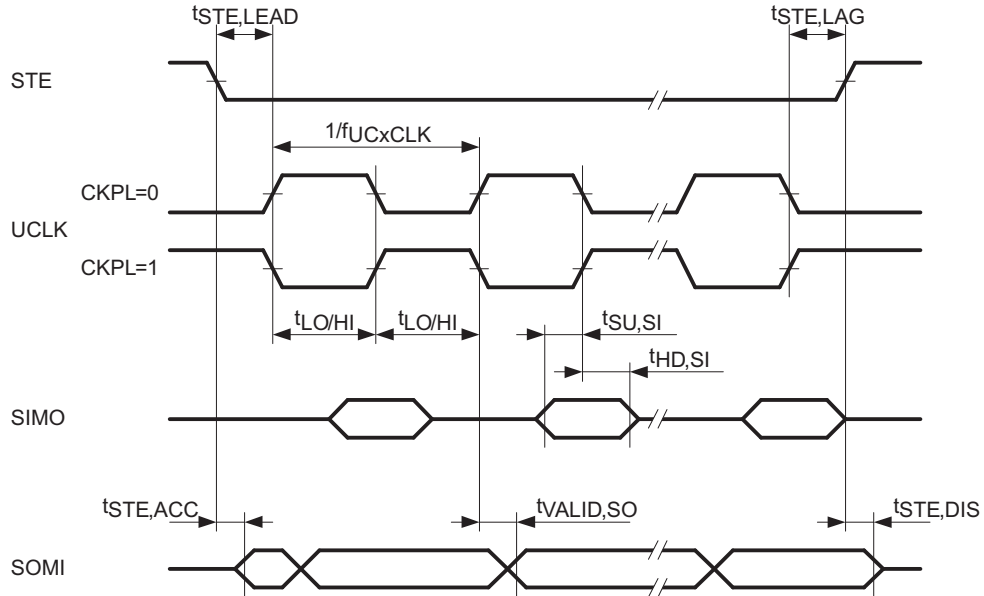


Figure 21. SPI Slave Mode, CKPH = 0

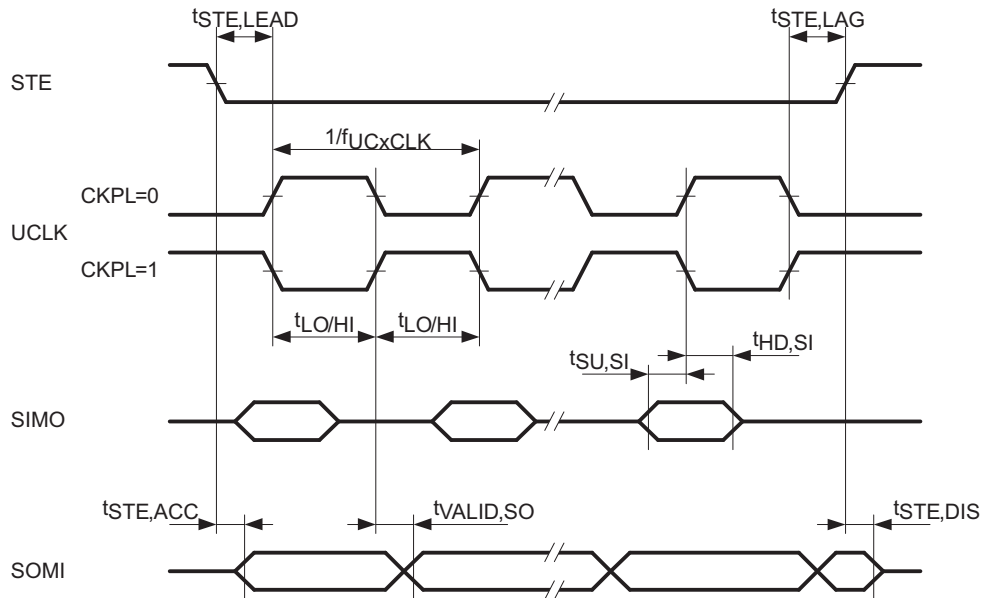


Figure 22. SPI Slave Mode, CKPH = 1

### USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 23](#))

| PARAMETER           | TEST CONDITIONS                                  | V <sub>CC</sub>  | MIN        | TYP        | MAX                 | UNIT |
|---------------------|--|--|------------|------------|---------------------|------|
| f <sub>USCI</sub>   | USCI input clock frequency                       |  |            |            | f <sub>SYSTEM</sub> | MHz  |
| f <sub>SCL</sub>    | SCL clock frequency                              | 2.2 V/3 V  | 0          |            | 400                 | kHz  |
| t <sub>HD,STA</sub> | Hold time (repeated) START                       | f <sub>SCL</sub> ≤ 100 kHz<br>f <sub>SCL</sub> > 100 kHz | 4<br>0.6   |            |                     | μs   |
| t <sub>SU,STA</sub> | Setup time for a repeated START                  | f <sub>SCL</sub> ≤ 100 kHz<br>f <sub>SCL</sub> > 100 kHz | 4.7<br>0.6 |            |                     | μs   |
| t <sub>HD,DAT</sub> | Data hold time                                   | 2.2 V/3 V  | 0          |            |                     | ns   |
| t <sub>SU,DAT</sub> | Data setup time                                  | 2.2 V/3 V  | 250        |            |                     | ns   |
| t <sub>SU,STO</sub> | Setup time for STOP                              | 2.2 V/3 V  | 4          |            |                     | μs   |
| t <sub>SP</sub>     | Pulse width of spikes suppressed by input filter | 2.2 V<br>3 V   | 50<br>50   | 150<br>100 | 600<br>600          | ns   |

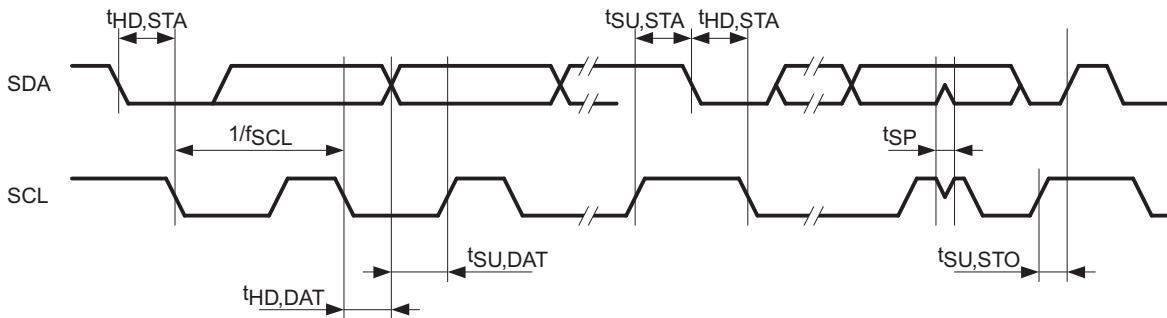


Figure 23. I2C Mode Timing

**Comparator\_A+<sup>(1)</sup>**

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                          |   | TEST CONDITIONS   | V <sub>CC</sub> | MIN  | TYP  | MAX                 | UNIT |
|------------------------------------|---|---|-----------------|------|------|---------------------|------|
| I <sub>(DD)</sub>                  |   | CAON = 1, CARSEL = 0, CAREF = 0   | 2.2 V           |      | 25   | 40                  | μA   |
|                                    |   |   | 3 V             |      | 45   | 60                  |      |
| I <sub>(Ref ladder/RefDiode)</sub> |   | CAON = 1, CARSEL = 0, CAREF = 1/2/3,<br>No load at P2.3/CA0 and P2.4/CA1  | 2.2 V           |      | 30   | 50                  | μA   |
|                                    |   |   | 3 V             |      | 45   | 71                  |      |
| V <sub>IC</sub>                    | Common-mode input voltage range                             | CAON = 1  | 2.2 V/3 V       | 0    |      | V <sub>CC</sub> - 1 | V    |
| V <sub>(Ref025)</sub>              | Voltage at 0.25 V <sub>CC</sub> node / V <sub>CC</sub>      | PCA0 = 1, CARSEL = 1, CAREF = 1,<br>No load at P2.3/CA0 and P2.4/CA1  | 2.2 V/3 V       | 0.23 | 0.24 | 0.25                |      |
| V <sub>(Ref050)</sub>              | Voltage at 0.5 V <sub>CC</sub> node / V <sub>CC</sub>       | PCA0 = 1, CARSEL = 1, CAREF = 2,<br>No load at P2.3/CA0 and P2.4/CA1  | 2.2 V/3 V       | 0.47 | 0.48 | 0.5                 |      |
| V <sub>(RefVT)</sub>               | See <a href="#">Figure 27</a> and <a href="#">Figure 28</a> | PCA0 = 1, CARSEL = 1, CAREF = 3,<br>No load at P2.3/CA0 and P2.4/CA1,<br>T <sub>A</sub> = 85°C  | 2.2 V           | 390  | 480  | 540                 | mV   |
|                                    |   |   | 3 V             | 400  | 490  | 550                 |      |
| V <sub>(offset)</sub>              | Offset voltage <sup>(2)</sup>                               |   | 2.2 V/3 V       | -30  |      | 30                  | mV   |
| V <sub>hys</sub>                   | Input hysteresis  | CAON = 1  | 2.2 V/3 V       | 0    | 0.7  | 1.4                 | mV   |
| t <sub>(response)</sub>            | Response time<br>(low-high and high-low)                    | T <sub>A</sub> = 25°C, Overdrive 10 mV,<br>Without filter: CAF = 0 <sup>(3)</sup><br>(see <a href="#">Figure 24</a> and <a href="#">Figure 25</a> ) | 2.2 V           | 80   | 165  | 300                 | ns   |
|                                    |   |   | 3 V             | 70   | 120  | 240                 |      |
|                                    |   | T <sub>A</sub> = 25°C, Overdrive 10 mV,<br>With filter: CAF = 1 <sup>(3)</sup><br>(see <a href="#">Figure 24</a> and <a href="#">Figure 25</a> )    | 2.2 V           | 1.4  | 1.9  | 2.8                 | μs   |
|                                    |   |   | 3 V             | 0.9  | 1.5  | 2.2                 |      |

(1) The leakage current for the Comparator\_A+ terminals is identical to I<sub>lk(Px,y)</sub> specification.

(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator\_A+ inputs on successive measurements. The two successive measurements are then summed together.

(3) Response time measured at P2.2/CAOUT/TA0/CA4.

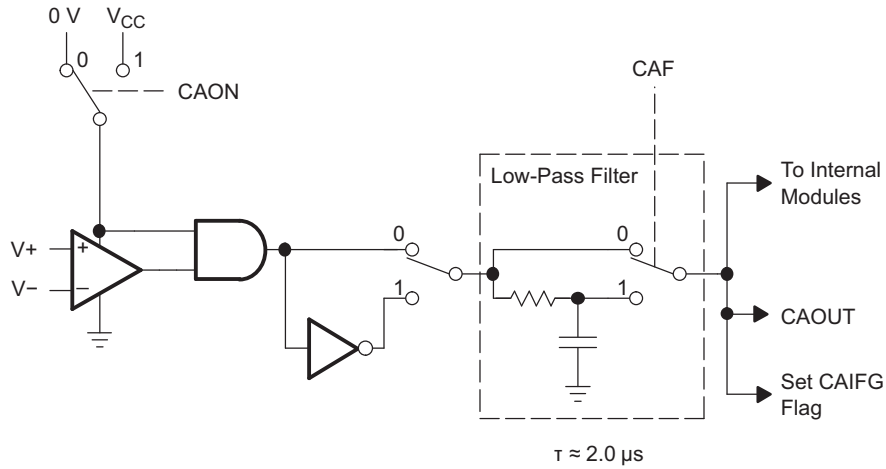


Figure 24. Comparator\_A+ Module Block Diagram

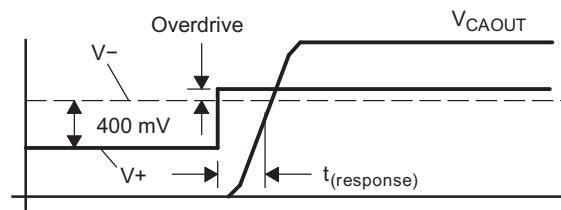


Figure 25. Overdrive Definition

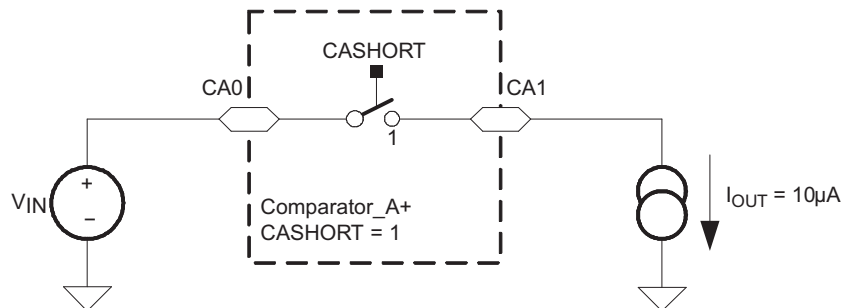


Figure 26. Comparator\_A+ Short Resistance Test Condition

Typical Characteristics - Comparator\_A+

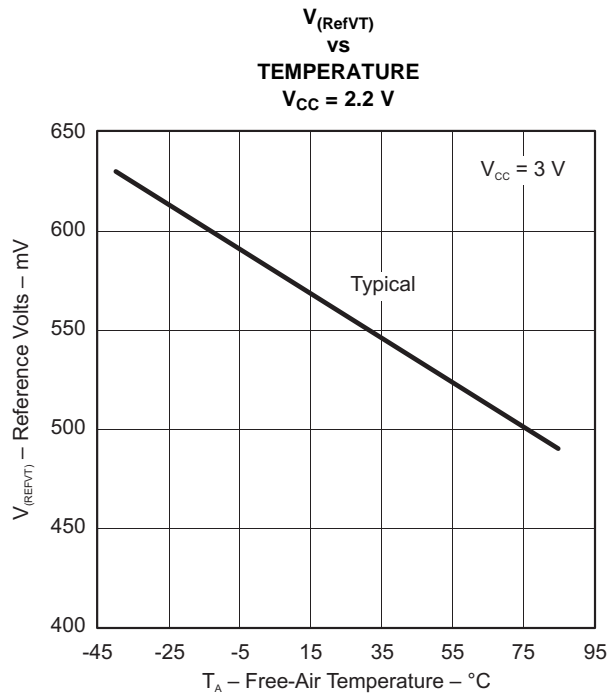


Figure 27.

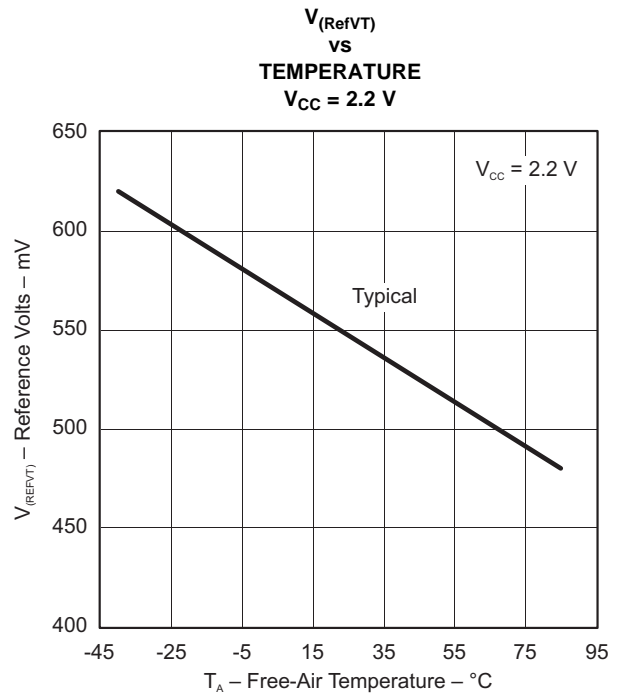


Figure 28.

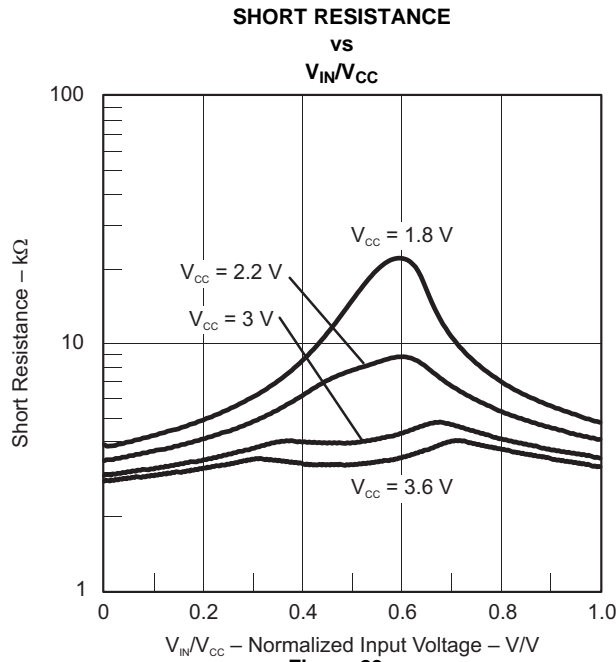


Figure 29.

## Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                   |   | TEST CONDITIONS       | V <sub>CC</sub> | MIN             | TYP             | MAX | UNIT             |
|-----------------------------|---|-----------------------|-----------------|-----------------|-----------------|-----|------------------|
| V <sub>CC (PGM/ERASE)</sub> | Program and erase supply voltage                    |                       |                 | 2.2             |                 | 3.6 | V                |
| f <sub>FTG</sub>            | Flash timing generator frequency                    |                       |                 | 257             |                 | 476 | kHz              |
| I <sub>PGM</sub>            | Supply current from V <sub>CC</sub> during program  |                       | 2.2 V/3.6 V     |                 | 1               | 5   | mA               |
| I <sub>ERASE</sub>          | Supply current from V <sub>CC</sub> during erase    |                       | 2.2 V/3.6 V     |                 | 1               | 7   | mA               |
| t <sub>CPT</sub>            | Cumulative program time <sup>(1)</sup>              |                       | 2.2 V/3.6 V     |                 |                 | 10  | ms               |
| t <sub>CMErase</sub>        | Cumulative mass erase time                          |                       | 2.2 V/3.6 V     | 20              |                 |     | ms               |
|                             | Program/erase endurance                             |                       |                 | 10 <sup>4</sup> | 10 <sup>5</sup> |     | cycles           |
| t <sub>Retention</sub>      | Data retention duration                             | T <sub>J</sub> = 25°C |                 | 100             |                 |     | years            |
| t <sub>Word</sub>           | Word or byte program time                           | See <sup>(2)</sup>    |                 |                 | 30              |     | t <sub>FTG</sub> |
| t <sub>Block, 0</sub>       | Block program time for first byte or word           | See <sup>(2)</sup>    |                 |                 | 25              |     | t <sub>FTG</sub> |
| t <sub>Block, 1-63</sub>    | Block program time for each additional byte or word | See <sup>(2)</sup>    |                 |                 | 18              |     | t <sub>FTG</sub> |
| t <sub>Block, End</sub>     | Block program end-sequence wait time                | See <sup>(2)</sup>    |                 |                 | 6               |     | t <sub>FTG</sub> |
| t <sub>Mass Erase</sub>     | Mass erase time                                     | See <sup>(2)</sup>    |                 |                 | 10593           |     | t <sub>FTG</sub> |
| t <sub>Seg Erase</sub>      | Segment erase time                                  | See <sup>(2)</sup>    |                 |                 | 4819            |     | t <sub>FTG</sub> |

- (1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.  
 (2) These values are hardwired into the flash controller's state machine (t<sub>FTG</sub> = 1/f<sub>FTG</sub>).

## RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |   | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|---|-----------------|-----|-----|------|
| V <sub>(RAMh)</sub> | RAM retention supply voltage <sup>(1)</sup> | CPU halted      | 1.6 |     | V    |

- (1) This parameter defines the minimum supply voltage V<sub>CC</sub> when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

## JTAG Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER             |   | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-----------------------|---|-----------------|-----|-----|-----|------|
| f <sub>TCK</sub>      | TCK input frequency <sup>(1)</sup>                  | 2.2 V           | 0   |     | 5   | MHz  |
|                       |   | 3 V             | 0   |     | 10  | MHz  |
| R <sub>Internal</sub> | Internal pulldown resistance on TEST <sup>(2)</sup> | 2.2 V/3 V       | 25  | 35  | 55  | kΩ   |

- (1) f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.  
 (2) TMS, TDI/TCLK, and TCK pullup resistors are implemented in all versions.

## JTAG Fuse<sup>(1)</sup>

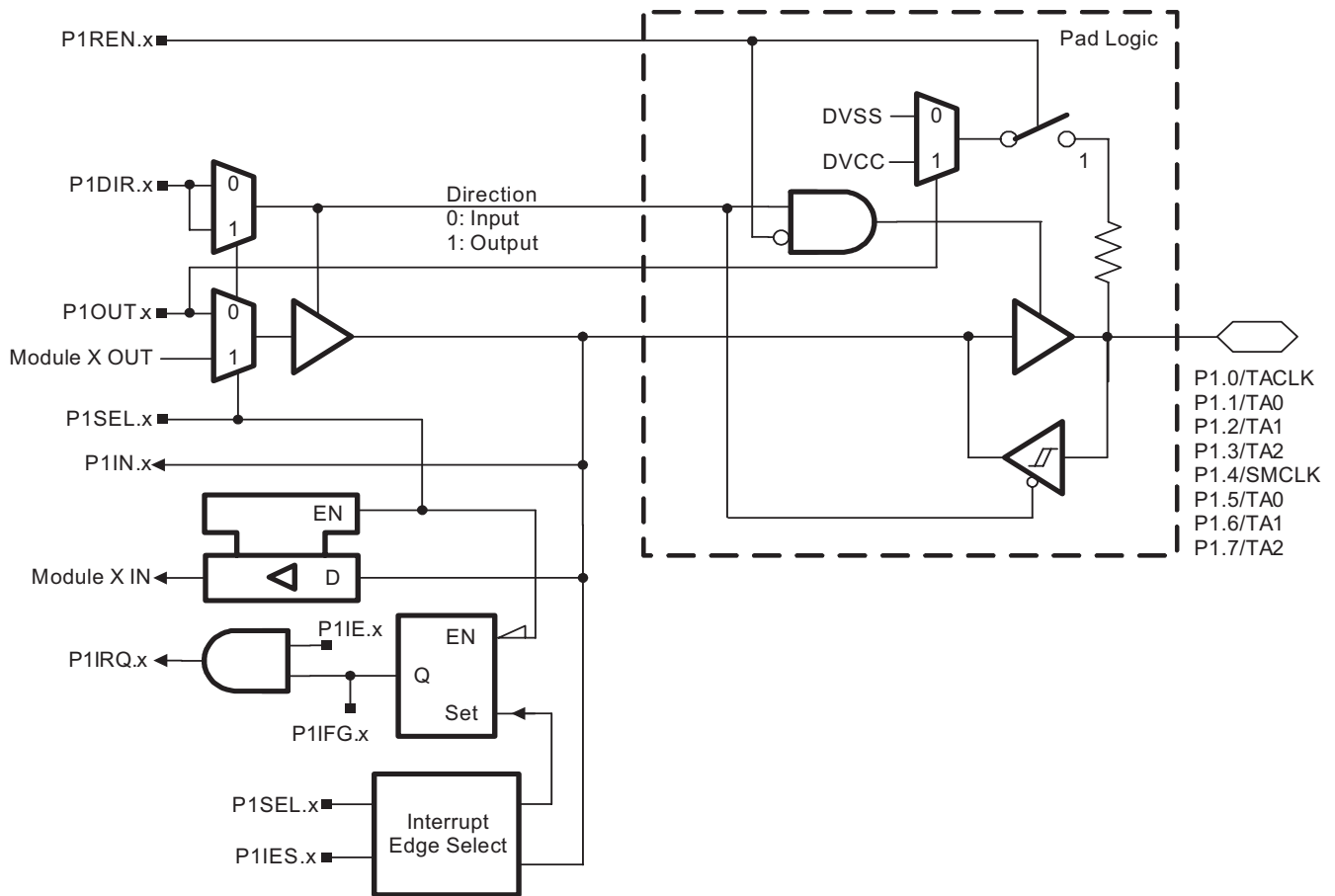
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |   | TEST CONDITIONS       | MIN | MAX | UNIT |
|---------------------|---|-----------------------|-----|-----|------|
| V <sub>CC(FB)</sub> | Supply voltage during fuse-blow condition | T <sub>A</sub> = 25°C | 2.5 |     | V    |
| V <sub>FB</sub>     | Voltage level on TEST for fuse blow       |                       | 6   | 7   | V    |
| I <sub>FB</sub>     | Supply current into TEST during fuse blow |                       |     | 100 | mA   |
| t <sub>FB</sub>     | Time to blow fuse                         |                       |     | 1   | ms   |

- (1) After the fuse is blown, no further access to the JTAG/Test and emulation features is possible, and the JTAG block is switched to bypass mode.

APPLICATION INFORMATION

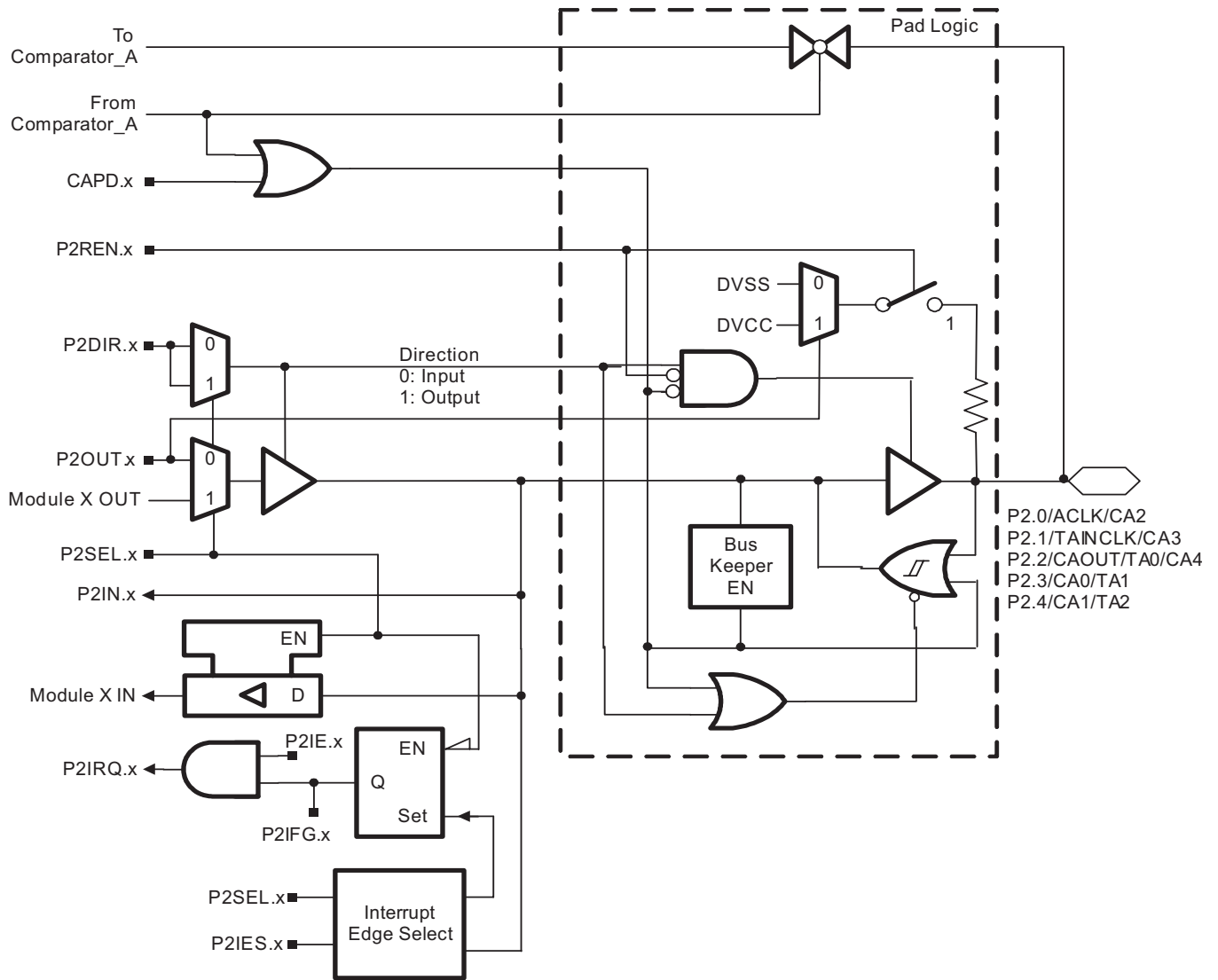
Port P1 Pin Schematic: P1.0 to P1.7, Input/Output With Schmitt Trigger



**Table 18. Port P1 (P1.0 to P1.7) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION       | CONTROL BITS / SIGNALS |         |
|-----------------|---|----------------|------------------------|---------|
|                 |   |                | P1DIR.x                | P1SEL.x |
| P1.0/TACLK      | 0 | P1.0 (I/O)     | I: 0, O: 1             | 0       |
|                 |   | Timer_A3.TACLK | 0                      | 1       |
|                 |   | DVSS           | 1                      | 1       |
| P1.1/TA0        | 1 | P1.1 (I/O)     | I: 0, O: 1             | 0       |
|                 |   | Timer_A3.CCI0A | 0                      | 1       |
|                 |   | Timer_A3.TA0   | 1                      | 1       |
| P1.2/TA1        | 2 | P1.2 (I/O)     | I: 0, O: 1             | 0       |
|                 |   | Timer_A3.CCI0A | 0                      | 1       |
|                 |   | Timer_A3.TA0   | 1                      | 1       |
| P1.3/TA2        | 3 | P1.3 (I/O)     | I: 0, O: 1             | 0       |
|                 |   | Timer_A3.CCI0A | 0                      | 1       |
|                 |   | Timer_A3.TA0   | 1                      | 1       |
| P1.4/SMCLK      | 4 | P1.4 (I/O)     | I: 0, O: 1             | 0       |
|                 |   | SMCLK          | 1                      | 1       |
| P1.5/TA0        | 5 | P1.5 (I/O)     | I: 0, O: 1             | 0       |
|                 |   | Timer_A3.CCI0A | 0                      | 1       |
|                 |   | Timer_A3.TA0   | 1                      | 1       |
| P1.6/TA1        | 6 | P1.6 (I/O)     | I: 0, O: 1             | 0       |
|                 |   | Timer_A3.CCI0A | 0                      | 1       |
|                 |   | Timer_A3.TA1   | 1                      | 1       |
| P1.7/TA2        | 7 | P1.7 (I/O)     | I: 0, O: 1             | 0       |
|                 |   | Timer_A3.CCI0A | 0                      | 1       |
|                 |   | Timer_A3.TA2   | 1                      | 1       |

Port P2 Pin Schematic: P2.0 to P2.4, Input/Output With Schmitt Trigger



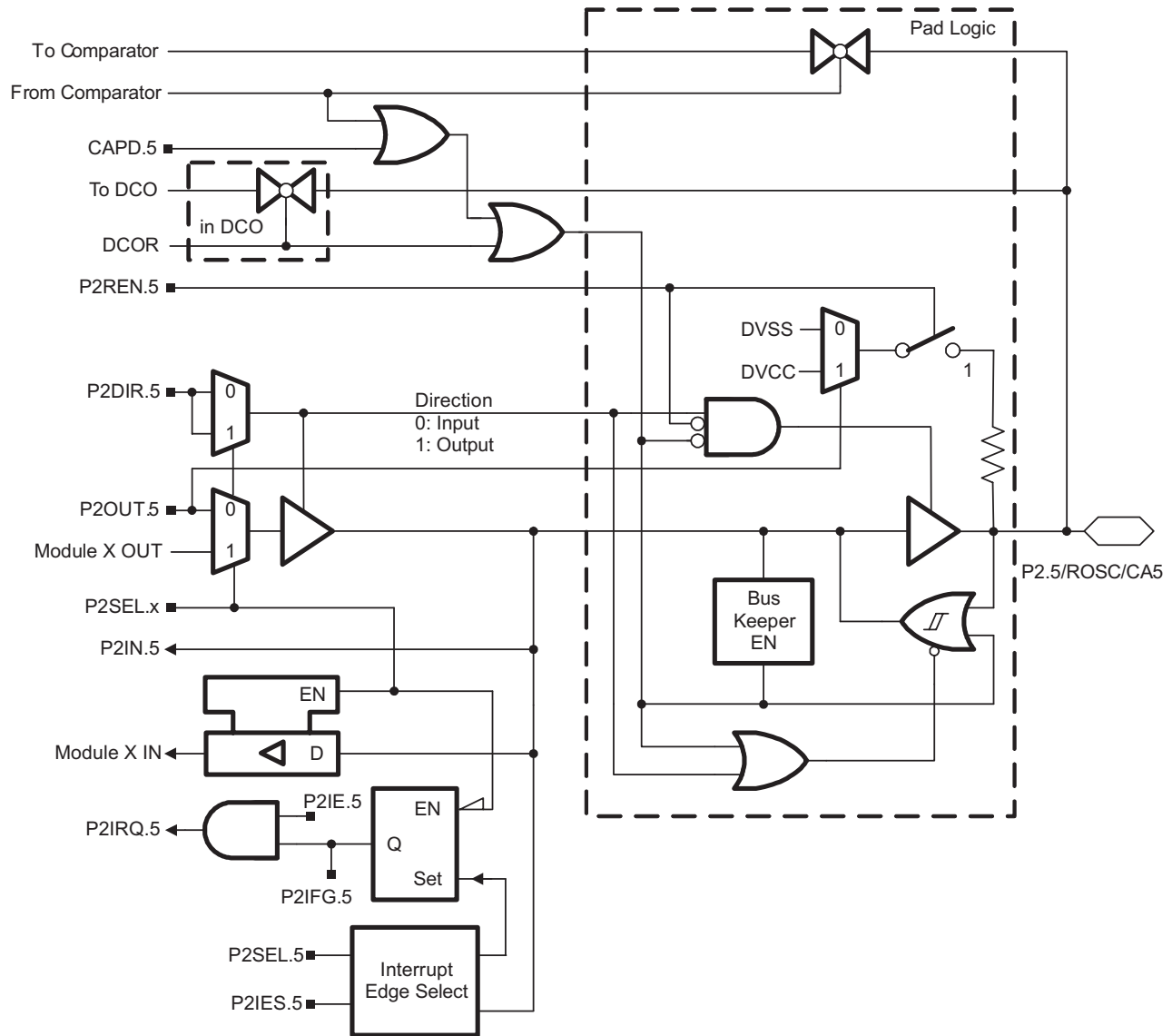
**Table 19. Port P2 (P2.0 to P2.4) Pin Functions**

| PIN NAME (P2.x)    | x | FUNCTION           | CONTROL BITS / SIGNALS <sup>(1)</sup> |            |         |
|--------------------|---|--------------------|---------------------------------------|------------|---------|
|                    |   |                    | CAPD.x                                | P2DIR.x    | P2SEL.x |
| P2.0/ACLK/CA2      | 0 | P2.0 (I/O)         | 0                                     | I: 0, O: 1 | 0       |
|                    |   | ACLK               | 0                                     | 1          | 1       |
|                    |   | CA2 <sup>(2)</sup> | 1                                     | X          | X       |
| P2.1/TAINCLK/CA3   | 1 | P2.1 (I/O)         | 0                                     | I: 0, O: 1 | 0       |
|                    |   | Timer_A3.TAINCLK   | 0                                     | 0          | 1       |
|                    |   | DVSS               | 0                                     | 1          | 1       |
|                    |   | CA3 <sup>(2)</sup> | 1                                     | X          | X       |
| P2.2/CAOUT/TA0/CA4 | 2 | P2.2 (I/O)         | 0                                     | I: 0, O: 1 | 0       |
|                    |   | CAOUT              | 0                                     | 1          | 1       |
|                    |   | TA0                | 0                                     | 0          | 1       |
|                    |   | CA4 <sup>(2)</sup> | 1                                     | X          | X       |
| P2.3/CA0/TA1       | 3 | P2.3 (I/O)         | 0                                     | I: 0, O: 1 | 0       |
|                    |   | CA0 <sup>(2)</sup> | 1                                     | X          | X       |
|                    |   | Timer_A3.TA1       | 0                                     | 1          | 1       |
| P2.4/CA1/TA2       | 4 | P2.4 (I/O)         | 0                                     | I: 0, O: 1 | 0       |
|                    |   | CA1 <sup>(2)</sup> | 1                                     | X          | X       |
|                    |   | Timer_A3.TA2       | 0                                     | 1          | 1       |

(1) X = Don't care

(2) Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

**Port P2 Pin Schematic: P2.5, Input/Output With Schmitt Trigger**



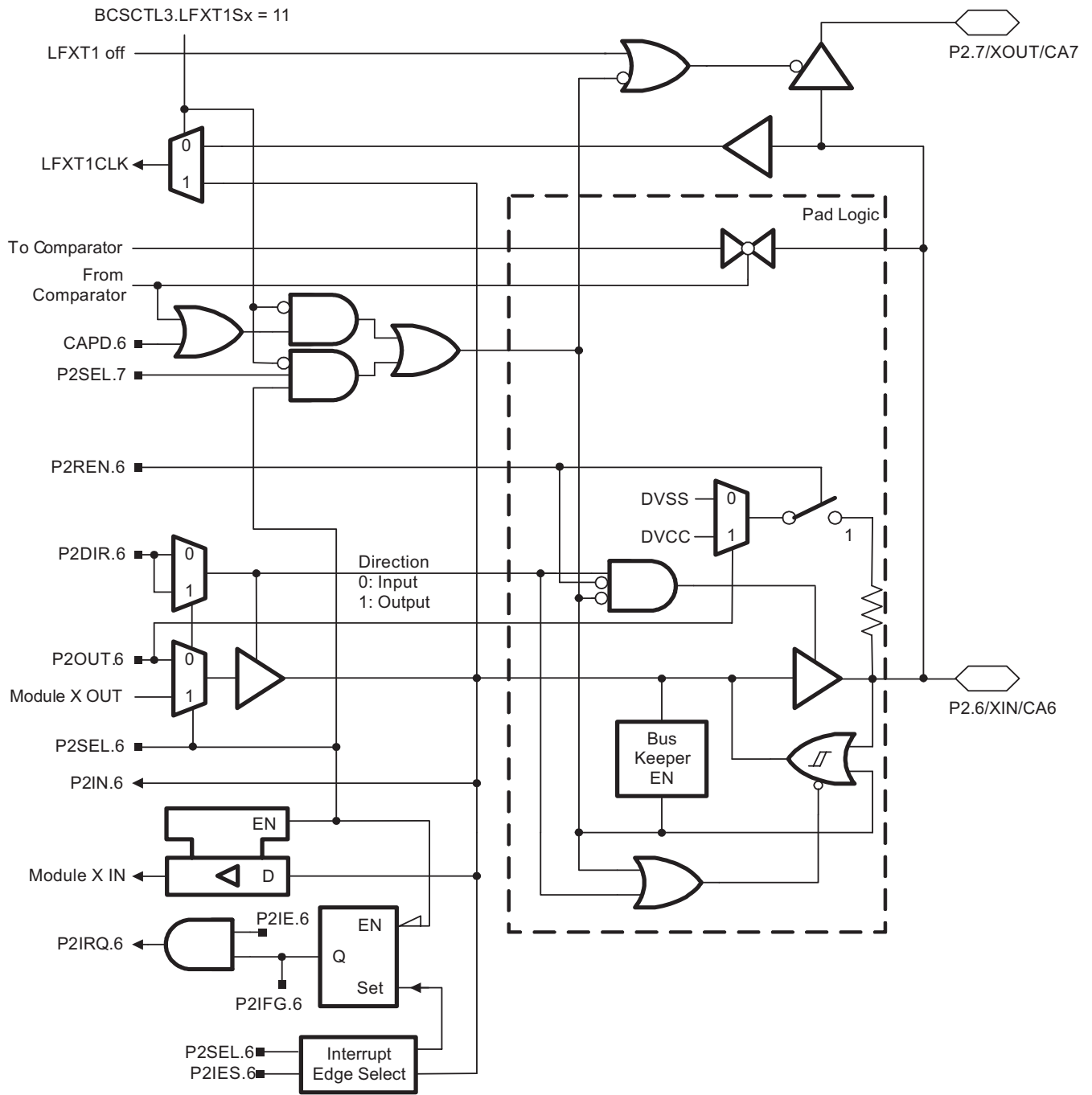
**Table 20. Port P2 (P2.5) Pin Functions**

| PIN NAME (P2.x)            | x | FUNCTION           | CONTROL BITS / SIGNALS <sup>(1)</sup> |      |            |         |
|----------------------------|---|--------------------|---------------------------------------|------|------------|---------|
|                            |   |                    | CAPD.5                                | DCOR | P2DIR.5    | P2SEL.5 |
| P2.5/R <sub>osc</sub> /CA5 | 5 | P2.5 (I/O)         | 0                                     | 0    | I: 0, O: 1 | 0       |
|                            |   | R <sub>osc</sub>   | 0                                     | 1    | X          | X       |
|                            |   | DV <sub>ss</sub>   | 0                                     | 0    | 1          | 1       |
|                            |   | CA5 <sup>(2)</sup> | 1                                     | 0    | X          | X       |

(1) X = Don't care

(2) Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger



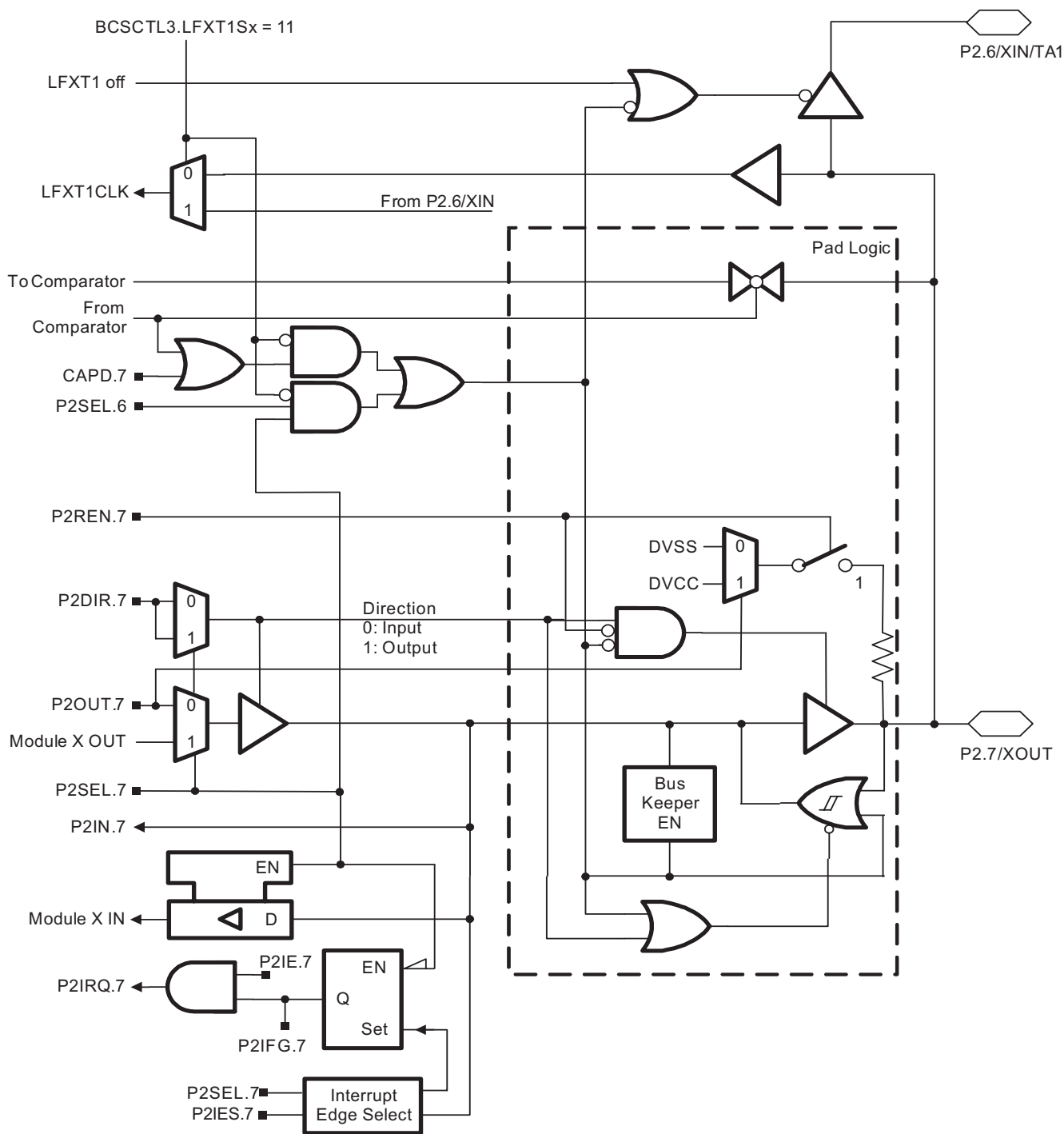
**Table 21. Port P2 (P2.6) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION           | CONTROL BITS / SIGNALS <sup>(1)</sup> |            |         |
|-----------------|---|--------------------|---------------------------------------|------------|---------|
|                 |   |                    | CAPD.6                                | P2DIR.6    | P2SEL.6 |
| P2.6/XIN/CA6    | 6 | P2.6 (I/O)         | 0                                     | I: 0, O: 1 | 0       |
|                 |   | XIN (default)      | X                                     | 1          | 1       |
|                 |   | CA6 <sup>(2)</sup> | 1                                     | X          | 0       |

(1) X = Don't care

(2) Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger



**Table 22. Port P2 (P2.7) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION           | CONTROL BITS / SIGNALS <sup>(1)</sup> |            |         |
|-----------------|---|--------------------|---------------------------------------|------------|---------|
|                 |   |                    | CAPD.7                                | P2DIR.7    | P2SEL.7 |
| P2.7/XOUT/CA7   | 7 | P2.7 (I/O)         | 0                                     | I: 0, O: 1 | 0       |
|                 |   | XOUT (default)     | X                                     | 1          | 1       |
|                 |   | CA7 <sup>(2)</sup> | 1                                     | X          | 0       |

(1) X = Don't care

(2) Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

Port P3 Pin Schematic: P3.0 to P3.5, Input/Output With Schmitt Trigger

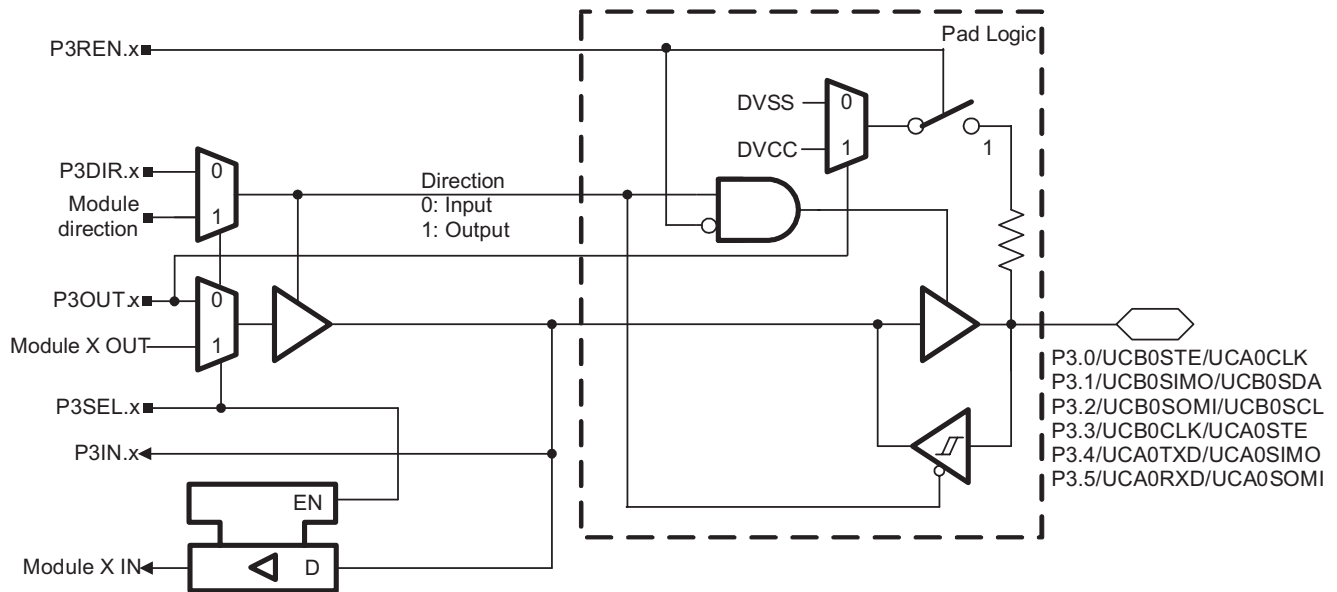


Table 23. Port P3 (P3.0 to P3.5) Pin Functions

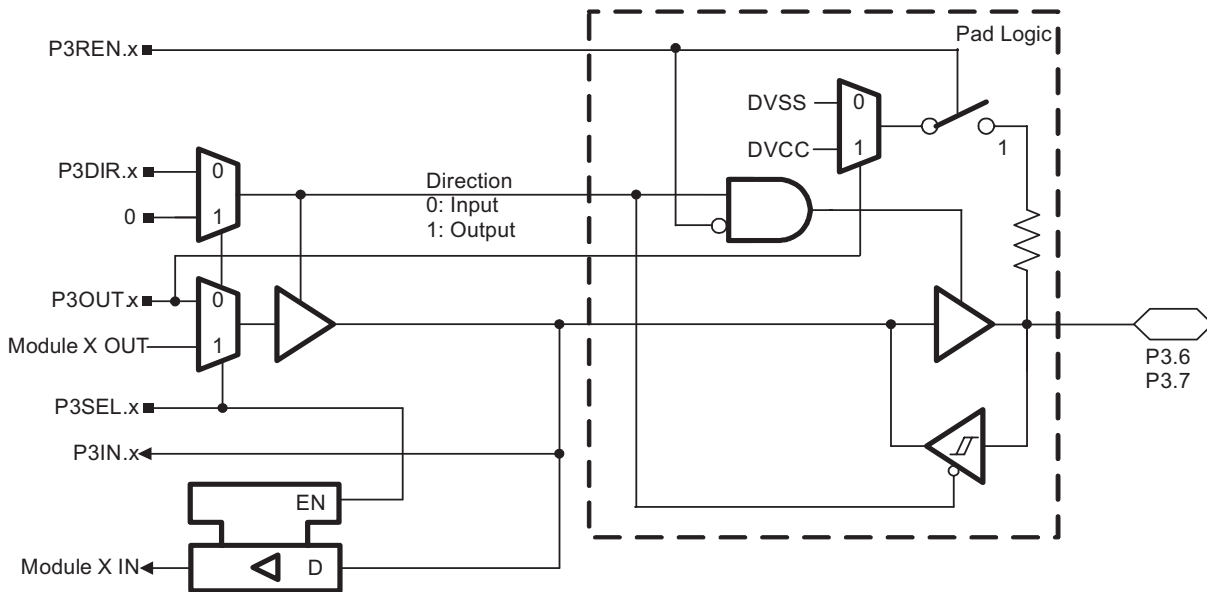
| PIN NAME (P3.x)           | x | FUNCTION                           | CONTROL BITS / SIGNALS <sup>(1)</sup> |         |
|---------------------------|---|------------------------------------|---------------------------------------|---------|
|                           |   |                                    | P3DIR.x                               | P3SEL.x |
| P3.0/UCB0STE/<br>UCA0CLK  | 0 | P3.0 (I/O)                         | I: 0, O: 1                            | 0       |
|                           |   | UCB0STE/UCA0CLK <sup>(2)</sup>     | X                                     | 1       |
| P3.1/UCB0SIMO/<br>UCB0SDA | 1 | P3.1 (I/O)                         | I: 0, O: 1                            | 0       |
|                           |   | UCB0SIMO/UCB0SDA <sup>(2)(3)</sup> | X                                     | 1       |
| P3.2/UCB0SOMI/<br>UCB0SCL | 2 | P3.2 (I/O)                         | I: 0, O: 1                            | 0       |
|                           |   | UCB0SOMI/UCB0SCL <sup>(2)(3)</sup> | X                                     | 1       |
| P3.3/UCB0CLK/<br>UCA0STE  | 3 | P3.3 (I/O)                         | I: 0, O: 1                            | 0       |
|                           |   | UCB0CLK/UCA0STE <sup>(2)</sup>     | X                                     | 1       |
| P3.4/UCA0TXD/<br>UCA0SIMO | 4 | P3.4 (I/O)                         | I: 0, O: 1                            | 0       |
|                           |   | UCA0TXD/UCA0SIMO <sup>(2)</sup>    | X                                     | 1       |
| P3.5/UCA0RXD/<br>UCA0SOMI | 5 | P3.5 (I/O)                         | I: 0, O: 1                            | 0       |
|                           |   | UCA0RXD/UCA0SOMI <sup>(2)</sup>    | X                                     | 1       |

(1) X = Don't care

(2) The pin direction is controlled by the USCI module.

(3) If the I2C functionality is selected, the output drives only the logical 0 to V<sub>SS</sub> level.

**Port P3 Pin Schematic: P3.6 and P3.7, Input/Output With Schmitt Trigger**



**Table 24. Port P3 (P3.6 and P3.7) Pin Functions**

| PIN NAME (P3.x) | x | FUNCTION   | CONTROL BITS / SIGNALS |         |
|-----------------|---|------------|------------------------|---------|
|                 |   |            | P3DIR.x                | P3SEL.x |
| P3.6            | 6 | P3.6 (I/O) | I: 0, O: 1             | 0       |
| P3.7            | 7 | P3.7 (I/O) | I: 0, O: 1             | 0       |

Port P4 Pin Schematic: P4.0 to P4.7, Input/Output With Schmitt Trigger

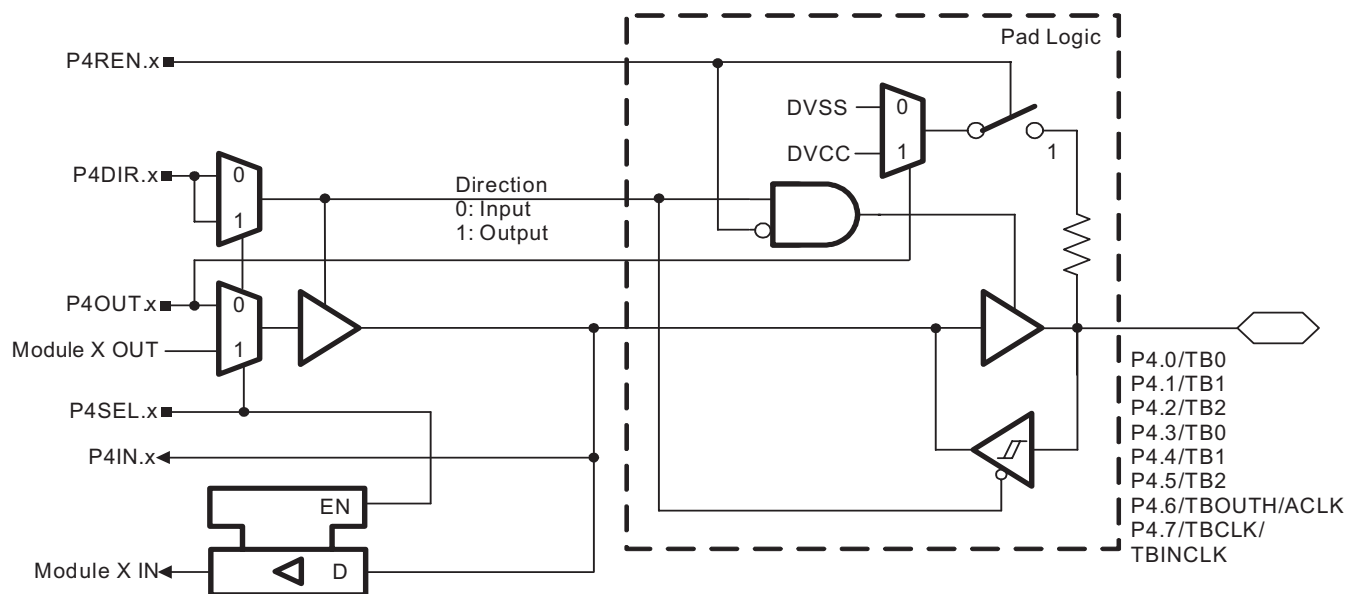
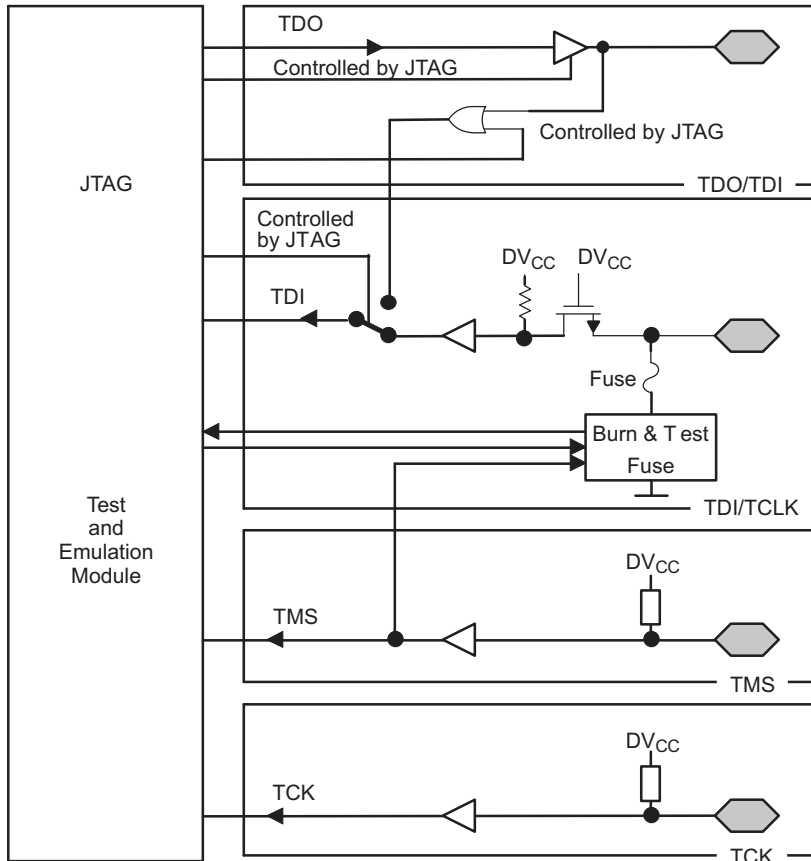


Table 25. Port P4 (P4.0 to P4.7) Pin Functions

| PIN NAME (P4.x)  | x | FUNCTION        | CONTROL BITS / SIGNALS |         |
|------------------|---|-----------------|------------------------|---------|
|                  |   |                 | P4DIR.x                | P4SEL.x |
| P4.0/TB0         | 0 | P4.0 (I/O)      | I: 0, O: 1             | 0       |
|                  |   | Timer_B3.CCI0A  | 0                      | 1       |
|                  |   | Timer_B3.OUT0   | 1                      | 1       |
| P4.1/TB1         | 1 | P4.1 (I/O)      | I: 0, O: 1             | 0       |
|                  |   | Timer_B3.CCI1A  | 0                      | 1       |
|                  |   | Timer_B3.OUT1   | 1                      | 1       |
| P4.2/TB2         | 2 | P4.2 (I/O)      | I: 0, O: 1             | 0       |
|                  |   | Timer_B3.CCI2A  | 0                      | 1       |
|                  |   | Timer_B3.OUT2   | 1                      | 1       |
| P4.3/TB0         | 3 | P4.3 (I/O)      | I: 0, O: 1             | 0       |
|                  |   | Timer_B3.CCI0B  | 0                      | 1       |
|                  |   | Timer_B3.OUT0   | 1                      | 1       |
| P4.4/TB1         | 4 | P4.4 (I/O)      | I: 0, O: 1             | 0       |
|                  |   | Timer_B3.CCI1B  | 0                      | 1       |
|                  |   | Timer_B3.OUT1   | 1                      | 1       |
| P4.5/TB2         | 5 | P4.5 (I/O)      | I: 0, O: 1             | 0       |
|                  |   | N/A             | 0                      | 1       |
|                  |   | Timer_B3.OUT2   | 1                      | 1       |
| P4.6/TBOUTH/ACLK | 6 | P4.6 (I/O)      | I: 0, O: 1             | 0       |
|                  |   | Timer_B3.TBOUTH | 0                      | 1       |
|                  |   | ACLK            | 1                      | 1       |
| P4.7/TBCLK       | 7 | P4.7 (I/O)      | I: 0, O: 1             | 0       |
|                  |   | Timer_B3.TBCLK  | 0                      | 1       |

JTAG Pins TMS, TCK, TDI/TCLK, TDO/TDI, Input/Output With Schmitt Trigger



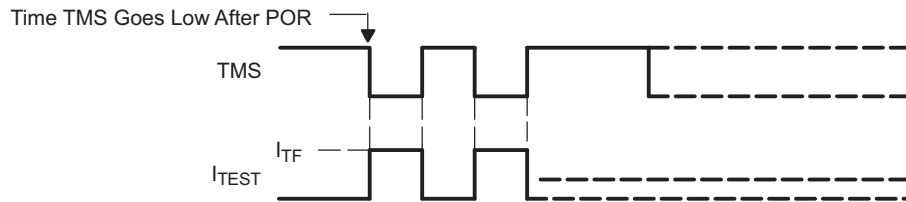
During Programming Activity and During Blowing of the Fuse, Pin TDO/TDI Is Used to Apply the Test Input Data for JTAG Circuitry

### JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current,  $I_{TF}$ , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see [Figure 30](#)). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).



**Figure 30. Fuse Check Mode Current**

## REVISION HISTORY

| LITERATURE NUMBER | SUMMARY  |
|-------------------|--|
| SLAS518           | PRODUCT PREVIEW data sheet release   |
| SLAS518A          | PRODUCTION DATA data sheet release   |
| SLAS518B          | The USCI parameter section was revised, pages 36 to 39.  |
|                   | Corrected the port schematics of port P2.6 and P2.7  |
|                   | Added in the DSBGA package version.  |
|                   | Corrected WDTIFG description in IFG1 register.   |
|                   | Corrected labels in Figure 17 and 18.  |
|                   | Corrected test conditions of Comparator_A+ from P1.0, P1.1 to P2.3 and P2.4.                           |
| SLAS518C          | Release of MSP430F2330IYFF and MSP430F2350IYFF   |
| SLAS518D          | Changed $T_{stg}$ , Programmed device, to -40°C to 150°C in <a href="#">Absolute Maximum Ratings</a> . |
| SLAS518E          | Changed $T_{stg}$ , Programmed device, to -55°C to 150°C in <a href="#">Absolute Maximum Ratings</a> . |

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F2330IRHAR | ACTIVE        | VQFN         | RHA                | 40   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | M430<br>F2330           | <a href="#">Samples</a> |
| MSP430F2330IRHAT | ACTIVE        | VQFN         | RHA                | 40   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | M430<br>F2330           | <a href="#">Samples</a> |
| MSP430F2330TRHAR | ACTIVE        | VQFN         | RHA                | 40   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 105   | M430<br>F2330T          | <a href="#">Samples</a> |
| MSP430F2330TRHAT | ACTIVE        | VQFN         | RHA                | 40   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 105   | M430<br>F2330T          | <a href="#">Samples</a> |
| MSP430F2350IRHAR | ACTIVE        | VQFN         | RHA                | 40   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | M430<br>F2350           | <a href="#">Samples</a> |
| MSP430F2350IRHAT | ACTIVE        | VQFN         | RHA                | 40   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | M430<br>F2350           | <a href="#">Samples</a> |
| MSP430F2350IYFFT | ACTIVE        | DSBGA        | YFF                | 49   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | M430F2350               | <a href="#">Samples</a> |
| MSP430F2350TRHAR | ACTIVE        | VQFN         | RHA                | 40   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 105   | M430<br>F2350T          | <a href="#">Samples</a> |
| MSP430F2350TRHAT | ACTIVE        | VQFN         | RHA                | 40   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 105   | M430<br>F2350T          | <a href="#">Samples</a> |
| MSP430F2370IRHAR | ACTIVE        | VQFN         | RHA                | 40   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | M430<br>F2370           | <a href="#">Samples</a> |
| MSP430F2370IRHAT | ACTIVE        | VQFN         | RHA                | 40   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | M430<br>F2370           | <a href="#">Samples</a> |
| MSP430F2370IYFFR | NRND          | DSBGA        | YFF                | 49   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | M430F2370               |                         |
| MSP430F2370IYFFT | ACTIVE        | DSBGA        | YFF                | 49   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | M430F2370               | <a href="#">Samples</a> |
| MSP430F2370TRHAR | ACTIVE        | VQFN         | RHA                | 40   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 105   | M430<br>F2370T          | <a href="#">Samples</a> |
| MSP430F2370TRHAT | ACTIVE        | VQFN         | RHA                | 40   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 105   | M430<br>F2370T          | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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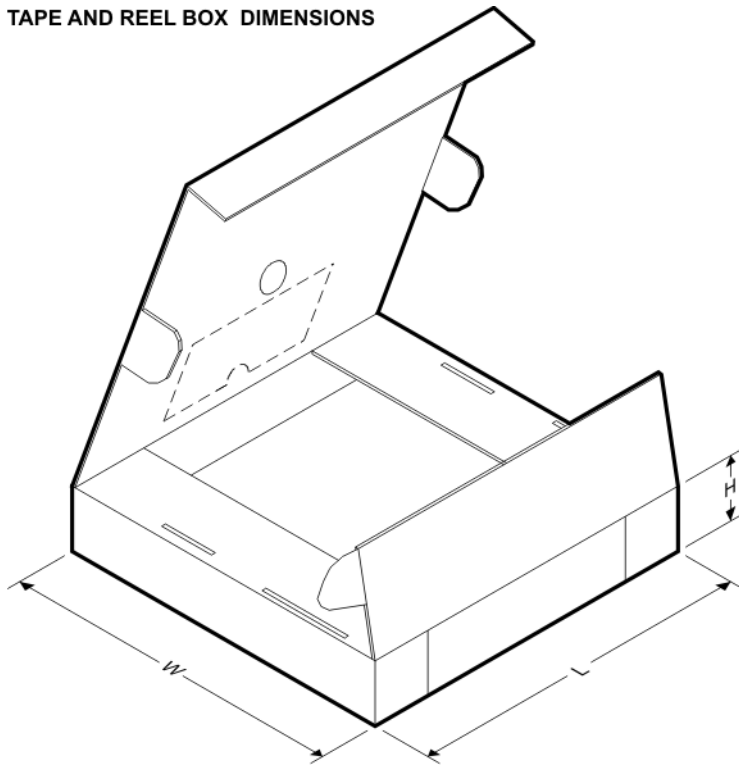
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F2330IRHAR | VQFN         | RHA             | 40   | 2500 | 330.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F2330IRHAT | VQFN         | RHA             | 40   | 250  | 180.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F2330TRHAR | VQFN         | RHA             | 40   | 2500 | 330.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F2330TRHAT | VQFN         | RHA             | 40   | 250  | 180.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F2350IRHAR | VQFN         | RHA             | 40   | 2500 | 330.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F2350IRHAT | VQFN         | RHA             | 40   | 250  | 180.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F2350TRHAR | VQFN         | RHA             | 40   | 2500 | 330.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F2350TRHAT | VQFN         | RHA             | 40   | 250  | 180.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F2370IRHAR | VQFN         | RHA             | 40   | 2500 | 330.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F2370IRHAT | VQFN         | RHA             | 40   | 250  | 180.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F2370TRHAR | VQFN         | RHA             | 40   | 2500 | 330.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| MSP430F2370TRHAT | VQFN         | RHA             | 40   | 250  | 180.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |

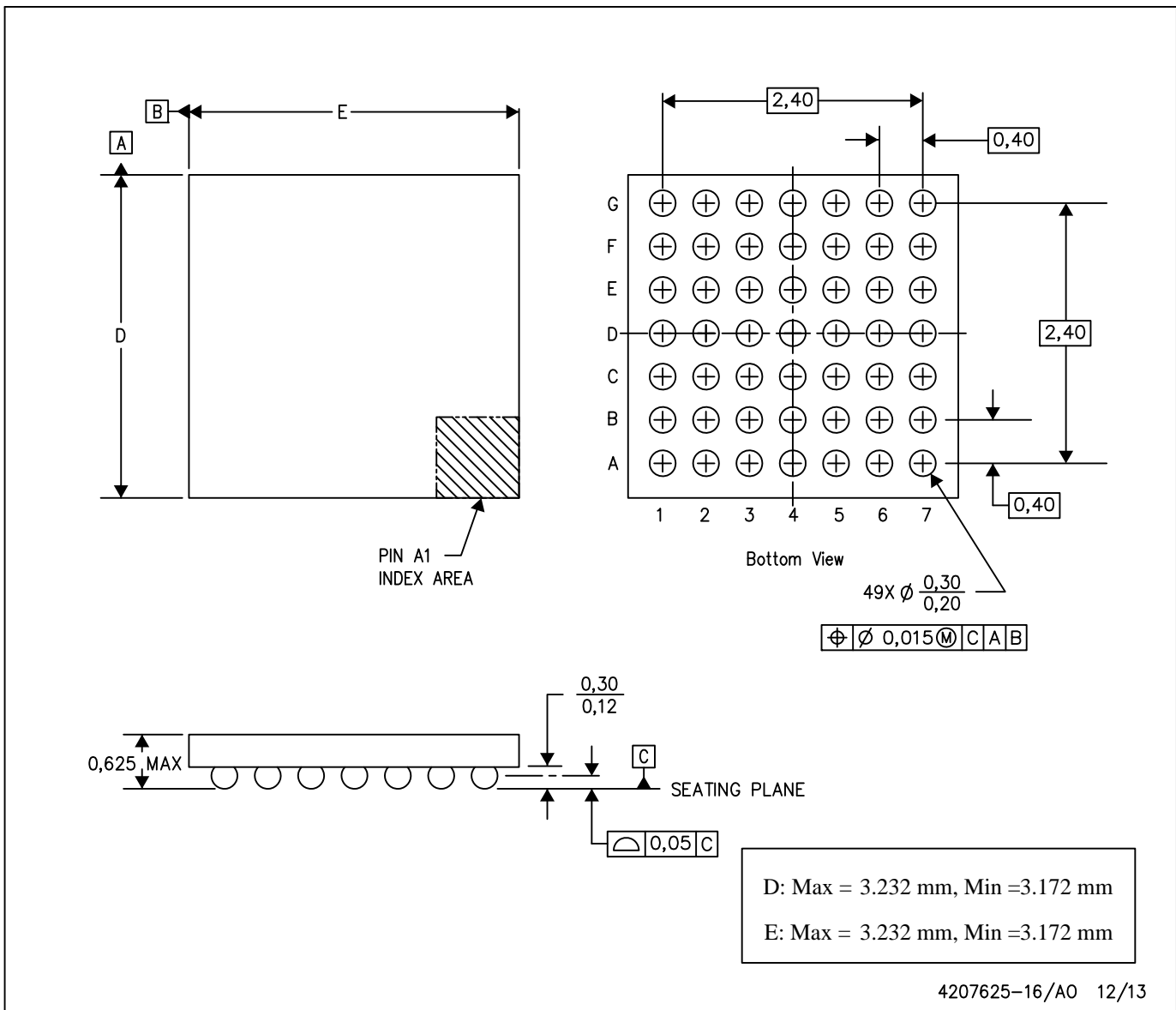
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F2330IRHAR | VQFN         | RHA             | 40   | 2500 | 367.0       | 367.0      | 35.0        |
| MSP430F2330IRHAT | VQFN         | RHA             | 40   | 250  | 210.0       | 185.0      | 35.0        |
| MSP430F2330TRHAR | VQFN         | RHA             | 40   | 2500 | 367.0       | 367.0      | 35.0        |
| MSP430F2330TRHAT | VQFN         | RHA             | 40   | 250  | 210.0       | 185.0      | 35.0        |
| MSP430F2350IRHAR | VQFN         | RHA             | 40   | 2500 | 367.0       | 367.0      | 35.0        |
| MSP430F2350IRHAT | VQFN         | RHA             | 40   | 250  | 210.0       | 185.0      | 35.0        |
| MSP430F2350TRHAR | VQFN         | RHA             | 40   | 2500 | 367.0       | 367.0      | 35.0        |
| MSP430F2350TRHAT | VQFN         | RHA             | 40   | 250  | 210.0       | 185.0      | 35.0        |
| MSP430F2370IRHAR | VQFN         | RHA             | 40   | 2500 | 367.0       | 367.0      | 35.0        |
| MSP430F2370IRHAT | VQFN         | RHA             | 40   | 250  | 210.0       | 185.0      | 35.0        |
| MSP430F2370TRHAR | VQFN         | RHA             | 40   | 2500 | 367.0       | 367.0      | 35.0        |
| MSP430F2370TRHAT | VQFN         | RHA             | 40   | 250  | 210.0       | 185.0      | 35.0        |

YFF (R-XBGA-N49)

DIE-SIZE BALL GRID ARRAY

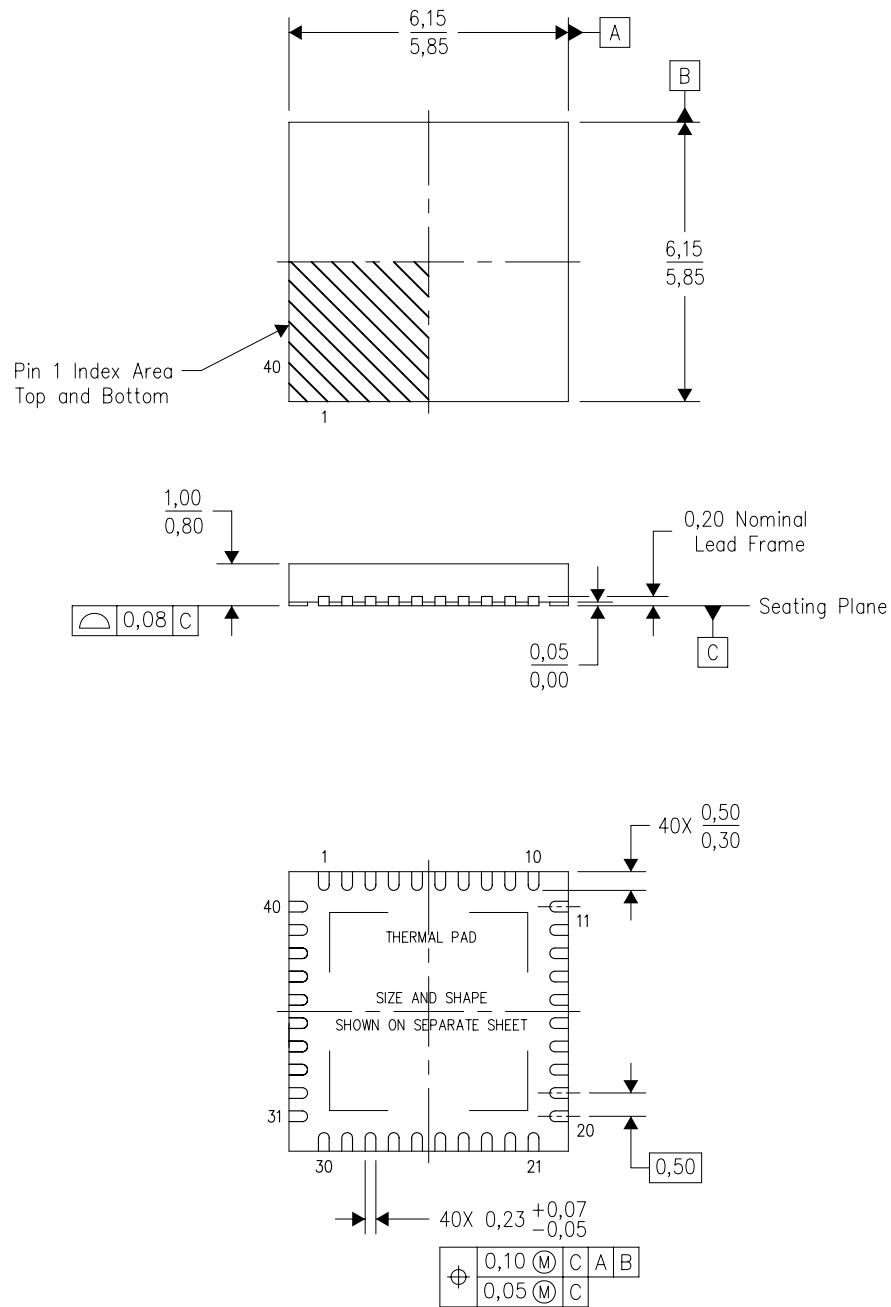


- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
 B. This drawing is subject to change without notice.  
 C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

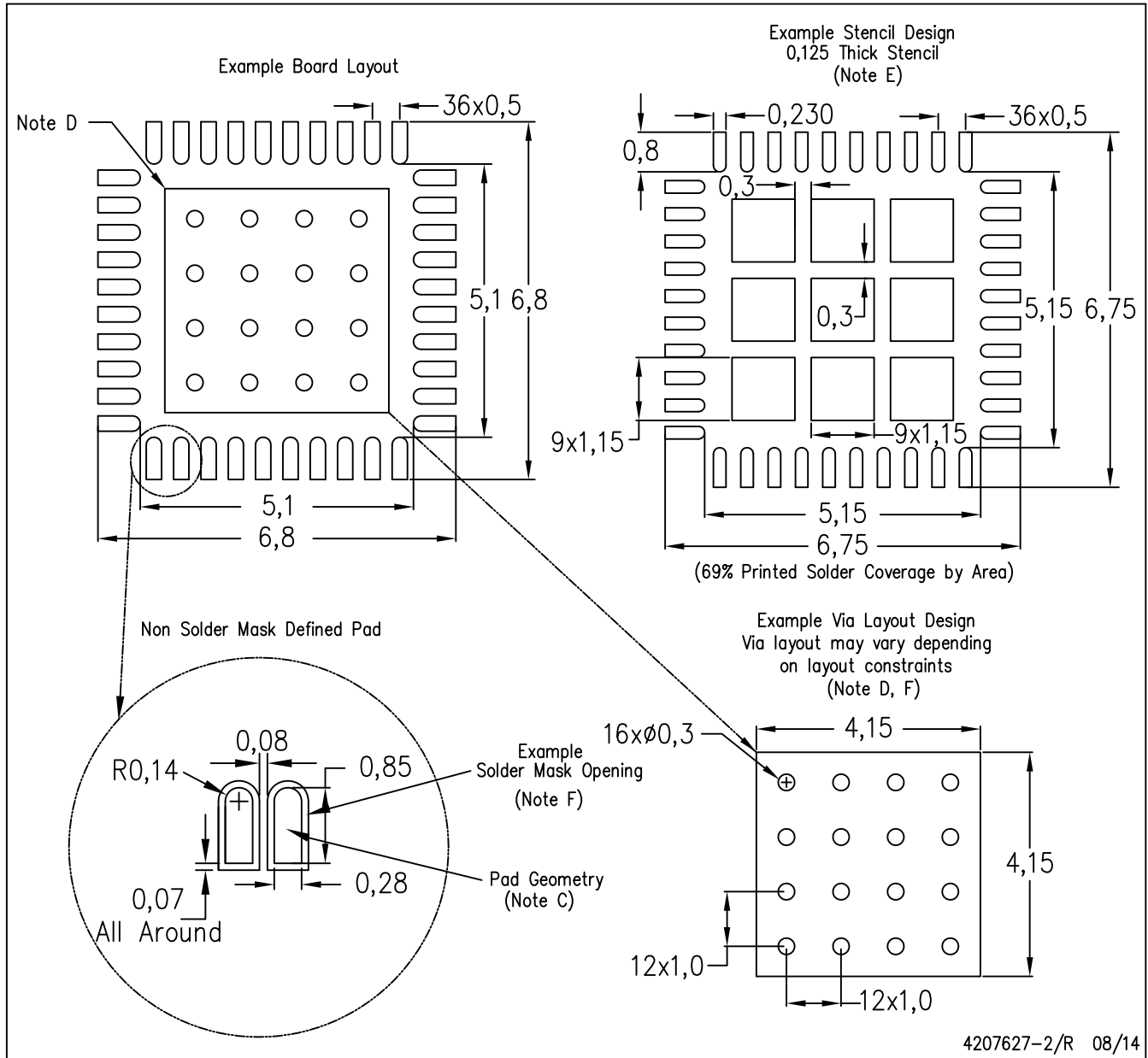
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- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) Package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Package complies to JEDEC MO-220 variation VJJD-2.



RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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