



**THE DATASHEET OF  
THS3201MDGNREP**



## 1.8-GHz LOW-DISTORTION CURRENT-FEEDBACK AMPLIFIER

### FEATURES

- **Unity Gain Bandwidth: 1.8 GHz**
- **High Slew Rate: 6700 V/μs (G = 2 V/V, R<sub>L</sub> = 100 Ω, 5-V Step)**
- **IMD<sub>3</sub>: -78 dBc at 20 MHz: (G = 10 V/V, R<sub>L</sub> = 100 Ω, 2-V<sub>PP</sub> Envelope)**
- **Noise Figure: 11 dB (G = 10 V/V, R<sub>G</sub> = 28 Ω, R<sub>F</sub> = 255 Ω)**
- **Input Referred Noise (f > 10 MHz)**
  - Voltage Noise: 1.65 nV/√Hz
  - Noninverting Current Noise: 13.4 pA/√Hz
  - Inverting Current Noise: 20 pA/√Hz
- **Output Drive: 100 mA**
- **Power-Supply Voltage Range: ±3.3 V to ±7.5 V**

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (-55°C/125°C) Temperature Range<sup>(1)</sup>**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

### APPLICATIONS

- **High-Resolution, High-Sampling-Rate Analog-to-Digital Converter Drivers**
- **High-Resolution, High-Sampling-Rate Digital-to-Analog Converter Output Buffers**
- **Test and Measurement**
- **ATE**

(1) Additional temperature ranges are available - contact factory

### DESCRIPTION

The THS3201 is a wide-band, high-speed current-feedback amplifier, designed to operate over a wide supply range of ±3.3 V to ±7.5 V for today's high-performance applications.

The wide supply range, combined with low distortion and high slew rate, makes the THS3201 ideally suited for arbitrary waveform driver applications. The distortion performance also enables driving high-resolution and high-sampling rate ADCs.

High-voltage operation capabilities make the THS3201 especially suitable for many test, measurement, and ATE applications where lower-voltage devices do not offer enough voltage swing capability. Output rise and fall times are nearly independent of step size (to first-order approximation), making the THS3201 ideal for buffering small to large step pulses with excellent linearity in high dynamic systems.

The THS3201 is offered in 8-pin SOIC and 8-pin MSOP with PowerPAD™ packages.

### RELATED DEVICES AND DESCRIPTIONS

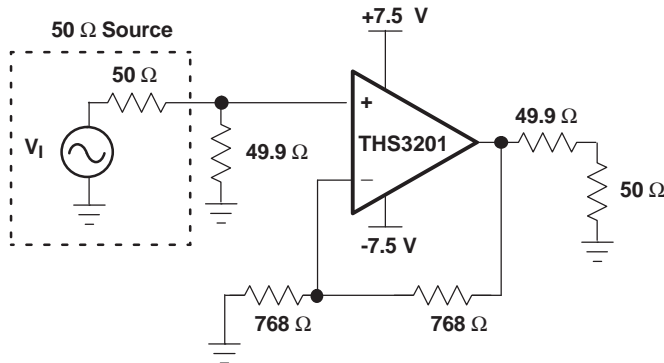
THS3202	±7.5-V 2-GHz Dual Low-Distortion CFB Amplifier
THS3001	±15-V 420-MHz Low-Distortion CFB Amplifier
THS3061/2	±15-V 300-MHz Low-Distortion CFB Amplifier
THS3122	±15-V Dual CFB Amplifier With 350-mA Drive
THS4271	±7.5-V 1.4-GHz Low-Distortion VFB Amplifier



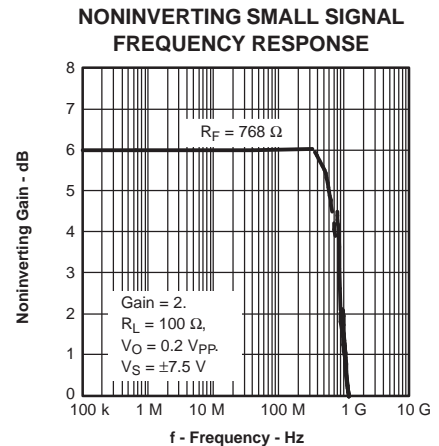
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

**Low-Noise, Low-Distortion, Wideband Application Circuit**



NOTE: Power supply decoupling capacitors not shown



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

$V_S$	Supply voltage	16.5 V
$V_I$	Input voltage	$\pm V_S$
$I_O$	Output current	175 mA
$V_{ID}$	Differential input voltage	$\pm 3$ V
	Continuous power dissipation	See Dissipation Ratings Table
$T_J$	Maximum junction temperature <sup>(2)</sup>	150°C
$T_J$	Maximum junction temperature, continuous operation, long-term reliability <sup>(3)</sup>	125°C
$T_{stg}$	Storage temperature range	-65°C to 150°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s	300°C
ESD ratings	Human body model	3000 V
	Charged device model	1500 V
	Machines model	100 V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The absolute maximum ratings under any condition are limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (3) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See Figure 1 for additional information on thermal derating.

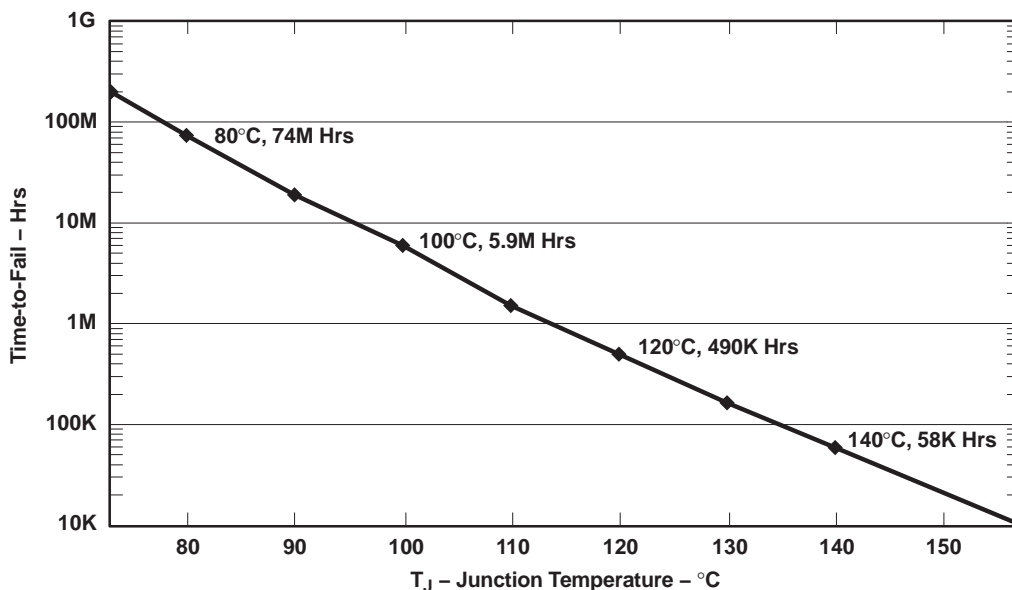


Figure 1. EME-G600 Estimated Wirebond Life

**DISSIPATION RATINGS**

PACKAGE	$\theta_{JC}$ (°C/W)	$\theta_{JA}$ (1) (°C/W)
D (8)	38.3	97.5
DGN (8) (2)	4.7	58.4

- (1) This data was taken using the JEDEC standard High-K test PCB.
- (2) The THS3201 may incorporate a thermal pad on the underside of the chip. This acts as a heat sink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature; which could permanently damage the device. See Texas Instruments technical briefs SLMA002 and SLMA004 for more information about utilizing the PowerPAD thermally enhanced package.

**RECOMMENDED OPERATING CONDITIONS**

		MIN	MAX	UNIT
Supply voltage	Dual supply	±3.3	±7.5	V
	Single supply	6.6	15	
T <sub>A</sub>	Operating free air temperature	-55	125	°C

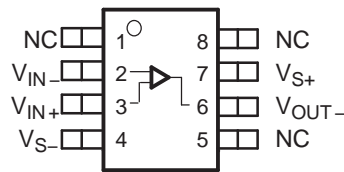
**PACKAGE/ORDERING INFORMATION**

PART NUMBER	PACKAGE TYPE	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY
THS3201MDEP (1)	SOIC-8	—	Rails, 75
THS3201MDREP (1)			Tape and reel, 2500
THS3201MDGNEP (1)	MSOP-8-PP	BLM	Rails, 80
THS3201MDGNREP			Tape and reel, 2500

(1) Product Preview

**PIN ASSIGNMENTS**

**D OR DGN PACKAGE  
(TOP VIEW)**



NC – No internal connection

- A. If a PowerPAD package is used, the thermal pad is electrically isolated from the active circuitry.

**ELECTRICAL CHARACTERISTICS**
 $V_S = \pm 7.5\text{ V}$ ;  $R_f = 1\text{ k}\Omega$ ,  $R_L = 100\ \Omega$ ,  $G = +2$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE		UNIT	MIN/ TYP/ MAX
		25°C	25°C	–55°C to 125°C		
<b>AC Performance</b>						
Small-signal bandwidth, –3 dB ( $V_O = 200\text{ mV}_{pp}$ )	$G = +1$ , $R_F = 1.2\text{ k}\Omega$	1.8			GHz	Typ
	$G = +2$ , $R_F = 768\ \Omega$	850			MHz	
	$G = +5$ , $R_F = 619\ \Omega$	565				
	$G = +10$ , $R_F = 487\ \Omega$	520				
Bandwidth for 0.1-dB flatness	$G = +2$ , $V_O = 200\text{ mV}_{pp}$ , $R_F = 768\ \Omega$	380			MHz	Typ
Large-signal bandwidth	$G = +2$ , $V_O = 2\text{ V}_{pp}$ , $R_F = 715\ \Omega$	880			MHz	Typ
Slew rate (25% to 75% level)	$G = +2$ , $V_O = 5\text{-V step}$ , $R_F = 768\ \Omega$ , Rise/fall	5400/4000			V/ $\mu\text{s}$	Typ
	$G = +2$ , $V_O = 10\text{-V step}$ , $R_F = 768\ \Omega$ , Rise/fall	9800/6700				
Rise and fall time	$G = +2$ , $V_O = 4\text{-V step}$ , $R_F = 768\ \Omega$ , Rise/fall	0.7/0.9			ns	Typ
Settling time to 0.1%	$G = -2$ , $V_O = 2\text{-V step}$	20			ns	Typ
Settling time to 0.01%		60				
Harmonic distortion						
Second-order harmonic	$G = +5$ , $f = 10\text{ MHz}$ , $V_O = 2\text{ V}_{pp}$ , $R_L = 100\ \Omega$	–64			dBc	Typ
Third-order harmonic		–73				
Third-order intermodulation distortion (IMD <sub>3</sub> )	$G = +10$ , $f_c = 20\text{ MHz}$ , $\Delta f = 1\text{ MHz}$ , $V_{O(\text{envelope})} = 2\text{ V}_{pp}$	–78			dBc	Typ
Noise figure	$G = +10$ , $f_c = 100\text{ MHz}$ , $R_F = 255\ \Omega$ , $R_G = 28$	11			dB	Typ
Input voltage noise	$f > 10\text{ MHz}$	1.65			nV/ $\sqrt{\text{Hz}}$	Typ
Input current noise (noninverting)	$f > 10\text{ MHz}$	13.4			pA/ $\sqrt{\text{Hz}}$	Typ
Input current noise (inverting)		20				
Differential gain	$G = +2$ , $R_L = 150\ \Omega$ , $R_F = 768\ \Omega$	NTSC	0.008		%	Typ
		PAL	0.004			
Differential phase	$G = +2$ , $R_L = 150\ \Omega$ , $R_F = 768\ \Omega$	NTSC	0.007		°	Typ
		PAL	0.011			
<b>DC Performance</b>						
Open-loop transimpedance gain	$V_O = \pm 4\text{ V}$ , $R_L = 1\text{ k}\Omega$	300	200	100	k $\Omega$	Min
Input offset voltage	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$	$\pm 0.7$	$\pm 4$	$\pm 6$	mV	Max
Average offset voltage drift	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$			$\pm 13$	$\mu\text{V}/^\circ\text{C}$	Typ
Input bias current (inverting)	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$	$\pm 13$	$\pm 65$	$\pm 90$	$\mu\text{A}$	Max
Average bias current drift (–)	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$			$\pm 400$	nA/ $^\circ\text{C}$	Typ
Input bias current (noninverting)	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$	$\pm 14$	$\pm 40$	$\pm 60$	$\mu\text{A}$	Max
Average bias current drift (+)	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$			$\pm 400$	nA/ $^\circ\text{C}$	Typ

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_S = \pm 7.5\text{ V}$ ;  $R_f = 1\text{ k}\Omega$ ,  $R_L = 100\ \Omega$ ,  $G = +2$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE		UNIT	MIN/ TYP/ MAX
		25°C	25°C	–55°C to 125°C		
<b>Input</b>						
Common-mode input range	$R_L = 1\text{ k}\Omega$	$\pm 5.1$	$\pm 5$	$\pm 5$	V	Min
Common-mode rejection ratio	$V_{CM} = \pm 3.75\text{ V}$	71	58	53	dB	Min
Inverting input impedance, $Z_{in}$	Open loop	16			$\Omega$	Typ
Input resistance	Noninverting	780			k $\Omega$	Typ
	Inverting	11			$\Omega$	
Input capacitance	Noninverting	1			pF	Typ
<b>Output</b>						
Voltage output swing	$R_L = 1\text{ k}\Omega$	$\pm 6$	$\pm 5.9$	$\pm 5.7$	V	Min
	$R_L = 100\ \Omega$	$\pm 5.8$	$\pm 5.7$	$\pm 5.35$		
Current output, sourcing	$R_L = 20\ \Omega$	115	105	100	mA	Min
Current output, sinking	$R_L = 20\ \Omega$	100	85	80	mA	Min
Closed-loop output impedance	$G = +1$ , $f = 1\text{ MHz}$	0.01			$\Omega$	Typ
<b>Power Supply</b>						
Minimum operating voltage	Absolute minimum		$\pm 3.3$	$\pm 3.3$	V	Min
Maximum operating voltage	Absolute maximum		$\pm 7.5$	$\pm 7.5$	V	Max
Maximum quiescent current	Output open	14	18	22	mA	Max
Power-supply rejection (+PSRR)	$V_{S+} = 7\text{ V to } 8\text{ V}$ , $R_L = 1\text{ k}\Omega$	69	60	56	dB	Min
Power-supply rejection (–PSRR)	$V_{S-} = -7\text{ V to } -8\text{ V}$ , $R_L = 1\text{ k}\Omega$	65	58	55	dB	Min

**ELECTRICAL CHARACTERISTICS**
 $V_S = \pm 5\text{ V}$ ;  $R_f = 1\text{ k}\Omega$ ,  $R_L = 100\ \Omega$ ,  $G = +2$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE		UNIT	MIN/ TYP/ MAX	
		25°C	25°C	–55°C to 125°C			
<b>AC Performance</b>							
Small-signal bandwidth, –3 dB ( $V_O = 200\text{ mV}_{pp}$ )	$G = +1$ , $R_F = 1.2\text{ k}\Omega$	1.3			GHz	Typ	
	$G = +2$ , $R_F = 715\ \Omega$	725			MHz		
	$G = +5$ , $R_F = 576\ \Omega$	540					
	$G = +10$ , $R_F = 464\ \Omega$	480					
Bandwidth for 0.1-dB flatness	$G = +2$ , $V_O = 200\text{ mV}_{pp}$ , $R_F = 715\ \Omega$	170			MHz	Typ	
Large-signal bandwidth	$G = +2$ , $V_O = 2\text{ V}_{pp}$ , $R_F = 715\ \Omega$	900			MHz	Typ	
Slew rate (25% to 75% level)	$G = +2$ , $V_O = 5\text{-V step}$ , $R_F = 715\ \Omega$ , Rise/Fall	5200/4000			V/ $\mu\text{s}$	Typ	
Rise and fall time	$G = +2$ , $V_O = 4\text{-V step}$ , $R_F = 715\ \Omega$ , Rise/Fall	0.7/0.9			ns	Typ	
Settling time to 0.1%	$G = -2$ , $V_O = 2\text{-V step}$	20			ns	Typ	
Settling time to 0.01%		60					
<b>Harmonic distortion</b>							
Second-order harmonic	$G = +5$ , $f = 10\text{ MHz}$ , $V_O = 2\text{ V}_{pp}$	$R_L = 100\ \Omega$	–69			dBc	Typ
Third-order harmonic	$G = +5$ , $f = 10\text{ MHz}$ , $V_O = 2\text{ V}_{pp}$	$R_L = 100\ \Omega$	–75			dBc	Typ
Third-order intermodulation distortion (IMD <sub>3</sub> )	$G = +10$ , $f_c = 20\text{ MHz}$ , $\Delta f = 1\text{ MHz}$ , $V_{O(\text{envelope})} = 2\text{ V}_{pp}$		–81			dBc	Typ
Noise figure	$G = +10$ , $f_c = 100\text{ MHz}$ , $R_F = 255\ \Omega$ , $R_G = 28$		11			dB	Typ
Input voltage noise	$f > 10\text{ MHz}$		1.65			nV/ $\sqrt{\text{Hz}}$	Typ
Input current noise (noninverting)	$f > 10\text{ MHz}$		13.4			pA/ $\sqrt{\text{Hz}}$	Typ
Input current noise (inverting)			20			pA/ $\sqrt{\text{Hz}}$	Typ
Differential gain	$G = +2$ , $R_L = 150\ \Omega$ , $R_F = 768\ \Omega$	NTSC	0.006			%	Typ
		PAL	0.004				
Differential phase	$G = +2$ , $R_L = 150\ \Omega$ , $R_F = 768\ \Omega$	NTSC	0.03			°	Typ
		PAL	0.04				
<b>DC Performance</b>							
Open-loop transimpedance gain	$V_O = \pm 2\text{ V}$ , $R_L = 1\text{ k}\Omega$		300	200	100	k $\Omega$	Min
Input offset voltage	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$		$\pm 0.7$	$\pm 3$	$\pm 5.5$	mV	Max
Average offset voltage drift	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$				$\pm 13$	$\mu\text{V}/^\circ\text{C}$	Typ
Input bias current (inverting)	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$		$\pm 13$	$\pm 65$	$\pm 90$	$\mu\text{A}$	Max
Average bias current drift (–)	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$				$\pm 400$	nA/ $^\circ\text{C}$	Typ
Input bias current (noninverting)	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$		$\pm 14$	$\pm 40$	$\pm 60$	$\mu\text{A}$	Max
Average bias current drift (+)	$V_{CM} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$				$\pm 400$	nA/ $^\circ\text{C}$	Typ

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_S = \pm 5\text{ V}$ ;  $R_f = 1\text{ k}\Omega$ ,  $R_L = 100\ \Omega$ ,  $G = +2$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE		UNIT	MIN/ TYP/ MAX
		25°C	25°C	–55°C to 125°C		
<b>Input</b>						
Common-mode input range	$R_L = 1\text{ k}\Omega$	$\pm 2.6$	$\pm 2.5$	$\pm 2.5$	V	Min
Common-mode rejection ratio	$V_{CM} = \pm 2.5\text{ V}$	71	56	50	dB	Min
Inverting input impedance, $Z_{in}$	Open loop, $R_L = 1\text{ k}\Omega$	17.5			$\Omega$	Typ
Input resistance	Noninverting	780			k $\Omega$	Typ
	Inverting	11			$\Omega$	
Input capacitance	Noninverting	1			pF	Typ
<b>Output</b>						
Voltage output swing	$R_L = 1\text{ k}\Omega$	$\pm 3.65$	$\pm 3.5$	$\pm 3.4$	V	Min
	$R_L = 100\ \Omega$	$\pm 3.45$	$\pm 3.33$	$\pm 3.2$		
Current output, sourcing	$R_L = 20\ \Omega$	115	105	90	mA	Min
Current output, sinking	$R_L = 20\ \Omega$	100	80	75	mA	Min
Closed-loop output impedance	$G = +1$ , $f = 1\text{ MHz}$	0.01			$\Omega$	Typ
<b>Power Supply</b>						
Minimum operating voltage	Absolute minimum		$\pm 3.3$	$\pm 3.3$	V	Min
Maximum operating voltage	Absolute maximum		$\pm 7.5$	$\pm 7.5$	V	Max
Maximum quiescent current		14	16.8	20.5	mA	Max
Power-supply rejection (+PSRR)	$V_{S+} = 4.5\text{ V to } 5.5\text{ V}$ , $R_L = 1\text{ k}\Omega$	69	60	56	dB	Min
Power-supply rejection (–PSRR)	$V_{S-} = -4.5\text{ V to } -5.5\text{ V}$ , $R_L = 1\text{ k}\Omega$	65	58	55	dB	Min

## TYPICAL CHARACTERISTICS

**Table of Graphs ( $V_S = \pm 7.5\text{ V}$ )**

		FIGURE NO.
Noninverting small-signal frequency response		2, 3
Inverting small-signal frequency response		4
Inverting large-signal frequency response		5, 6
0.1-dB gain flatness frequency response		7
Capacitive load frequency response		8
Recommended switching resistance	vs Capacitive load	9
2nd harmonic distortion	vs Frequency	10
3rd harmonic distortion	vs Frequency	11
2nd-order harmonic distortion, $G = 2$	vs Output voltage	12
3rd-order harmonic distortion, $G = 2$	vs Output voltage	13
2nd-order harmonic distortion, $G = 5$	vs Output voltage	14
3rd-order harmonic distortion, $G = 5$	vs Output voltage	15
2nd-order harmonic distortion, $G = 10$	vs Output voltage	16
3rd-order harmonic distortion, $G = 10$	vs Output voltage	17
3rd-order intermodulation distortion ( $IMD_3$ )	vs Frequency	18
S-Parameter	vs Frequency	19, 20
Input voltage and current noise	vs Frequency	21
Noise figure	vs Frequency	22
Transimpedance	vs Frequency	23
Input offset voltage	vs Case temperature	24
Input bias and offset current	vs Case temperature	25
Slew rate	vs Output voltage	26
Settling time		27, 28
Quiescent current	vs Supply voltage	29
Output voltage	vs Load resistance	30
Rejection ratio	vs Frequency	31
Noninverting small-signal transient response		32
Inverting large-signal transient response		33
Overdrive recovery time		34
Differential gain	vs Number of loads	35
Differential phase	vs Number of loads	36
Closed-loop output impedance	vs Frequency	37

**Table of Graphs ( $V_S = \pm 5\text{ V}$ )**

		<b>Figure No.</b>
Noninverting small-signal frequency response		38
Inverting small-signal frequency response		39
0.1-dB gain flatness frequency response		40
2nd-order harmonic distortion	vs Frequency	41
3rd-order harmonic distortion	vs Frequency	42
2nd-order harmonic distortion, G = 2	vs Output voltage	43
3rd-order harmonic distortion, G = 2	vs Output voltage	44
2nd-order harmonic distortion, G = 5	vs Output voltage	45
3rd-order harmonic distortion, G = 5	vs Output voltage	46
2nd-order harmonic distortion, G = 10	vs Output voltage	47
3rd-order harmonic distortion, G = 10	vs Output voltage	48
3rd-order intermodulation distortion (IMD <sub>3</sub> )	vs Frequency	49
S-Parameter	vs Frequency	50, 51
Slew rate	vs Output voltage	52
Noninverting small-signal transient response		53
Inverting large-signal transient response		54
Overdrive recovery time		55

**$V_S = \pm 7.5$  V Graphs**

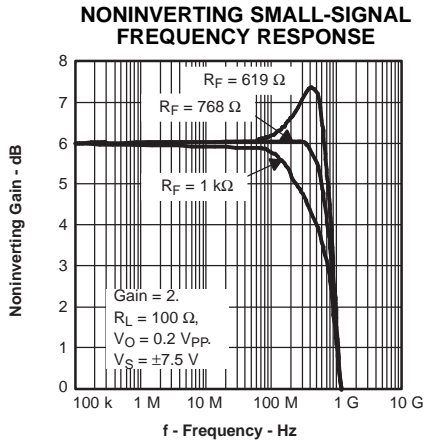


Figure 2.

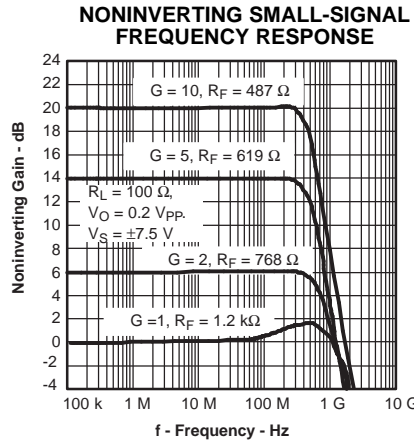


Figure 3.

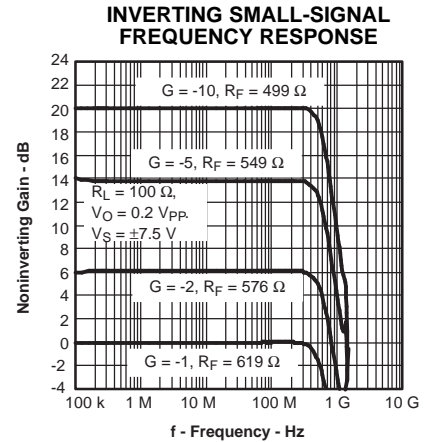


Figure 4.

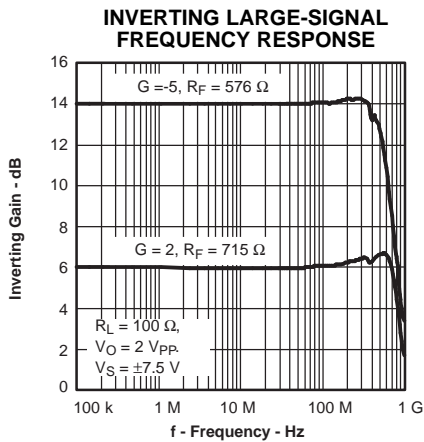


Figure 5.

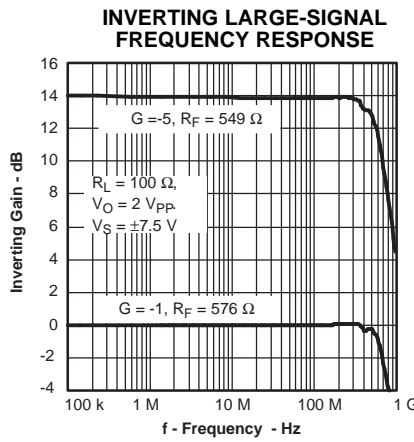


Figure 6.

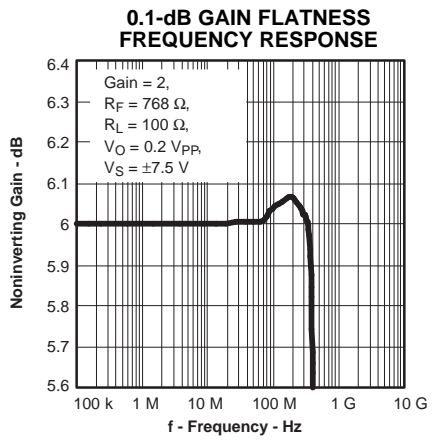


Figure 7.

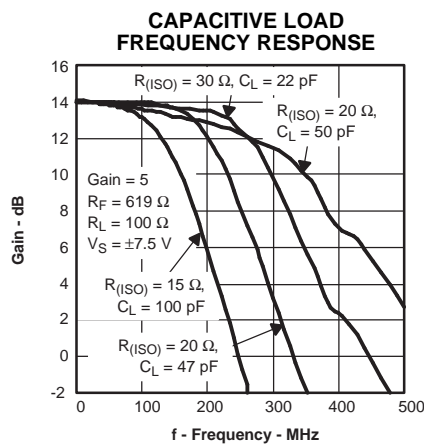


Figure 8.

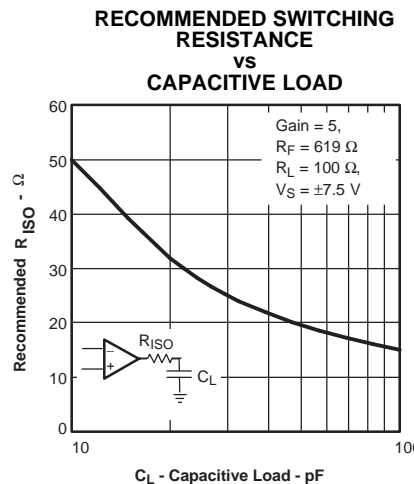


Figure 9.

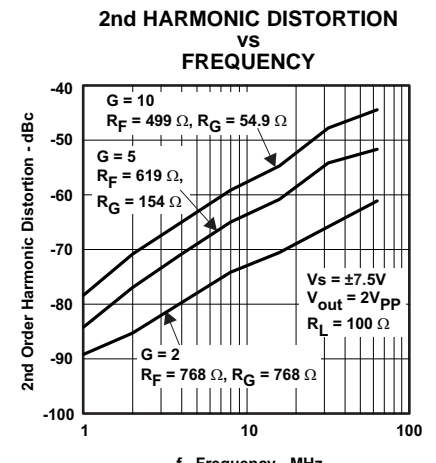


Figure 10.

$V_S = \pm 7.5\text{ V}$  Graphs (continued)

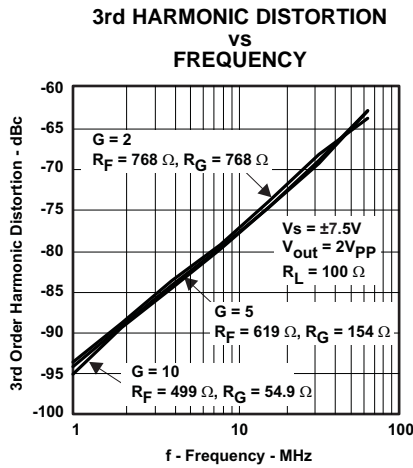


Figure 11.

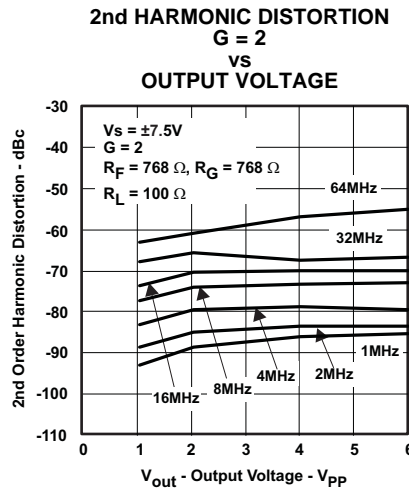


Figure 12.

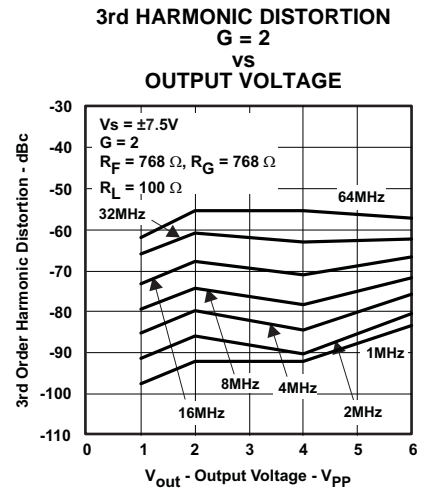


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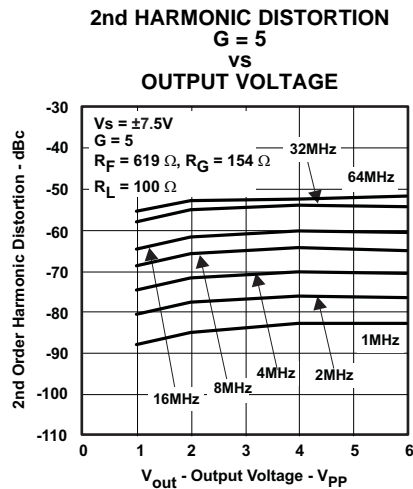


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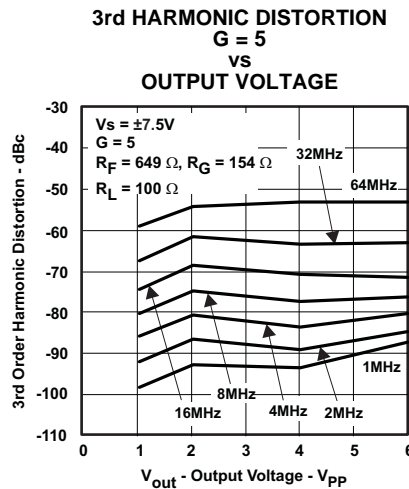


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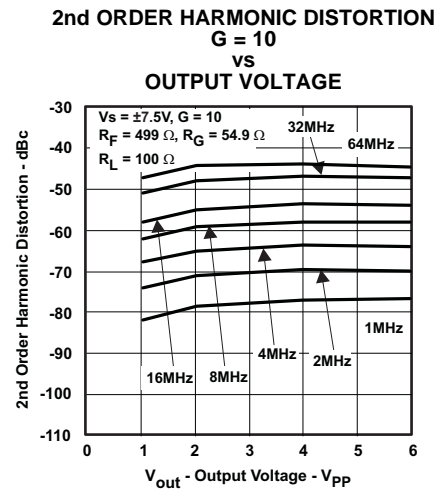


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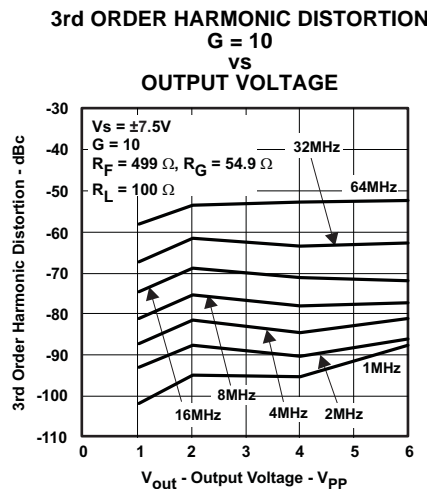


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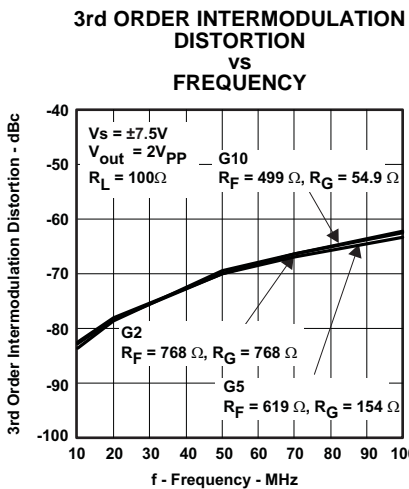


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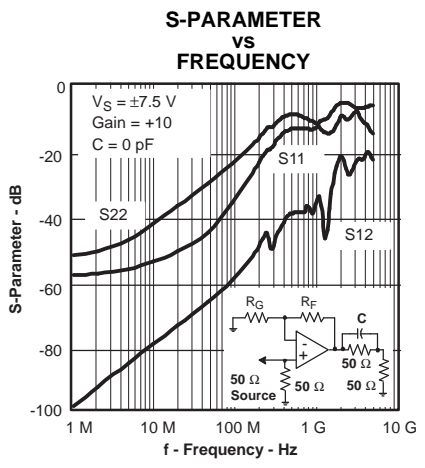


Figure 19.

$V_S = \pm 7.5$  V Graphs (continued)

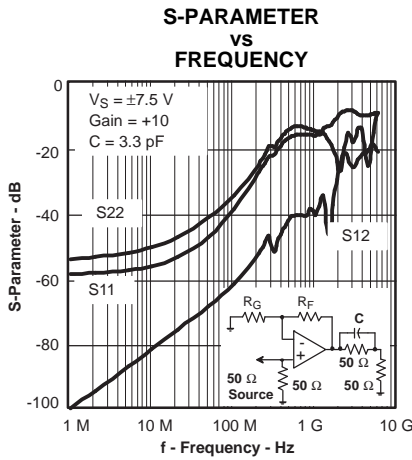


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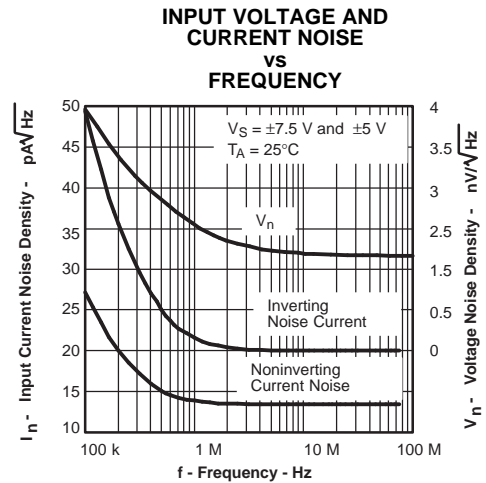


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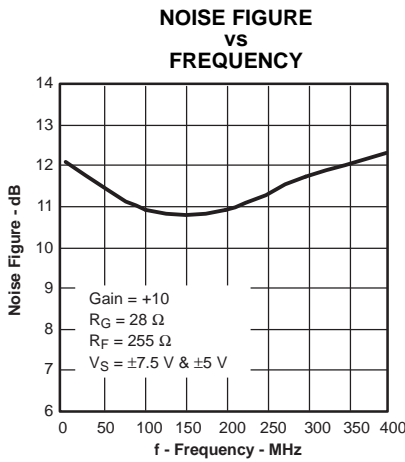


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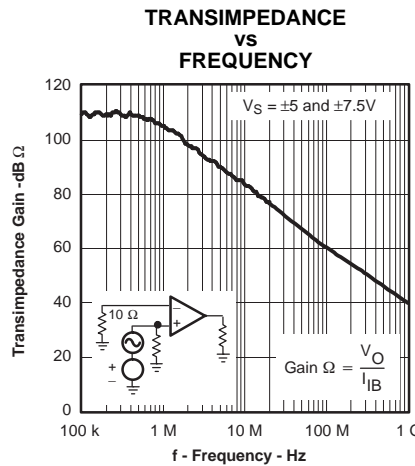


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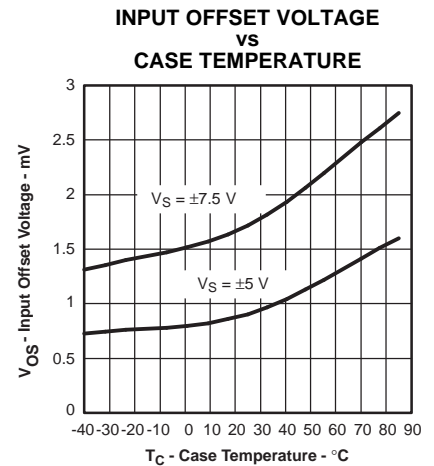


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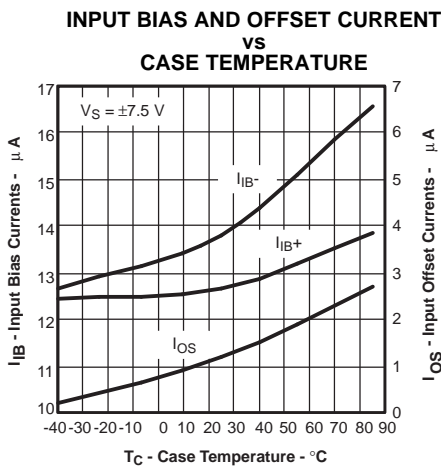


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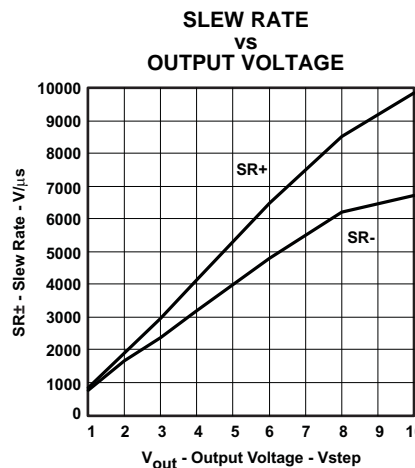


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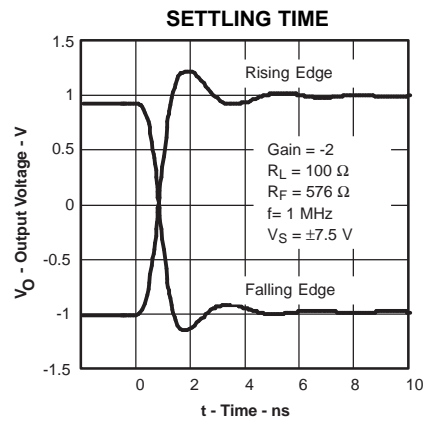


Figure 27.

**$V_S = \pm 7.5$  V Graphs (continued)**

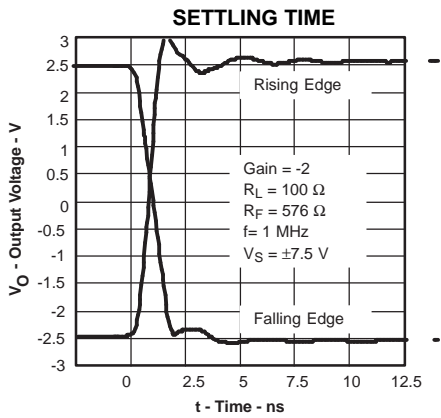


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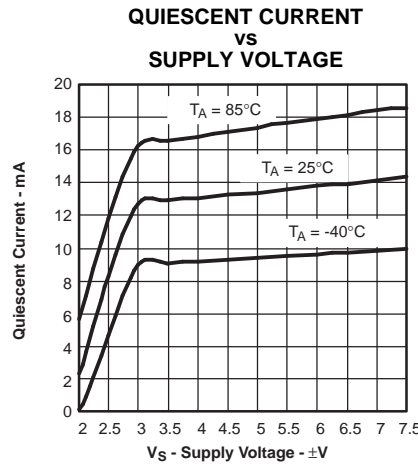


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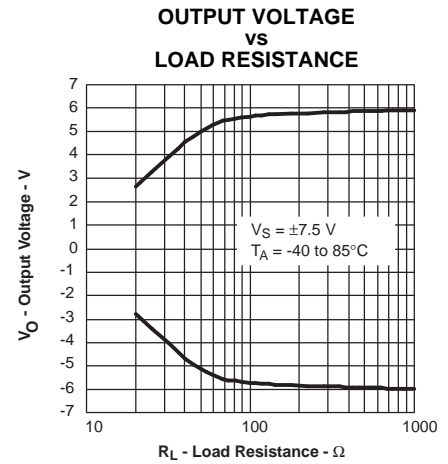


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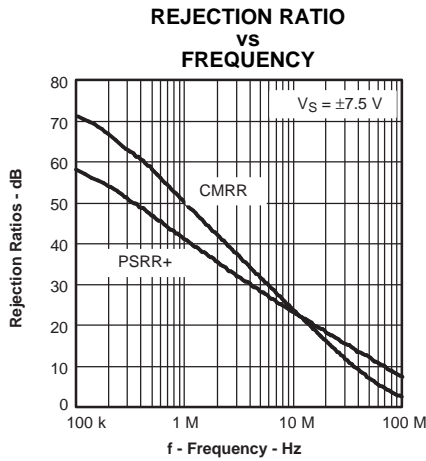


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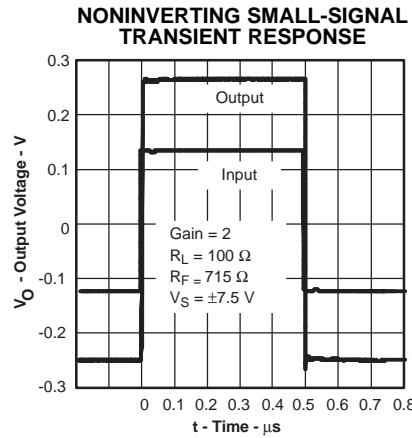


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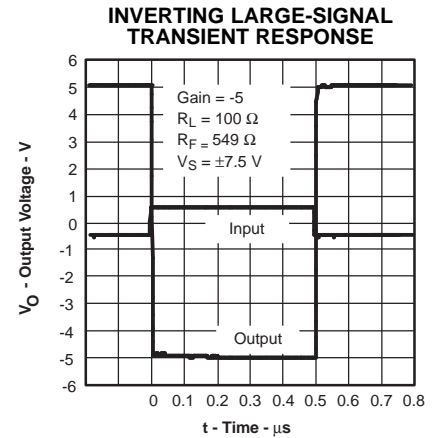


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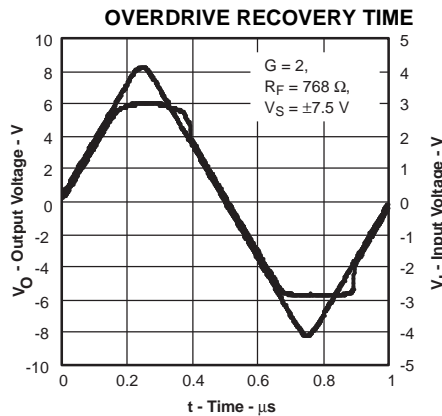


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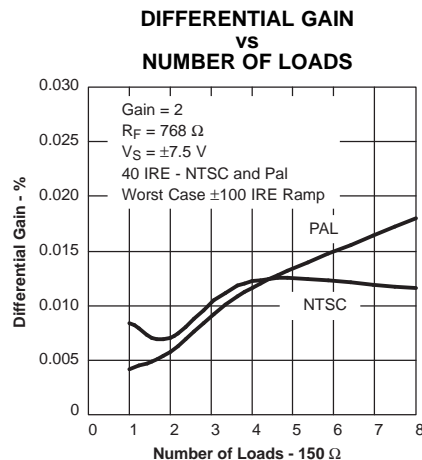


Figure 35.

$V_S = \pm 7.5$  V Graphs (continued)

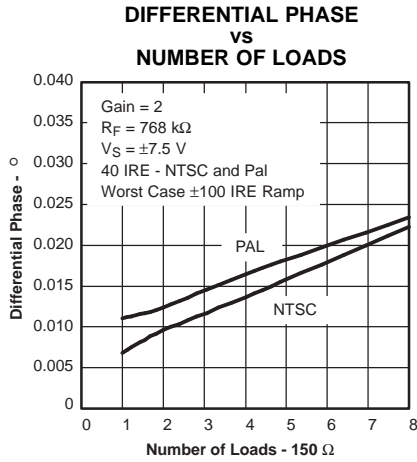


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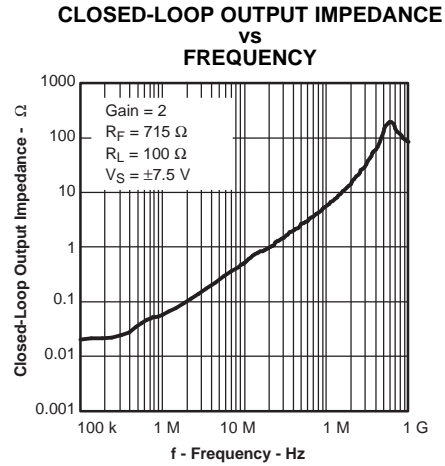


Figure 37.

$V_S = \pm 5$  V Graphs

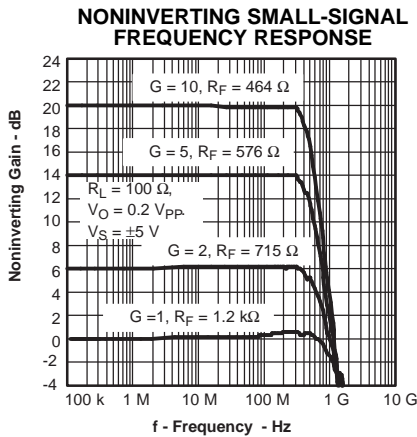


Figure 38.

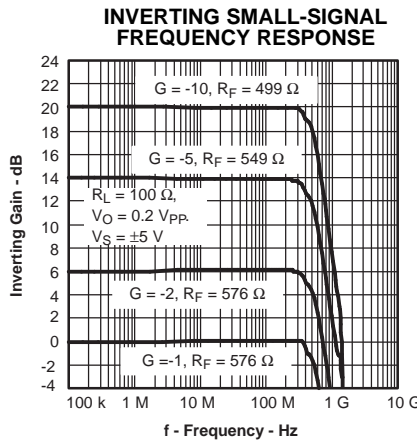


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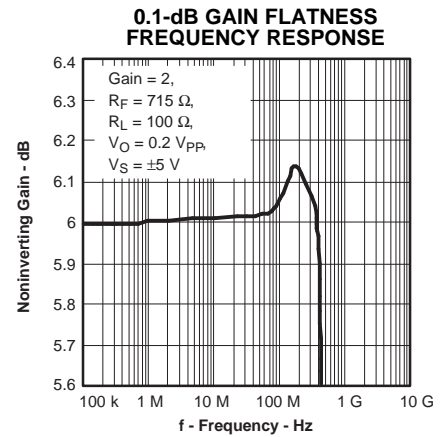


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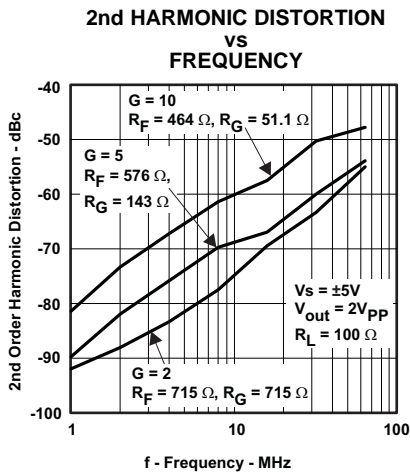


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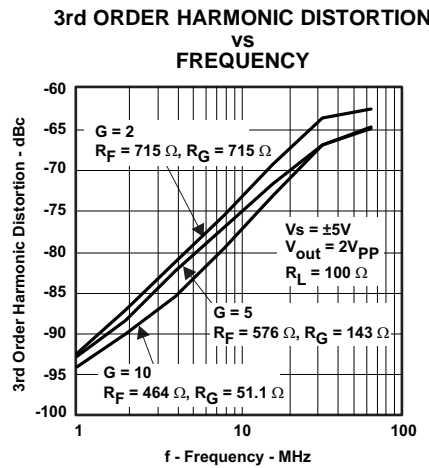


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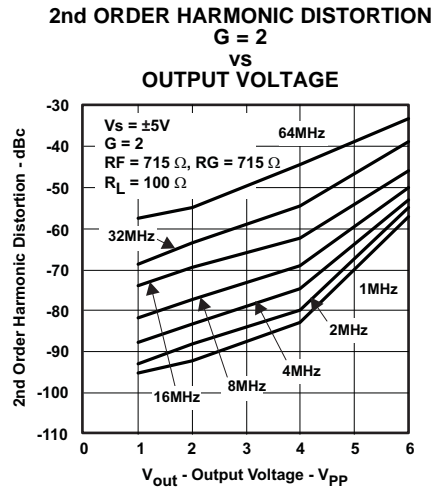
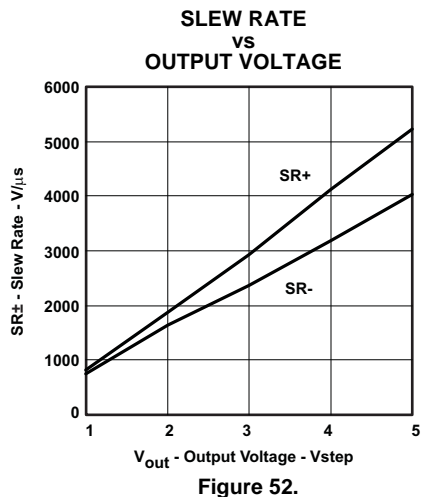
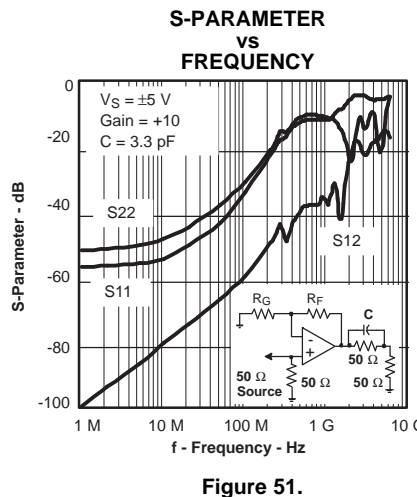
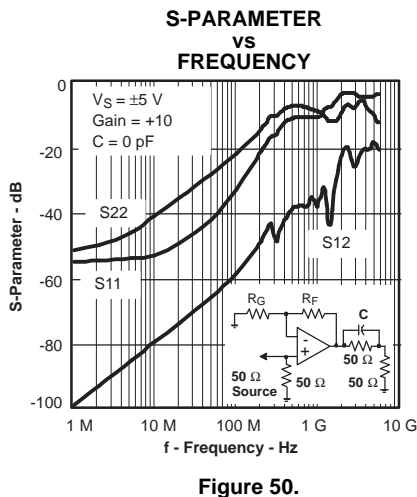
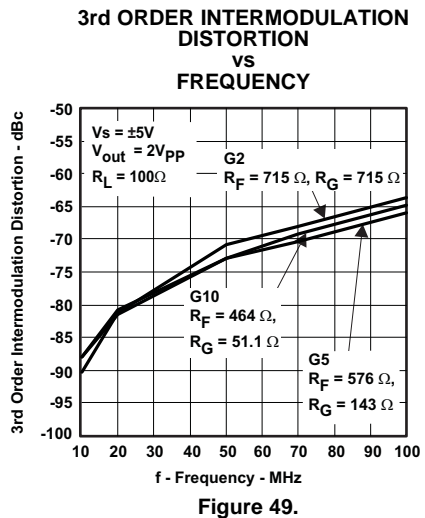
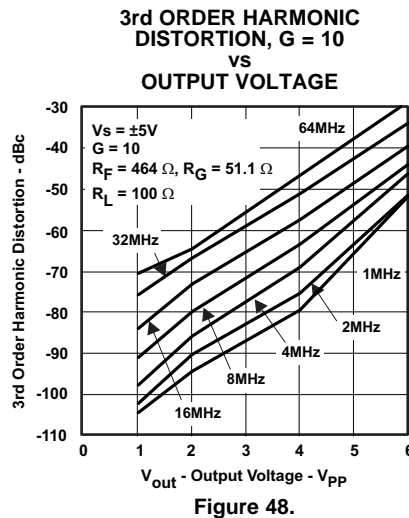
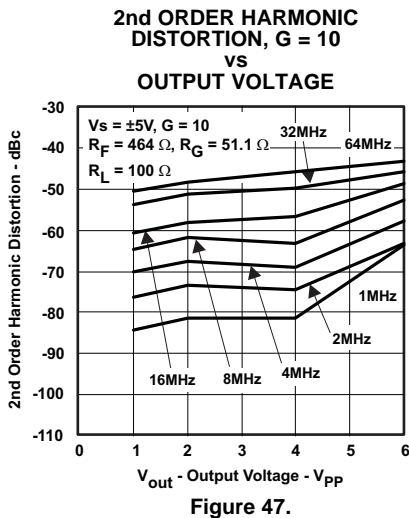
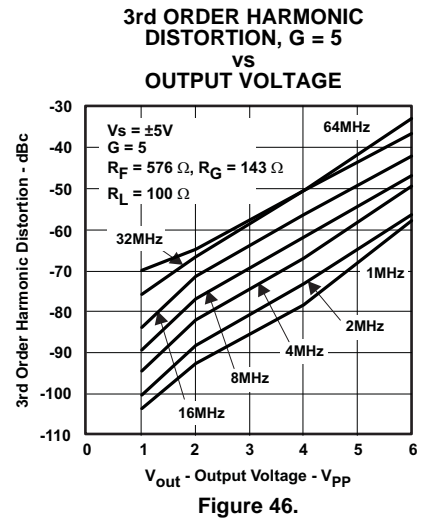
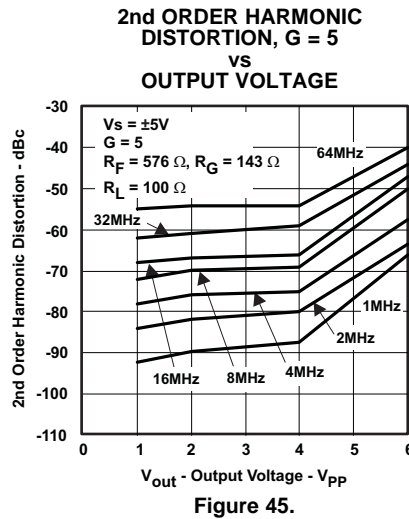
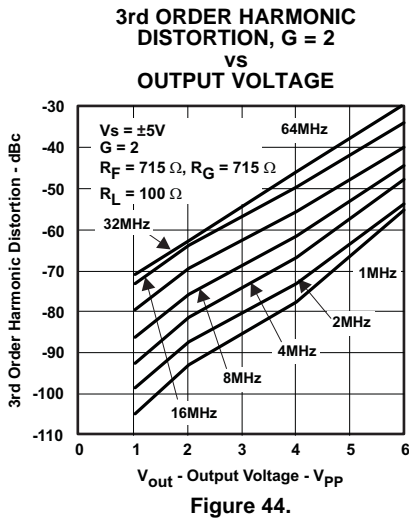


Figure 43.

$V_s = \pm 5$  V Graphs (continued)



$V_S = \pm 5\text{ V}$  Graphs (continued)

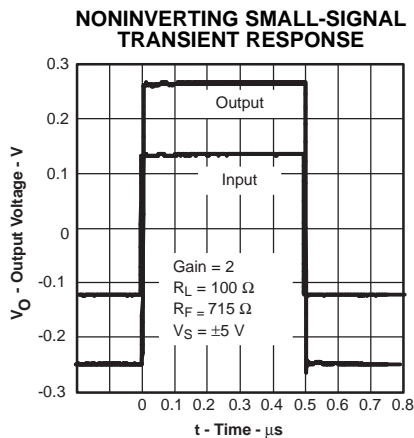


Figure 53.

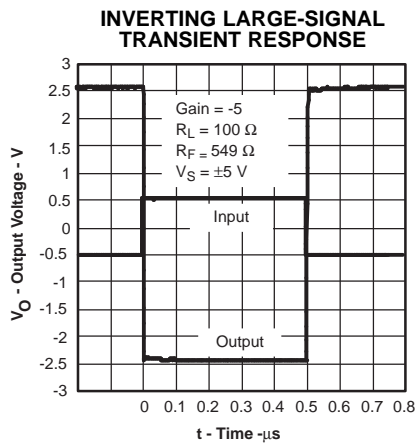


Figure 54.

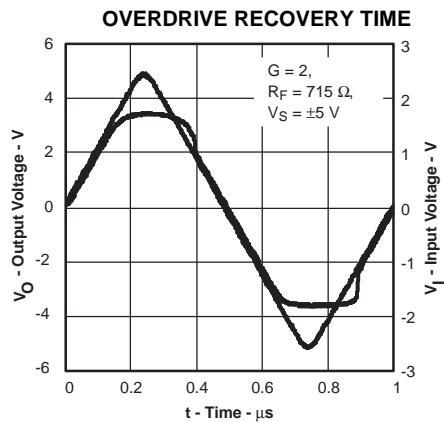


Figure 55.

APPLICATION INFORMATION

Wideband Noninverting Operation

The THS3201 is a unity gain stable 1.8-GHz current-feedback operational amplifier, designed to operate from a  $\pm 3.3\text{-V}$  to  $\pm 7.5\text{-V}$  power supply.

Figure 56 shows the THS3201 in a noninverting gain of 2-V/V configuration typically used to generate the performance curves. Most of the curves are characterized using signal sources with 50- $\Omega$  source impedance, and with measurement equipment presenting a 50- $\Omega$  load impedance. The 49.9- $\Omega$  shunt resistor at the  $V_I$  terminal in Figure 56 matches the source impedance of the test generator.

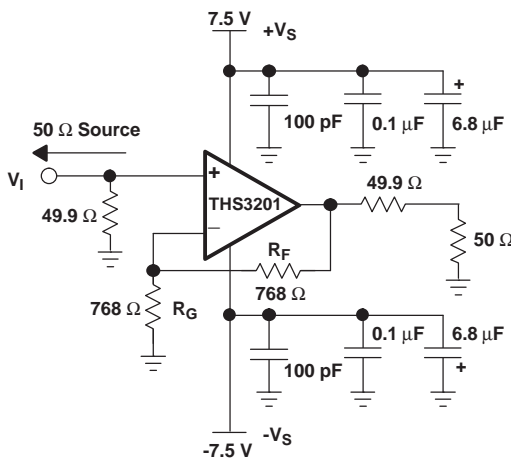


Figure 56. Wideband Noninverting Gain Configuration

Unlike voltage-feedback amplifiers, current-feedback amplifiers are highly dependent on the feedback resistor  $R_F$  for maximum performance and stability. Table 1 shows the optimal gain setting resistors  $R_F$  and  $R_G$  at different gains to give maximum bandwidth with minimal peaking in the frequency response. Higher bandwidths can be achieved, at the expense of added peaking in the frequency response, by using even lower values for  $R_F$ . Conversely, increasing  $R_F$  decreases the bandwidth, but stability is improved.

Table 1. Recommended Resistor Values for Optimum Frequency Response

THS3201 $R_F$ for AC When $R_{load} = 100 \Omega$			
Gain (V/V)	Supply Voltage (V)	$R_G$ ( $\Omega$ )	$R_F$ ( $\Omega$ )
1	$\pm 7.5$	—	1.2 k
	$\pm 5$	—	1.2 k
2	$\pm 7.5$	768	768
	$\pm 5$	715	715
5	$\pm 7.5$	154.9	619
	$\pm 5$	143	576
10	$\pm 7.5$	54.9	487
	$\pm 5$	51.1	464
-1	$\pm 7.5$	619	619
	$\pm 5$	576	576
-2	$\pm 7.5$ and $\pm 5$	287	576
-5	$\pm 7.5$ and $\pm 5$	110	549
-10	$\pm 7.5$ and $\pm 5$	49.9	499

Wideband Inverting Gain Operation

Figure 57 shows the THS3201 is a typical inverting gain configuration, where the input and output impedances and signal gain from Figure 56 are retained in an inverting circuit configuration.

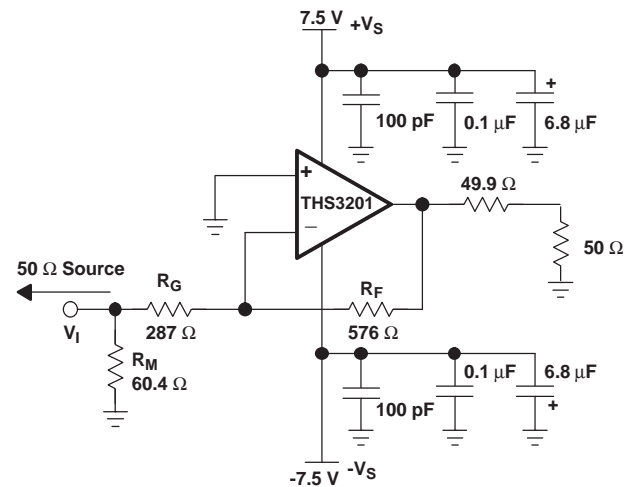


Figure 57. Wideband Inverting Gain Configuration

### Single Supply Operation

The THS3201 has the capability to operate from a single-supply voltage ranging from 6.6 V to 15 V. When operating from a single power supply, care must be taken to ensure the input signal and amplifier is biased appropriately to allow for the maximum output voltage swing. The circuits shown in [Figure 58](#) demonstrate methods to configure an amplifier in a manner conducive for single-supply operation

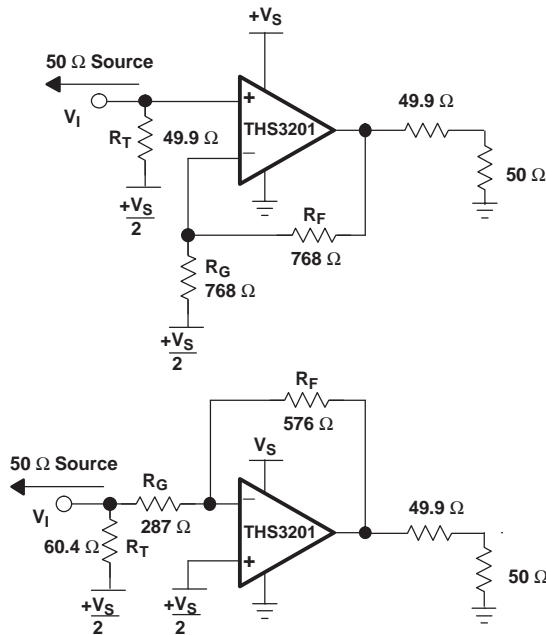


Figure 58. DC-Coupled Single-Supply Operation

### Video HDTV Drivers

The exceptional bandwidth and slew rate of the THS3201 matches the demands for professional video and HDTV. Most commercial HDTV standards require a video passband of 30 MHz. To ensure high signal quality with minimal degradation of performance, a 0.1-dB gain flatness should be at least 7x the passband frequency to minimize group delay variations requiring 210-MHz 0.1-dB frequency flatness from the amplifier. High slew rates ensure there is minimal distortion of the video signal. Component video and RGB video signals require fast transition times and fast settling times to keep high signal quality. The THS8135, for example, is a 240-MSPS video DAC and has a transition time approaching 4 ns. The THS3201 is a perfect candidate for interfacing the output of such high-performance video components.

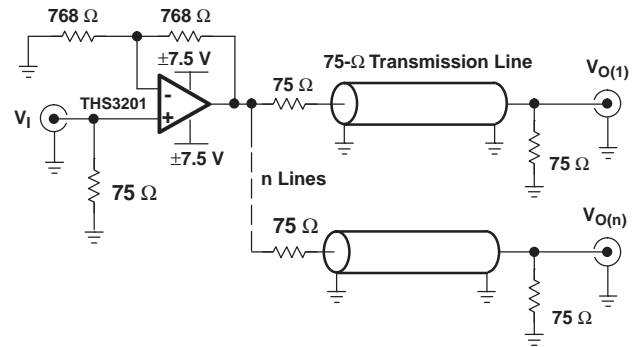


Figure 59. Video Distribution Amplifier Application

### ADC Driver Application

The THS3201 can be used as a high-performance ADC driver in applications such as radio receiver IF stages and test and measurement devices. All high-performance ADCs have differential inputs. The THS3201 can be used in conjunction with a transformer as a drive amplifier in these applications. [Figure 60](#) and [Figure 61](#) show two different approaches.

In [Figure 60](#), a transformer is used after the amplifier to convert the signal to differential. The advantage of this approach is fewer components are required.  $R_{OUT}$  and  $R_T$  are required for impedance matching the transformer.

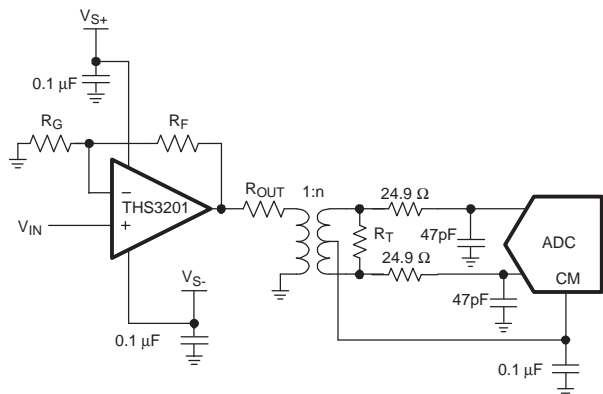


Figure 60. Differential ADC Driver Circuit 1

In [Figure 61](#), a transformer is used before two amplifiers to convert the signal to differential. The two amplifiers then amplify the differential signal. The advantage to this approach is each amplifier is required to drive one half the voltage as before.  $R_T$  is used to impedance match the transformer.

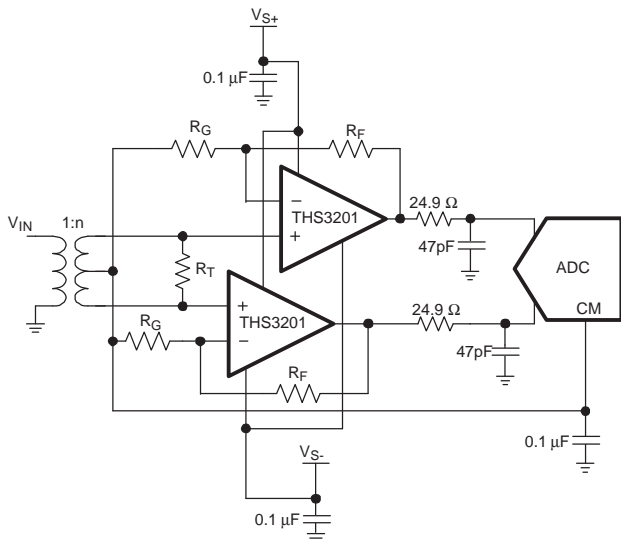


Figure 61. Differential ADC Driver Circuit 2

It is almost universally recommended to use a resistor and capacitor between the operational amplifier output and the ADC input as shown in Figure 60 and Figure 61.

This resistor-capacitor (RC) combination has multiple functions:

- The capacitor is a local charge reservoir for ADC.
- The resistor isolates the amplifier from the ADC.
- In conjunction, they form a low-pass noise filter.

During the sampling phase, current is required to charge the ADC input sampling capacitors. By placing external capacitors directly at the input pins, most of the current is drawn from them. They are seen as a low-impedance source. They can be thought of as serving much the same purpose as a power-supply bypass capacitor - to supply transient current - with the amplifier then providing the bulk charge.

Typically, a low-value capacitor in the range of 10 pF to 100 pF provides the required transient charge reservoir.

The capacitance and the switching action of the ADC is one of the worst loading scenarios that a high-speed amplifier encounters. The resistor provides a simple means of isolating the associated phase shift from the feedback network and maintaining the phase margin of the amplifier.

Typically, a low-value resistor in the range of 10 Ω to 100 Ω provides the required isolation. Together, the R and C form a real pole in the s-plane located at the frequency:

$$f_p = \frac{1}{2\pi RC}$$

Placing this pole at about 10x the highest frequency of interest ensures it has no impact on the signal. Since the resistor is typically a small value, it is bad practice to place the pole at (or near) frequencies of interest. At the pole frequency, the amplifiers see a load with a magnitude of:

$$\sqrt{2} \times R$$

If R is only 10 Ω, the amplifier is heavily loaded above the pole frequency, and generates excessive distortion.

### DAC Driver Application

The THS3201 can be used as a high-performance DAC output driver in applications such as radio transmitter stages, and arbitrary waveform generators. All high-performance DACs have differential current outputs. Two THS3201s can be used as a differential drive amplifier in these applications as shown in Figure 62.

R<sub>PU</sub> on the DAC output is used to convert the output current to voltage. The 24.9-Ω resistor and 47-pF capacitor between each DAC output and the operational amplifier input is used to reduce the images generated at multiples of the sampling rate. The values shown form a pole a 136 MHz. R<sub>OUT</sub> sets the output impedance of each amplifier.

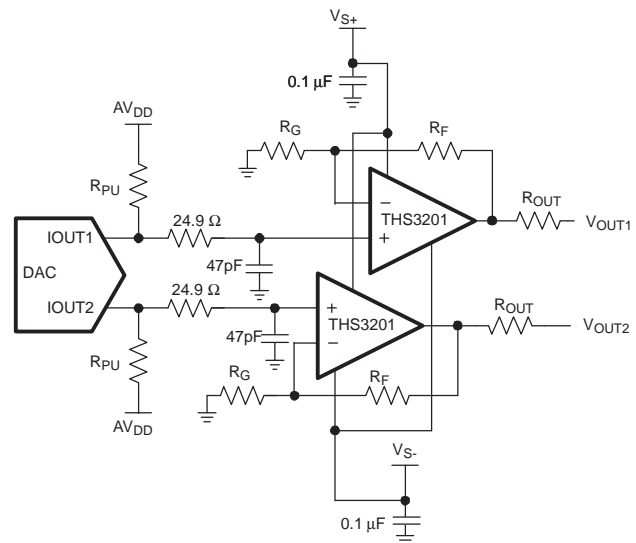


Figure 62. Differential DAC Driver Circuit

## Printed-Circuit Board Layout Techniques for Optimal Performance

Achieving optimum performance with high-frequency amplifier-like devices in the THS3201 requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include:

- Minimize parasitic capacitance to any power or ground plane for the negative input and output pins by voiding the area directly below these pins and connecting traces and the feedback path. Parasitic capacitance on the output and negative input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins and the feedback path. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance (<0.25 in) from the power-supply pins to high frequency 0.1- $\mu$ F and 100-pF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (6.8  $\mu$ F or more) tantalum decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board. The primary goal is to minimize the impedance seen in the differential-current return paths. For driving differential loads with the THS3201, adding a capacitor between the power-supply pins improves 2nd order harmonic distortion performance. This also minimizes the current loop formed by the differential drive.
- Careful selection and placement of external components preserve the high frequency performance of the THS3201. Resistors should be a low-reactance type. Surface-mount resistors work best and allow a tighter overall layout. Again, keep their leads and PC board trace length as short as possible. Never use wirebound-type resistors in a high-frequency application. Since the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Other network components, such as input termination resistors, should be placed close to the gain-setting resistors. Even with a low-parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values >2 k $\Omega$ , this parasitic capacitance can add a pole and/or a zero that can effect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations.
- Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (<4 pF) may not need an  $R_S$  since the THS3201 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an  $R_S$  are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for these techniques).
- A 50- $\Omega$  environment is not necessary onboard and, in fact, a higher-impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS3201 is used, as well as a terminating shunt resistor at the input of the destination device.
- Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.
- Socketing a high-speed part such as the THS3201 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost

impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering THS3201 parts directly onto the board.

### PowerPAD Design Considerations

The THS3201 is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 63(a) and Figure 63(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 63(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

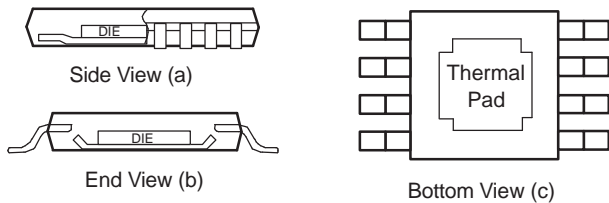


Figure 63. Views of Thermally Enhanced Package

Although there are many ways to properly heat sink the PowerPAD package, the following steps define the recommended approach.

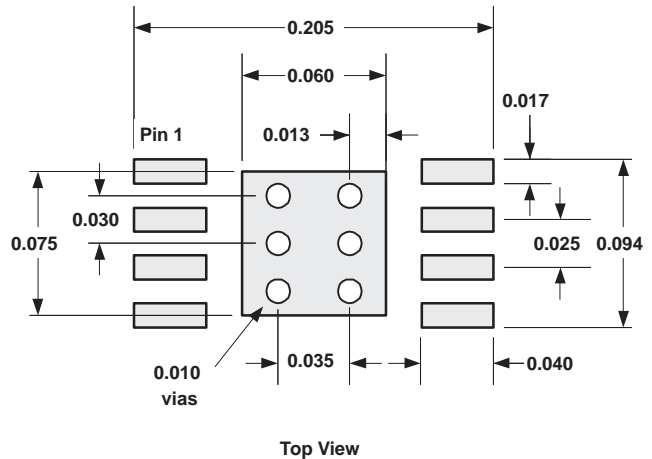


Figure 64. DGN PowerPAD PCB Etch and Via Pattern

### PowerPAD PCB Layout Considerations

1. Prepare the PCB with a top-side etch pattern as shown in Figure 64. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 10 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal-pad area. This helps dissipate the heat generated by the THS3201 IC. These additional vias may be larger than the 10-mil diameter vias directly under the thermal-pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS3201 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal-pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal-pad area. This prevents solder from

being pulled away from the thermal-pad area during the reflow process.

7. Apply solder paste to the exposed thermal-pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

### Power Dissipation and Thermal Considerations

To maintain maximum output capabilities, the THS3201 does not incorporate automatic thermal shutoff protection. The designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of 150°C is exceeded. For the best performance, design for a maximum junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade.

The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

where:

$P_{Dmax}$  is the maximum power dissipation in the amplifier (W).

$T_{max}$  is the absolute maximum junction temperature (°C).

$T_A$  is the ambient temperature (°C).

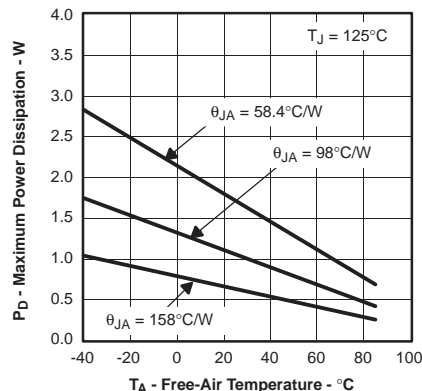
$\theta_{JA} = \theta_{JC} + \theta_{CA}$

$\theta_{JC}$  is the thermal coefficient from the silicon junctions to the case (°C/W).

$\theta_{CA}$  is the thermal coefficient from the case to ambient air (°C/W).

For systems where heat dissipation is more critical, the THS3201 is offered in an 8-pin MSOP with PowerPAD and the THS3201 is available in the SOIC-8 PowerPAD package offering even better thermal performance. The thermal coefficient for the PowerPAD packages are substantially improved over the traditional SOIC. Maximum power dissipation levels are listed in the Dissipation Ratings table.. The data for the PowerPAD packages assume a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application report SLMA002. Figure 65 also shows

the effect of not soldering the PowerPAD to a PCB. The thermal impedance increases substantially, which may cause serious heat and performance issues. Be sure to always solder the PowerPAD to the PCB for optimum performance.



Results are With No Air Flow and PCB Size = 3"x3"

$\theta_{JA} = 58.4^{\circ}\text{C/W}$  for 8-Pin MSOP w/PowerPad (DGN)

$\theta_{JA} = 98^{\circ}\text{C/W}$  for 8-Pin SOIC High Test PCB (D)

$\theta_{JA} = 158^{\circ}\text{C/W}$  for 8-Pin MSOP w/PowerPad w/o Solder

**Figure 65. Maximum Power Dissipation vs Ambient Temperature**

When determining whether or not the device satisfies the maximum power-dissipation requirement, it is important to not only consider quiescent power dissipation, but also dynamic power dissipation. Often times, this is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

### Design Tools

#### Evaluation Fixture, Spice Models, and Applications Support

TI is committed to providing its customers with the highest quality of applications support. To support this goal, an evaluation board has been developed for the THS3201 operational amplifier. The board is easy to use, allowing for straightforward evaluation of the device. The evaluation board can be ordered through the TI web site, [www.ti.com](http://www.ti.com), or through your local TI sales representative. The schematic diagram, board layers, and bill of materials of the evaluation boards are in [Figure 66](#) through [Figure 70](#).



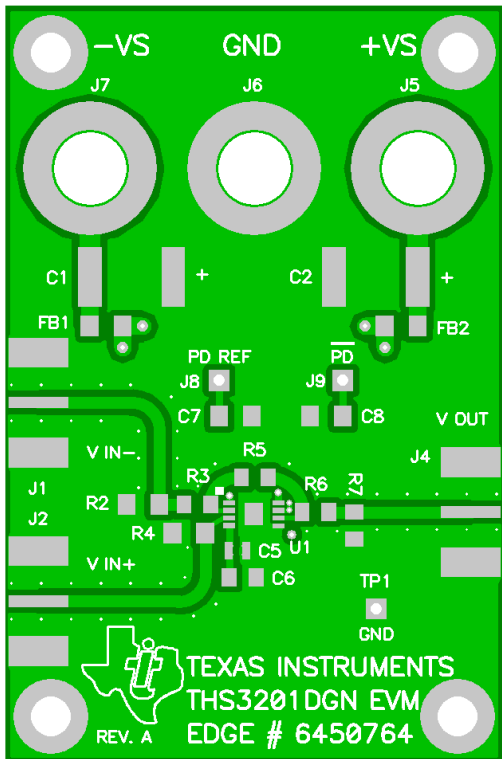


Figure 67. THS3201 EVM Board Layout (Top Layer)

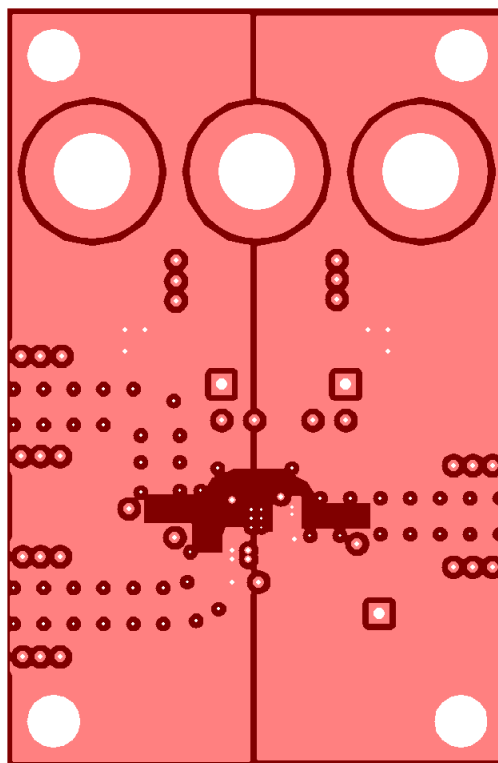


Figure 69. THS3201 EVM Board Layout (Third Layer, Power)

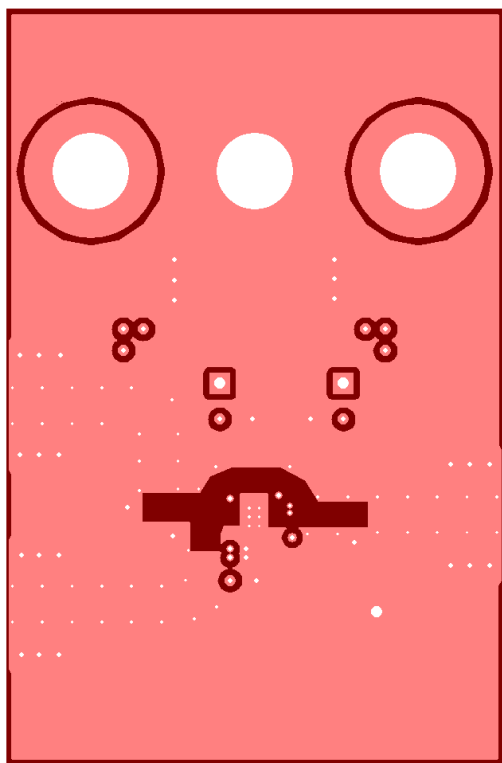


Figure 68. THS3201 EVM Board Layout (Second Layer, Ground)

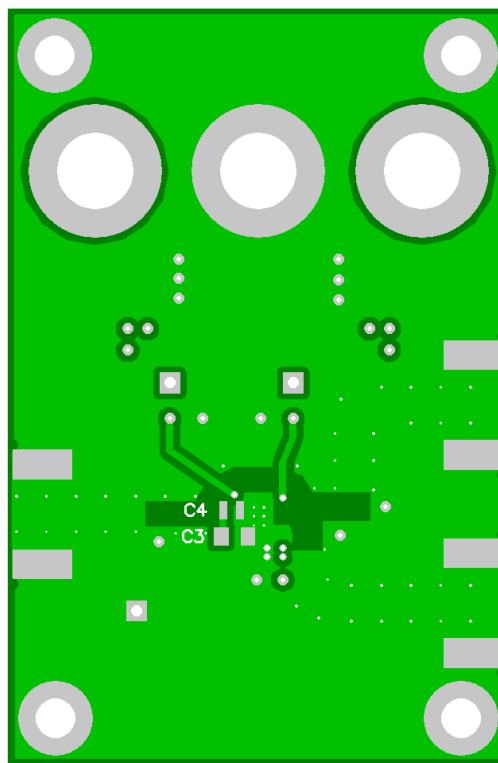


Figure 70. THS3201 EVM Board Layout (Bottom Layer)

**Table 2. Bill of Materials<sup>(1)</sup>**

THS3201DGN EVM					
ITEM	DESCRIPTION	SMD SIZE	REF DES	PCB QUANTITY	MANUFACTURER PART NUMBER
1	Bead, ferrite, 3 A, 80 $\Omega$	1206	FB1, FB2	2	(Steward) HI1206N800R-00
2	Cap, 22 F, tanatalum, 25 V, 10%	D	C1, C2	2	(AVX) TAJD226K025R
3	Cap, 100 pF, ceramic, 5%, 150 V	AQ12	C4, C5	2	(AVX) AQ12EM101JAJME
4	Cap, 0.1 F, ceramic, X7R, 50 V	0805	C3, C6	2	(AVX) 08055C104KAT2A
6	Open	0805	R7	1	
7	Resistor, 49.9 $\Omega$ , 1/8 W, 1%	0805	R6	1	(Phycomp) 9C08052A49R9FKHFT
9	Resistor, 768 $\Omega$ , 1/8 W, 1%	0805	R3, R5	2	(Phycomp) 9C08052A7680FKHFT
10	Open	1206	C7, C8	2	
11	Resistor, 0 $\Omega$ , 1/4 W, 1%	1206	R2	1	(KOA) RK73Z2BLTD
12	Resistor, 49.9 $\Omega$ , 1/4 W, 1%	1206	R4	1	(Phycomp) 9C12063A49R9FKRFT
13	Test point, black		TP1	1	(Keystone) 5001
14	Open		J8, J9	2	
15	Jack, Banana Receptance, 0.25" dia. hole		J5, J6, J7	3	(HH Smith) 101
16	Connector, edge, SMA PCB jack		J1, J2, J4	3	(Johnson) 142-0701-801
17	Standoff, 4-40 hex, 0.625" length			4	(Keystone) 1804
18	Screw, Phillips, 4-40, .250"			4	SHR-0440-016-SN
19	IC, THS3201		U1	1	(Texas Instruments) THS3201DGN
20	Board, printed circuit			1	(Texas Instruments) Edge # 6447972 Rev.A

(1) The components shown in the BOM were used in test by TI. Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and  $R_F$ -amplifier circuits, where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS4500 family of devices is available through the TI web site ([www.ti.com](http://www.ti.com)). The Product Information Center (PIC) is available for design assistance and detailed product information. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

### Additional Reference Material

- PowerPAD™ Made Easy, application brief (SLMA004)
- PowerPAD™ Thermally-Enhanced Package, technical brief (SLMA002)
- Voltage Feedback vs Current Feedback Amplifiers (SLVA051)
- Current Feedback Analysis and Compensation (SLOA021)
- Current Feedback Amplifiers: Review, Stability, and Application (SBOA081)
- Effect of Parasitic Capacitance in Op Amp Circuits (SLOA013)

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS3201MDGNREP	NRND	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	BLM	
V62/05609-01YE	NRND	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	BLM	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF THS3201-EP :**

- Catalog: [THS3201](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3201MDGNREP	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

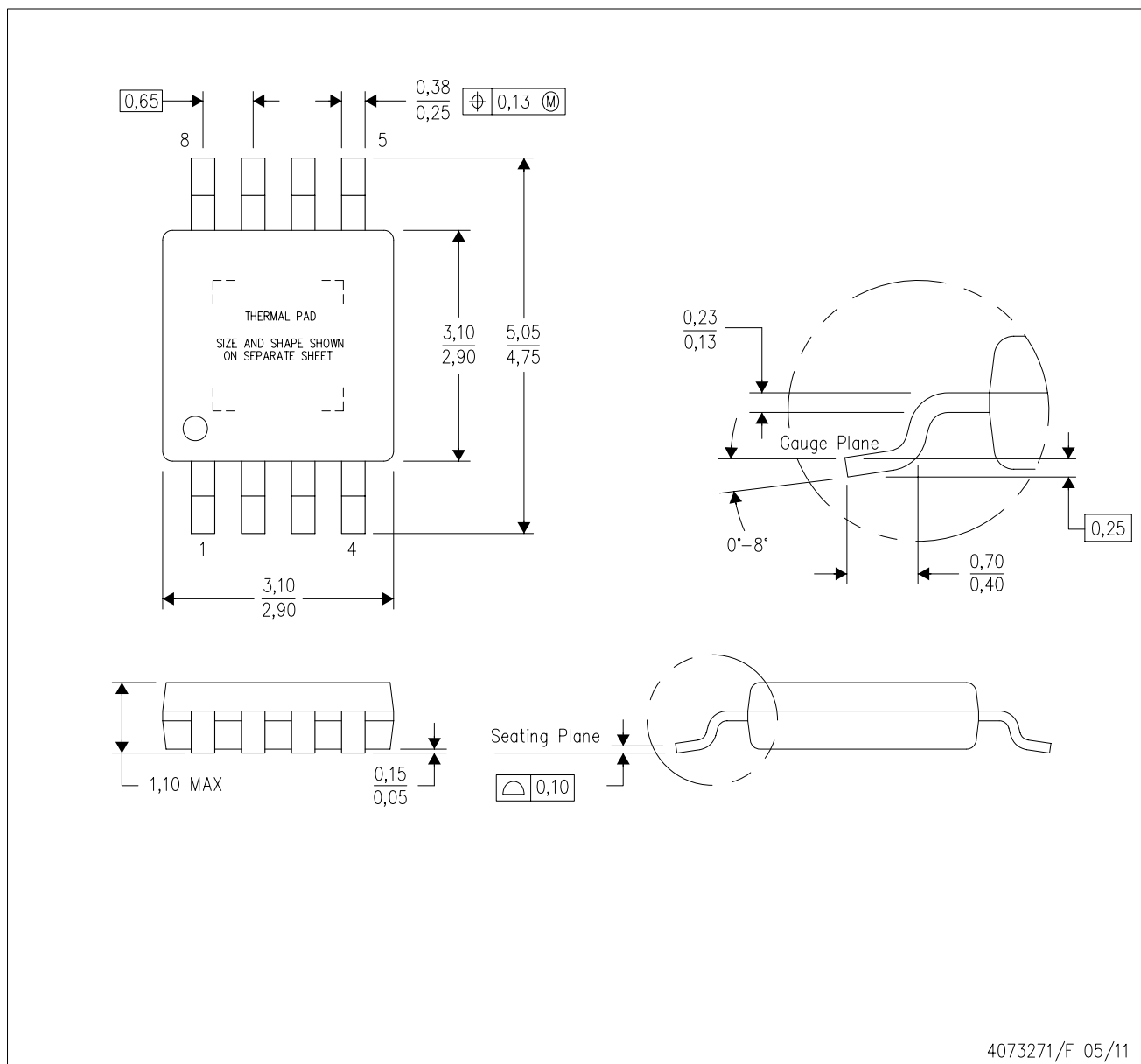


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3201MDGNREP	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

DGN (S-PDSO-G8)

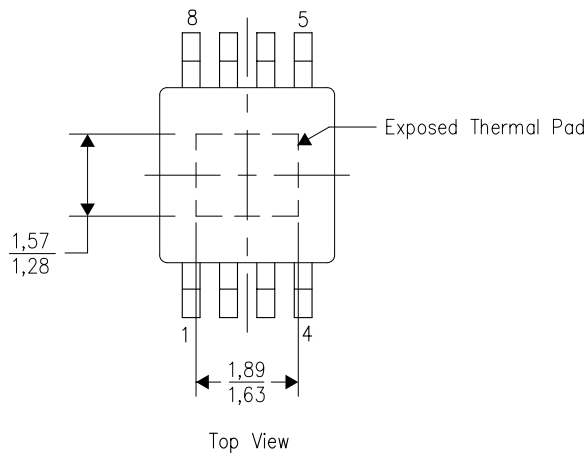
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

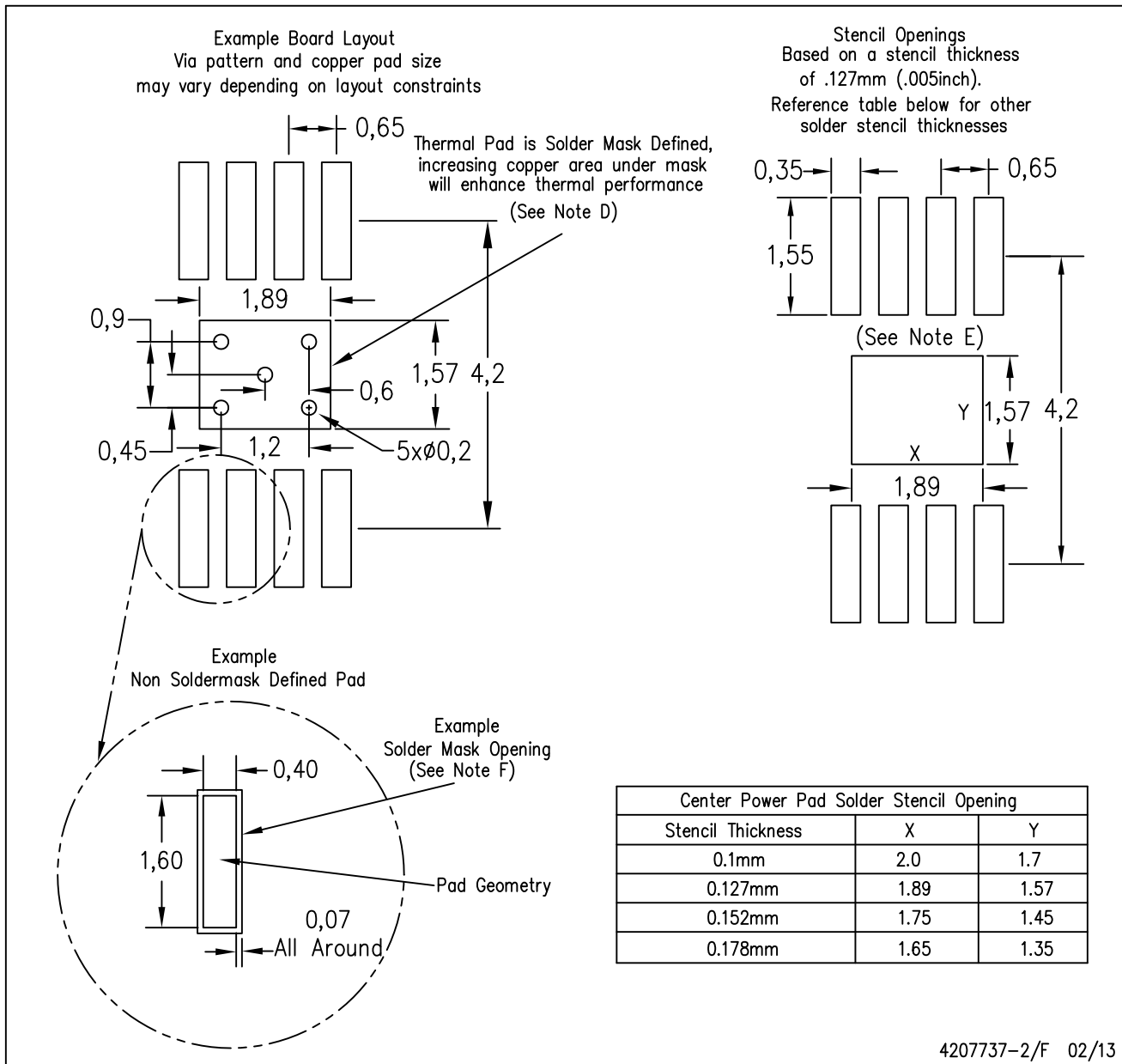


Exposed Thermal Pad Dimensions

4206323-2/1 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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