THE DATASHEET OF

TPS80010ARSMR

TPS80010 PMU for Alkaline Battery-Powered Applications

1 Features

- 1.8-V Buck DC-DC Converter
- 3.1-V Boost DC-DC Converter with 3-V Post-Regulation LDO
- Over 91% Conversion Efficiency
- Current-Limited Start-Up for Both DC-DC Converters
- Load Switch With Current-Limited Turnon
- Battery-Level Monitor Switch
- 32-Pin, 4-mm × 4-mm × 1-mm VQFN Package
- ESD Performance Tested per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 500-V Charged-Device Model (C101)

2 Applications

- Wireless Mice
- Wireless Keyboards
- Game Controllers

3 Description

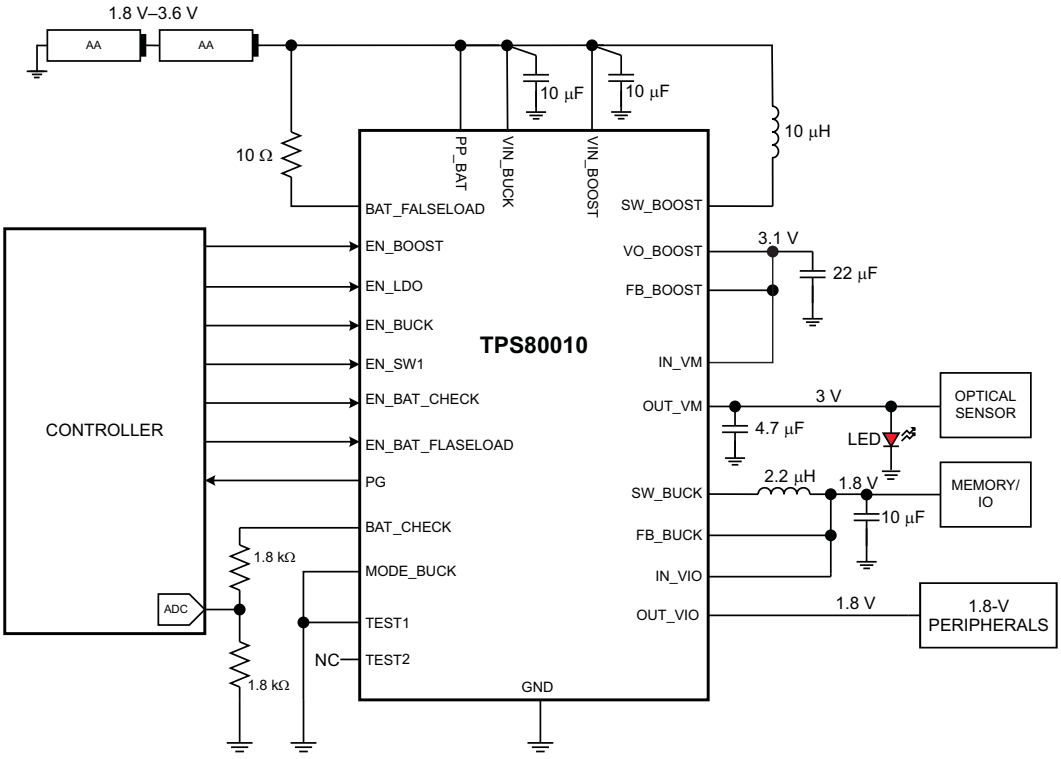
The TPS80010 device provides an integrated power-management solution for 2-cell alkaline battery applications such as wireless mice, keyboards, and video game controllers. The VBUCK 1.8-V output is powered by a buck converter with a load capacity of 100 mA. A Power Good (PG) signal is generated when VBUCK is greater than 90% of its target output voltage. Integrated in the TPS80010 is an 80-mΩ load switch that can be connected to the VBUCK output, allowing more system design flexibility when connecting to multiple loads. The 3.1-V VBOOST output is powered by a boost converter. The VBOOST output voltage is post-regulated by the integrated 3-V LDO. This post-regulation provides a low-noise supply level through the specified battery range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS80010	VQFN (32)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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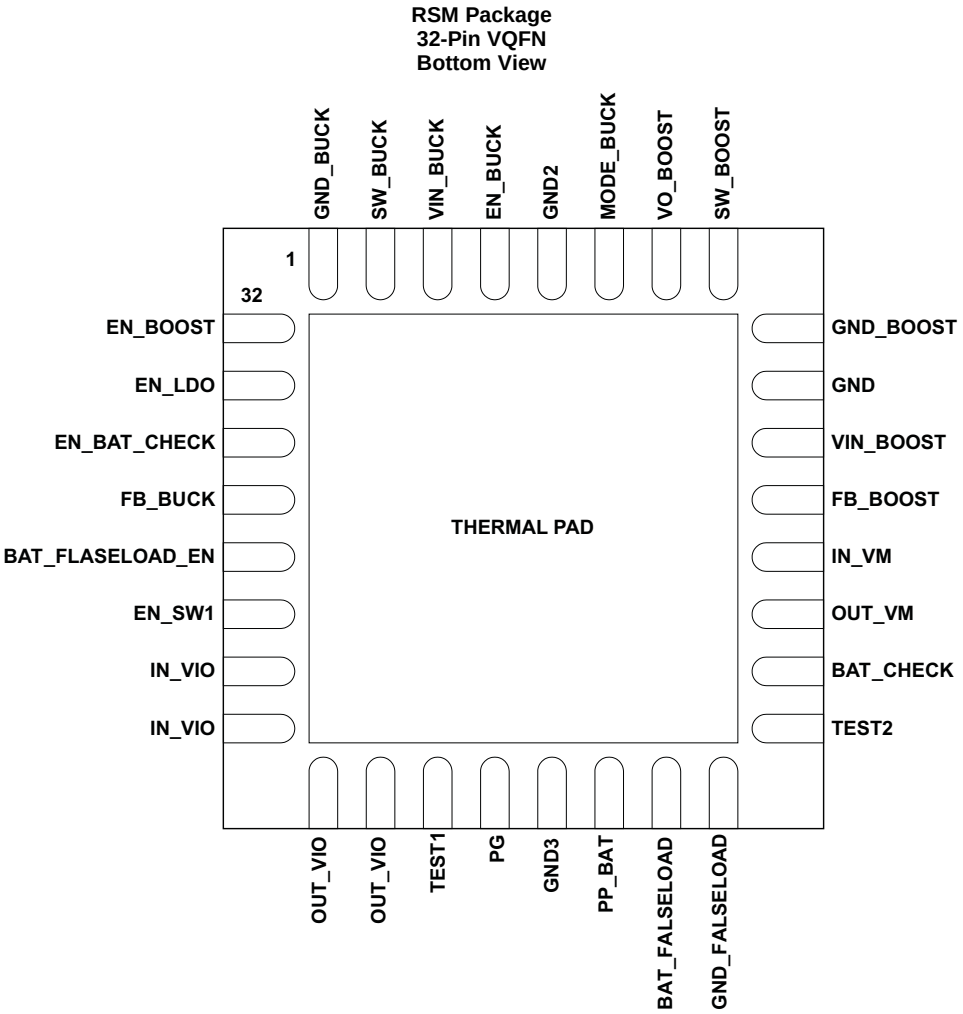
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2010) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed values in *Thermal Information* table	5

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BAT_CHECK	15	O	Battery monitor switch output. Connect to ADC for battery-level check.
BAT_FALSELOAD	18	I	Battery monitor input for false-load check
BAT_FALSELOAD_EN	28	I	Battery false load switch enable
EN_BAT_CHECK	30	I	Battery-check path enable
EN_BOOST	32	I	Boost converter enable
EN_BUCK	4	I	Buck converter enable
EN_LDO	31	I	Boost post-regulation LDO enable
EN_SW1	27	I	Buck-load switch (SW1) enable
FB_BOOST	12	I	Boost-converter feedback input
FB_BUCK	29	I	Buck converter feedback input
GND	10	–	Ground
GND2	5	–	Device ground
GND3	20	–	Device ground
GND_BOOST	9	–	Boost converter ground
GND_BUCK	1	–	Buck converter ground

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
GND_FALSELOAD	17	O	False load ground
IN_VIO	25, 26	–	Internal I/O power supply. Load switch 1 input. Connect externally to buck output
IN_VM	13	I	Boost post-regulation LDO input. Connect externally to VO_BOOST.
MODE_BUCK	6	I	Buck converter mode control. High for PWM, low for PFM.
OUT_VIO	23, 24	O	Load switch 1 output
OUT_VM	14	O	Boost post-regulation LDO output
PG	21	O	Buck Power Good indication output. High when V_{BUCK} > 1.7 V.
PP_BAT	19	I	Battery input for level check
SW_BOOST	8	I/O	Boost converter switching node. Inductor connection.
SW_BUCK	2	O	Buck converter switching output. Inductor connection.
TEST1	22	I/O	Test pin1 (tie to GND)
TEST2	16	O	Test pin 2 (do not connect)
VIN_BOOST	11	–	Boost-converter power supply
VIN_BUCK	3	–	Buck converter power supply
VO_BOOST	7	O	Boost converter regulated output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage (all pins)	–0.3	3.6	V
V_O	Output voltage (all pins)	–0.3	3.6	V
T_J	Junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_A = 0°C to 85°C; typical values are at T_A = 25°C

		MIN	NOM	MAX	UNIT
V_{BAT}	Input voltage, VIN BOOST, VIN_BUCK, PP_BAT pins	1.95		3.6	V
V_{IO} (IN_VIO)	Digital I/O operating voltage		1.8	V_{BAT}	V
T_A	Ambient temperature	0	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS80010 RSM (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 0°C to 85°C; typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Quiescent current	V_{BAT} = 3 V, all modules enabled		51		µA
I_{OFF}	Off current	V_{BAT} = 3 V		1		µA
DIGITAL I/O						
$R_{PULLDOWN}$	Internal pulldown resistor	EN_BOOST, EN_LDO, EN_SW1, EN_BAT_CHECK, EN_BAT_FALSELOAD	157	275	383	kΩ
V_{IH}	Input logic-high voltage	EN_BOOST, EN_LDO, EN_SW1, EN_BAT_CHECK, EN_BAT_FALSELOAD	0.7 × V_{IO}			V
		EN_BUCK, BUCK_MODE	0.7 × V_{BAT}			
V_{IL}	Input logic-low voltage	EN_BOOST, EN_LDO, EN_SW1, EN_BAT_CHECK, EN_BAT_FALSELOAD			0.3 × V_{IO}	V
		EN_BUCK, BUCK_MODE			0.7 × V_{BAT}	
V_{OH}	Output logic-high voltage	PG	V_{IO} – 0.2			V
V_{OL}	Output logic-low voltage	PG			0.2	V
I_{L_DIG}	Logic-output load current				1	mA
BUCK CONVERTER						
V_{IN}	Input voltage at VIN_BUCK		1.95		3.6	V
I_O	Output current				100	mA
V_{FB}	Feedback voltage (output accuracy)	PWM, I_O = 0 mA to 100 mA, V_{IN} ≥ 1.85 V to 3.6 V, V_{BUCK} = 1.8 V	–1.5%		1.5%	
		PFM		1		
V_{BUCK}	Buck output voltage			1.8		V
I_{SW}	Switch current limit		0.56	0.7	0.84	A
I_{RUSH}	Inrush current	V_{IN} = 2 V		150		mA
	Line regulation	PWM, I_O = 100 mA		0.9%		
		PFM, I_O = 100 mA		0.9%		
	Load regulation	PWM, V_{IN} = 2.4 V, I_O = 0 mA to 100 mA		–0.5%		
		PFM, V_{IN} = 2.4 V, I_O = 0 mA to 100 mA		0.5%		
	Efficiency	PFM , I_O = 100 mA, V_{IN} = 2.4 V, V_{BUCK} = 1.8 V		92%		
		PWM, I_O = 100 mA, V_{IN} = 2.4 V, V_{BUCK} = 1.8 V		90%		
I_Q	Quiescent current	PFM, I_O = 0 mA, no switching		21		µA
		PFM, I_O = 0 mA, switching		25		
		PWM, I_O = 0 mA		5		mA
	Shutdown current			0.005	0.15	µA
	Leakage current into SW_BUCK			0.01	1	µA
R_{REC}	Rectifier on-resistance	V_{GS} = 3.6 V		185	380	mΩ
R_{MAIN}	Main SW on-resistance	V_{GS} = 3.6 V		240	480	mΩ
ΔV_{LN}	Line transient output variation	PFM, I_O = 50 mA, V_{IN} = 2 V → 3.6 V, Δt = 25 µs		10	20	mV
ΔV_{LD}	Load transient output variation	PFM, V_{IN} = 2.4 V, V_{BUCK} = 1.8 V, I_O = 1 mA → 100 mA, Δt = 1 µs		30	40	mV
V_{RIP}	Output ripple	PWM, I_O = 100 mA, V_{IN} = 2.4 V		1	10	mVpp
		PFM, I_O = 10 mA, V_{IN} = 3.6 V		10	20	
f_{SW}	Switching frequency		2	2.25	2.5	MHz
UVLO	Undervoltage lockout threshold			1.7		V
C_L	Load capacitance			10		µF
L	Inductor			2.2		µH

Electrical Characteristics (continued)

T_A = 0°C to 85°C; typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOAD SWITCH						
R_{ON}	Switch on-resistance	V_{GS} = 1.8 V		80	120	mΩ
	Maximum load current				360	mA
	Turnon inrush current				100	mA
I_{OFF}	Off-state current	Switch turned off, I_O = 0 mA			1	µA
POWER GOOD RESET						
V_{THRESH}	Power good threshold voltage		1.68	1.7	1.72	V
V_{HYS}	Power good hysteresis			10	15	mV
BOOST CONVERTER						
V_{IN}	Input voltage at VIN_BOOST	Boost mode	1.8		3.1	V
		V_{IN} > V_{BOOST} mode, V_{BOOST} = V_{IN}	3.1		3.6	
V_{BOOST}	Output voltage	T_A = 0°C–50°C, V_{IN} = 1.8 V to 3.1 V, I_O = 0 mA to 50 mA	3	3.1	3.2	V
I_O	Output current	V_{IN} = 1.8 V to 3.6 V			50	mA
I_{SW}	Switch current limit		200	350	475	mA
I_{RUSH}	Inrush current	V_{IN} = 2 V		150		mA
R_{REC}	Rectifier on-resistance	V_{BOOST} = 3.1 V		1		Ω
R_{MAIN}	Main SW on-resistance			1		Ω
	Line regulation	V_{IN} = 2 V to 3 V, I_O = 50 mA		0.5%		
	Load regulation	V_{IN} = 2 V, I_O = 0–50 mA		0.5%		
	Boost efficiency	V_{IN} = 2.4 V, I_O = 5 mA		91%		
f_{SW}	Oscillator frequency	V_{IN} = 2.4 V, I_O = 50 mA		91		kHz
				625		
I_Q	Quiescent current	From V_{IN} supply, I_O = 0 mA, V_{IN} = 1.8 V, V_{BOOST} = 3.1 V		1	2.5	µA
		From V_{BOOST}, I_O = 0 mA, V_{IN} = 1.8 V, V_{BOOST} = 3.1 V		4	6.5	
	Shutdown current			0.1	1	
	Leakage current into SW_BOOST			0.1	1	
V_{UVLO}	V_{IN} decreasing			0.5	0.7	V
ΔV_{LN}	Line transient output variation	I_O = 10 mA, V_{IN} = 1.8 V → V_{BOOST}, ΔT = 25 µs		10		mV
ΔV_{LD}	Load transient output variation	V_{IN} = 2.4 V, V_{BOOST} = 3.1 V, I_O = 1 mA → 50 mA, Δt = 1 µs		5	10	mV
V_{RIP}	Output ripple	V_{IN} = 1.8 V, I_O = 50 mA		4	10	mVpp
I_{OFF}	Off-mode current			0.1	1	µA
C_L	Load capacitance		6	10	22	µF
L	Inductance			10		µH
POST REGULATION LDO						
V_{IN}	Input voltage at IN_VM		3.1		3.6	V
V_{LDO}	Output voltage	10 µA ≤ I_O ≤ I_{OMAX}	2.91	3	3.09	V
I_O	Output current	Normal mode			50	mA
I_{LIMIT}	Current limit	V_{LDO} > 1 V	300	400	500	mA
I_{SHORT}	Short circuit current	Output shorted to ground	30	60	150	mA
VREG	Line regulation	dV_{LDO}/dV_{IN} at I_O = Max			0.2%	
LREG	Load regulation	V_{LDO} (I_{OMIN}) – V_{LDO}(I_{OMAX})			40	mV
ΔV_{LN}	Load transient response	I_O = 20 mA/µs, V_{IN} = 3.1 V		50	100	mV
I_Q	Quiescent current	I_O = 0 mA		16	17.6	µA

Electrical Characteristics (continued)

T_A = 0°C to 85°C; typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power-supply ripple rejection	f = 120 Hz to 1 kHz at $I_O = I_{OMAX}/2$, V_{IN} = 3.1 V	40			dB
V_{RIP_NORM}	Output ripple	V_{BAT} < 3.1 V, I_O = 50 mA, $V_{IN} = V_{BOOST}$		0.1	1	mVpp
V_{RIP_HIBAT}	Output ripple	V_{BAT} > 3.1 V, I_O = 50 mA, $V_{IN} = V_{BOOST}$		4	10	mVpp
	Boost plus LDO efficiency	V_{BAT} = 2.4 V, I_O = 5 mA, $V_{IN} = V_{BOOST}$		87%		
		V_{BAT} = 2.4 V, I_O = 50 mA, $V_{IN} = V_{BOOST}$		88%		
C_L	Load capacitance	Ceramic capacitor, ESR = 10 mΩ to 150 mΩ	4.7	10	22	µF
BATTERY LOAD MONITOR						
V_{OP}	Operating voltage			1.8	3.6	V
V_{IN}	Input voltage at PP_BAT		1.8		3.6	V
V_{OUT}	Output voltage at BAT_CHECK				V_{IN}	V
I_{LOAD}	Load current				10	mA
R_{ON}	Switch on-resistance	V_{IN} = 1.8 V to 3.6 V		12	15	Ω
BATTERY LOAD SWITCH						
V_{OP}	Operating voltage			1.8	3.6	V
V_{IN}	Input voltage at BAT_FALSELOAD				3.6	V
I_{IN}	Input current			240	360	mA
R_{ON}	Switch on-resistance				500	mΩ

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
BUCK CONVERTER					
t_{START}	Start-up time			10	ms
LOAD SWITCH					
	Output rise time; 10%–90% of final V_O, C_L = 100 µF		2	4	ms
t_{ON}	Turnon time; C_L = 100 µF			6	ms
t_{OFF}	Turnoff time; C_L = 100 µF			10	ms
POWER GOOD RESET					
Δt_{PG}	Power good time-out delay	100	150	200	ms
BOOST CONVERTER					
t_{START}	Start-up time; from enable, V_{BOOST} = 10% → 90%		0.25	10	ms
POST REGULATION LDO					
t_{ON}	Turn-on time; I_O = 0 mA, V_{LDO} = 90%, C_L = 2.9 µF		130	500	µs
t_{OFF}	Turn-off time; I_O = 0 mA, V_{LDO} < 0.5 V, C_L = 2.9 µF		3.9	5	ms

6.7 Typical Characteristics

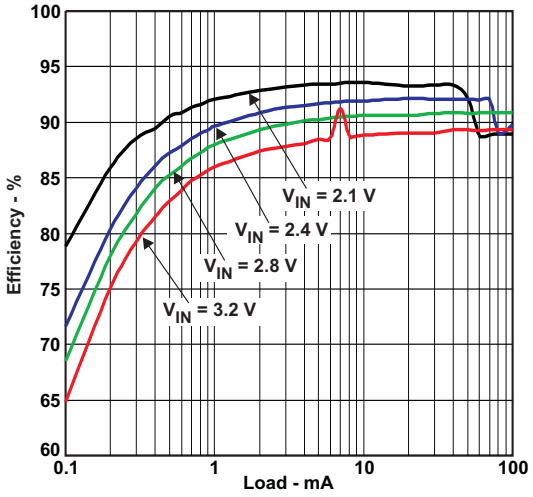


Figure 1. Buck Efficiency, MODE_BUCK = 0

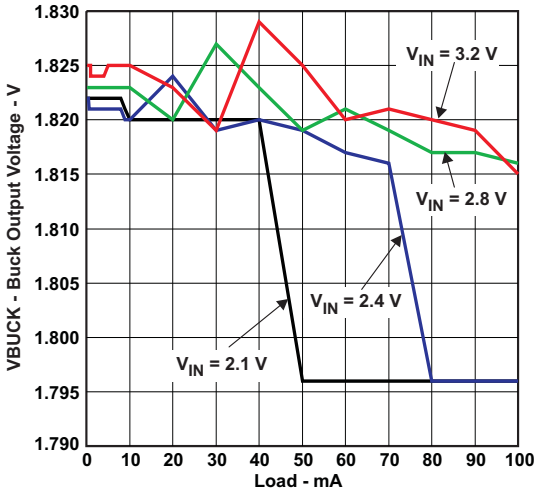


Figure 2. Buck Output Voltage vs Load, MODE_BUCK = 0

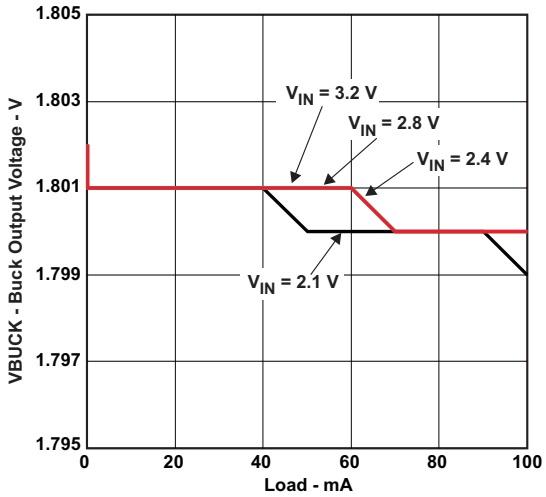


Figure 3. Buck Output Voltage vs Load, MODE_BUCK = 1

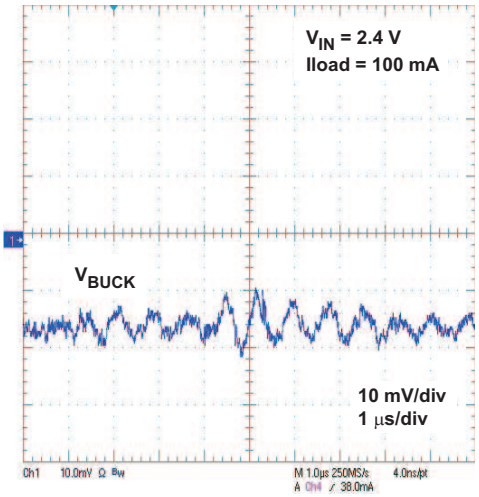


Figure 4. Buck Output-Voltage Ripple, PWM

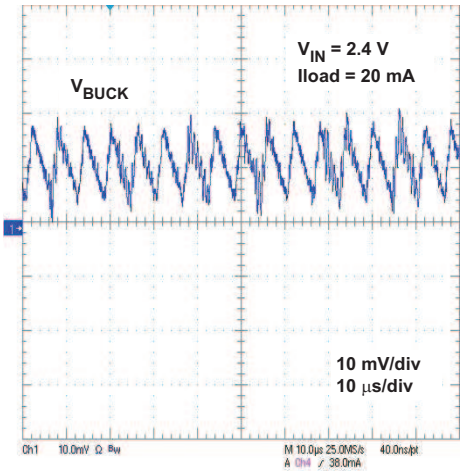


Figure 5. Buck Output-Voltage Ripple, PFM

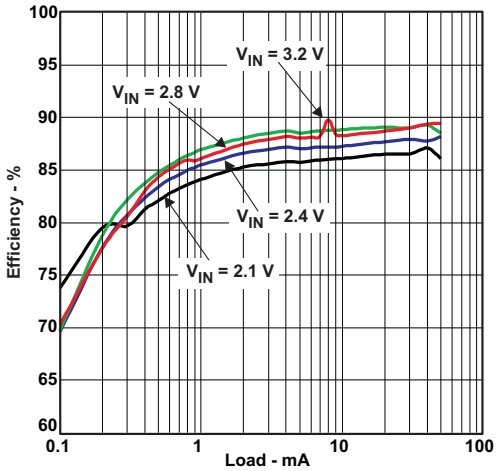


Figure 6. Boost With LDO Efficiency

Typical Characteristics (continued)

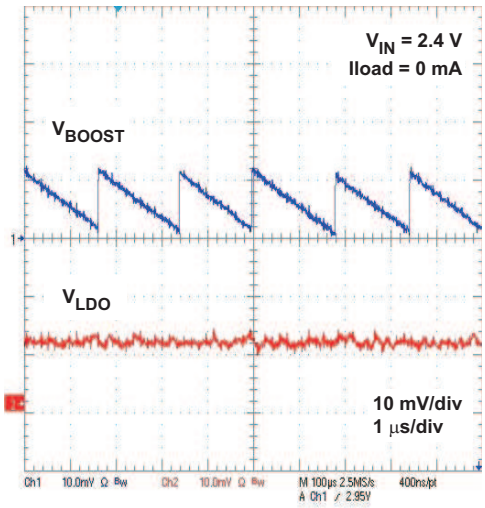


Figure 7. Boost Output Voltage Ripple

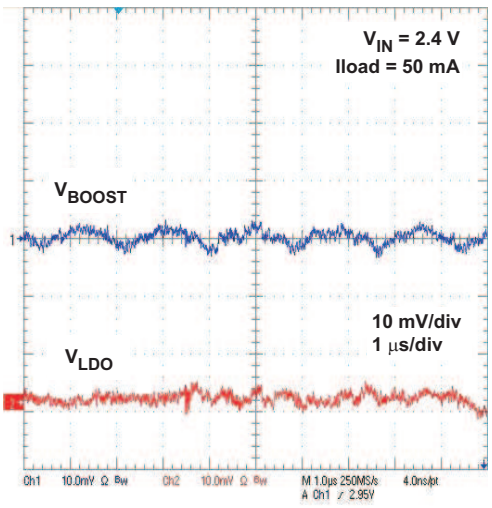


Figure 8. Boost Output Voltage Ripple

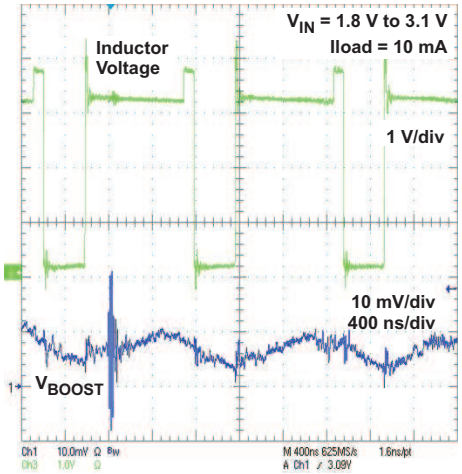


Figure 9. Boost Switching Waveform, Continuous-Current Mode

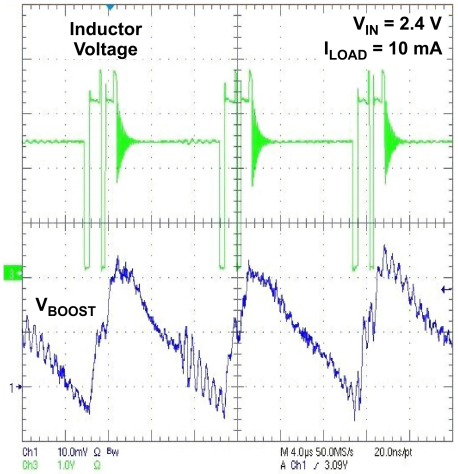


Figure 10. Boost Switching Waveform, Discontinuous-Current Mode

7 Detailed Description

7.1 Overview

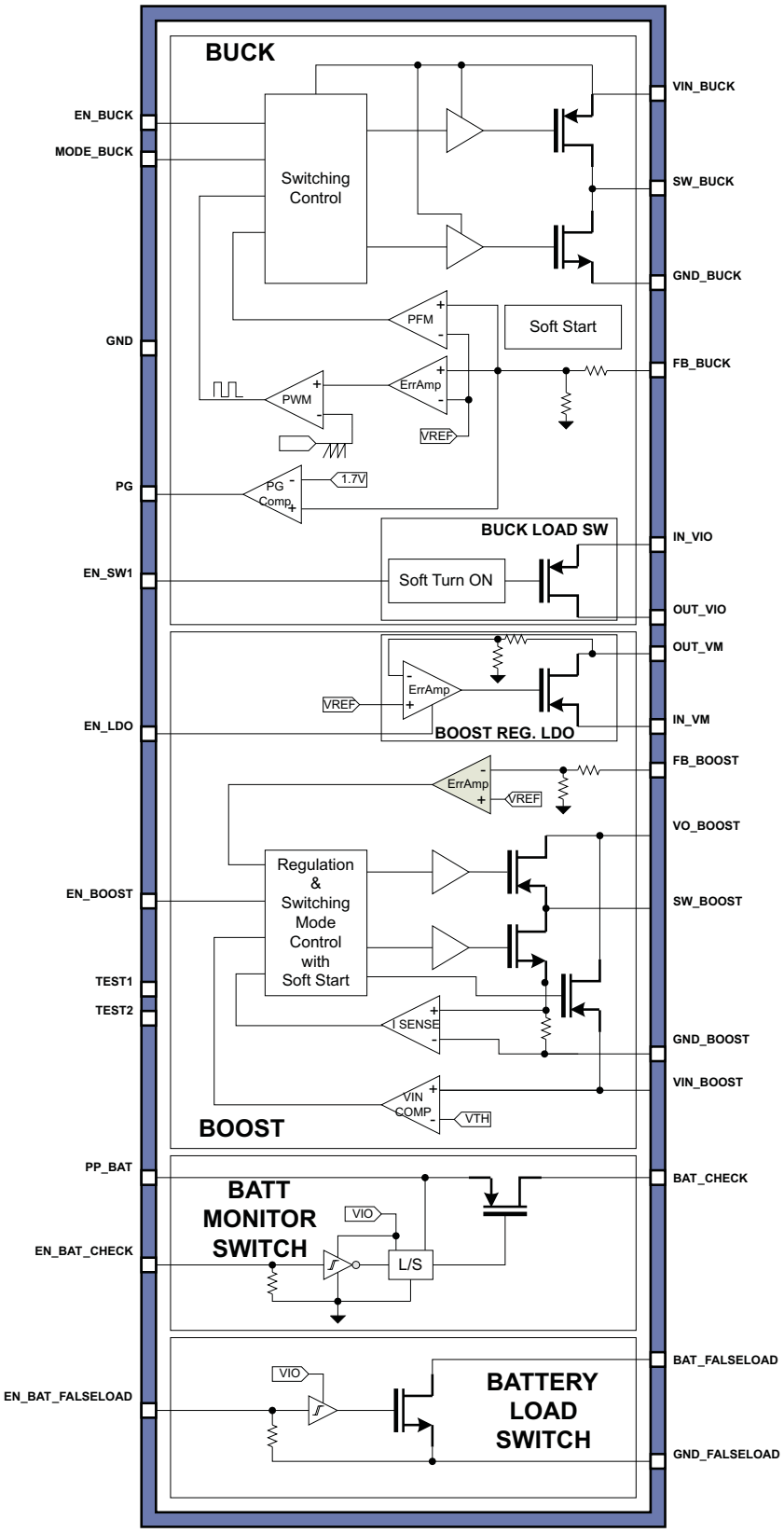
The TPS80010 provides a system level solution for 2-cell alkaline battery applications. Popular applications include handheld devices including wireless mice, keyboards, and video game controllers. The TPS80010 provides two DC-DC converters, a load switch, post-regulation LDO, and battery monitoring switch—each with their own enable pins to allow for maximum flexibility.

The buck converter operates at a fixed voltage, 1.8 V, and can provide up to 150 mA load. Automatic switching is implemented to maximize power efficiency. In moderate to heavy loads the converter operates in PWM mode; as load current decreases it switches to PFM mode. PWM can be forced regardless of load size by disabling this power save mode (PFM mode). The buck allows for several loads to be connected to its output, due to the power distributing load switch connected externally to the output of the buck.

The boost converter regulates at a fixed voltage of 3.1 V, and can provide up to 50 mA load current. It contains a discontinuous current mode to maintain efficiency at low load currents. The boost provides a low noise supply at low input voltages due to a post regulation LDO.

The battery monitoring switch is used to check battery lifetime. Using a false load implementation and the battery voltage it can determine the battery impedance and therefore health.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable

The TPS80010 includes two DC-DC converters, a load switch, post-regulation LDO, and battery monitoring switch. Each of these circuits has a dedicated enable pin with an internal pulldown resistor, $R_{PULLDOWN}$, that can be driven by standard logic or by an open-drain driver. The EN_BUCK pin not only enables the buck converter, but also serves as the master enable for the device. No other circuitry in the TPS80010 can operate without EN_BUCK set high.

7.3.2 Buck DC-DC Converter and Load Switch

The synchronous step-down (buck) converter in the TPS80010 provides a fixed 1.8-V output with a load capacity of 150 mA. This converter operates with a fixed switching frequency of 2.25 MHz during pulse-width-modulation (PWM) operation at moderate to heavy loads. As the load current decreases, the converter automatically switches to a power-save mode and operates in pulse-frequency-modulation (PFM) mode to maximize power efficiency. During PFM operation, the converter positions the output at a voltage about 1% greater than the nominal output voltage. This feature minimizes the output voltage drops during sudden load transients. The power-save mode can be disabled by setting the MODE_BUCK pin high.

The buck converter has internal soft-start circuitry that limits the inrush current during startup to 150 mA, allowing a slow and controlled output-voltage ramp. Once the output voltage reaches 1.7 V, the output monitoring circuitry generates a Power Good (PG) output signal.

The TPS80010 also includes a load switch that is to be connected externally to the buck output voltage. This switch provides flexibility in the design and power distribution of the end application by allowing several loads (such as memory, I/O, Bluetooth, and so forth) to be connected to the same supply while being able to power down or disconnect some of these loads selectively when the end application goes to a low-power mode of operation. This switch has a controlled turnon to limit the inrush current caused by the load, and hence the load transient to the buck converter.

7.3.3 Boost DC-DC Converter and Post-Regulation LDO

The TPS80010 includes a synchronous step-up (boost) converter that provides a 3.1-V fixed output at 50-mA load current. The boost converter is controlled by a hysteretic current-mode controller. This controller regulates the output voltage by keeping the inductor ripple current constant and adjusting the offset of this inductor current depending on the output load. If the required average input current is lower than the average inductor current defined by this constant ripple, the converter goes into discontinuous-current mode (DCM) to keep the efficiency high at low-load conditions. The boost also has a soft-start circuit that limits the inrush current to 150 mA.

To provide a clean, low-noise supply when V_{BAT} > 3.1 V, the output of the boost is post-regulated by a 3-V LDO. This post-regulation allows the TPS80010 to provide a solid 3-V supply rail to the end application across the full input or battery-voltage range while minimizing the number of external components. To minimize power loss through the power path, the LDO allows for 100-mV input-voltage headroom at 50-mA load.

7.3.4 Battery Monitoring Switch and False Load

The TPS80010 implements a battery-voltage monitor switch to briefly check battery lifetime. The integrated false-load switch connects a specified load to the battery. When this *false* load is applied, the battery monitor switch is turned on, gating the sensed battery voltage to the ADC in the system. Based on this measurement, the system can determine the battery impedance and, therefore, battery health.

7.4 Device Functional Modes

The step-down converter has two modes of operations to maximize efficiency: Pulse frequency modulation (PFM) and pulse width modulation (PWM).

PFM mode is for:

- Light loads
- Automatic transition from this mode to PWM mode automatically when MODE_BUCK pin is pulled low
- Increasing output voltage setting by 1%
- Better accuracy

PWM mode is for:

- Moderate to heavy loads
- Small output ripple
- Pulling MODE_BUCK pin high to result in PWM mode over all load range

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS80010 is ideal for dual-cell alkaline battery-powered and noise-sensitive applications. The application controller has the ability to enable resources on the power management IC to allow for maximum flexibility. The device resources are often used to power memory, IO, and optical sensors. These devices are common in wireless keyboards and video game controllers.

8.2 Typical Application

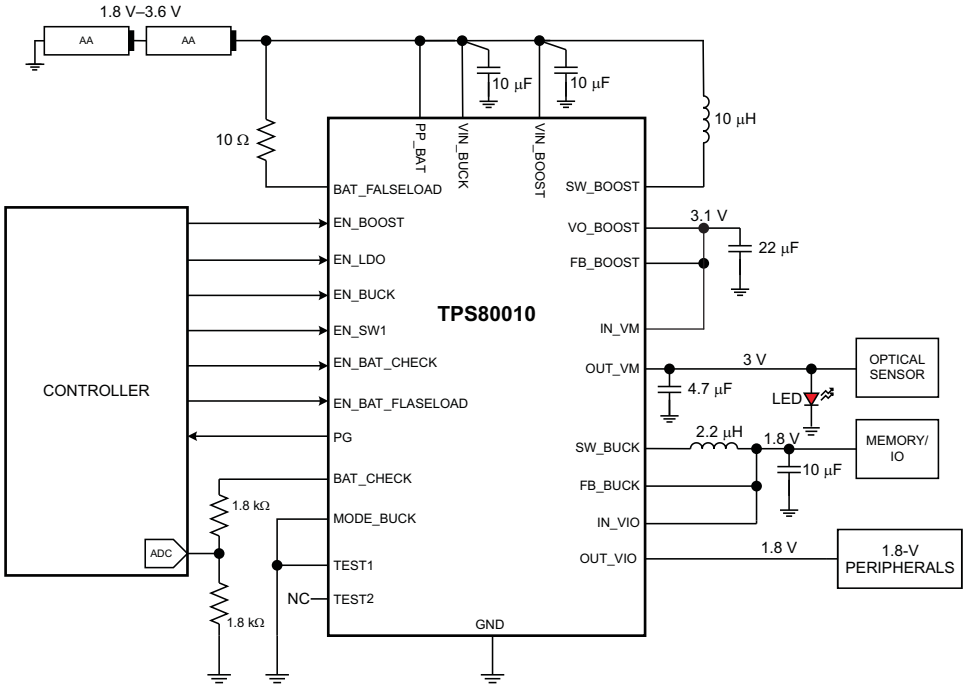


Figure 11. TPS80010 Typical Application Diagram

8.2.1 Design Requirements

The design requirements for TPS80010 are located in Table 1.

Table 1. TPS80010 Design Requirements

RESOURCE	VOLTAGE
Buck	1.8 V
Boost	3.1 V

8.2.2 Detailed Design Procedure

8.2.2.1 Buck Output Filter Design

The TPS80010 buck regulator is designed to operate with inductors in the range of 1.5 µH to 4.7 µH and with output capacitors in the range of 4.7 µF to 22 µF. The part is optimized for operation with a 2.2-µH inductor and 10-µF output capacitor.

Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter must not be less than 1-µH effective inductance and 3.5-µF effective capacitance.

8.2.2.2 Buck Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{BUCK}.

The inductor selection also has an impact on the output-voltage ripple in PFM mode. Higher inductor values lead to lower output-voltage ripple and higher PFM frequency; lower inductor values lead to a higher output-voltage ripple but lower PFM frequency.

Equation 1 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current, as calculated with Equation 2. This is recommended because during heavy load transients, the inductor current rises above the calculated value.

$$\Delta I_L = V_{BUCK} \times \frac{1 - \frac{V_{BUCK}}{V_{IN}}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{Omax} + \frac{\Delta I_L}{2}$$

where

- f = Switching frequency (2.25 MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current (2)

A more conservative approach is to select the inductor current rating just for the switch current limit, I_{LIMF}, of the converter.

Accepting larger values of ripple current allows the use of lower inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil have a strong impact on the efficiency of the DC-DC conversion and consist of both the losses in the DC resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

8.2.2.3 Buck Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS80010 buck regulator allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V- and Z5U-dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated with Equation 3.

$$I_{RMSCout} = V_{BUCK} \times \frac{1 - \frac{V_{BUCK}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (3)$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor in Equation 4.

$$\Delta V_{BUCK} = V_{BUCK} \times \frac{1 - \frac{V_{BUCK}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (4)$$

At light-load currents, the converter operates in power-save mode, and the output-voltage ripple depends on the output-capacitor and inductor values. Larger output-capacitor and inductor values minimize the voltage ripple in PFM mode and tighten DC output accuracy in PFM mode.

8.2.2.4 Buck Input Capacitor Selection

An input capacitor is required for best input voltage filtering and for minimizing the interference with other circuits caused by high input-voltage spikes. For most applications, a 4.7-µF to 10-µF ceramic capacitor is recommended. Because a ceramic capacitor loses up to 80% of its initial capacitance at 5 V, TI recommends that 10-µF input capacitors be used for input voltages > 4.5 V. The input capacitor can be increased without any limit for better input-voltage filtering. Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the VIN_BUCK pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 2. Recommended Component List for Buck Converter

COMPONENT	VALUE	PART	SUPPLIER	SIZE
Inductor	2.2 µH	LQM2HPN2R2MJ0L	Murata	2.5 mm × 2 mm × 1.2 mm (1008)
		LPS3015-222ML	Coilcraft	3 mm × 3 mm × 1.5 mm
Cacitor (IN)	10 µF	GRM188R60J106ME47D	Murata	0603
Capacitor (OUT)	10 µF	GRM188R60J106ME47D	Murata	0603

8.2.2.5 Boost Inductor Selection

To ensure proper operation of the TPS80010 boost DC-DC converter, a suitable inductor must be connected between pins VIN_BOOST and SW_BOOST. Inductor values of 4.7 µH show good performance over the whole input and output voltage range.

Choosing other inductance values affects the switching frequency f proportional to 1/L as shown in Equation 5.

$$L = \frac{1}{f \times 200\ mA} \times \frac{V_{IN} \times (V_{BOOST} - V_{IN})}{V_{BOOST}} \quad (5)$$

Choosing inductor values higher than 4.7 µH can improve efficiency due to reduced switching frequency and correspondingly reduced switching losses. Using inductor values less than 2.2 µH is not recommended.

Having selected an inductance value, the peak current for the inductor in steady-state operation can be calculated. Equation 6 gives the peak current estimate.

$$I_{L,MAX} = \left\{ \frac{V_{BOOST} \times I_{BOOST}}{0.8 \times V_{IN}} + 100\ mA \right\} \quad \text{continuous current operation}$$

$$I_{L,MAX} = 200\ mA \quad \text{discontinuous current operation} \quad (6)$$

$I_{L,MAX}$ is the required minimum inductor-current rating. The load-transient or overcurrent conditions may require an even higher current rating.

The condition in Equation 7 provides an easy way to determine whether the device is in continuous or discontinuous operation. As long as the condition is true, the device operates in continuous-current mode. If the condition becomes false, discontinuous-current operation is established.

$$\frac{V_{BOOST} \times I_O}{V_{IN}} > 0.8 \times 100\ mA \quad (7)$$

Due to the use of current hysteretic control in the TPS80010 boost, the series resistance of the inductor can impact the operation of the main switch. There is a simple calculation that can ensure proper operation of the TPS80010 boost converter. The relationship between the series resistance (R_{IN}), the input voltage (V_{IN}), and the switch current limit (I_{SW}) is shown in Equation 8.

$$R_{IN} < \frac{V_{IN}}{I_{SW}} \quad (8)$$

Examples include Equation 9 and Equation 10.

$$I_{SW} = 400\ mA,\ V_{IN} = 2.5\ V \quad (9)$$

In Equation 9, $R_{IN} < 2.5\ V / 400\ mA$; therefore, R_{IN} must be less than 6.25 Ω.

$$I_{SW} = 400\ mA,\ V_{IN} = 1.8\ V \quad (10)$$

In Equation 10, $R_{IN} < 1.8\ V / 400\ mA$; therefore, R_{IN} must be less than 4.5 Ω.

8.2.2.6 Boost Input Capacitor

The input capacitor must be at least 10 µF to improve transient behavior of the regulator and EMI behavior of the total power-supply circuit. The input capacitor must be a ceramic capacitor and be placed as close as possible to the VIN_BOOST and GND pins of the IC. These capacitors must be X7R or X5R ceramic capacitors.

8.2.2.7 Boost Output Capacitor

For the output capacitor C_{OUT}, TI recommends using small X7R or X5R ceramic capacitors placed as close as possible to the VO_BOOST and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, the use of a small ceramic capacitor with a capacitance value of around 4.7 µF in parallel with the larger one is recommended. This small capacitor must be placed as close as possible to the VO_BOOST and GND pins of the IC.

A minimum *effective* capacitance value of 6 µF must be used; 10 µF is recommended. If the inductor value exceeds 4.7 µH, the value of the effective output capacitance value must be half the inductance value or higher for stability reasons; see Equation 11.

$$C_{OUT} \geq \frac{L}{2} \times \frac{\mu F}{\mu H} \quad (11)$$

NOTE

When choosing the output capacitor, be aware of the effects of bias voltage, temperature, and tolerance on the effective capacitance of the component. A capacitor in a 0603 package size suffers more capacitance degradation than a 0805 package at a similar bias voltage. For example, either a 22-µF 0603-sized capacitor or a 10-µF 0805-sized capacitor is required to work with a nominal 10-µH inductor.

The TPS80010 boost is not sensitive to ESR in terms of stability. Using low-ESR capacitors, such as ceramic capacitors, is recommended to minimize output-voltage ripple. If heavy load changes are expected, the output capacitor value must be increased to avoid output voltage drops during fast load transients.

Table 3. Recommended Component List for Boost Converter

COMPONENT	VALUE	PART	SUPPLIER	SIZE
Inductor	10 µH	CBC3225T100MR	Taiyo Yuden	3.2 mm × 2.5 mm × 2.5 mm (1210)
		DO3314-103ML	Coilcraft	3.3 mm × 3.3 mm × 1.4 mm

Table 3. Recommended Component List for Boost Converter (continued)

COMPONENT	VALUE	PART	SUPPLIER	SIZE
Capacitor (IN)	10 µF	GRM188R60J106ME47D	Murata	0603
Capacitor (OUT)	22 µF	AMK107BJ226MA-T	Taiyo Yuden	0603

8.2.3 Application Curves

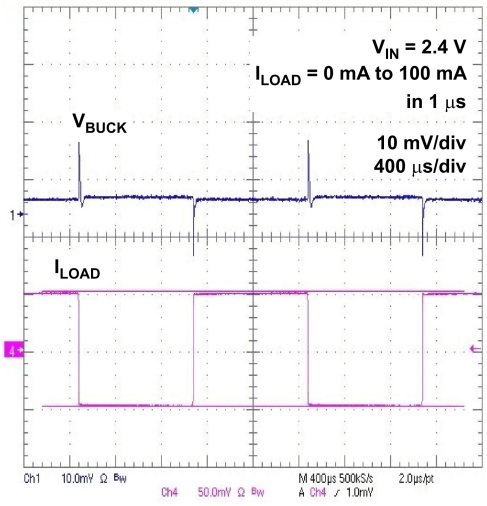


Figure 12. Buck Output Load Transient Response

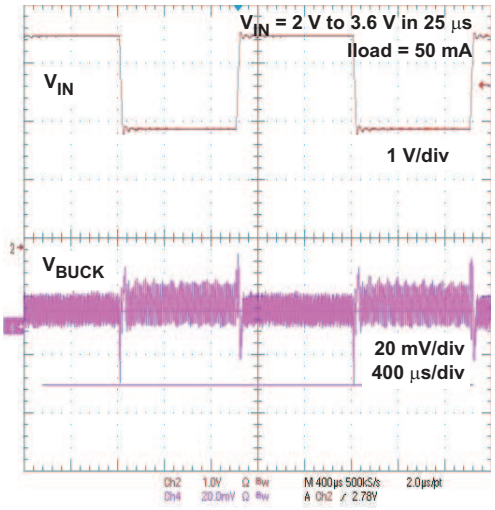


Figure 13. Buck Output Line Transient Response

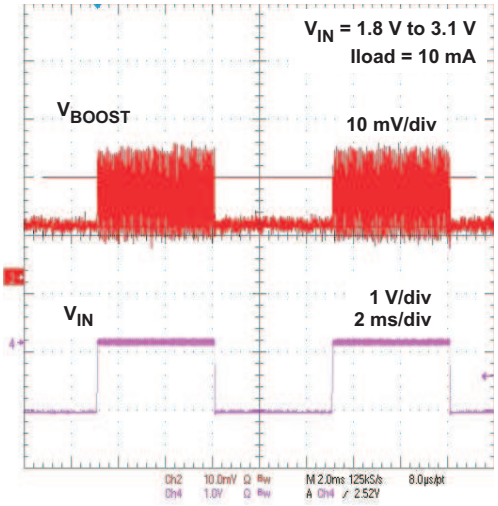


Figure 14. Boost Line Transient Response

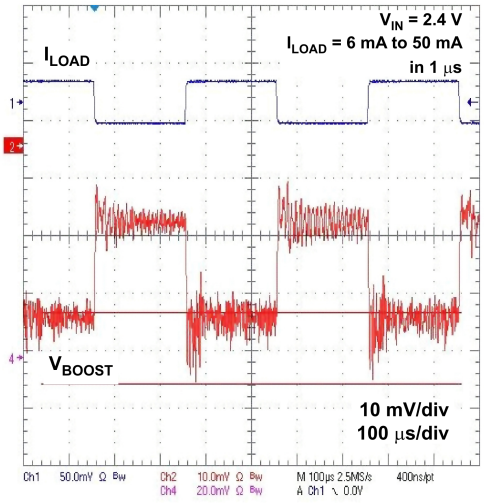


Figure 15. Boost Load Transient Response

9 Power Supply Recommendations

The TPS80010 was originally designed for dual-cell alkaline battery applications. Therefore, the device has working input voltage ranges from 1.95 V to 3.6 V. As long as the input voltage range is followed, the input supply can be from other regulated supplies.

10 Layout

10.1 Layout Guidelines

The VIN_BOOST and VIN_BUCK pins must be bypassed to ground with a low-ESR ceramic bypass capacitor. Texas Instruments recommends the typical bypass capacitance is 10 μF.

- The optimum placement is closest to the VIN_BUCK and VIN_BOOST pins of the device. Minimize the loop area formed by the bypass capacitor connection, the VINDCDC and VINLDO pins, and the thermal pad of the device.
- The thermal pad must be tied to the PCB ground plane with multiple vias.
- The FB _BOOST, FB_BUCK, SW_BOOST, SW_BCUK, and OUT_VM pins (feedback and output pins) traces must be routed away from any potential noise source to avoid coupling.
- Output capacitance must be placed immediately at the output pins. Excessive distance from the capacitance to output pins may cause poor converter performance.

10.2 Layout Example

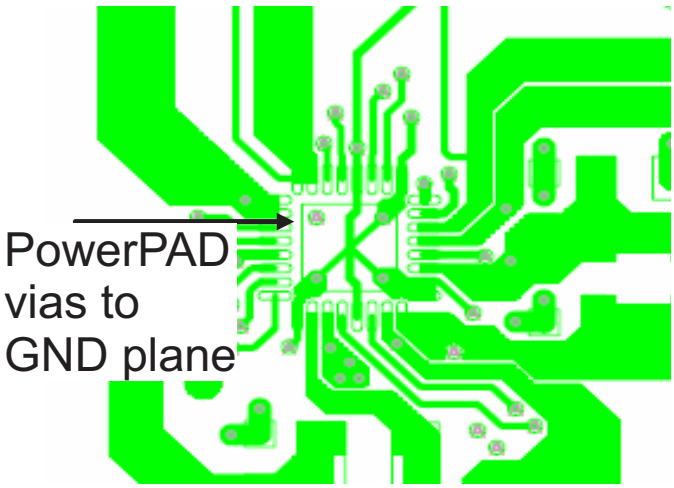


Figure 16. TPS80010 Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS80010ARSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 80010A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

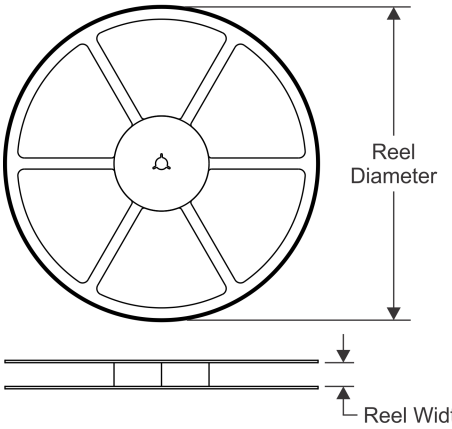
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

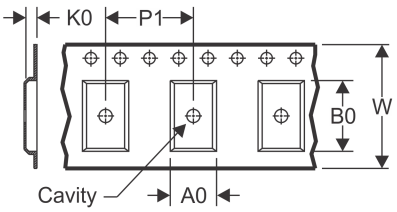
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

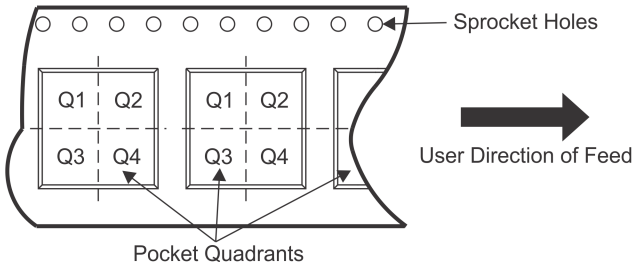


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

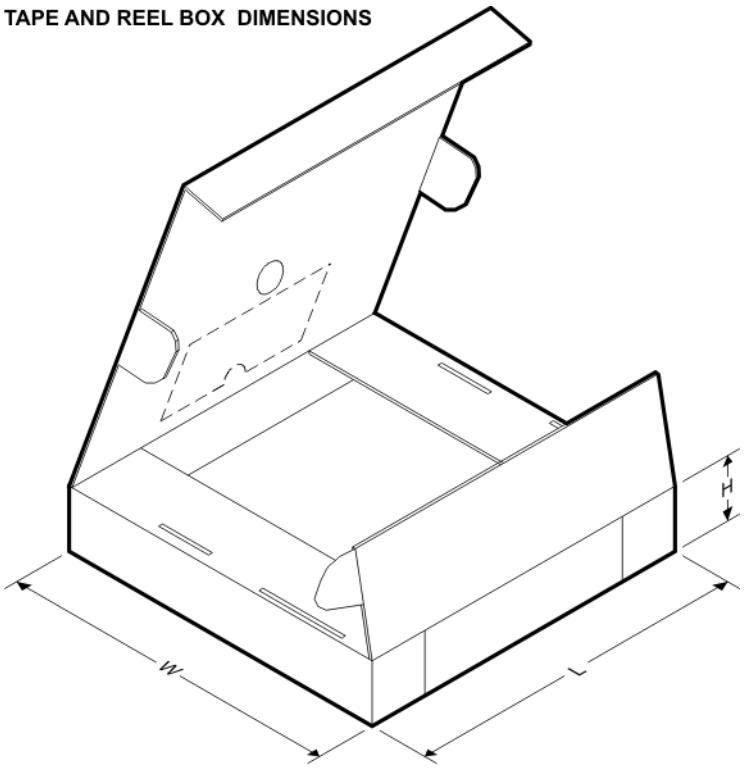
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS80010ARSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS80010ARSMR	VQFN	RSM	32	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

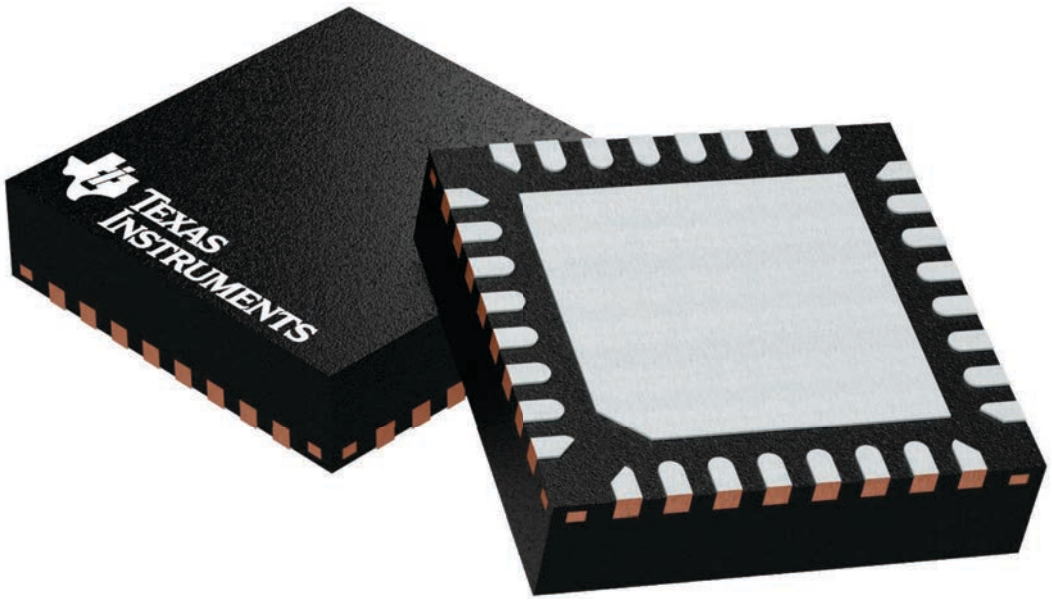
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



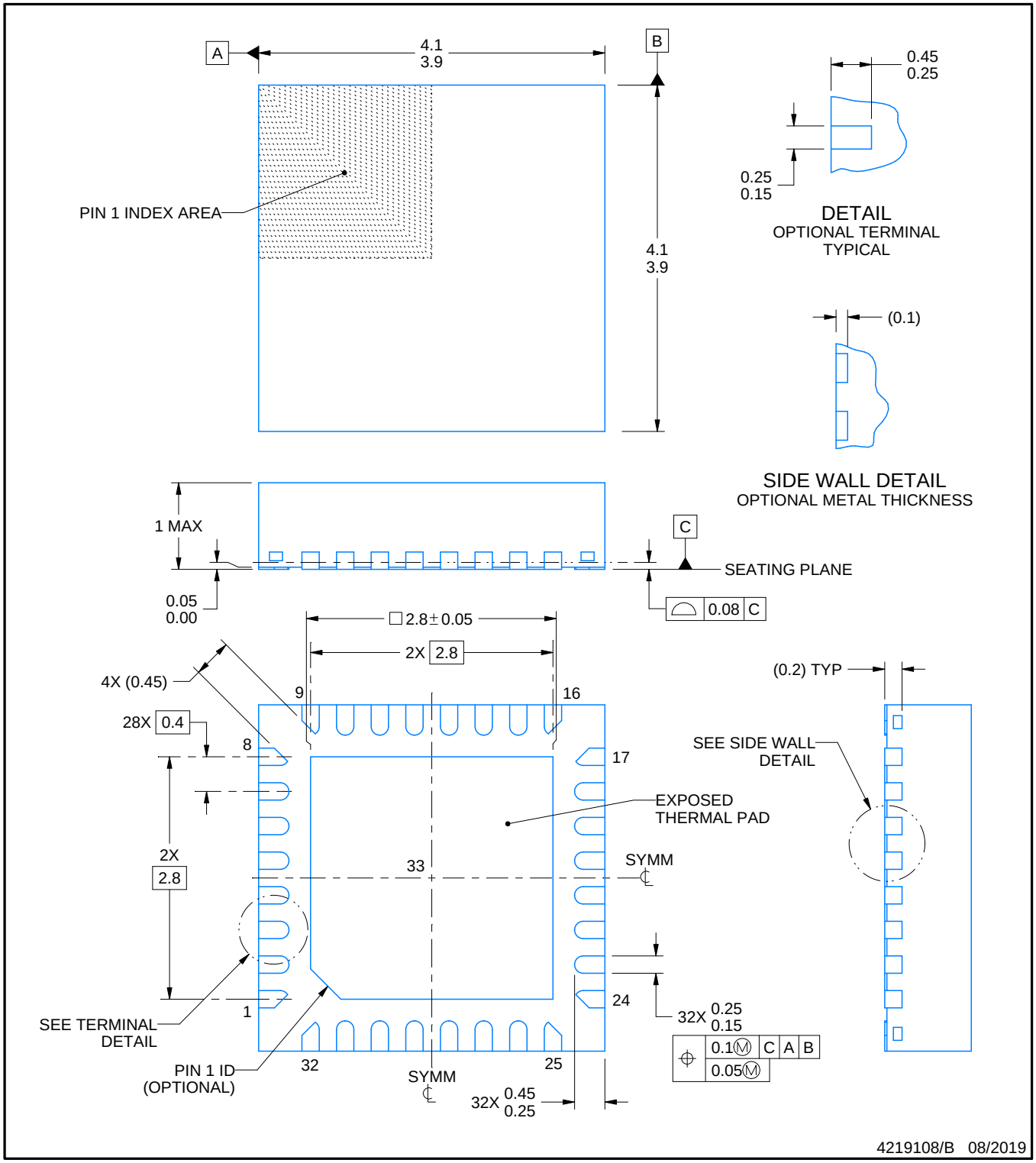
4224982/A

PACKAGE OUTLINE

RSM0032B

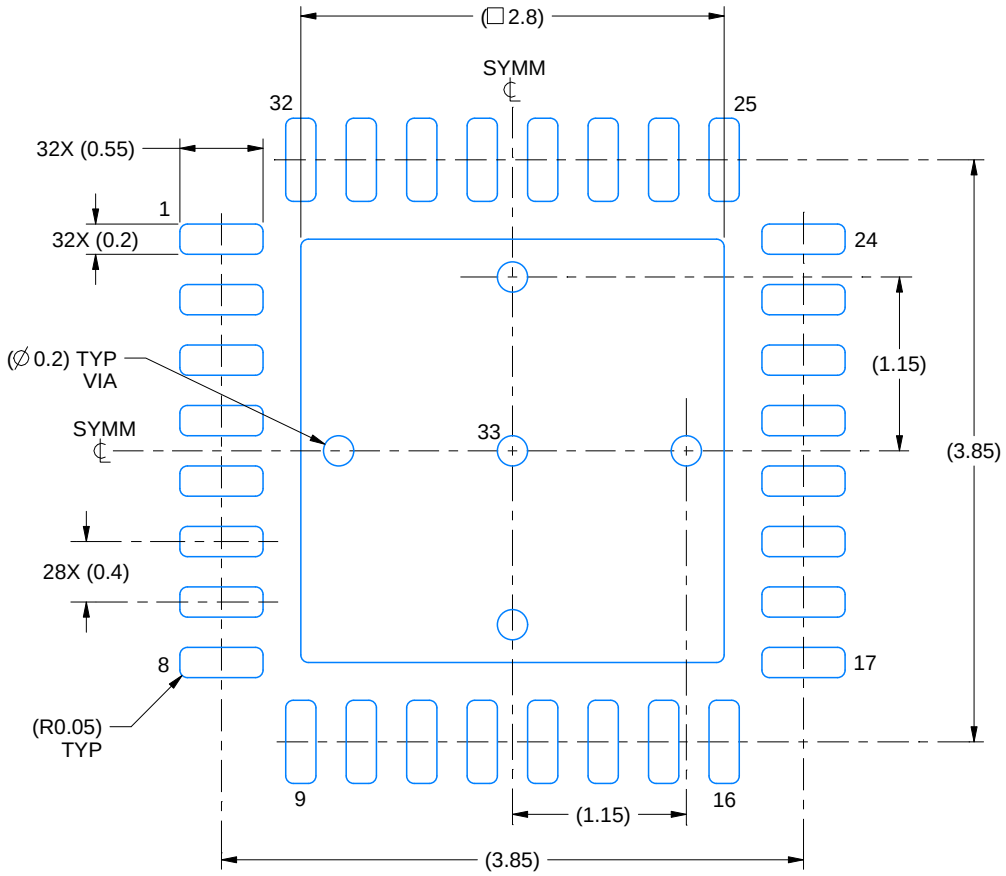
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

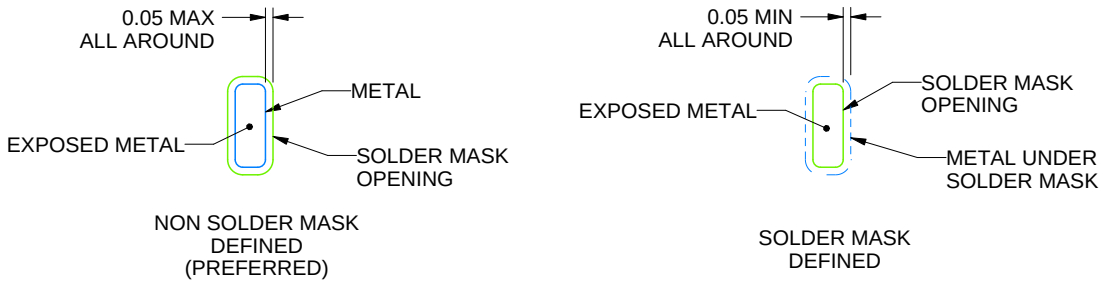


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

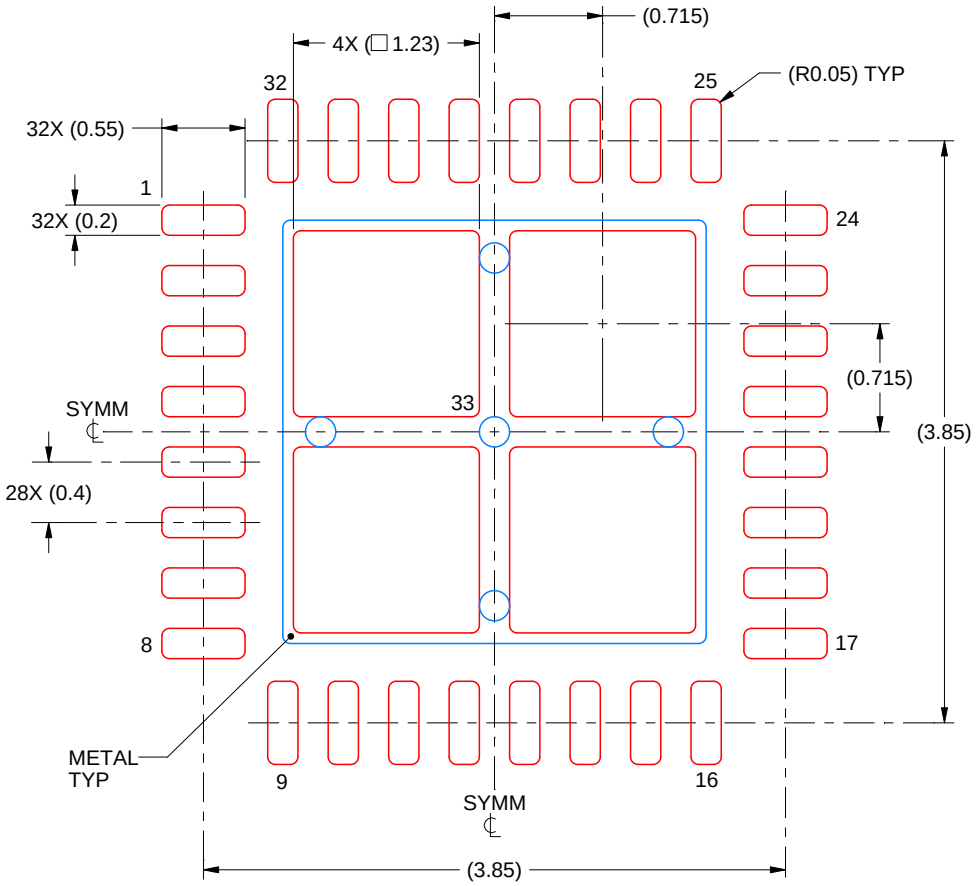


SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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