



**THE DATASHEET OF
SN74ABTH32316PN**

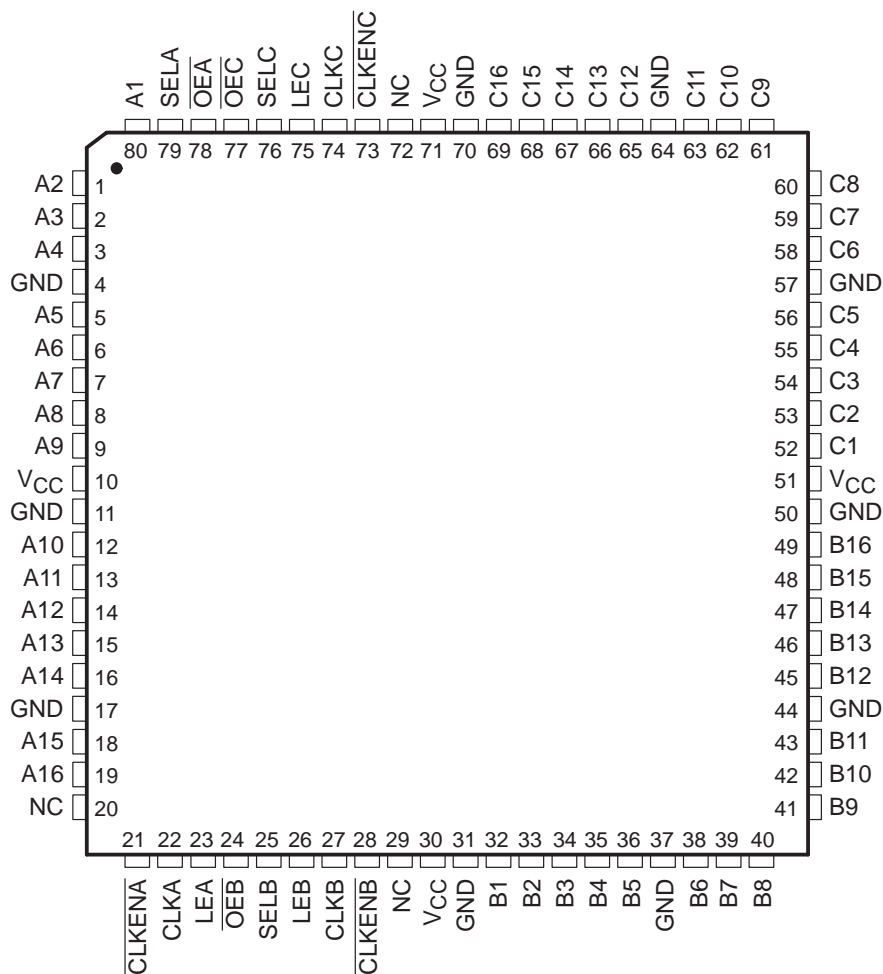


SN54ABTH32316, SN74ABTH32316 16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

SCBS179E – JUNE 1992 – REVISED MAY 1997

- **Members of the Texas Instruments Widebus+™ Family**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **UBE™ (Universal Bus Exchanger) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5 V$, $T_A = 25^\circ C$**
- **High-Impedance State During Power Up and Power Down**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include 80-Pin Plastic Thin Quad Flat (PN) Package With $12 \times 12\text{-mm}$ Body Using 0.5-mm Lead Pitch and 84-Pin Ceramic Quad Flat (HT) Package**

'ABTH32316 . . . PN PACKAGE
(TOP VIEW)



NC – No internal connection



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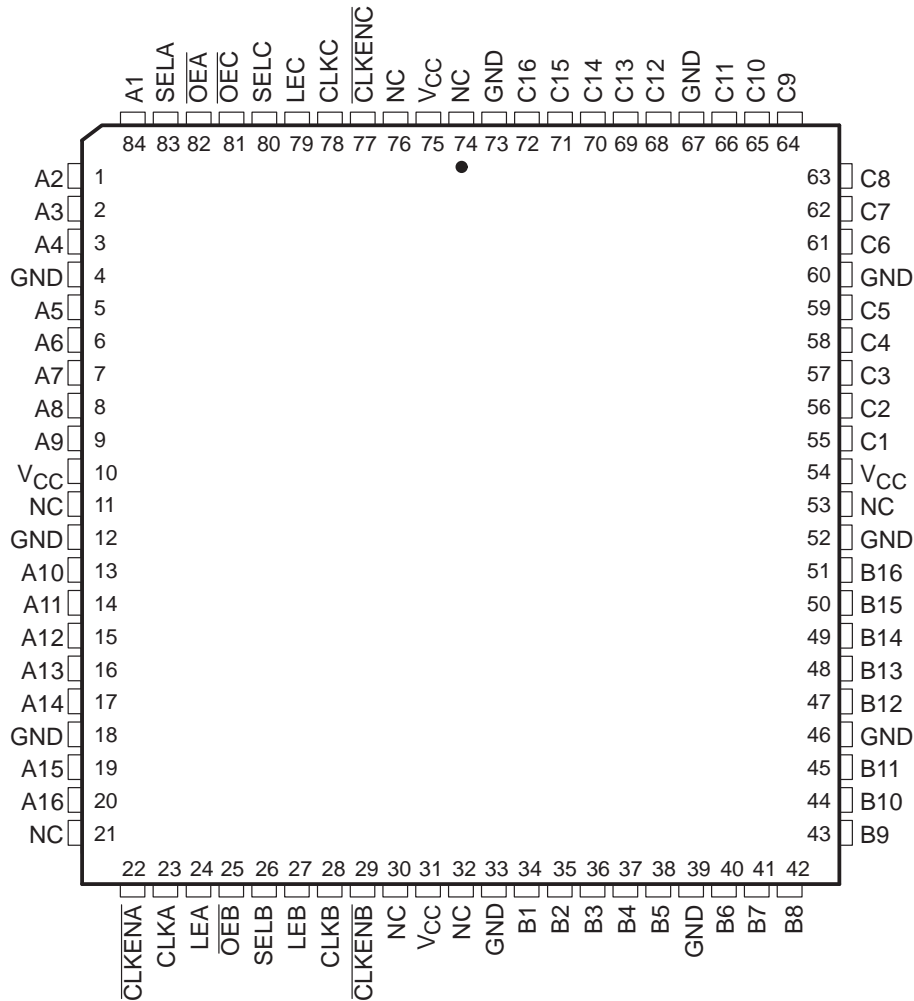
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SN54ABTH32316 . . . HT PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABTH32316 consist of three 16-bit registered input/output (I/O) ports. These registers combine D-type latches and flip-flops to allow data flow in transparent, latch, and clock modes. Data from one input port can be exchanged to one or more of the other ports. Because of the universal storage element, multiple combinations of real-time and stored data can be exchanged among the three ports.

Data flow in each direction is controlled by the output-enable (\overline{OEA} , \overline{OEB} , and \overline{OEC}), select-control (SELA, SELB, and SELC), latch-enable (LEA, LEB, and LEC), and clock (CLKA, CLKB, and CLKC) inputs. The A data register operates in the transparent mode when LEA is high. When LEA is low, data is latched if CLKA is held at a high or low logic level. If LEA and clock-enable A (\overline{CLKENA}) are low, data is stored on the low-to-high transition of CLKA. Output data selection is accomplished by the select-control pins. All three ports have active-low output enables, so when the output-enable input is low, the outputs are active; when the output-enable input is high, the outputs are in the high-impedance state.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH32316 is characterized for operation over the full military temperature range of -55°C to 125°C .
 The SN74ABTH32316 is characterized for operation from -40°C to 85°C .

Function Tables

STORAGE†

INPUTS				OUTPUT
CLKENA	CLKA	LEA	A	
H	X	L	X	Q_0^{\ddagger}
L	↑	L	L	L
L	↑	L	H	H
X	H	L	X	Q_0^{\ddagger}
X	L	L	X	Q_0^{\ddagger}
X	X	H	L	L
X	X	H	H	H

† A-port register shown. B and C ports are similar but use $\overline{\text{CLKENB}}$, $\overline{\text{CLKENC}}$, CLKB , CLKC , LEB , and LEC .

‡ Output level before the indicated steady-state input conditions were established

A-PORT OUTPUT

INPUTS		OUTPUT A
$\overline{\text{OEA}}$	SELA	
H	X	Z
L	H	Output of C register
L	L	Output of B register

B-PORT OUTPUT

INPUTS		OUTPUT B
$\overline{\text{OEB}}$	SELB	
H	X	Z
L	H	Output of A register
L	L	Output of C register

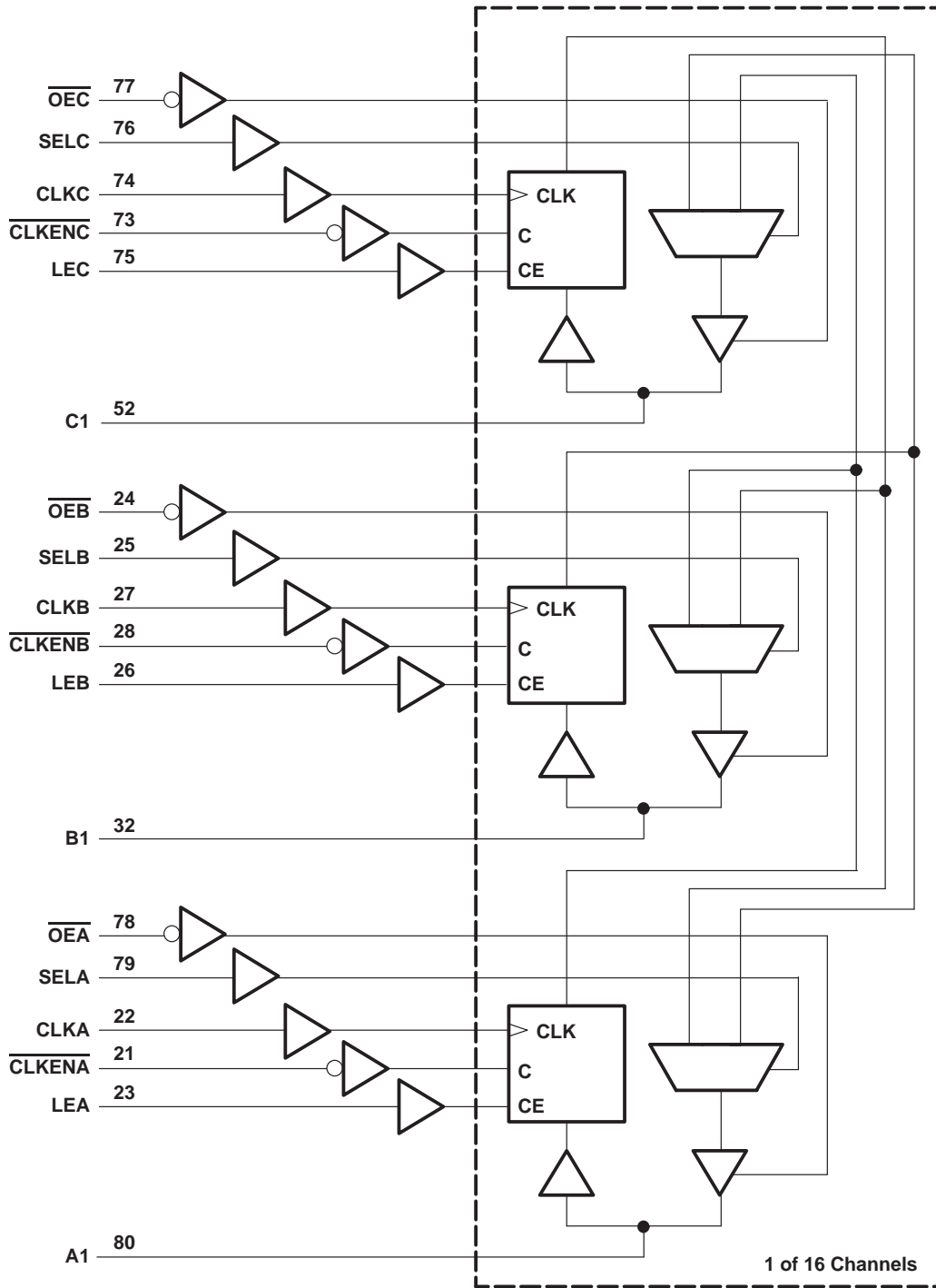
C-PORT OUTPUT

INPUTS		OUTPUT C
$\overline{\text{OEC}}$	SELC	
H	X	Z
L	H	Output of B register
L	L	Output of A register

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logic diagram (positive logic)



Pin numbers shown are for the PN package.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABTH32316	96 mA
SN74ABTH32316	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): PN package	62°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABTH32316		SN74ABTH32316		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused control pins must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ABTH32316			SN74ABTH32316			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA	-1.2			-1.2			V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = -3 mA	2.5			2.5			V
		V _{CC} = 5 V, I _{OH} = -3 mA	3			3			
		V _{CC} = 4.5 V, I _{OH} = -24 mA	2			2			
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 48 mA	0.55						V
		V _{CC} = 4.5 V, I _{OL} = 64 mA				0.55			
V _{hys}			100			100			mV
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND	±1			±1			μA
	A, B, or C ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND	±100			±20			
I _I (hold)	A, B, or C ports	V _{CC} = 4.5 V, V _I = 0.8 V	100			100			μA
		V _{CC} = 4.5 V, V _I = 2 V	-100			-100			
I _{OZPU} ‡		V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$	±50			±50			μA
I _{OZPD} ‡		V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$	±50			±50			μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V	±100			±100			μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V, Outputs high	50			50			μA
I _O §		V _{CC} = 5.5 V, V _O = 2.5 V	-50	-100	-180	-50	-100	-180	mA
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs high	2			2			mA
		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs low	40			40			
		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs disabled	1			1			
ΔI _{CC} ¶		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	1			0.5			mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V	3			3			pF
C _{io}	A, B, or C ports	V _O = 2.5 V or 0.5 V	11.5			11.5			pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This parameter is specified by characterization.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABTH32316		SN74ABTH32316		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	150	0	150	MHz
t _w	Pulse duration	LE high	3.3		3.3		ns
		CLK high or low	3.3		3.3		
t _{su}	Setup time	A, B, or C before CLK↑	2.6		2.4		ns
		A or B before LE↓	2.5		2.1		
		CLKEN before CLK↑	3.5		3.2		
t _h	Hold time	A, B, or C after CLK↑	1.8		1.4		ns
		A or B after LE↓	2.4		2.1		
		CLKEN after CLK↑	1.5		1.1		



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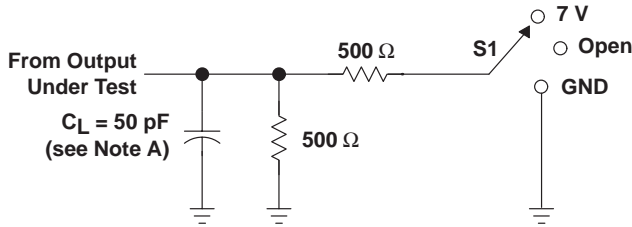
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABTH32316		SN74ABTH32316		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			150		150		MHz
t_{PLH}	A, B, or C	C, B, or A	0.8	6.5	1.4	6.1	ns
t_{PHL}			0.5	6.8	1.1	6.6	
t_{PLH}	SEL	A, B, or C	0.8	6.7	1.4	6.5	ns
t_{PHL}			0.8	6.8	1.8	6.5	
t_{PLH}	LE	A, B, or C	1.5	8	2.6	7.5	ns
t_{PHL}			1.5	7.4	2.6	6.9	
t_{PLH}	CLK	A, B, or C	1.5	8	2.5	7.5	ns
t_{PHL}			1.5	7.2	2.5	6.7	
t_{PZH}	\overline{OE}	A, B, or C	0.8	6.7	1.5	6.4	ns
t_{PZL}			1.5	7.1	2.4	6.8	
t_{PHZ}	\overline{OE}	A, B, or C	0.8	7.2	1.5	6	ns
t_{PLZ}			0.8	6.4	1.9	6.1	

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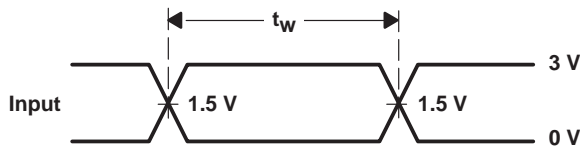
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PARAMETER MEASUREMENT INFORMATION

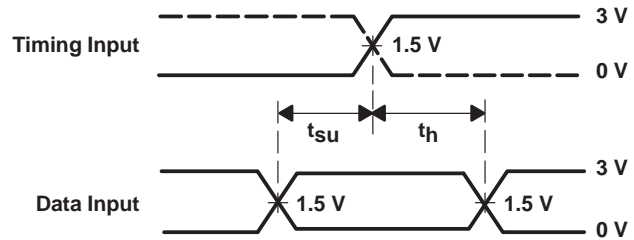


LOAD CIRCUIT

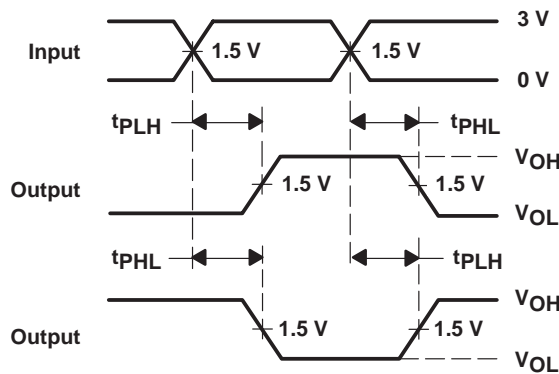
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



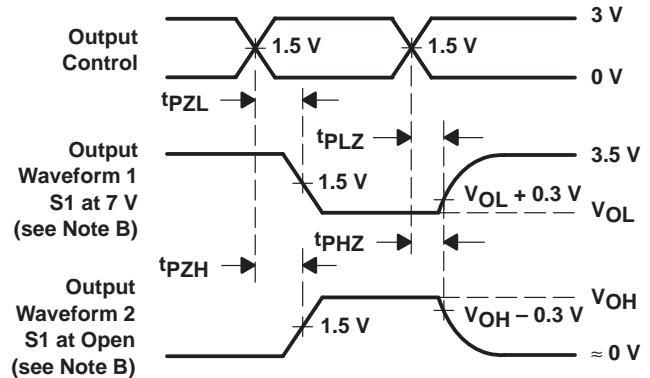
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS






VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9680801QXA	ACTIVE	CFP	HT	84	250	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9680801QX A SNJ54ABTH32316 HT	
SN74ABTH32316PN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ABTH32316	
SNJ54ABTH32316HT	ACTIVE	CFP	HT	84	250	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9680801QX A SNJ54ABTH32316 HT	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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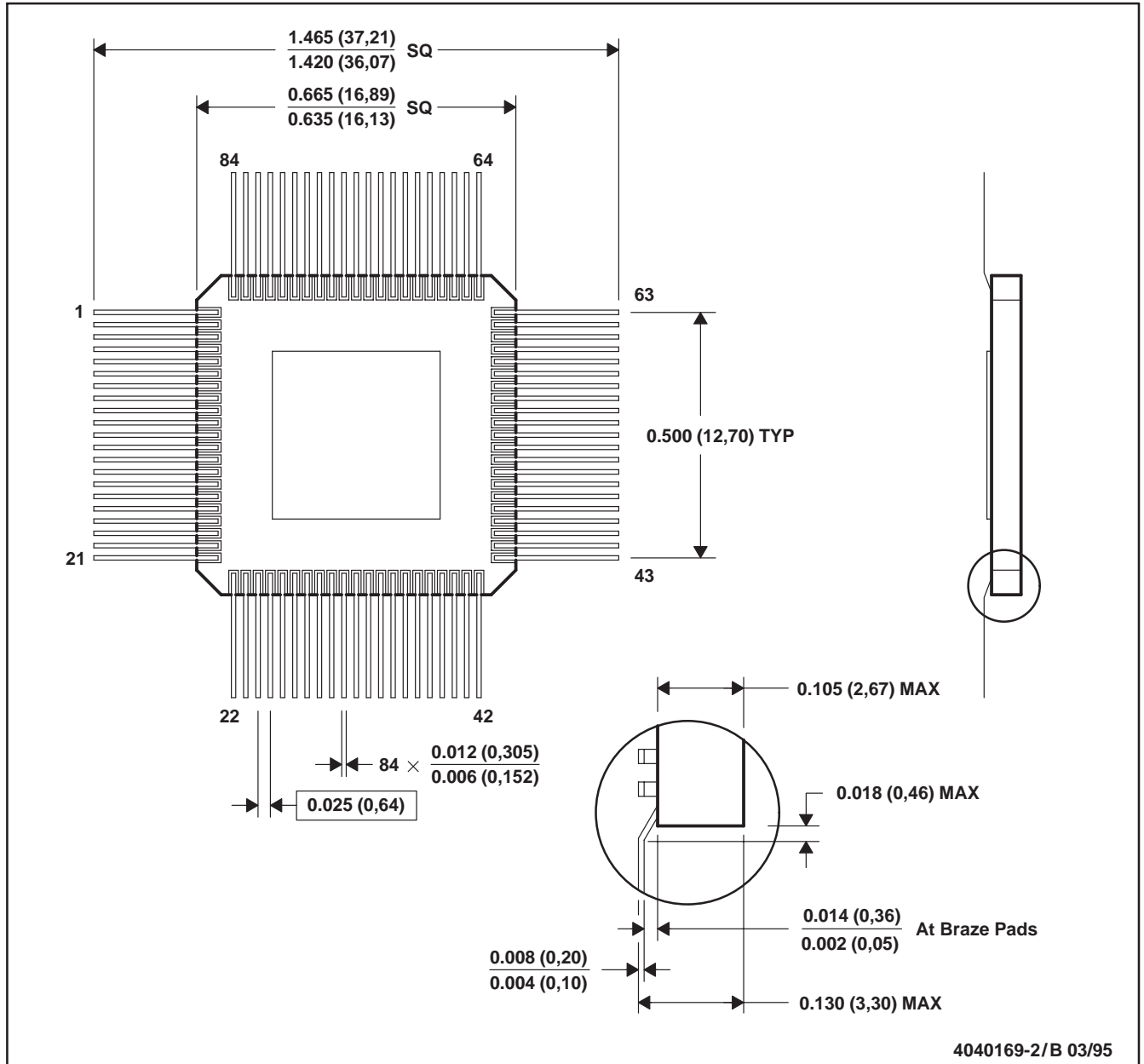
- Catalog: [SN74ABTH32316](#)
- Military: [SN54ABTH32316](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

HT (S-CQFP-F84)

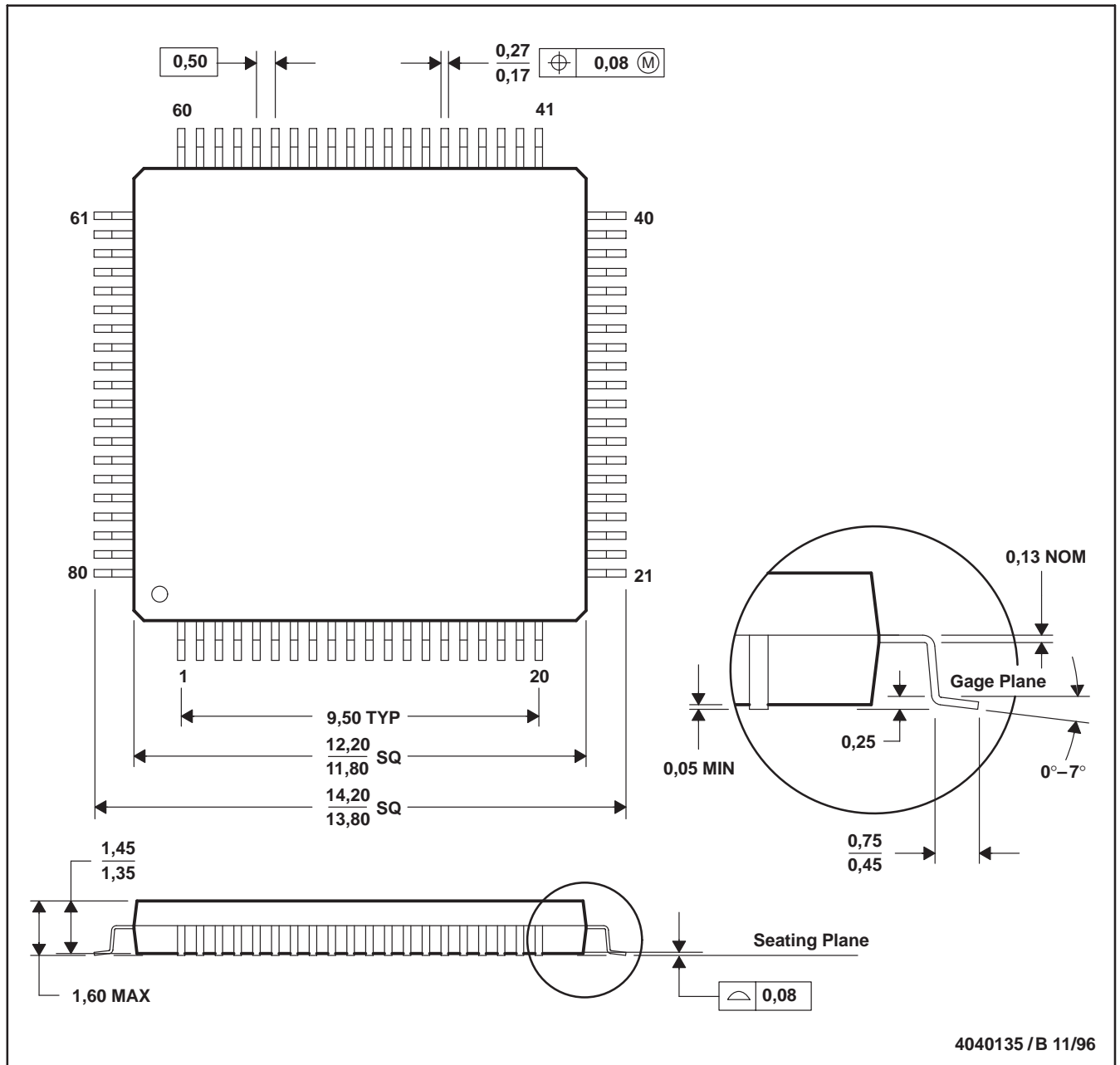
CERAMIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MO-090 AA

PN (S-PQFP-G80)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

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