FAIRCHILD SEMICONDUCTOR®

August 2011

FMS6144A
Four-Channel, 6th-Order SD VoltagePlus™ Video Filter Driver

Features

- Four-Channel 6th-Order 8MHz (SD) Filter
- Drives Single, AC- or DC-Coupled Video Loads (150Ω)
- Transparent Input Clamping
- Supply Range: 3.3V to 5.0V
- AC- or DC-Coupled Inputs and Outputs
- Robust 9kV ESD Protection
- Lead-Free TSSOP 14-Pin Package

Applications

- Cable Set-Top Boxes
- Satellite Set-Top Boxes
- DVD Players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

Description

The FMS6144A VoltagePlus™ video filter is intended to replace passive LC filters and drivers with a cost-effective integrated device. Four 6th-order filters provide improved image quality compared to typical 2nd and 3rd order passive solutions.

The FMS6144A may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required *(see the Applications section for details)*.

The outputs can drive AC- or DC-coupled single (150Ω) or dual (75Ω) video loads. DC coupling the outputs removes the need for large output coupling capacitors. The input DC levels are offset approximately +280mV at the output *(see the Applications section for details)*.

Related Applications Notes

AN-6024 – FMS6xxx Product Series Understanding Analog Video Signal Clamps, Bias, DC Restore, and AC or DC coupling Methods

AN-6041 – PCB Layout Considerations for Video Filter / Drivers

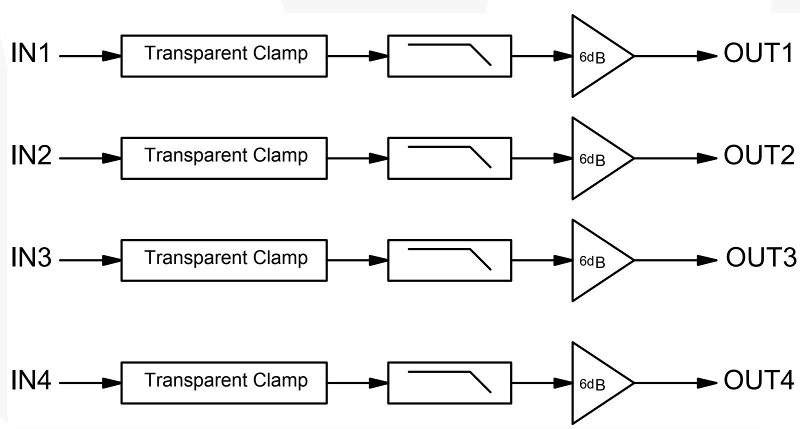


Figure 1. Block Diagram

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FMS6144AMTC14X	-40°C to +85°C	14-Lead TSSOP	2500 per Reel

Pin Configuration

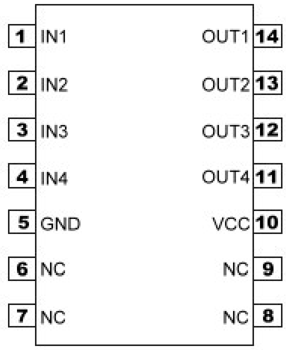


Figure 2. 14-Lead TSSOP (Top View)

Pin Definitions

Pin#	Name	Type	Description
1	IN1	Input	Video Input Channel 1
2	IN2	Input	Video Input Channel 2
3	IN3	Input	Video Input Channel 3
4	IN4	Input	Video Input Channel 4
5	GND	Input	Device Ground Connection
6	NA	NA	No Connection
7	NA	NA	No Connection
8	NA	NA	No Connection
9	NA	NA	No Connection
10	Vcc	Input	Positive Power Supply
11	OUT4	Output	Filtered Output Channel 4
12	OUT3	Output	Filtered Output Channel 3
13	OUT2	Output	Filtered Output Channel 2
14	OUT1	Output	Filtered Output Channel 1

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC}+0.3	V
V_{OUT}	Maximum Output Current, Do Not Exceed		50	mA

Electrostatic Discharge Information

Symbol	Parameter	Min	Unit
ESD	Human Body Model, JESD22-A114	9	kV
	Charged Device Model, JESD22-C101	2	

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+300	°C
Θ_{JA}	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		90		°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		+85	°C
V_{CC}	Supply Voltage Range	3.14	3.30	5.25	V

DC Electrical Characteristics

T_A=25°C, V_{CC}=3.3V, R_S=37.5Ω, all inputs are AC-coupled with 0.1uF, and all outputs are AC coupled with 220µF into 150Ω load; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Supply						
V_{CC}	Supply Voltage Range	V_S Range	3.14	3.30	5.25	V
I_{CC}	Quiescent Supply Current(1)	V_S=+3.3V, No Load		21	24	mA
		V_S=+5.0V, No Load		25	29	
V_{IN}	Video Input Voltage Range	Referenced to GND if DC Coupled		1.4		V_{PP}
PSRR	Power Supply Rejection Ratio	DC (all Channels)		-65		dB

Note:
1. 100% tested at T_A=25°C

AC Electrical Characteristics

T_A=25°C, V_{CC}=3.3V, R_S=37.5Ω, all inputs are AC-coupled with 0.1uF, and all outputs are AC coupled with 220µF into 150Ω load, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV	Channel Gain(2)	Active Video Input Range = $1V_{PP}$	5.8	6.0	6.2	dB
$BW_{0.1dB}$	±0.1dB Bandwidth	R_{SOURCE}=75Ω, R_L=150Ω		5		MHz
$BW_{-1.0dB}$	-1.0 dB Bandwidth	R_{SOURCE}=75Ω, $R_{L=}$150Ω		7		MHz
$BW_{3.0dB}$	-3.0 dB Bandwidth	R_{SOURCE}=75Ω, $R_{L=}$150Ω		8		MHz
Att_{27M}	Normalized Stopband Attenuation(2)	R_{SOURCE}=75Ω, f=27MHz	45	60		dB
DG	Differential Gain - NTSC/PAL	Active Video Input Range = $1V_{PP}$		0.6		%
DP	Differential Phase - NTSC/PAL	Active Video Input Range = $1V_{PP}$		0.6		°
THD	Total Harmonic Distortion	f=1.00MHz; V_{OUT}=1.4V_{PP}		0.2		%
X_{talk}	Crosstalk (Channel to Channel)	f=1.00MHz; V_{OUT}=1.4V_{PP}		-65		dB
SNR	Peak Signal to RMS Noise	NTC-7 Weighting: 100kHz to 4.2MHz		74		dB
T_{pd}	Propagation Delay	Delay from Input to Output; 100KHz to 4.5MHz		90		ns
CLG	Chroma-Luma Gain(2)	400Khz to 3.58Mhz	95	100	105	%
CLD	Chroma-Luma Delay	400Khz to 3.58Mhz		7.5		ns

Note:
2. 100% tested at T_A=25°C

Typical Performance Characteristics

Unless otherwise noted, T_A = 25°C, V_{CC} = 2.7V, R_S = 37.5Ω, and AC-coupled output into 150Ω load.

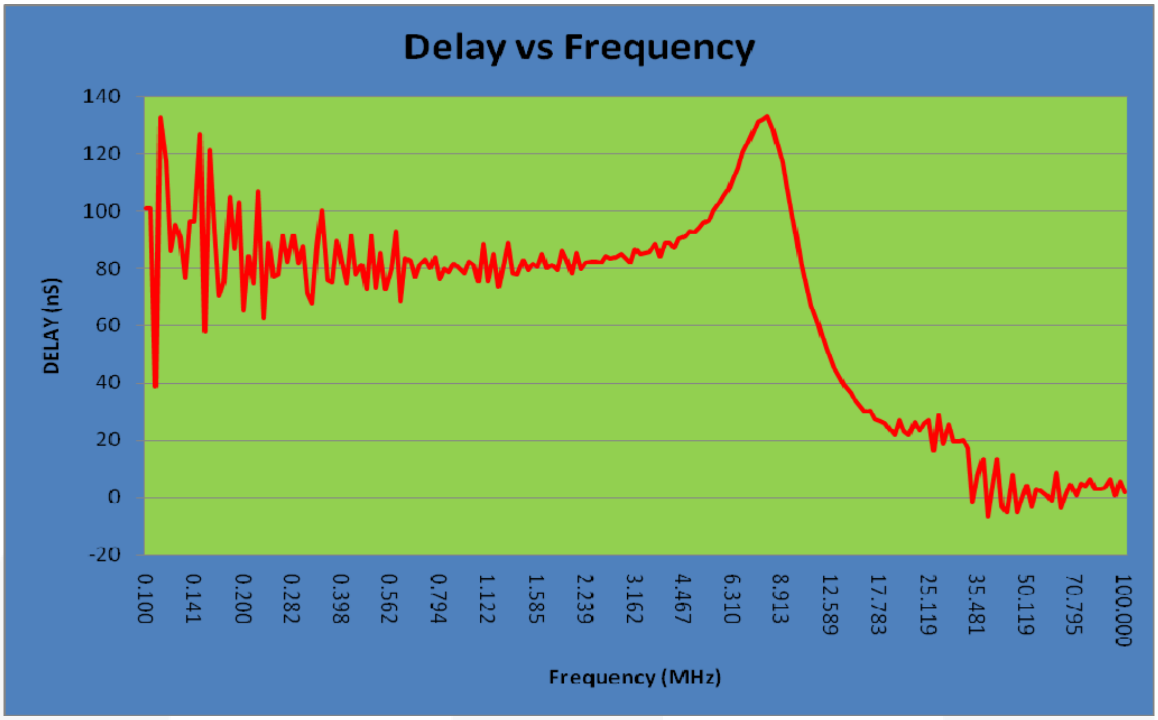


Figure 3. Delay vs. Frequency

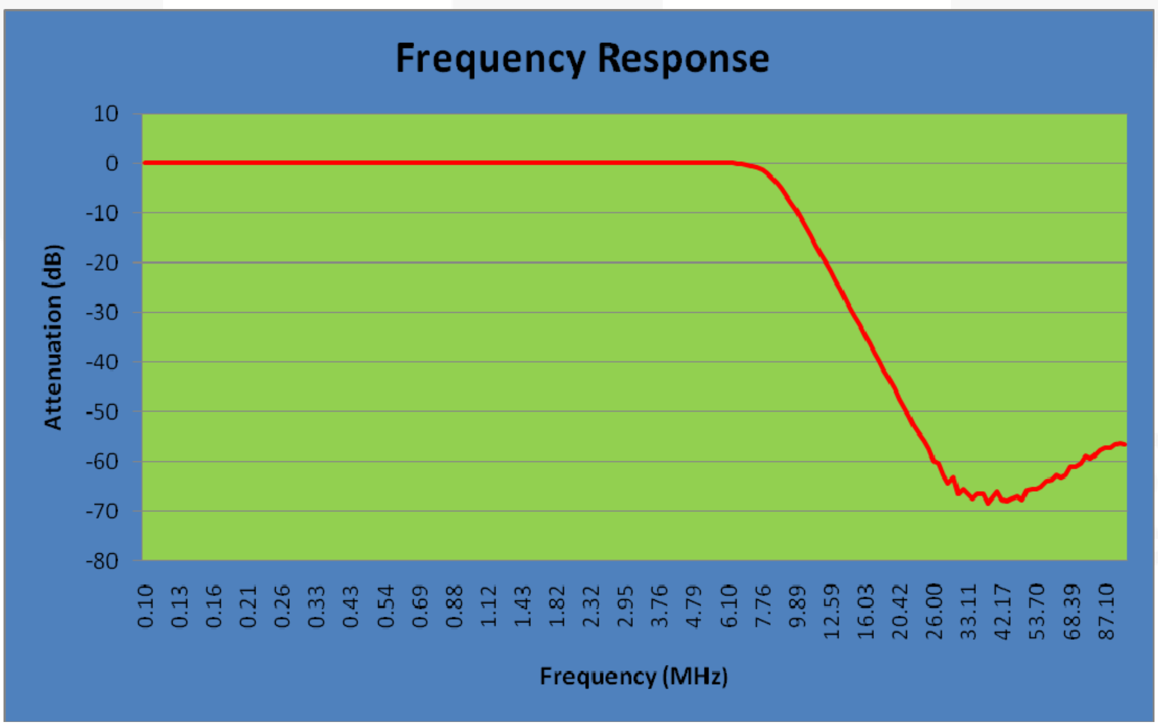


Figure 4. Frequency Response

Typical Performance Characteristics

Unless otherwise noted, T_A = 25°C, V_{CC} = 2.7V, R_S = 37.5Ω, and AC-coupled output into 150Ω load.

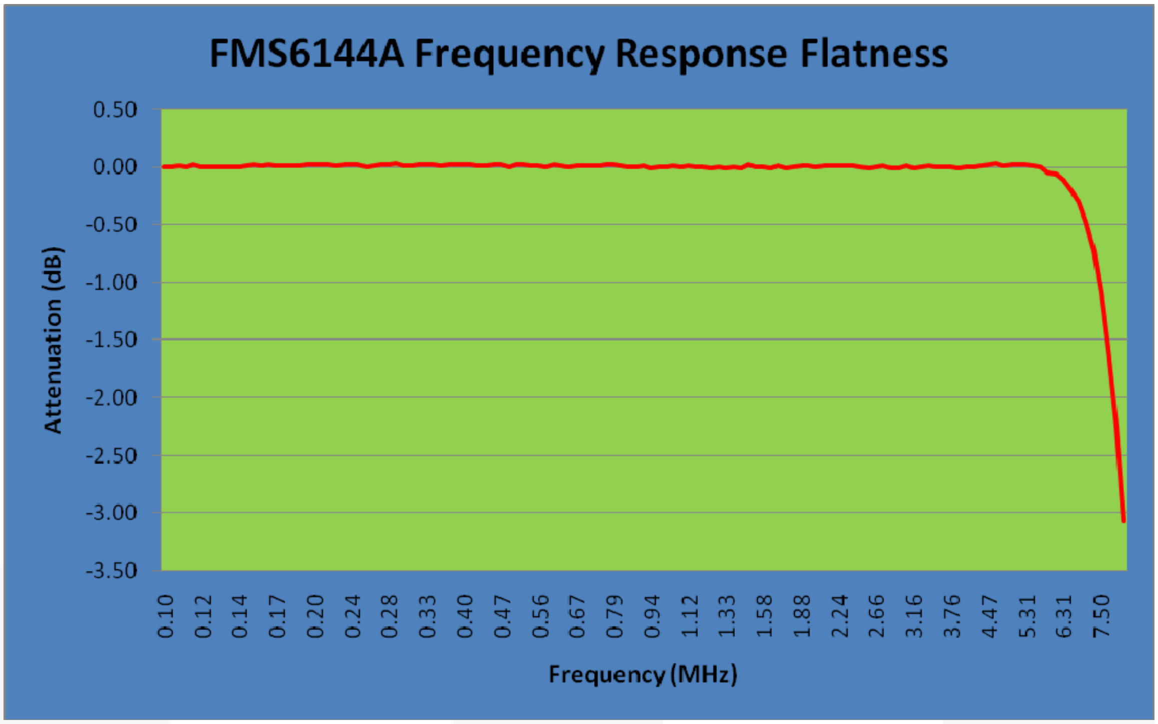


Figure 5. Frequency Response Flatness

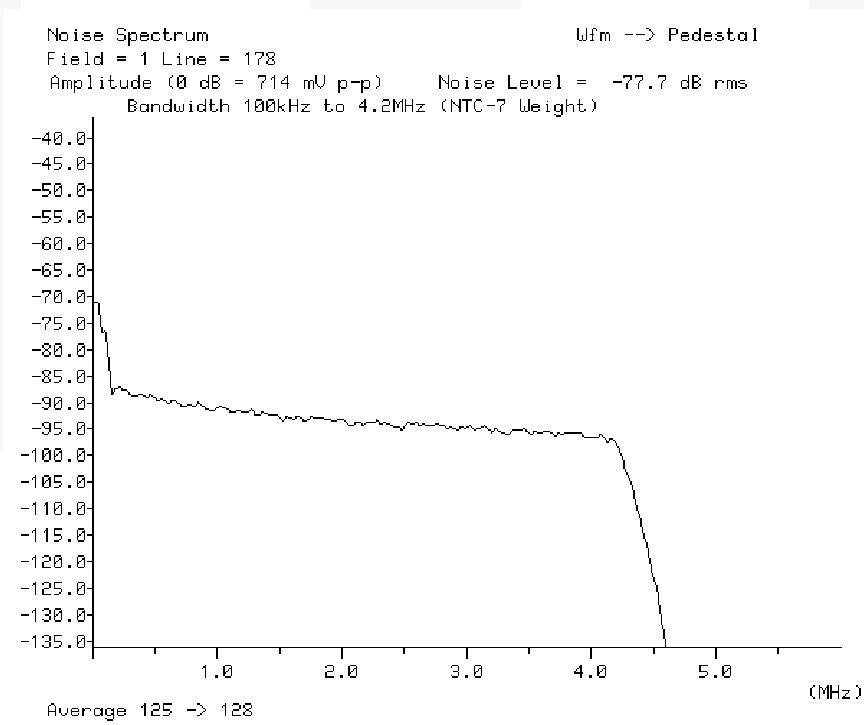


Figure 6. Noise vs. Frequency

Typical Performance Characteristics

Unless otherwise noted, T_A = 25°C, V_{CC} = 2.7V, R_S = 37.5Ω, and AC-coupled output into 150Ω load.

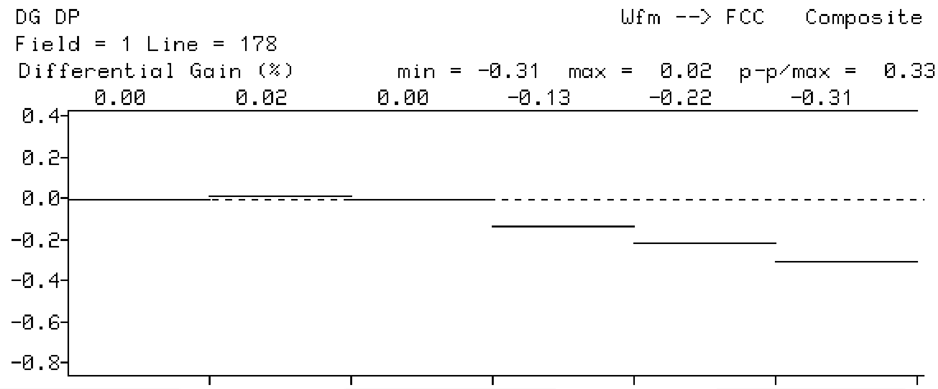


Figure 9. Differential Gain

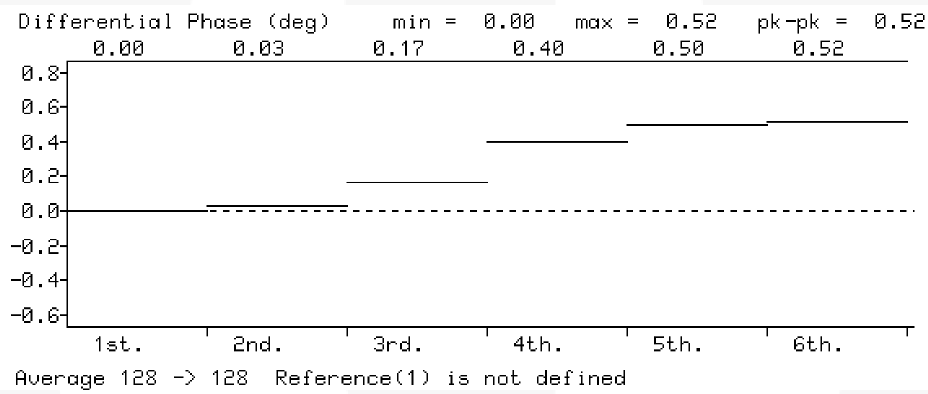


Figure 10. Differential Phase

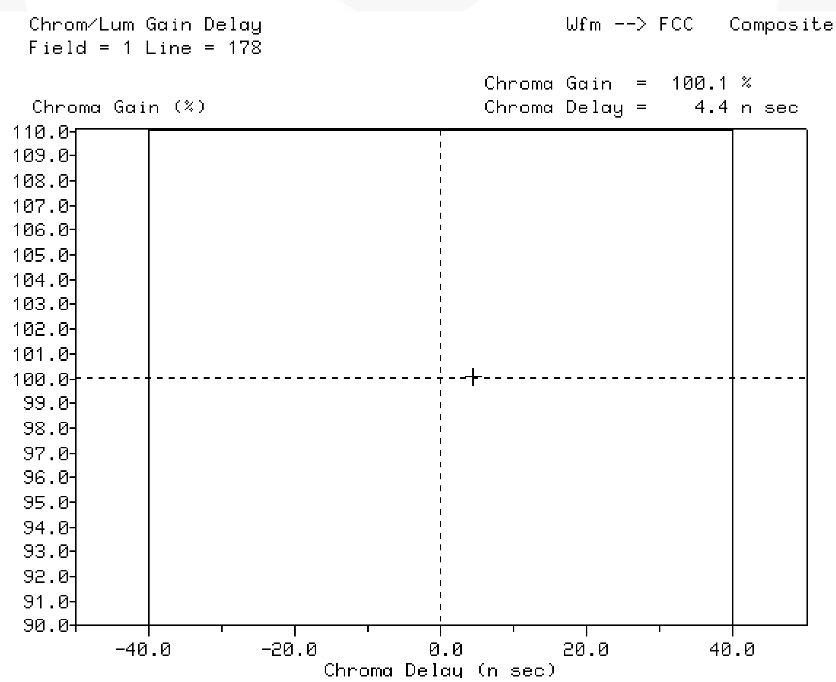


Figure 11. Chroma / Luma Gain & Delay

Applications Information

The following circuit may be used for direct DC-coupled drive by DACs with an output voltage range of 0V to $1.4V_{PP}$.

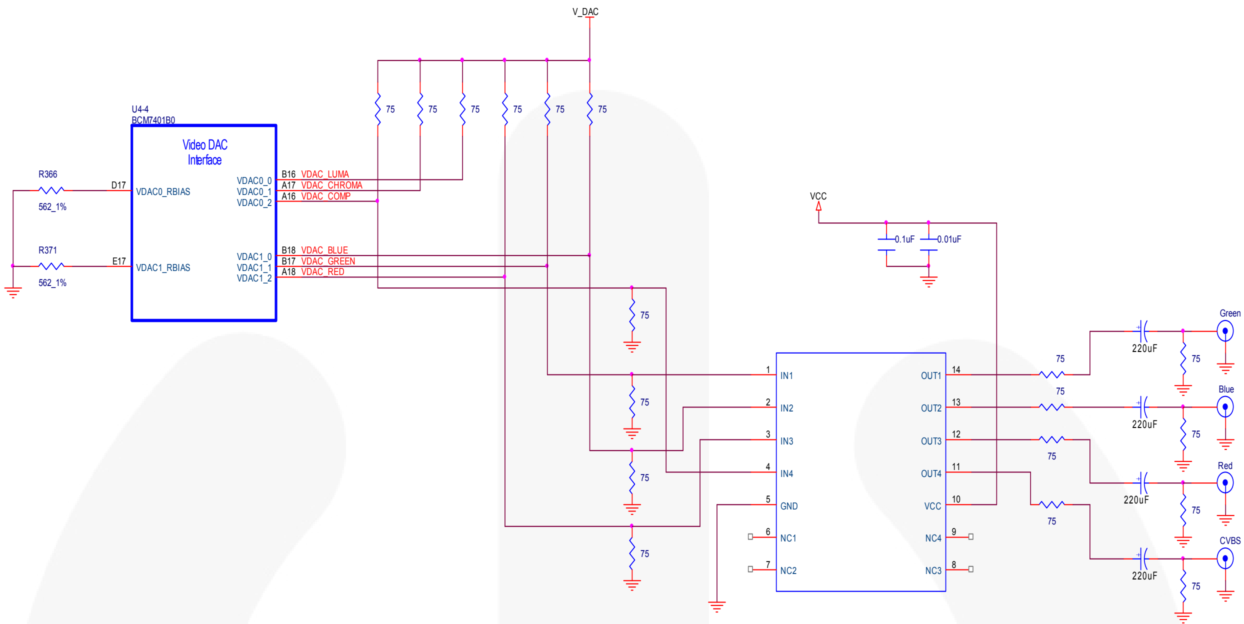


Figure 12. Typical Application

Application Information

Application Circuits

The FMS6144A VoltagePlus™ video filter provides 6dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in Figure 13:

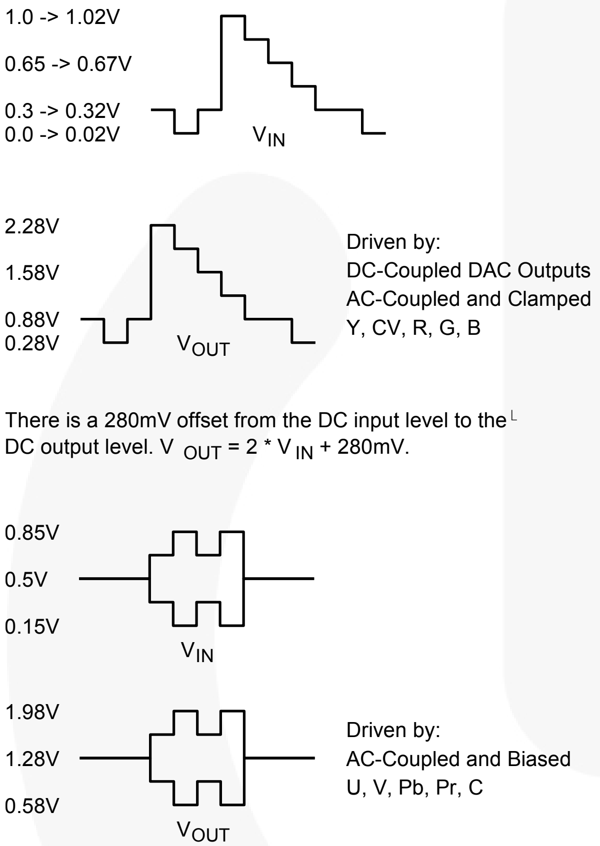


Figure 13. Typical Voltage Levels

The FMS6144A provides an internal diode clamp to support AC-coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the FMS6144A without an AC-coupling capacitor. When the input is AC coupled, the diode clamp sets the sync tip (or lowest voltage) just below ground. The worst-case sync tip compression due to the clamp cannot exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within its acceptable range.

For symmetric signals like Chroma, U, V, Pb, and Pr; the average DC bias is fairly constant and the inputs can be AC-coupled with the addition of a pull-up resistor to set the DC input voltage. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown in Figure 14.

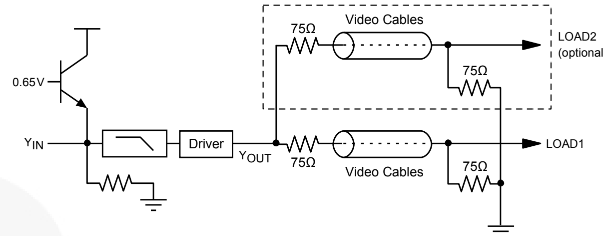


Figure 14. Input Clamp Circuit

I/O Configurations

For a DC-coupled DAC drive with DC-coupled outputs, use the configurationin Figure 15.

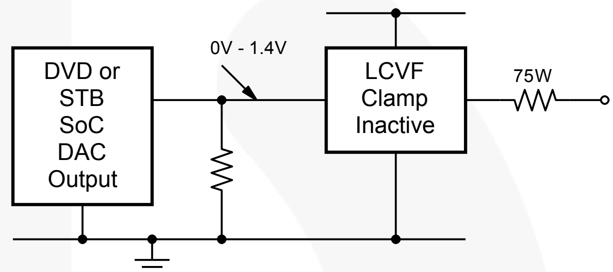


Figure 15. DC-Coupled Inputs and Outputs

Alternatively, if the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC coupled as follows:

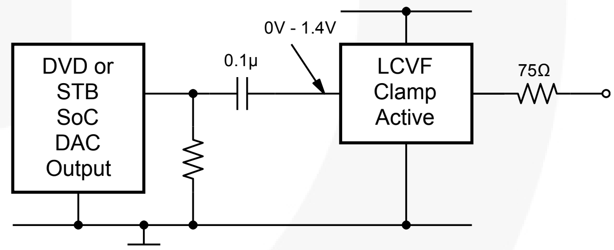


Figure 16. AC-Coupled Inputs, DC-Coupled Outputs

When FMS6144A is driven by an unknown external source or a SCART switch with its own clamping circuitry, the inputs should be AC coupled like Figure 17.

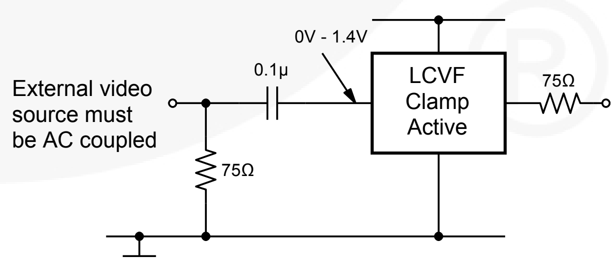


Figure 17. SCART with DC-Coupled Outputs

The same method can be used for biased signals, with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is 800kΩ ±20%, so the external resistance should be 7.5MΩ to set the DC level to 500mV.

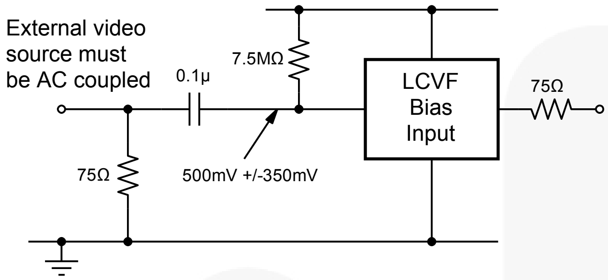


Figure 18. Biased SCART with DC-Coupled Outputs

The same circuits can be used with AC-coupled outputs if desired.

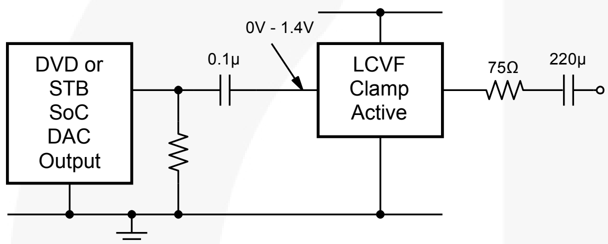


Figure 19. DC-Coupled Inputs, AC-Coupled Outputs

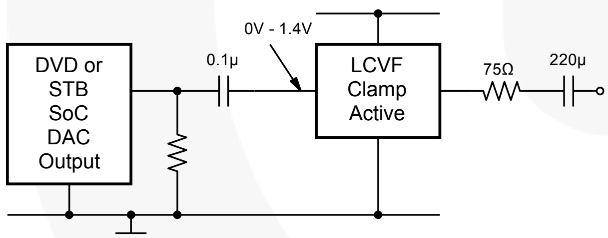


Figure 20. AC-Coupled Inputs and Outputs

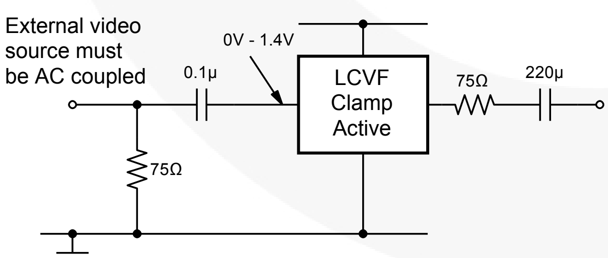


Figure 21. Biased SCART with AC-Coupled Outputs

NOTE: The video tilt or line time distortion is dominated by the AC-coupling capacitor. The value may need to be increased beyond 220µF to obtain satisfactory operation in some applications.

Power Dissipation

The output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the power dissipation and internal temperature rise.

$$T_J = T_A + P_D \bullet \theta_{JA} \quad (1)$$

where:

$$P_D = P_{CH1} + P_{CH2} + P_{CH3} \quad (2)$$

and

$$P_{CHX} = V_{CC} \bullet I_{CH} - (V_O^2/R_L) \quad (3)$$

where:

$$V_O = 2V_{IN} + 0.280V \quad (4)$$

$$I_{CH} = (I_{CC}/3) + (V_O/R_L) \quad (5)$$

V_{IN} = RMS value of input signal

I_{CC} = 19mA

V_{CC} = 3.3V.

R_L = channel load resistance

Board layout can also affect thermal characteristics. Refer to the *Layout Considerations* section for details.

The FMS6144A is specified to operate with output currents typically less than 50mA, more than sufficient for a dual (75Ω) video load. Internal amplifiers are current limited to a maximum of 100mA and should withstand brief-duration short-circuit conditions. This capability is not guaranteed.

Layout Considerations

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. Fairchild offers a four-layer board with full power and ground planes board to guide layout and aid device evaluation. The demo board is a four-layer board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For best results, follow the steps and recommended routing rules below.

Recommended Routing / Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Traces should run on top of the ground plane at all times.
- No trace should run over ground/power splits.
- Avoid routing at 90-degree angles.
- Minimize clock and video data trace length differences.
- Include 10µF and 0.1µF ceramic power supply bypass capacitors.
- Place the 0.1µF capacitor within 2.54mm (0.1in) of the device power pin.
- Place the 10µF capacitor within 19.05mm (0.75in) of the device power pin.
- For multi-layer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device body at least 12.7mm (0.5in) on all sides. Include a metal paddle under the device on the top layer.
- Minimize all trace lengths to reduce series inductance.

Output Considerations

The outputs are DC offset from the input by 150mV therefore $V_{OUT} = 2 \cdot V_{IN}$ DC + 150mV. This offset is required for optimal performance from the output driver and is held at the minimum value to decrease the standing DC current into the load. Since the FMS6144A has a 2x (6dB) gain, the output is typically connected via a 75Ω series back-matching resistor followed by the 75Ω video cable. Because of the inherent divide by two of this configuration, the blanking level at the load of the video signal is always less than 1V. When AC-coupling the output, ensure that the coupling capacitor passes the lowest frequency content in the video signal and that line time distortion (video tilt) is kept as low as possible.

The selection of the coupling capacitor is a function of the subsequent circuit input impedance and the leakage current of the input being driven. To obtain the highest quality output video signal, the series termination resistor must be placed as close to the device output pin as possible. This greatly reduces the parasitic capacitance and inductance effect on the output driver. The distance from the device pin to the series termination resistor should be no greater than 2.54mm (0.1in).

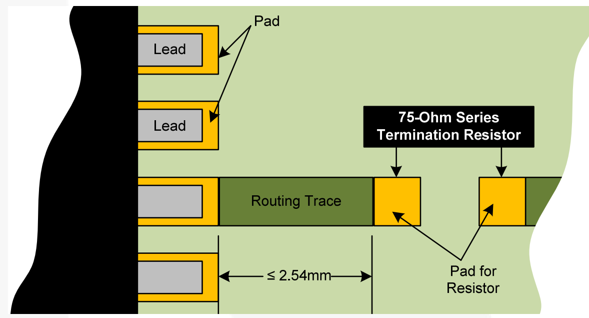


Figure 22. Termination Resistor Placement

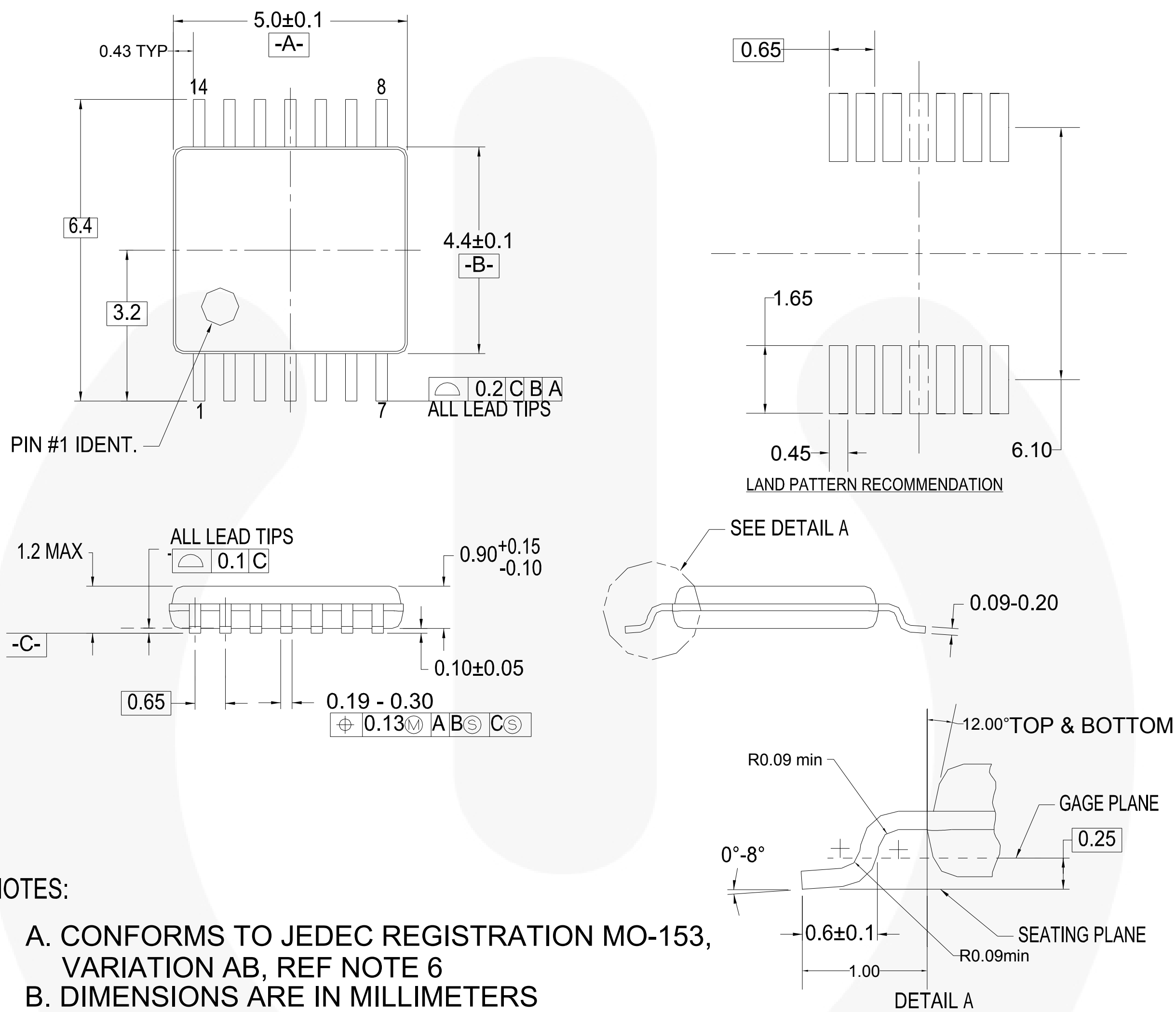
Thermal Considerations

Since the interior of most systems, such as set-top boxes, TVs, and DVD players; are at +70ºC; consideration must be given to providing an adequate heat sink for the device package for maximum heat dissipation. When designing a system board, determine how much power each device dissipates. Ensure that devices of high power are not placed in the same location, such as directly above (top plane) or below (bottom plane) each other, on the PCB.

PCB Thermal Layout Considerations

- Understand the system power requirements and environmental conditions.
- Maximize thermal performance of the PCB.
- Consider using 70µm of copper for high-power designs.
- Make the PCB as thin as possible by reducing FR4 thickness.
- Use vias in power pad to tie adjacent layers together.
- Remember that baseline temperature is a function of board area, not copper thickness.
- Modeling techniques provide a first-order approximation.

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
E. LANDPATTERN STANDARD: SOP65P640X110-14M
F. DRAWING FILE NAME: MTC14REV6

Figure 23. 14-Lead TSSOP

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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SuperSOT™-6
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TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I57

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