



**THE DATASHEET OF
SN74LV4040APWRG4**

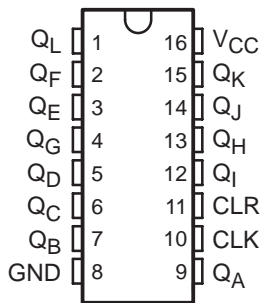


SN54LV4040A, SN74LV4040A 12-BIT ASYNCHRONOUS BINARY COUNTERS

SCES2261 – APRIL 1999 – REVISED MAY 2005

- 2-V to 5.5-V V_{CC} Operation
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

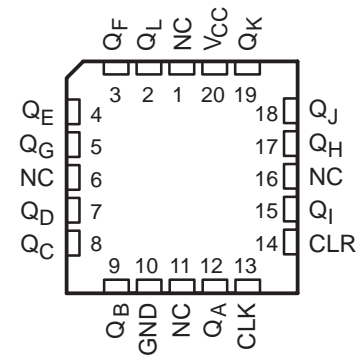
SN54LV4040A . . . J OR W PACKAGE
SN74LV4040A . . . D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LV4040A . . . RGY PACKAGE
(TOP VIEW)



SN54LV4040A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74LV4040AN	SN74LV4040AN
	QFN – RGY	Reel of 1000	SN74LV4040ARGYR	LW040A
	SOIC – D	Tube of 40	SN74LV4040AD	LV4040A
		Reel of 2500	SN74LV4040ADR	
	SOP – NS	Reel of 2000	SN74LV4040ANSR	74LV4040A
	SSOP – DB	Reel of 2000	SN74LV4040ADBR	LW040A
	TSSOP – PW	Tube of 90	SN74LV4040APW	LW040A
Reel of 2000		SN74LV4040APWR		
Reel of 250		SN74LV4040APWT		
TVSOP – DGV	Reel of 2000	SN74LV4040ADGVR	LW040A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV4040AJ	SNJ54LV4040AJ
	CFP – W	Tube of 150	SNJ54LV4040AW	SNJ54LV4040AW
	LCCC – FK	Tube of 55	SNJ54LV4040AFK	SNJ54LV4040AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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SN54LV4040A, SN74LV4040A 12-BIT ASYNCHRONOUS BINARY COUNTERS

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description/ordering information (continued)

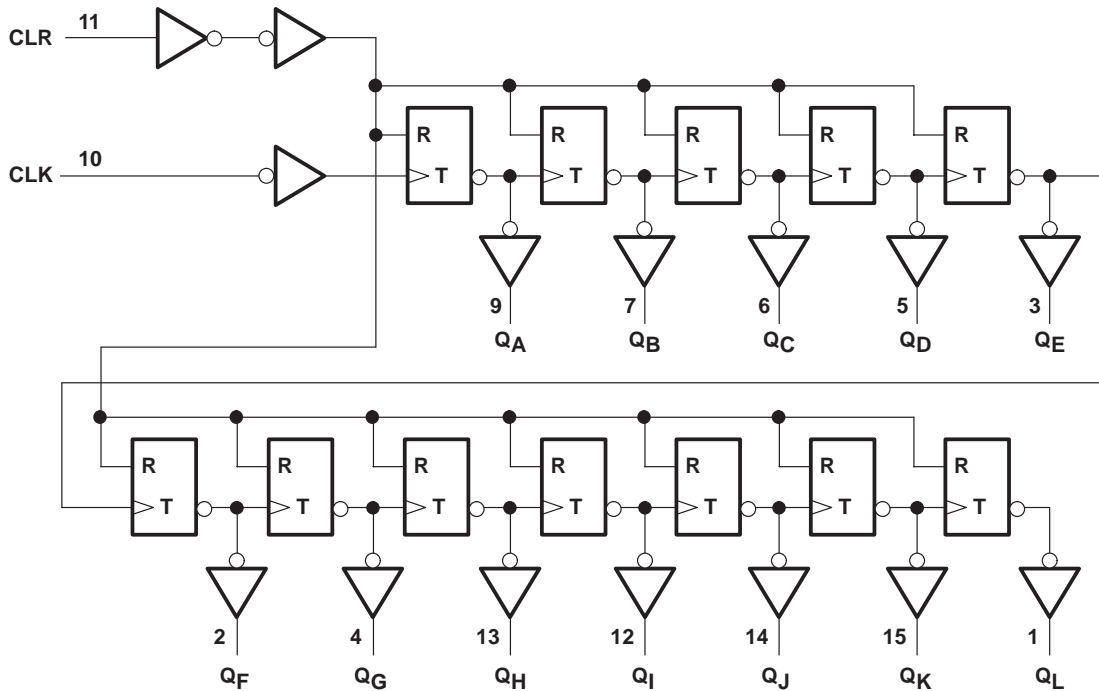
The 'LV4040A devices are 12-bit asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE
(each buffer)

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

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absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
(see Note 3): DB package	82°C/W
(see Note 3): DGV package	120°C/W
(see Note 3): N package	67°C/W
(see Note 3): NS package	64°C/W
(see Note 3): PW package	108°C/W
(see Note 4): RGY package	39°C/W
Storage temperature range, T_{Stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LV4040A, SN74LV4040A 12-BIT ASYNCHRONOUS BINARY COUNTERS

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recommended operating conditions (see Note 5)

		SN54LV4040A		SN74LV4040A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3	V _{CC} × 0.3	
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50	-50	μA
		V _{CC} = 2.3 V to 2.7 V		-2	-2	mA
		V _{CC} = 3 V to 3.6 V		-6	-6	
		V _{CC} = 4.5 V to 5.5 V		-12	-12	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	50	μA
		V _{CC} = 2.3 V to 2.7 V		2	2	mA
		V _{CC} = 3 V to 3.6 V		6	6	
		V _{CC} = 4.5 V to 5.5 V		12	12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V		200	200	ns/V
		V _{CC} = 3 V to 3.6 V		100	100	
		V _{CC} = 4.5 V to 5.5 V		20	20	
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV4040A			SN74LV4040A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} - 0.1			V _{CC} - 0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I _{OL} = 2 mA	2.3 V			0.4			0.4	
	I _{OL} = 6 mA	3 V			0.44			0.44	
	I _{OL} = 12 mA	4.5 V			0.55			0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±1			±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			20			20	μA
I _{off}	V _I or V _O = 0 to 5.5 V	0			5			5	μA
C _i	V _I = V _{CC} or GND	3.3 V		1.9			1.9		pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV4040A		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	7		7		7		ns
		CLR high	6.5		6.5		6.5		
t_{su}	Setup time	CLR inactive before CLK↓	6.5		6.5		6.5		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV4040A		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		5		ns
		CLR high	5		5		5		
t_{su}	Setup time	CLR inactive before CLK↓	5		5		5		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV4040A		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		5		ns
		CLR high	5		5		5		
t_{su}	Setup time	CLR inactive before CLK↓	5		5		5		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV4040A		SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	50*	115*		40*		40	MHz	
			$C_L = 50\text{ pF}$	40	95		35		35		
t_{PLH}	CLK	Q_A	$C_L = 15\text{ pF}$	8.7*	19.4*		1*	23*	1	23	ns
t_{PHL}				8.7*	19.4*		1*	23*	1	23	
t_{PHL}	CLR	Any Q	$C_L = 15\text{ pF}$	9.3*	19.9*		1*	24*	1	24	ns
t_{PLH}	$\overline{\text{CLK}}$	Q_A	$C_L = 50\text{ pF}$	10.5	24.1		1	28	1	28	ns
t_{PHL}				10.5	24.1		1	28	1	28	
t_{PHL}	CLR	Any Q	$C_L = 50\text{ pF}$	11.7	24.5		1	28	1	28	ns
Δt_{pd}	Q_n	Q_{n+1}	$C_L = 50\text{ pF}$		1.7	5.9		7		7	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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12-BIT ASYNCHRONOUS BINARY COUNTERS

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ C$			SN54LV4040A		SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	75*	160*		75*		75		MHz
			$C_L = 50 \text{ pF}$	55	130		50		50		
t_{PLH}	CLK	Q_A	$C_L = 15 \text{ pF}$	6.1*	11.9*		1*	14*	1	14	ns
t_{PHL}				6.1*	11.9*		1*	14*	1	14	
t_{PHL}	CLR	Any Q	$C_L = 15 \text{ pF}$	7.1*	12.8*		1*	15*	1	15	ns
t_{PLH}	$\overline{\text{CLK}}$	Q_A	$C_L = 50 \text{ pF}$	7.5	15.4		1	17.5	1	17.5	ns
t_{PHL}				7.5	15.4		1	17.5	1	17.5	
t_{PHL}	CLR	Any Q	$C_L = 50 \text{ pF}$	9	16.3		1	18.5	1	18.5	ns
Δt_{pd}	Q_n	Q_{n+1}	$C_L = 50 \text{ pF}$	1.2	4.4			5		5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ C$			SN54LV4040A		SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	150*	235*		125*		125		MHz
			$C_L = 50 \text{ pF}$	95	185		80		80		
t_{PLH}	CLK	Q_A	$C_L = 15 \text{ pF}$	4.2*	7.3*		1*	8.5*	1	8.5	ns
t_{PHL}				4.2*	7.3*		1*	8.5*	1	8.5	
t_{PHL}	CLR	Any Q	$C_L = 15 \text{ pF}$	5.3*	8.6*		1*	10*	1	10	ns
t_{PLH}	$\overline{\text{CLK}}$	Q_A	$C_L = 50 \text{ pF}$	5.3	9.3		1	10.5	1	10.5	ns
t_{PHL}				5.3	9.3		1	10.5	1	10.5	
t_{PHL}	CLR	Any Q	$C_L = 50 \text{ pF}$	6.8	10.6		1	12	1	12	ns
Δt_{pd}	Q_n	Q_{n+1}	$C_L = 50 \text{ pF}$	0.8	3.1			3.5		3.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3 V$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ C$ (see Note 6)

PARAMETER		SN74LV4040A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.5	-0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.99		V

NOTE 6: Characteristics are for surface-mount packages only.

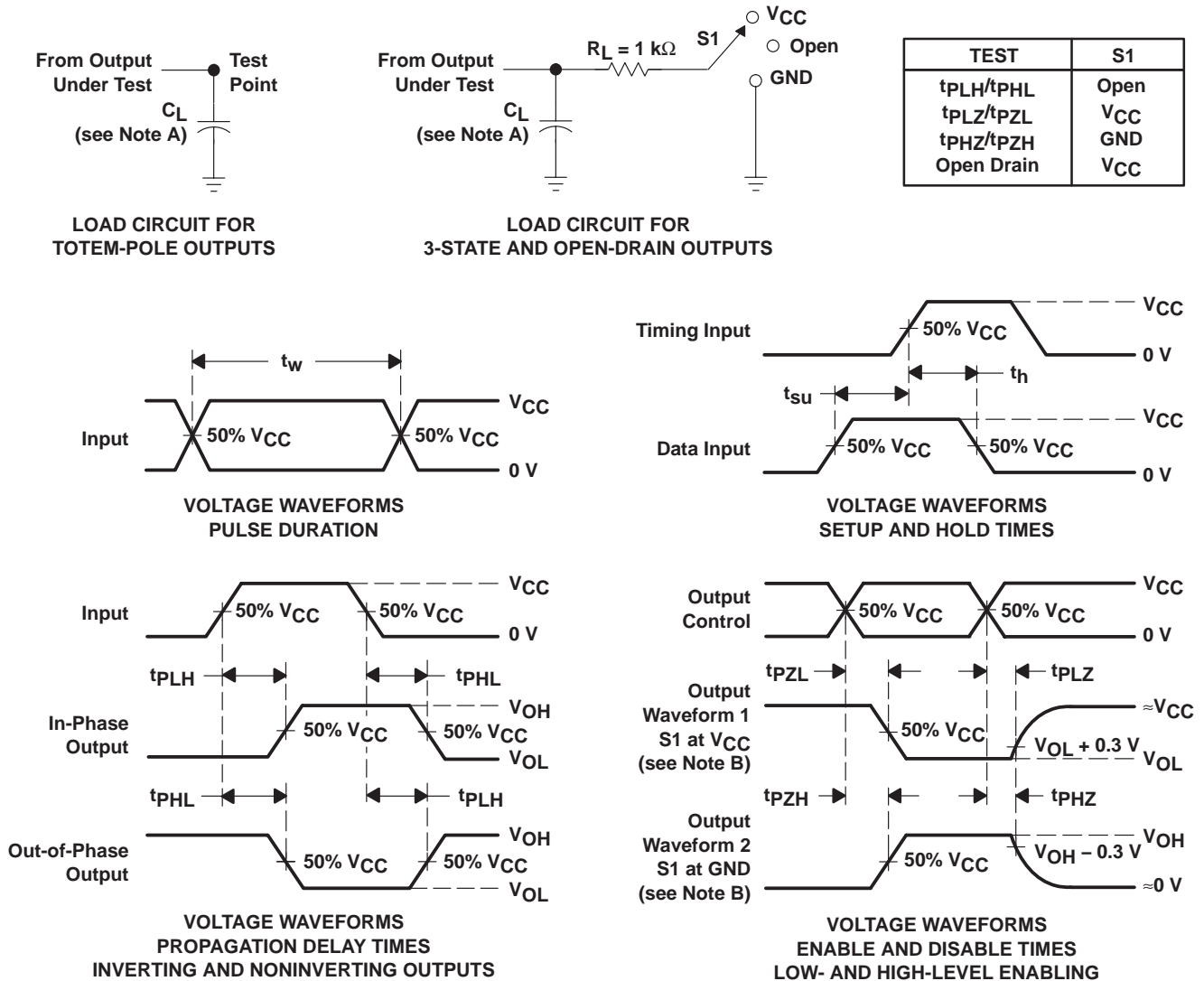
operating characteristics, $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	3.3 V	11.9	pF
			5 V	13.1	

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time, with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4040AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4040A	Samples
SN74LV4040ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A	Samples
SN74LV4040ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4040A	Samples
SN74LV4040ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A	Samples
SN74LV4040ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4040A	Samples
SN74LV4040AN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4040AN	Samples
SN74LV4040ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4040A	Samples
SN74LV4040APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A	Samples
SN74LV4040APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A	Samples
SN74LV4040APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A	Samples
SN74LV4040APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A	Samples
SN74LV4040ARGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LW040A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LV4040A :

- Enhanced Product: [SN74LV4040A-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4040ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4040ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4040ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV4040APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4040APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4040ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4040ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV4040ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV4040ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LV4040APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV4040APWT	TSSOP	PW	16	250	367.0	367.0	35.0
SN74LV4040ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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