



# THE DATASHEET OF NBSG11MNG



# NBSG11

## 2.5V/3.3V SiGe 1:2 Differential Clock Driver with RSECL\* Outputs

\*Reduced Swing ECL

### Description

The NBSG11 is a 1-to-2 differential fanout buffer, optimized for low skew and Ultra-Low JITTER.

Inputs incorporate internal 50 Ω termination resistors and accept Negative ECL (NECL), Positive ECL (PECL), CML, LVCMOS, LVTTTL, or LVDS. Outputs are Reduced Swing ECL (RSECL), 400 mV. All outputs loaded with 50 Ω to  $V_{CC} - 2\text{ V}$ .

### Features

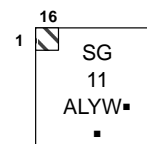
- Maximum Input Clock Frequency up to 12 GHz Typical
- Maximum Input Data Rate up to 12 Gb/s Typical
- 30 ps Typical Rise and Fall Times
- 125 ps Typical Propagation Delay
- RSPECL Output with Operating Range:  $V_{CC} = 2.375\text{ V}$  to  $3.465\text{ V}$  with  $V_{EE} = 0\text{ V}$
- RSNECL Output with RSNECL or NECL Inputs with Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -2.375\text{ V}$  to  $-3.465\text{ V}$
- RSECL Output Level (400 mV Peak-to-Peak Output), Differential Output Only
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LVEL Devices
- These are Pb-Free Devices



ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM\*



- |   |                     |
|---|---------------------|
| A | = Assembly Location |
| L | = Wafer Lot         |
| Y | = Year              |
| W | = Work Week         |
| ▪ | = Pb-Free Package   |

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

# NBSG11

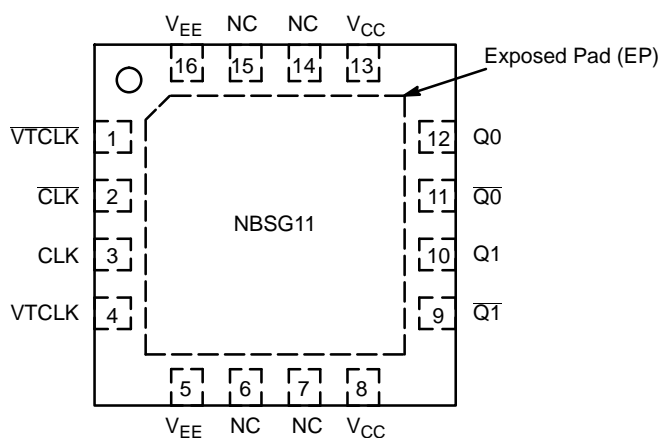


Figure 1. QFN16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	$\overline{\text{VTCLK}}$	–	Internal 50 $\Omega$ Termination Pin. See Table 2.
2	$\overline{\text{CLK}}$	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input. Internal 75 k $\Omega$ to $V_{EE}$ and 36.5 k $\Omega$ to $V_{CC}$ .
3	CLK	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input. Internal 75 k $\Omega$ to $V_{EE}$ .
4	VTCLK	–	Internal 50 $\Omega$ Termination Pin. See Table 2.
5,16	$V_{EE}$	–	Negative Supply Voltage
6,7,14,15	NC	–	No Connect
8,13	$V_{CC}$	–	Positive Supply Voltage
9	$\overline{Q1}$	RSECL Output	Inverted Differential Output 1. Typically Terminated with 50 $\Omega$ to $V_{TT} = V_{CC} - 2.0 \text{ V}$ .
10	Q1	RSECL Output	Noninverted Differential Output 1. Typically Terminated with 50 $\Omega$ to $V_{TT} = V_{CC} - 2.0 \text{ V}$ .
11	$\overline{Q0}$	RSECL Output	Inverted Differential output 0. Typically Terminated with 50 $\Omega$ to $V_{TT} = V_{CC} - 2.0 \text{ V}$ .
12	Q0	RSECL Output	Noninverted Differential Output 0. Typically Terminated with 50 $\Omega$ to $V_{TT} = V_{CC} - 2.0 \text{ V}$ .
–	EP	–	The Exposed Pad (EP) on the QFN–16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die but may be electrically and thermally connected to $V_{EE}$ on the PC board.

1. All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation. The thermally exposed pad on package bottom (see case drawing) must be attached to a heat-sinking conduit.
2. In the differential configuration when the input termination pins ( $\overline{\text{VTCLK}}$ ,  $\overline{\text{VTCLK}}$ ) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.

# NBSG11

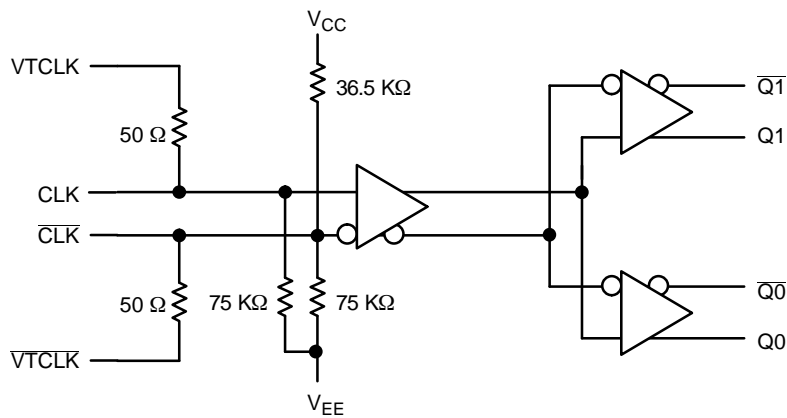


Figure 2. Logic Diagram

Table 2. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK and V̄TCLK to V <sub>CC</sub>
LVDS	Connect VTCLK and V̄TCLK together
AC-COUPLED	Bias VTCLK and V̄TCLK Inputs within (VIHCMR) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTTL, LVCMOS	An external voltage should be applied to the unused complementary differential input. Nominal voltage is 1.5 V for LVTTTL and V <sub>CC</sub> /2 for LVCMOS inputs.

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor (CLK, C̄LK)	75 kΩ
Internal Input Pullup Resistor (C̄LK)	36.5 kΩ
ESD Protection	Human Body Model Machine Model > 2 kV > 100 V
Moisture Sensitivity (Note 3)	Pb-Free Level 1
Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in
Transistor Count	125
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

3. For additional information, see Application Note AND8003/D.

# NBSG11

**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	Positive Power Supply	$V_{EE} = 0\text{ V}$		3.6	V
$V_{EE}$	Negative Power Supply	$V_{CC} = 0\text{ V}$		-3.6	V
$V_I$	Positive Input Negative Input	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	3.6 -3.6	V V
$V_{INPP}$	Differential Input Voltage $ D - \bar{D} $	$V_{CC} - V_{EE} \geq 2.8\text{ V}$ $V_{CC} - V_{EE} < 2.8\text{ V}$		2.8 $ V_{CC} - V_{EE} $	V V
$I_{out}$	Output Current	Continuous Surge		25 50	mA mA
$T_A$	Operating Temperature Range			-40 to +85	°C
$T_{stg}$	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) (Note 4)	0 lfpm 500 lfpm		41.6 35.2	°C/W °C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	2S2P (Note 4)		4.0	°C/W
$T_{sol}$	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

# NBSG11

**Table 5. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT**  $V_{CC} = 2.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	

## POWER SUPPLY CURRENT

$I_{EE}$	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
----------	-------------------------------	----	----	----	----	----	----	----	----	----	----

## RSPECL OUTPUTS (Note 6)

$V_{OH}$	Output HIGH Voltage	1450	1530	1575	1525	1565	1600	1550	1590	1625	mV
$V_{OUTPP}$	Output Voltage Amplitude	350	410	525	350	410	525	350	410	525	mV

## DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 4 & 6) (Note 7)

$V_{IH}$	Input HIGH Voltage	1200		$V_{CC}$	1200		$V_{CC}$	1200		$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage	0		$V_{IH} - 150$	0		$V_{IH} - 150$	0		$V_{IH} - 150$	mV
$V_{th}$	Input Threshold Reference Voltage Range (Note 8)	950		$V_{CC} - 75$	950		$V_{CC} - 75$	950		$V_{CC} - 75$	mV
$V_{ISE}$	Single-Ended Input Voltage ( $V_{IH} - V_{IL}$ )	150		2600	150		2600	150		260	mV

## DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 5 & 7) (Note 9)

$V_{IHD}$	Differential Input HIGH Voltage	1200		$V_{CC}$	1200		$V_{CC}$	1200		$V_{CC}$	mV
$V_{ILD}$	Differential Input LOW Voltage	0		$V_{CC} - 75$	0		$V_{CC} - 75$	0		$V_{CC} - 75$	mV
$V_{ID}$	Differential Input Voltage ( $V_{IHD} - V_{ILD}$ )	75		2600	75		2600	75		2600	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Note 10) (Figure 8)	1200		2500	1200		2500	1200		2500	mV
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ )		80	150		80	150		80	150	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ )		25	100		25	100		25	100	$\mu\text{A}$

## TERMINATION RESISTORS

$R_{TIN}$	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	$\Omega$
-----------	-------------------------------------	----	----	----	----	----	----	----	----	----	----------

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .
- All loading with  $50\ \Omega$  to  $V_{CC} - 2\text{ V}$ .
- $V_{th}$ ,  $V_{IH}$ ,  $V_{IL}$ , and  $V_{ISE}$  parameters must be complied with simultaneously.
- $V_{th}$  is applied to the complementary input when operating in single-ended mode.  $V_{th} = (V_{IH} - V_{IL}) / 2$ .
- $V_{IHD}$ ,  $V_{ILD}$ ,  $V_{ID}$  and  $V_{IHCMR}$  parameters must be complied with simultaneously.
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# NBSG11

**Table 6. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 11)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>POWER SUPPLY CURRENT</b>											
$I_{EE}$	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
<b>RSPECL OUTPUTS</b> (Note 12)											
$V_{OH}$	Output HIGH Voltage	2250	2330	2375	2325	2365	2400	2350	2390	2425	mV
$V_{OUTPP}$	Output Voltage Amplitude	350	410	525	350	410	525	350	410	525	mV
<b>DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED</b> (Figures 4 & 6) (Note 13)											
$V_{IH}$	Input HIGH Voltage	1200		$V_{CC}$	1200		$V_{CC}$	1200		$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage	0		$V_{IH} - 150$	0		$V_{IH} - 150$	0		$V_{IH} - 150$	mV
$V_{th}$	Input Threshold Reference Voltage Range (Note 14)	950		$V_{CC} - 75$	950		$V_{CC} - 75$	950		$V_{CC} - 75$	mV
$V_{ISE}$	Single-Ended Input Voltage ( $V_{IH} - V_{IL}$ )	150		2600	150		2600	150		260	mV
<b>DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY</b> (Figures 5 & 7) (Note 15)											
$V_{IHD}$	Differential Input HIGH Voltage	1200		$V_{CC}$	1200		$V_{CC}$	1200		$V_{CC}$	mV
$V_{ILD}$	Differential Input LOW Voltage	0		$V_{CC} - 75$	0		$V_{CC} - 75$	0		$V_{CC} - 75$	mV
$V_{ID}$	Differential Input Voltage ( $V_{IHD} - V_{ILD}$ )	75		2600	75		2600	75		2600	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Note 16) (Figure 8)	1200		3300	1200		3300	1200		3300	mV
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ )		80	150		80	150		80	150	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ )		25	100		25	100		25	100	$\mu\text{A}$
<b>TERMINATION RESISTORS</b>											
$R_{TIN}$	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	$\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Input and output parameters vary 1:1 with  $V_{CC}$ .

12. All loading with  $50\ \Omega$  to  $V_{CC} - 2\text{ V}$ .

13.  $V_{th}$ ,  $V_{IH}$ ,  $V_{IL}$ , and  $V_{ISE}$  parameters must be complied with simultaneously.

14.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.  $V_{th} = (V_{IH} - V_{IL}) / 2$ .

15.  $V_{IHD}$ ,  $V_{ILD}$ ,  $V_{ID}$  and  $V_{IHCMR}$  parameters must be complied with simultaneously.

16.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# NBSG11

**Table 7. DC CHARACTERISTICS, NECL or RSNECL INPUT WITH NECL OUTPUT**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V}$  to  $-2.375\text{ V}$   
(Note 17)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>POWER SUPPLY CURRENT</b>											
$I_{EE}$	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
<b>RSPECL OUTPUTS (Note 18)</b>											
$V_{OH}$	Output HIGH Voltage	-1050	-970	-925	-975	-935	-900	-950	-910	-875	mV
$V_{OUTPP}$	Output Voltage Amplitude	350	410	525	350	410	525	350	410	525	mV
<b>DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 4 &amp; 6) (Note 19)</b>											
$V_{IH}$	Input HIGH Voltage	$V_{EE} + 1200$		$V_{CC}$	$V_{EE} + 1200$		$V_{CC}$	$V_{EE} + 1200$		$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage	$V_{EE}$		$V_{IH} - 150$	$V_{EE}$		$V_{IH} - 150$	$V_{EE}$		$V_{IH} - 150$	mV
$V_{th}$	Input Threshold Reference Voltage Range (Note 20)	$V_{EE} + 950$		$V_{CC} - 75$	$V_{EE} + 950$		$V_{CC} - 75$	$V_{EE} + 950$		$V_{CC} - 75$	mV
$V_{ISE}$	Single-Ended Input Voltage ( $V_{IH} - V_{IL}$ )	150		2600	150		2600	150		260	mV
<b>DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 5 &amp; 7) (Note 21)</b>											
$V_{IHD}$	Differential Input HIGH Voltage	$V_{EE} + 1200$		$V_{CC}$	$V_{EE} + 1200$		$V_{CC}$	$V_{EE} + 1200$		$V_{CC}$	mV
$V_{ILD}$	Differential Input LOW Voltage	$V_{EE}$		$V_{CC} - 75$	$V_{EE}$		$V_{CC} - 75$	$V_{EE}$		$V_{CC} - 75$	mV
$V_{ID}$	Differential Input Voltage ( $V_{IHD} - V_{ILD}$ )	75		2600	75		2600	75		2600	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Note 22) (Figure 8)	$V_{EE} + 1200$		0	$V_{EE} + 1200$		0	$V_{EE} + 1200$		0	mV
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ )		80	150		80	150		80	150	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ )		25	100		25	100		25	100	$\mu\text{A}$
<b>TERMINATION RESISTORS</b>											
$R_{TIN}$	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	$\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

17. Input and output parameters vary 1:1 with  $V_{CC}$ .

18. All loading with  $50\ \Omega$  to  $V_{CC} - 2\text{ V}$ .

19.  $V_{th}$ ,  $V_{IH}$ ,  $V_{IL}$ , and  $V_{ISE}$  parameters must be complied with simultaneously.

20.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.  $V_{th} = (V_{IH} - V_{IL}) / 2$ .

21.  $V_{IHD}$ ,  $V_{ILD}$ ,  $V_{ID}$  and  $V_{IHCMR}$  parameters must be complied with simultaneously.

22.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# NBSG11

**Table 8. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V}$  to  $-2.375\text{ V}$  or  $V_{CC} = 2.375\text{ V}$  to  $3.465\text{ V}$ ;  $V_{EE} = 0\text{ V}$

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Input Clock Frequency (See Figure 3. $F_{max}/JITTER$ ) (Note 23)	10.5	12		10.5	12		10.5	12		GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential	90	125	160	90	125	160	90	125	160	ps
$t_{SKEW}$	Duty Cycle Skew (Note 24) Within-Device Skew (Note 25) Device-to-Device Skew (Note 26)		3 6 25	15 15 50		3 6 25	15 15 50		3 6 25	15 15 50	ps
$t_{JITTER}$	RMS Random Clock Jitter $f_{in} < 10\text{ GHz}$ Peak-to-Peak Data Dependent Jitter $f_{in} < 10\text{ Gb/s}$		0.2 10.7	1		0.2 10.7	1		0.2 10.7	1	ps
$V_{INPP}$	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 27)	75		2600	75		2600	75		2600	mV
$t_r$ , $t_f$	Output Rise/Fall Times (20% – 80%) @ 1 GHz	15	30	55	20	30	55	20	30	55	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

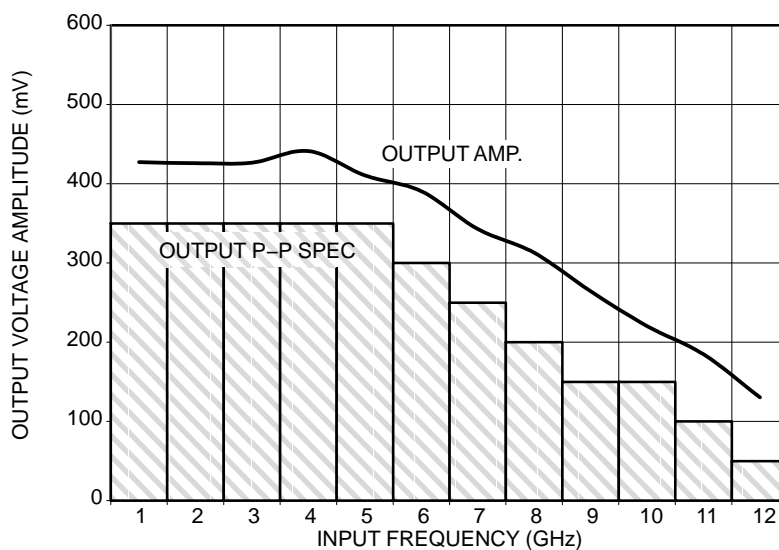
23. Measured using a 500 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$  for QFN package. For minimum  $f_{max}$  value of 10.5 GHz, output amplitude is approximately 200 mV (as shown in Figure 3, where output P-P spec is shown as a minimum/guarantee of around 150 mV). Input edge rates 40 ps (20% – 80%).

24. See Figure 9.  $t_{SKEW} = |t_{PLH} - t_{PHL}|$  for a nominal 50% Differential Clock Input Waveform.

25. Within-Device skew is defined as identical transitions on similar paths through a device.

26. Device-to-device skew for identical transitions at identical  $V_{CC}$  levels.

27.  $V_{INPP}$  (MAX) cannot exceed  $V_{CC} - V_{EE}$ .



**Figure 3. Output Amplitude ( $V_{OUTPP}$ ) vs. Input Frequency ( $F_{IN}$ ) at Ambient Temperature (Typical)**

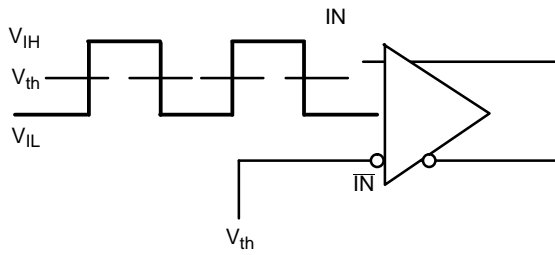


Figure 4. Differential Input Driven Single-Ended

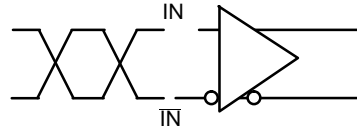


Figure 5. Differential Inputs Driven Differentially

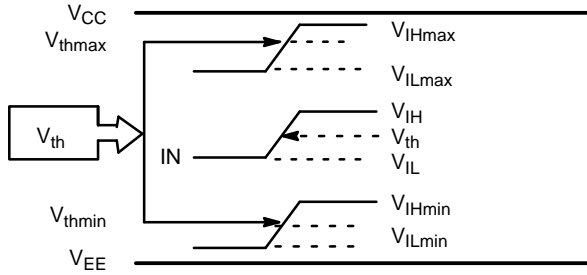


Figure 6.  $V_{th}$  Diagram

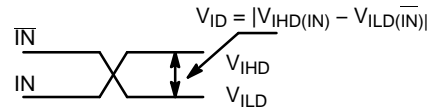


Figure 7. Differential Inputs Driven Differentially

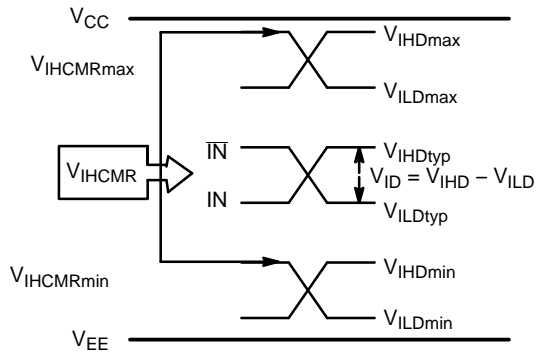
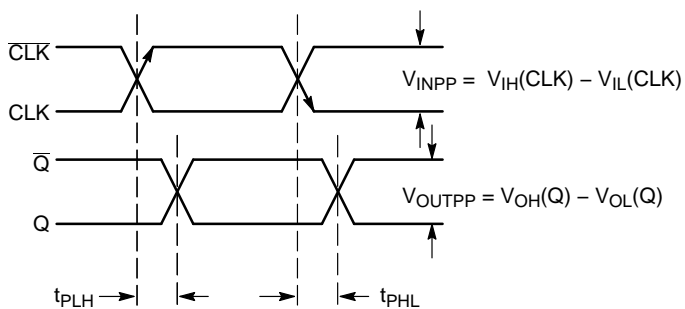
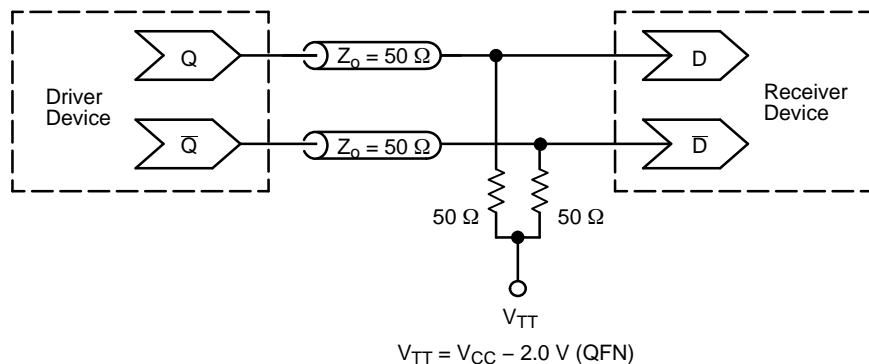


Figure 8.  $V_{IHCMR}$  Diagram

# NBSG11



**Figure 9. AC Reference Measurement**



**Figure 10. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)**

## ORDERING INFORMATION

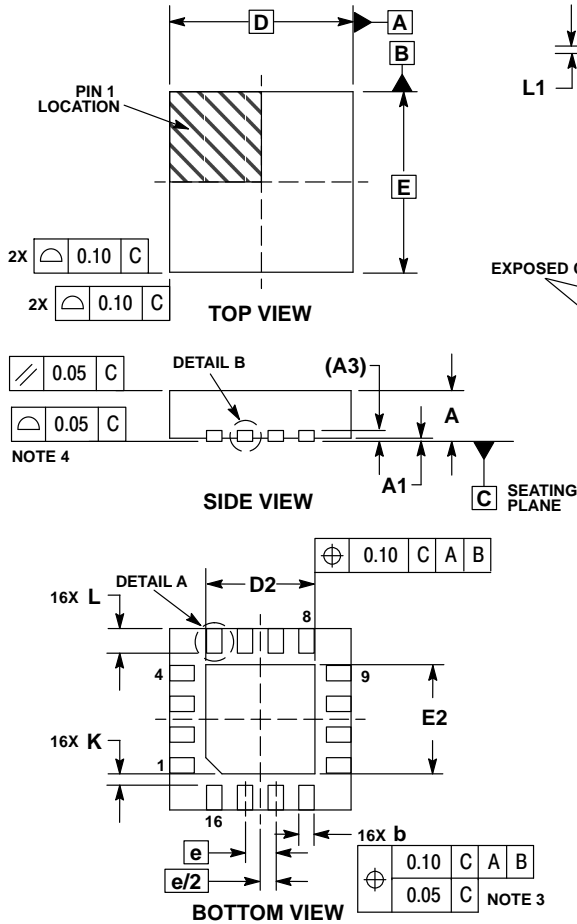
Device	Package	Shipping†
NBSG11MNG	QFN16 (Pb-Free / Halide-Free)	123 Units / Tube
NBSG11MNR2G	QFN16 (Pb-Free / Halide-Free)	3000 / Tape & Reel
NBSG11MNHTBG	QFN16 (Pb-Free / Halide-Free)	100 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NBSG11

## PACKAGE DIMENSIONS

QFN16 3x3, 0.5P  
CASE 485G  
ISSUE F



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
K	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View NBSG11MNG](#) on WIN SOURCE

 [ON Semiconductor](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management