THE DATASHEET OF

EN2340QI

EN2340QI 4A PowerSoC

Step-Down DC-DC Switching Converter with Integrated Inductor

DESCRIPTION

The EN2340QI is a Power System on a Chip (PowerSoC) DC-DC converter. It integrates MOSFET switches, small-signal control circuits, compensation and an integrated inductor in an advanced 8x11x3mm QFN module. It offers high efficiency, excellent line and load regulation over temperature and up to the full 4A load range. The EN2340QI operates over a wide input voltage range and is specifically designed to meet the precise voltage and fast transient requirements of high-performance products. The EN2340QI features frequency synchronization to an external clock, power OK output voltage monitor, programmable soft-start along with thermal and over current protection. The device's advanced circuit design, ultra high switching frequency, integrated inductor technology delivers high-quality, and non-isolated DC-DC conversion.

Intel Enpirion Power Solutions significantly help in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, overall system level reliability is improved given the small number of components required with Intel Enpirion solution.

All Enpirion products are RoHS compliant, halogen free and are compatible with lead-free manufacturing environments.

FEATURES

- Integrated Inductor, MOSFETs, Controller
- Wide Input Voltage Range: 4.5V – 14V
- Guaranteed 4A I_{OUT} at 85°C with No Airflow
- Frequency Synchronization (External Clock)
- 1% Initial V_{OUT} Accuracy
- High Efficiency (Up to 95%)
- Output Enable Pin and Power OK signal
- Programmable Soft-Start Time
- Pin Compatible with the EN2342QI
- Under Voltage Lockout Protection (UVLO)
- Programmable Over Current Protection
- Thermal Shutdown and Short Circuit Protection
- RoHS Compliant, MSL Level 3, 260°C Reflow

APPLICATIONS

- Space Constrained Applications
- Distributed Power Architectures
- Output Voltage Ripple Sensitive Applications
- Beat Frequency Sensitive Applications
- Servers, Embedded Computing Systems, LAN/SAN Adapter Cards, RAID Storage Systems, Industrial Automation, Test and Measurement, and Telecommunications

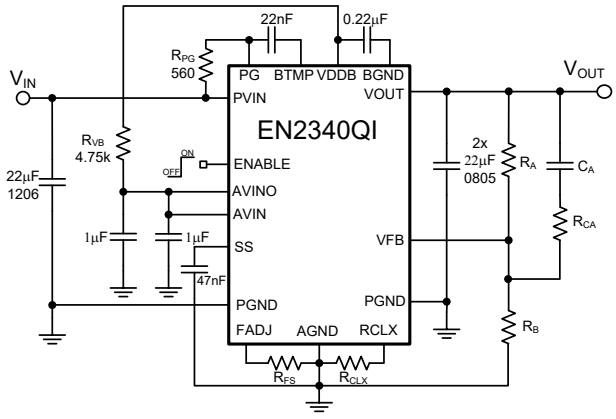


Figure 1. Simplified Application Circuit (Footprint Optimized)

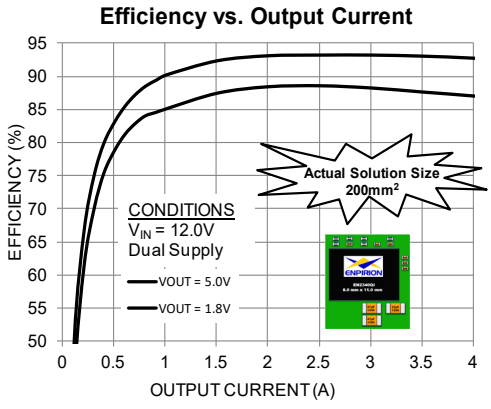


Figure 2. Highest Efficiency in Smallest Solution Size

ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
EN2340QI	EN2340QI	-40°C to +125°C	68-pin (8mm x 11mm x 3mm) QFN T&R
EN2340QI-E	EN2340QI	QFN Evaluation Board	

Packing and Marking Information: https://www.inel.com/support/quality-and-reliability/packing.html

PIN FUNCTIONS

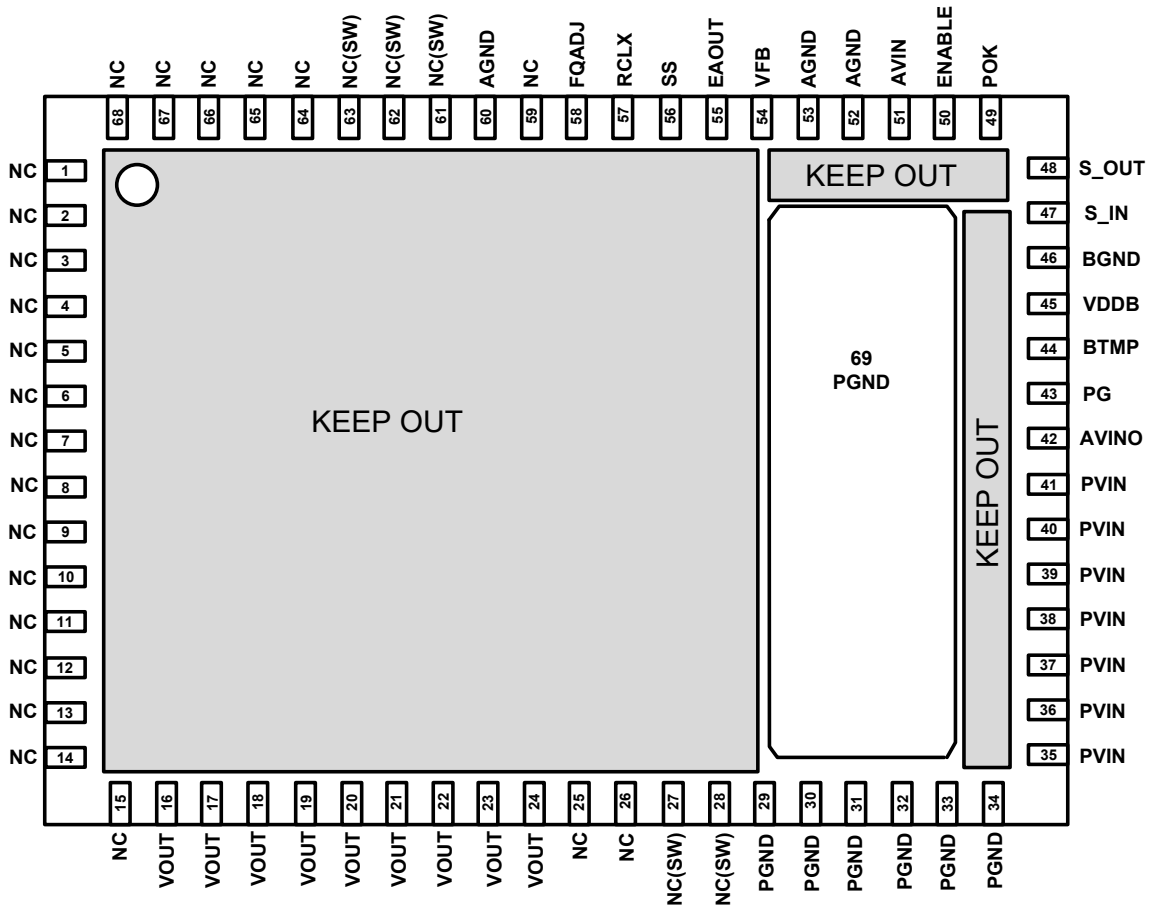


Figure 3. Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. All pins including NC pins must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: Shaded area highlights exposed metal below the package that is not to be mechanically or electrically connected to the PCB. Refer to Figure 15 for details.

NOTE C: White 'dot' on top left is pin 1 indicator on top of the device package.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1-15, 25-26, 59, 64-68	NC	-	NO CONNECT – These pins may be internally connected. Do not connect them to each other or to any other electrical signal. Failure to follow this guideline may result in device damage.
16-24	VOUT	Power	Regulated converter output. Connect these pins to the load and place output capacitor between these pins and PGND pins 29-34.
27-28, 61-63	NC(SW)	-	NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. They are not to be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in damage to the device.
29-34	PGND	Ground	Input/output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
35-41	PVIN	Power	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pins 29-34.
42	AVINO	Power	Internal 3.3V linear regulator output. Connect this pin to AVIN (Pin 51) for applications where operation from a single input voltage (PVIN) is required. If AVINO is being used, place a 1µF, X5R/X7R, capacitor between AVINO and AGND as close as possible to AVINO.
43	PG	Analog	PMOS gate. Place a 22nF, X5R/X7R, capacitor between this pin and BTMP. A 560Ω may be used between PVIN and PG to reduce noise inside the controller in extreme ambient conditions.
44	BTMP	Analog	Bottom plate ground. See pin 43 description.
45	VDDB	Power	Internal regulated voltage used for the internal control circuitry. Place a 0.22µF, X5R/X7R, capacitor between this pin and BGND.
46	BGND	Ground	Ground for VDDB. See pin 45 description.
47	S_IN	Digital	Digital synchronization input. This pin accepts either an input clock to phase lock the internal switching frequency or a S_OUT signal from another EN2340QI. Leave this pin floating if not used.
48	S_OUT	Digital	Digital synchronization output. PWM signal is output on this pin. Leave this pin floating if not used.
49	POK	Digital	Power OK is an open drain transistor (pulled up to AVIN or similar voltage) used for power system state indication. POK is logic high when VOUT is within -10% of VOUT nominal. Leave this pin floating if not used.
50	ENABLE	Analog	Output enable. Applying a logic high to this pin enables the output and initiates a soft-start. Applying a logic low disables the output. ENABLE logic cannot be higher than AVIN (refer to Absolute Maximum Ratings). Do not leave floating. See Power Up/Down Sequencing section for details.

PIN	NAME	TYPE	FUNCTION
51	AVIN	Power	3.3V Input power supply for the controller. Place a 1µF, X5R/X7R, capacitor between AVIN and AGND.
52, 53, 60	AGND	Ground	Analog ground. This is the ground return for the controller. All AGND pins need to be connected to a quiet ground.
54	VFB	Analog	External feedback input. The feedback loop is closed through this pin. A voltage divider at VOUT is used to set the output voltage. The mid-point of the divider is connected to VFB. A phase lead network from this pin to VOUT is also required to stabilize the loop.
55	EAOUT	Analog	Optional error amplifier output. Allows for customization of the control loop.
56	SS	Analog	Soft-start node. The soft-start capacitor is connected between this pin and AGND. The value of this capacitor determines the startup time.
57	RCLX	Analog	Programmble over-current protection. Placement of a resistor on this pin will adjust the over-current protection threshold. See Table 2 for the recommended RCLX Value to set OCP at the nominal value specified in the Electrical Characteristics table. No current limit protection when this pin is left floating.
58	FQADJ	Analog	Adding a resistor (R_{FS}) to this pin will adjust the switching frequency of the EN2340QI. See Table 1 for suggested resistor values on R_{FS} for various PVIN/VOUT combinations to maximize efficiency. Do not leave floating.
69	PGND	Ground	Not a perimeter pin. Device thermal pad to be connected to the system GND plane for heat-sinking purposes.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
PVIN, VOUT, PG		-0.5	15	V
ENABLE, POK		-0.3	AV_{IN}+0.3	V
Dual Supply PVIN Rising and Falling Slew Rate (1)		0.3	25	V/ms
Single Supply PVIN Rising and Falling Slew Rate (1)		0.3	6	V/ms
Pin Voltages – AVINO, AVIN, S_IN, S_OUT		2.5	6.0	V
Pin Voltages – VFB, SS, EAOUT, RCLX, FQADJ, VDDB, BTMP		-0.5	2.75	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V
CDM (Charged Device Model)		±500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	PV_{IN}	4.5	14	V
AVIN: Controller Supply Voltage	AVIN	2.5	5.5	V
Output Voltage Range (2)	V_{OUT}	0.75	5	V
Output Current Range	I_{OUT}		4	A
Operating Ambient Temperature Range	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	160	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	35	°C
Thermal Resistance: Junction to Ambient (0 LFM) (3)	θ_{JA}	18	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	2	°C/W

(1) PVIN rising and falling slew rates cannot be outside of specification. For accurate power up sequencing, use a fast ENABLE logic after both AVIN and PVIN is high.

(2) Maximum $V_{OUT} \leq V_{IN}$ - 2.5V.

(3) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: V_{IN} = 12V, Minimum and Maximum values are over operating ambient temperature range (-40°C ≤ T_A ≤ +85°C) unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	PV_{IN}		4.5		14.0	V
Controller Input Voltage	AVIN		2.5		5.5	V
AVIN Under Voltage Lock-Out Rising	$AVIN_{UVLOR}$	Voltage above which UVLO is not asserted	1.7	2.2	2.4	V
AVIN Under Voltage Lock-Out Falling	$AVIN_{OVLOF}$	Voltage below which UVLO is asserted	1.7	2.1	2.3	V
AVIN pin Input Current	I_{AVIN}			7		mA
Internal Linear Regulator Output	AVINO			3.3		V
Shut-Down Supply Current	$IPVIN_S$	PVIN=12V, AVIN=3.3V, ENABLE=0V		500		µA
	$IAVIN_S$	PVIN=12V, AVIN=3.3V, ENABLE=0V		100		µA
Feedback Pin Voltage	V_{FB}	VIN = 12V, I_{LOAD} = 0, TA = 25°C Only	0.7425	0.750	0.7575	V
Feedback Pin Voltage	V_{FB}	4.5V ≤ VIN ≤ 14V; 0A ≤ I_{LOAD} ≤ 4A	0.735	0.750	0.765	V
Feedback Pin Input Leakage Current	I_{FB}	VFB pin input leakage current[4]	-5		5	nA
V_{OUT} Rise Time	t_{RISE}	C_{SS} = 47nF [5] [6]		3.2		ms
Soft-Start Capacitor Range	C_{SS_RANGE}		10	47	68	nF
Continuous Output Current	I_{OUT_CONT}		0		4	A
Over Current Trip Level	I_{OCP}	Reference Table 2		6		A
Disable Threshold	$V_{DISABLE}$	ENABLE pin logic Low	0.0		0.95	V
ENABLE Threshold	V_{ENABLE}	ENABLE pin logic High	1.25		AVIN	V
ENABLE Lockout Time	$T_{ENLOCKOUT}$			8		ms
ENABLE Input Current	I_{ENABLE}	370k internal pull-down [4]		4		µA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency	F_{SW}	R_{FS} =3kΩ		1.0		MHz
External SYNC Clock Frequency Lock Range	F_{PLL_LOCK}	Range of SYNC clock frequency (See Table 1)	0.8		1.8	MHz
S_IN Threshold – Low	$V_{S\_IN\_LO}$	S_IN clock logic low level (4)			0.8	V
S_IN Threshold – High	$V_{S\_IN\_HI}$	S_IN clock logic high level (4)	1.8		2.5	V
S_OUT Threshold – Low	$V_{S\_OUT\_LO}$	S_OUT clock logic low level (4)			0.8	V
S_OUT Threshold – High	$V_{S\_OUT\_HI}$	S_OUT clock logic high level (4)	1.8		2.5	V
POK Lower Threshold	POK_{LT}	V_{OUT} / V_{OUT_NOM}		90		%
POK Output low Voltage	V_{POKL}	With 4mA current sink into POK			0.4	V
POK Output Hi Voltage	V_{POKH}	PVIN range: 4.5V ≤ V_{IN} ≤ 14V			AVIN	V
POK V_{OH} Leakage Current	I_{POKL}	POK High (4)			1	µA

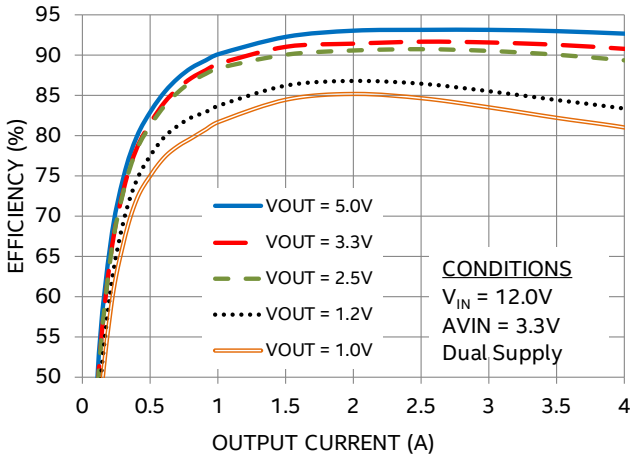
(4) Parameter not production tested but is guaranteed by design.

(5) Rise time calculation begins when AVIN > V_{UVLO} and ENABLE = HIGH.

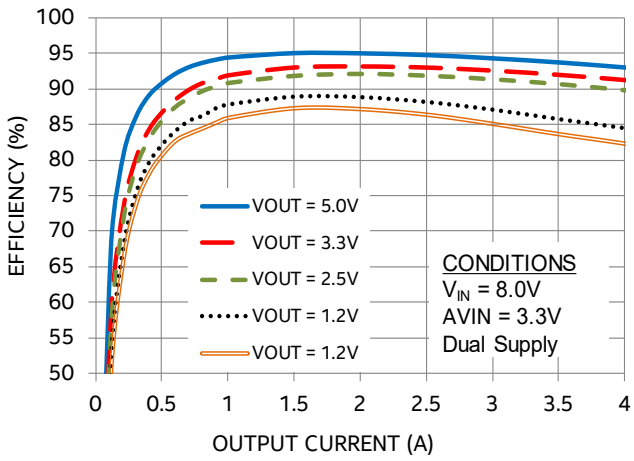
(6) V_{OUT} Rise Time Accuracy does not include soft-start capacitor tolerance.

TYPICAL PERFORMANCE CURVES

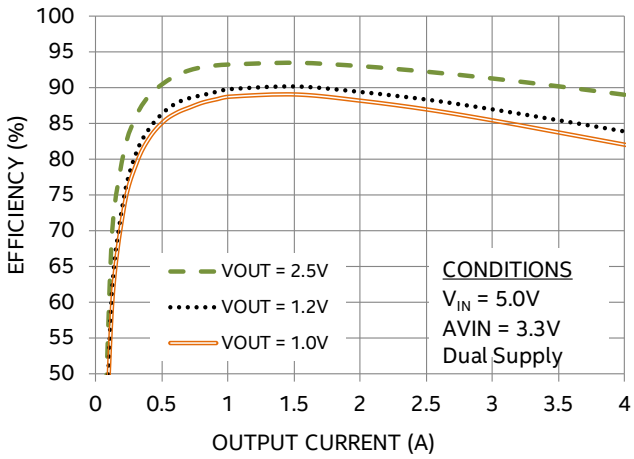
Efficiency vs. Output Current



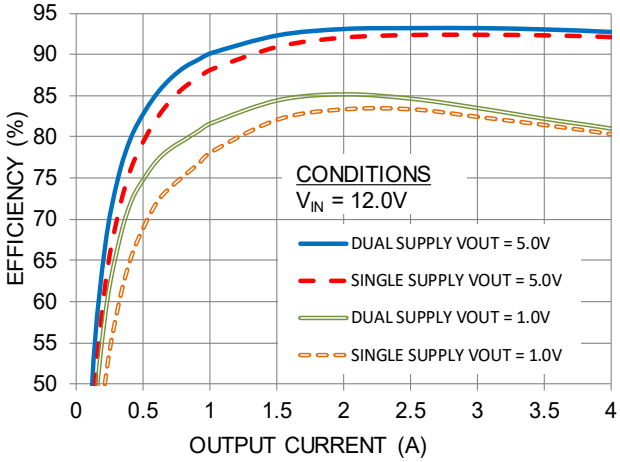
Efficiency vs. Output Current



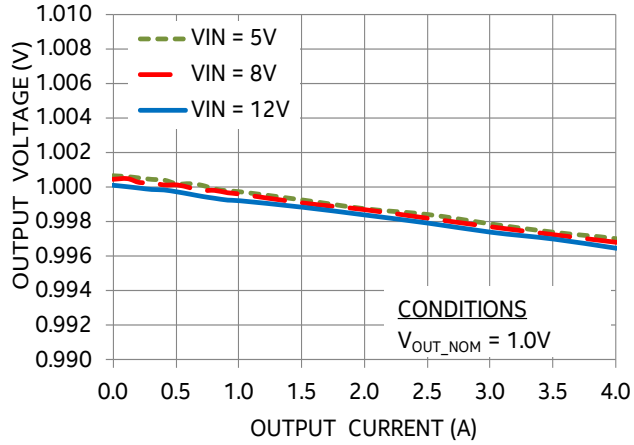
Efficiency vs. Output Current



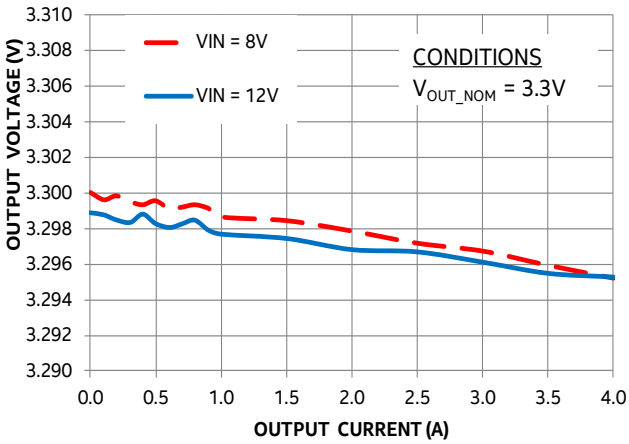
Efficiency vs. Output Current



Output Voltage vs. Output Current

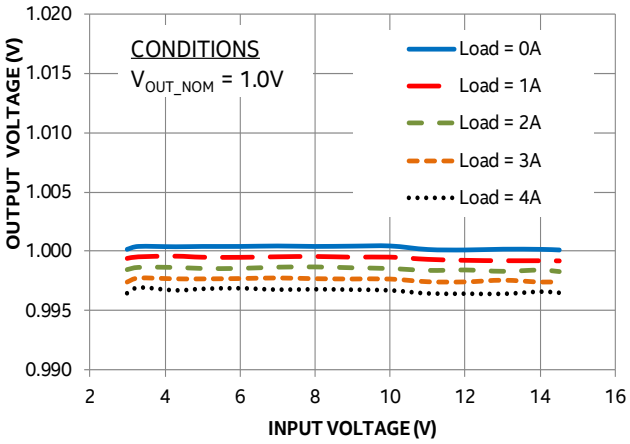


Output Voltage vs. Output Current

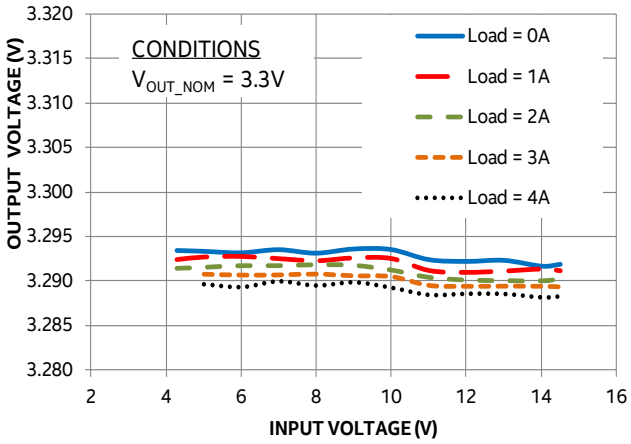


TYPICAL PERFORMANCE CURVES (CONTINUED)

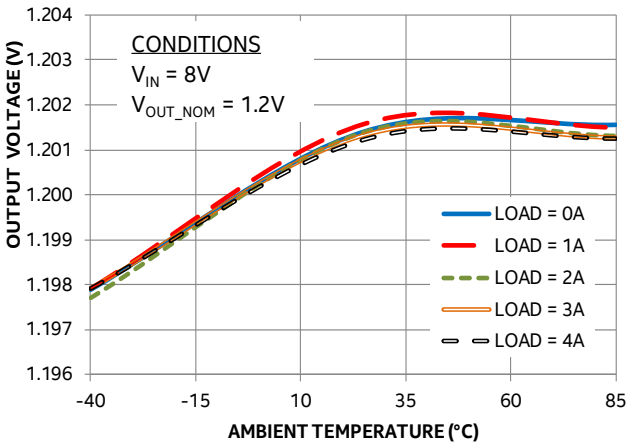
Output Voltage vs. Input Voltage



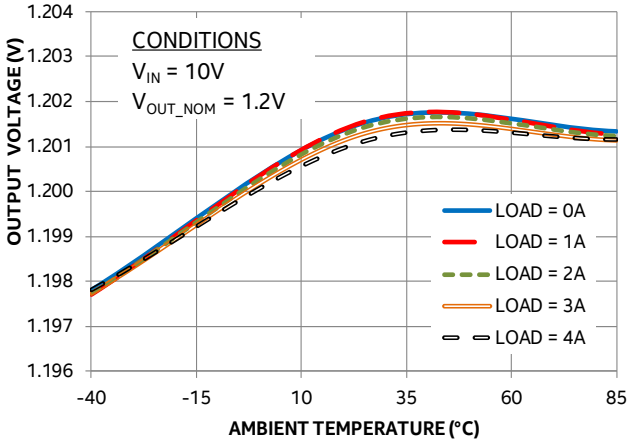
Output Voltage vs. Input Voltage



Output Voltage vs. Temperature



Output Voltage vs. Temperature



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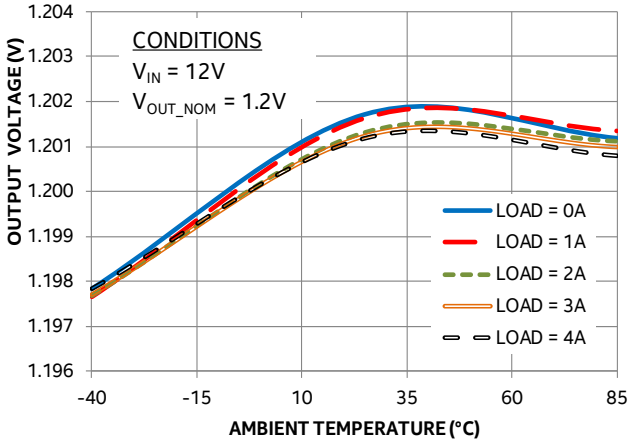
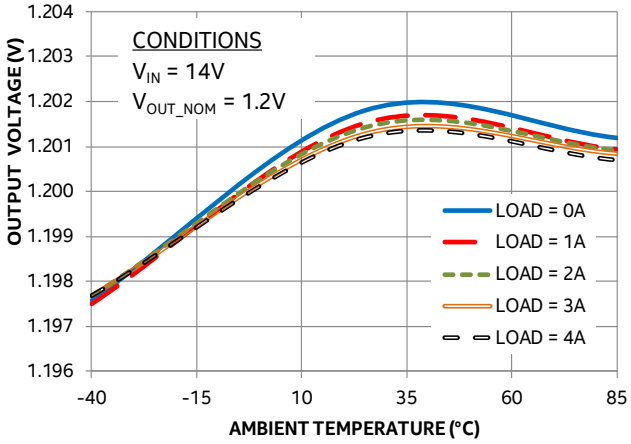
Output Voltage vs. Temperature

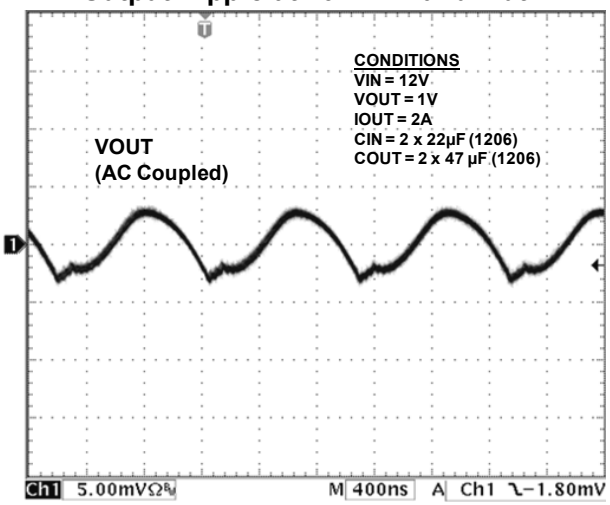


Output Voltage vs. Temperature

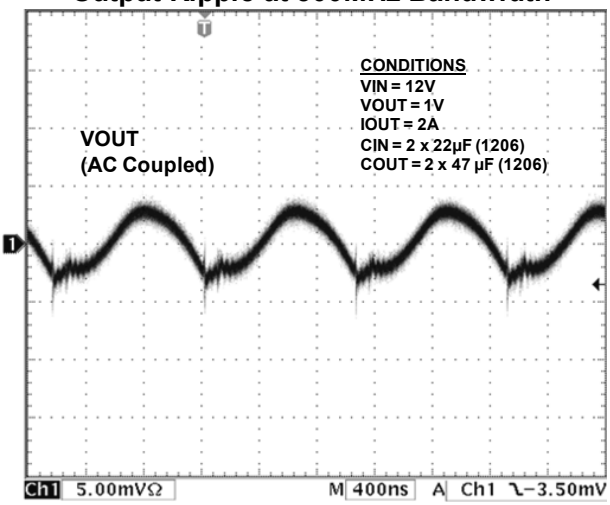


TYPICAL PERFORMACE CHARACTERISTICS

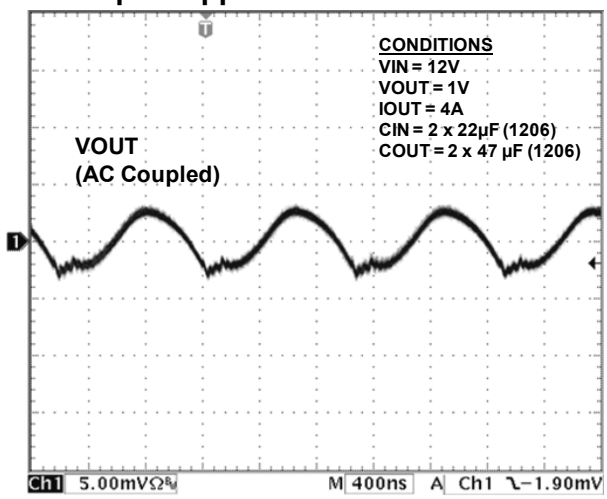
Output Ripple at 20MHz Bandwidth



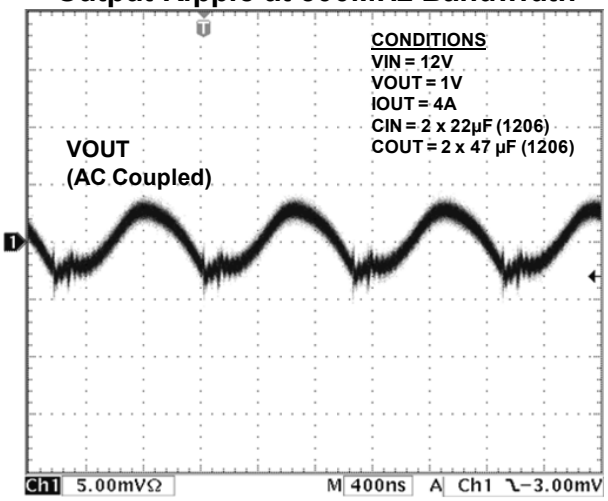
Output Ripple at 500MHz Bandwidth



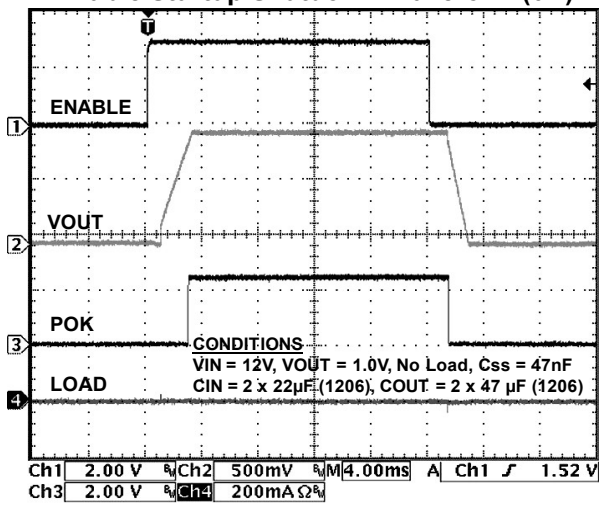
Output Ripple at 20MHz Bandwidth



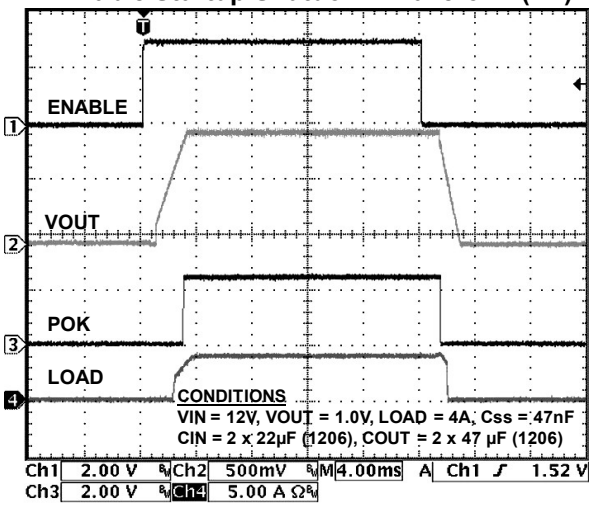
Output Ripple at 500MHz Bandwidth



Enable Startup/Shutdown Waveform (0A)

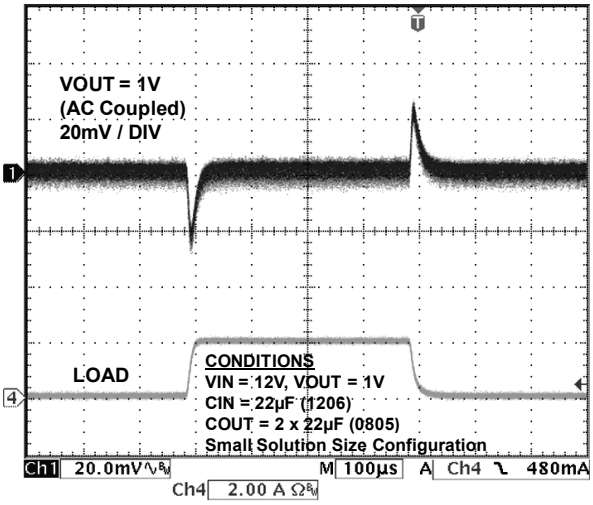


Enable Startup/Shutdown Waveform (4A)

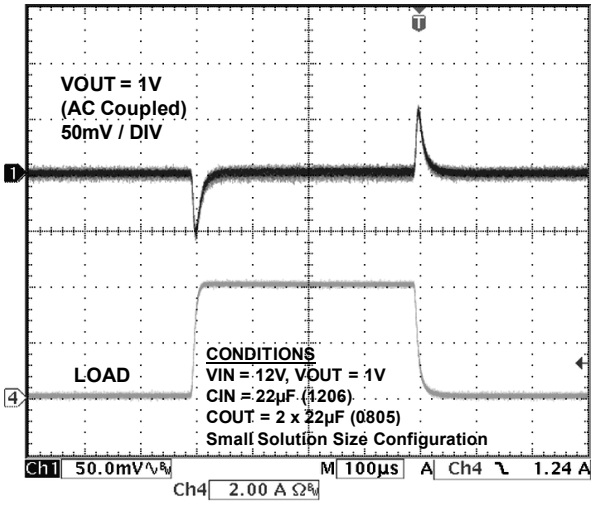


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

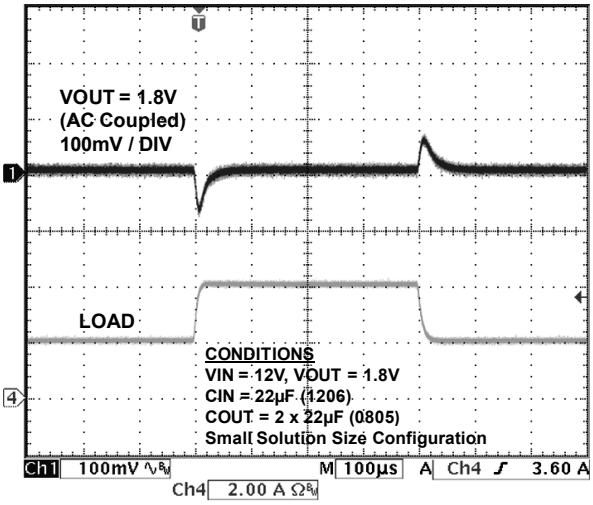
Load Transient from 50mA to 2A



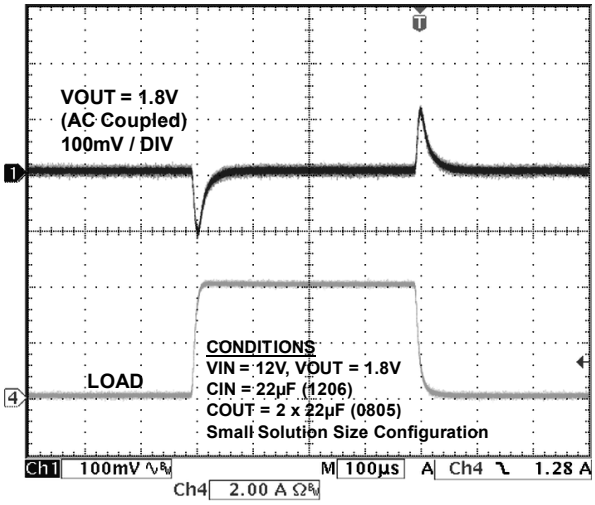
Load Transient from 50mA to 4A



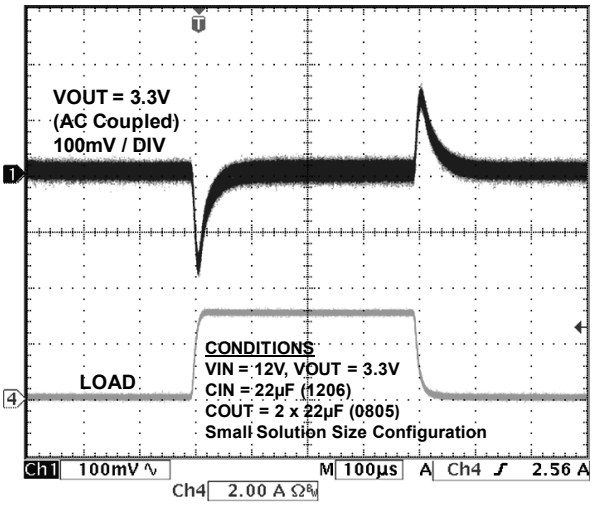
Load Transient from 2A to 4A



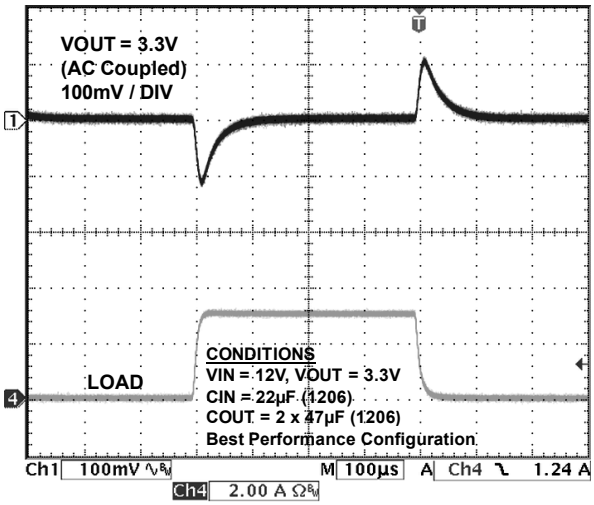
Load Transient from 50mA to 4A



Load Transient from 50mA to 3A



Load Transient from 50mA to 3A



FUNCTIONAL BLOCK DIAGRAM

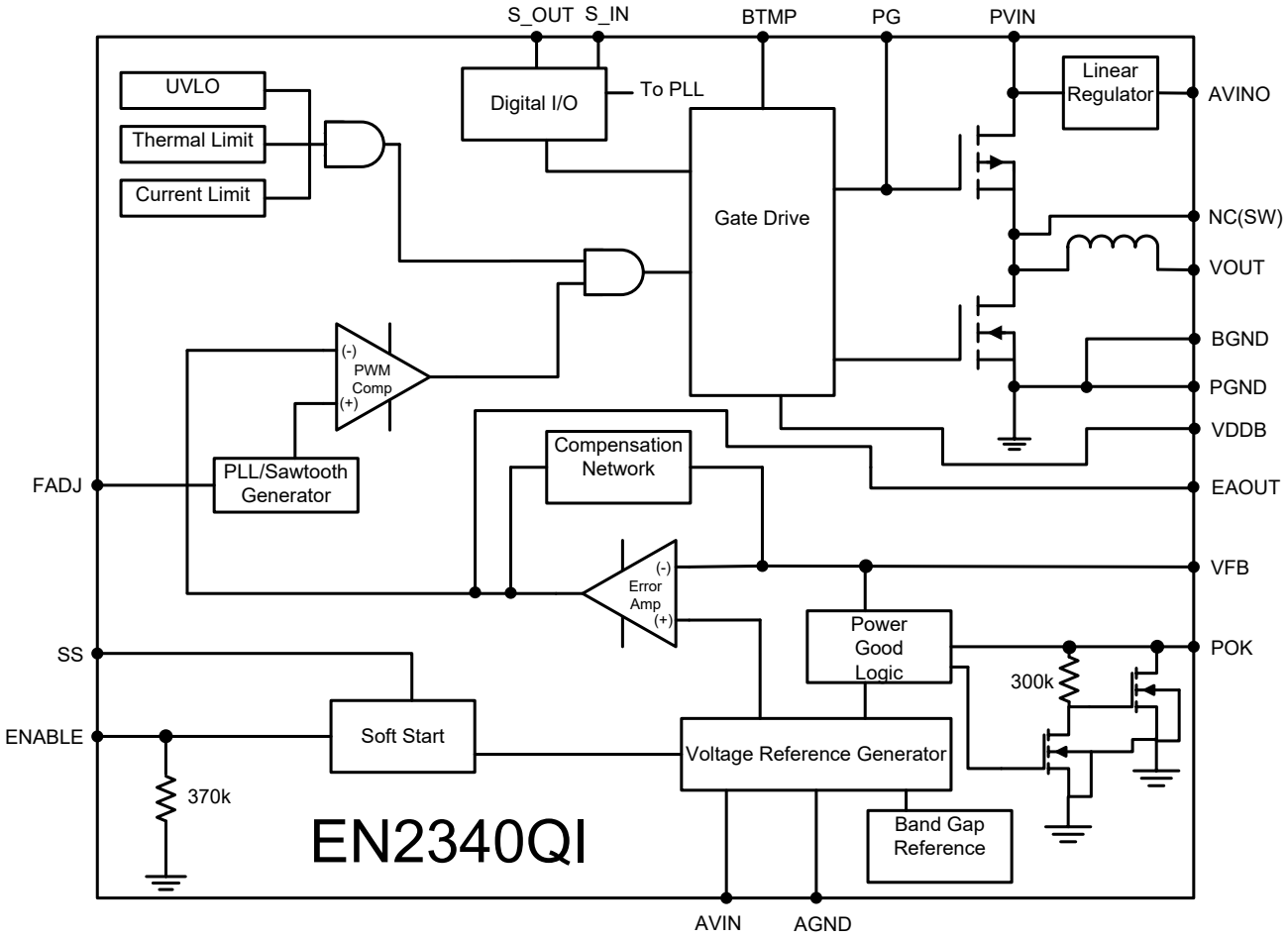


Figure 4. Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous DC-DC Step-Down PowerSoC

The EN2340QI is a highly integrated synchronous, buck converter with integrated controller, power MOSFET switches and inductor. The nominal input voltage (PVIN) range is 4.5V to 14V and can support up to 4A of continuous output current. The output voltage is programmed using an external resistor divider network. The control loop utilizes a Type IV Voltage-Mode compensation network and maximizes on a low-noise PWM topology. Much of the compensation circuitry is internal to the device. However, a phase lead capacitor is required along with the output voltage feedback resistor divider to complete the Type IV compensation network. The high switching frequency of the EN2340QI enables the use of small size input and output filter capacitors, as well as a wide loop bandwidth within a small foot print.

Protection Features:

The power supply has the following protection features:

- Programmable Over-Current Protection
- Thermal Shutdown with Hysteresis
- Under-Voltage Lockout Protection

Additional Features:

- Switching Frequency Synchronization
- Programmable Soft-Start
- Power OK Output Monitoring

Power Up Sequence

The EN2340QI is designed to be powered by either a single input supply (PVIN) or two separate supplies: one for PVIN and the other for AVIN. The EN2340QI is not "hot pluggable." Refer to the PVIN Slew Rate specification on page 6.

Single Input Supply Application (PVIN):

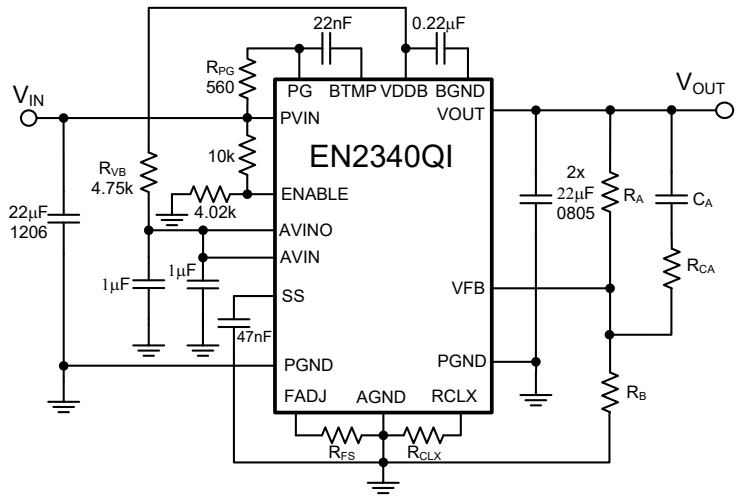


Figure 5. Single Input Supply Schematic

The EN2340QI has an internal linear regulator that converts PVIN to 3.3V. The output of the linear regulator is provided on the AVINO pin once the device is enabled. AVINO should be connected to AVIN on the EN2340QI. In this application, the following external components are required: Place a 1µF, X5R/X7R capacitor between AVINO and AGND as close as possible to AVINO. Place a 1µF, X5R/X7R capacitor between AVIN and AGND as close as possible to AVIN. In addition, place a resistor (R_{VB}) between VDDB and AVIN, as shown in Figure 5. Intel recommends R_{VB}=4.75kΩ. In this application, ENABLE cannot be asserted before PVIN. See diagram below for a recommended startup and shutdown sequencing.

If no external enable signal is used, a resister divider (see Figure 5) from PVIN to ENABLE and then to ground can be used to enable and disable the device at a programmed PVIN voltage level. The lower resistor (4.02k) can be adjusted to set startup and shutdown at a specific PVIN voltage level. See ENABLE and DISABLE thresholds in the Electrical Characteristics table.

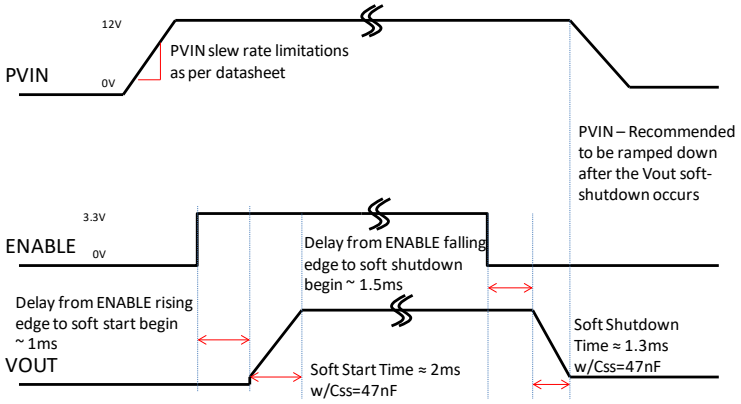


Figure 6. Single Supply Startup/Shutdown Sequence

Dual Input Supply Application (PVIN and AVIN):

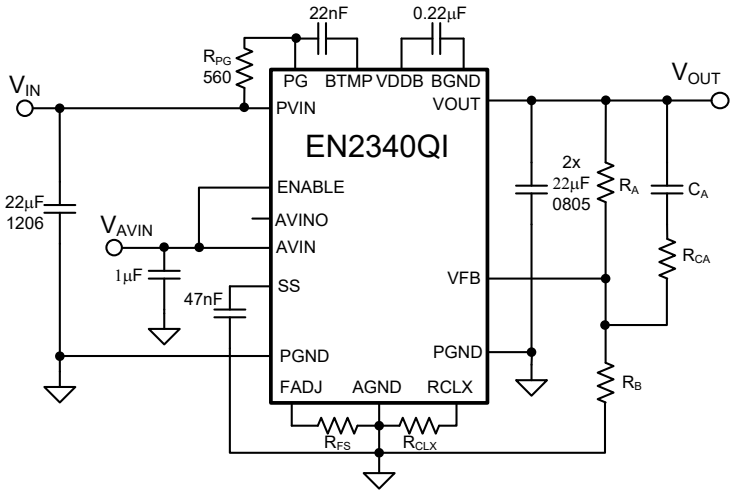


Figure 7. Dual Input Supply Schematic

In this application, place a 1µF, X5R/X7R, capacitor between AVIN and AGND as close as possible to AVIN. Refer to Figure 7 for a recommended schematic for a dual input supply application.

For dual input supply applications, the sequencing of the two input supplies, PVIN and AVIN, is very important. There are two common acceptable turn-on sequences for the device. AVIN can always come up before PVIN. If PVIN comes up before AVIN, then ENABLE must be toggled last, after AVIN is asserted. Do not turn off AVIN before PVIN and ENABLE during shutdown. Doing so will disable the internal controller while there may still be energy in the system. The device will not soft-shutdown properly and damage may occur. See diagram below for a recommended startup and shutdown sequencing.

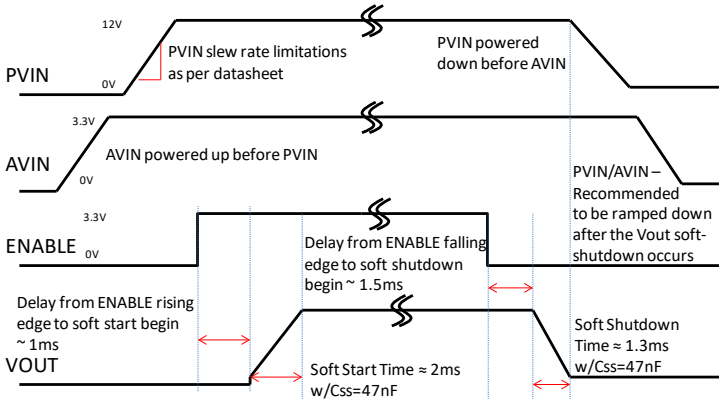


Figure 8. Dual Supply Startup/Shutdown Sequencing

Enable Operation

The ENABLE pin provides a means to enable normal operation or to shut down the device. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted (high) the device will undergo a normal soft-start. A logic low will disable the converter. A logic low will power down the device in a controlled manner and the device is subsequently shut down. The ENABLE signal has to be low for at least the ENABLE Lockout Time (8ms) in order for the device to be re-enabled. To ensure accurate startup sequencing the ENABLE/DISABLE signal should be faster than 1V/100µs. A slower ENABLE/DISABLE signal may result in a delayed startup and shutdown response.

Pre-Bias Precaution

The EN2340QI is not designed to be turned on into a pre-biased output voltage. Be sure the output capacitors are not charged or the output of the EN2340QI is not pre-biased when the EN2340QI is first enabled.

Frequency Synchronization

The switching frequency of the EN2340QI can be phase-locked to an external clock source to move unwanted beat frequencies out of band. The internal switching clock of the EN2340QI can be phase locked to a clock signal applied to the S_IN pin. An activity detector recognizes the presence of an external clock signal and automatically phase-locks the internal oscillator to this external clock. Phase-lock will occur as long as the input clock frequency is in the range of 0.8MHz to 1.8MHz. The external clock frequency must be within ±10% of the nominal switching frequency set by the R_{FS} resistor. It is recommended to use a synchronized clock frequency close to the typical frequency recommendations in Table 1. A 3.01kΩ resistor from FQADJ to ground is recommended for clock frequencies within ±10% of 1MHz. When no clock is present, the device reverts to the free running frequency of the internal oscillator set by the R_{FS} resistor.

The efficiency performance of the EN2340QI for various PVIN/VOUT combinations can be optimized by adjusting the switching frequency. Table 1 shows recommended R_{FS} values for various PVIN/VOUT combinations in order to optimize performance of the EN2340QI.

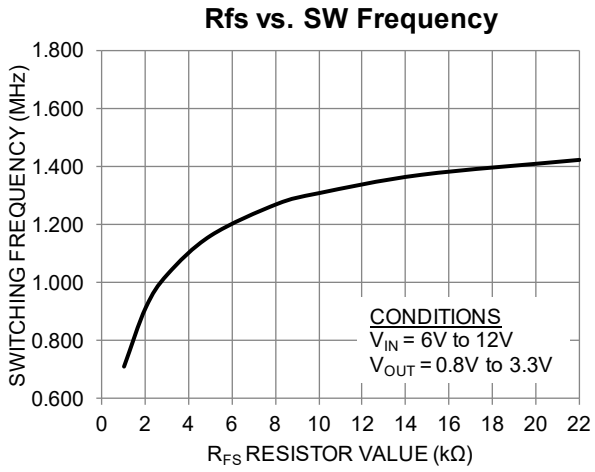


Figure 9. Typical R_{FS} vs. Switching Frequency

Table 1. Recommended R_{FS} Values

PVIN	VOUT	R_{FS}	Typical Fsw
12V	5.0V	30k	1.7 MHz
	3.3V	15k	1.38 MHz
	2.5V	10k	1.3 MHz
	1.8V	4.87k	1.15 MHz
	1.2V	1.65k	0.95 MHz
	<1.0V	1.3k	0.8 MHz
5V	2.5V	22.1k	1.4 MHz
	1.8V	10k	1.3 MHz
	1.5V	6.65k	1.25 MHz
	1.2V	4.87k	1.15 MHz
	<1.0V	3.01k	1.0 MHz

Spread Spectrum Mode

The external clock frequency may be swept between 0.8MHz and 1.8MHz at repetition rates of up to 10 kHz in order to reduce EMI frequency components.

Soft-Start Operation

Soft start is a means to ramp the output voltage gradually upon start-up. The output voltage rise time is controlled by the choice of soft-start capacitor, which is placed between the SS pin (pin 56) and the AGND pin (pin 52). During start-up of the converter, the reference voltage to the error amplifier is linearly increased to

its final level by an internal current source of approximately 10µA. The soft-start time is measured from when V_{IN} > V_{UVLOR} and ENABLE pin voltage crosses its logic high threshold to when V_{OUT} reaches its programmed value. The total soft-start time can be calculated by:

Soft Start Time (ms): $T_{SS} \approx C_{ss}$ [nF] x 0.067

Typical soft-start time is approximately 3.2ms with SS capacitor value of 47nF.

POK Operation

The POK signal is an open drain signal (requires a pull up resistor to AVIN or similar voltage) from the converter indicating the output voltage is within the specified range. Typically, a 100kΩ or lower resistance is used as the pull-up resistor. The POK signal will be logic high (AVIN) when the output voltage is above 90% of the programmed voltage level. If the output voltage is below this point, the POK signal will be a logic low. The POK signal can be used to sequence down-stream converters by tying to their enable pins.

Over-Current Protection (OCP)

The current limit function is achieved by sensing the current flowing through a sense PFET. When the sensed current exceeds the current limit for more than 32 cycles, both power FETs are turned off for the rest of the switching cycle. If the over-current condition is removed, the over-current protection circuit will re-enable PWM operation. In the event the OCP circuit trips consistently in normal operation, the device enters a hiccup mode. While in hiccup mode, the device is disabled for a short while and restarted with a normal soft-start. The hiccup time is approximately 32ms. This cycle can continue indefinitely as long as the over current condition persists. The OCP trip point depends on PVIN, VOUT and the RCLX resistor.

Generally, the higher the RCLX value, the higher the current limit threshold for a given input and output voltage condition.

Note: If the RCLX pin is left open, the output current will be unlimited and the device will not have current limit protection.

Reference Table 2 for a list of recommended resistor values on RCLX that will set the OCP trip point at the typical value of 6A, also specified in the Electrical Characteristics table.

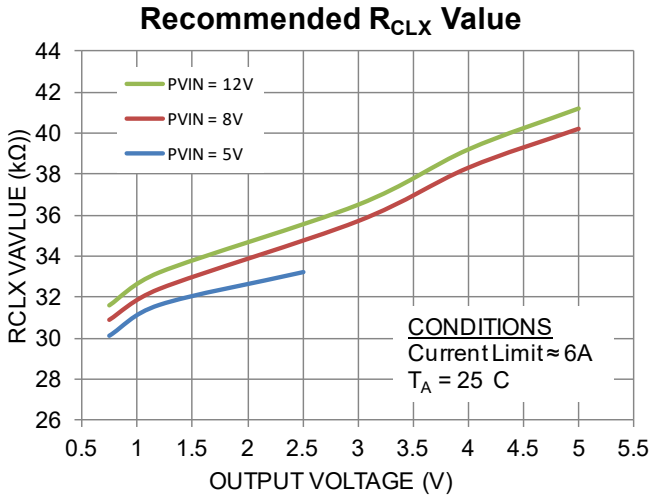


Figure 10. Typical RCLX vs. Output Voltage

Table 2. Recommended R_{CLX} Values

PVIN	V_{OUT} Range	R_{CLX} Value	Current Limit
5V	0.75V < V_{OUT} ≤ 1.2V	30.1kΩ	6A
	1.2V < V_{OUT} ≤ 2.0V	31.6kΩ	6A
	2.0V < V_{OUT} ≤ 2.5V	33.2kΩ	6A
8V	0.75V < V_{OUT} ≤ 1.2V	30.9kΩ	6A
	1.2V < V_{OUT} ≤ 2.0V	32.4kΩ	6A
	2.0V < V_{OUT} ≤ 3.0V	35.7kΩ	6A
	3.0V < V_{OUT} ≤ 4.0V	38.3kΩ	6A
	4.0V < V_{OUT} ≤ 5.0V	40.2kΩ	6A
12V	0.75V < V_{OUT} ≤ 1.2V	31.6kΩ	6A
	1.2V < V_{OUT} ≤ 2.0V	33.2kΩ	6A
	2.0V < V_{OUT} ≤ 3.0V	36.5kΩ	6A
	3.0V < V_{OUT} ≤ 4.0V	39.2kΩ	6A
	4.0V < V_{OUT} ≤ 5.0V	41.2kΩ	6A

Thermal Overload Protection

Thermal shutdown circuit will disable device operation when the junction temperature exceeds approximately 160°C. After a thermal shutdown event, when the junction temperature drops by approx 35°C, the converter will re-start with a normal soft-start.

Input Under-Voltage Lock-Out (UVLO)

Internal circuits ensure that the converter will not start switching until the AVIN input voltage is above the specified minimum voltage. Hysteresis, input de-glitch and output leading edge blanking ensures high noise immunity and prevents false UVLO triggers.

APPLICATION INFORMATION

Output Voltage Programming and Loop Compensation

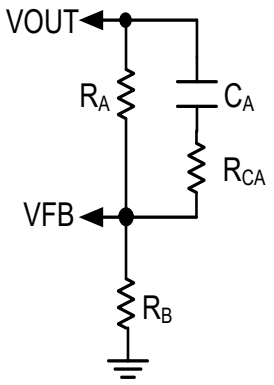
The EN2340QI output voltage is programmed using a simple resistor divider network. A phase lead capacitor (C_A) plus a resistor (R_{CA}) are required for stabilizing the loop. Figure 11 shows the required components and the equations to calculate their values. The values recommended for C_A and R_{CA} will vary with each PVIN and VOUT combination. The EN2340 solution can be optimized for either smallest size or highest performance. Please see Table 6 for a list of recommended C_A and R_{CA} values for each solution option.

The EN2340QI output voltage is determined by the voltage presented at the VFB pin. This voltage is set by way of a resistor divider between VOUT and AGND with the midpoint going to VFB. Since VFB is a sensitive node, do not touch the VFB node while the device is in operation as doing so may introduce parasitic capacitance into the control loop that causes the device to behave abnormally and damage may occur.

The EN2340QI uses a Type IV compensation network. Most of this network is integrated. However a phase lead capacitor and a resistor are required in parallel with the upper resistor of the external feedback network (see Figure 11). Total compensation is optimized for either low output ripple or small solution size, and will result in a wide loop bandwidth and excellent load transient performance for most applications. See Table 6 for compensation values for both options based on input and output voltage conditions.

In some cases modifications to the compensation may be required. The EN2340QI provides the capability to modify the control loop response to allow for customization for specific applications.

The EN2342QI uses a Type IV Voltage Mode compensation network. Type IV Voltage Mode control is a proprietary Intel Enpirion control scheme that maximizes control loop bandwidth to deliver excellent load transient responses and maintain output regulation with pin point accuracy. For ease of use, most of this network has been customized and is integrated within the device package.



$$R_A = \frac{180}{\sqrt{VOUT}} \quad (R_A \text{ in } k\Omega)$$

Round R_A up to closest standard value higher than the calculated value.

$$R_B = \frac{V_{FB} \times R_A}{(V_{OUT} - V_{FB})}$$

(V_{FB} is 0.75V nominal)

Figure 11. External Feedback Compensation. See Table 6 for details

Input Capacitor Selection

The EN2340QI requires a 22µF/1206 input capacitor. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X5R or X7R rated. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling. Table 3 contains a list of recommended input capacitors.

Table 3. Recommended Input Capacitors

Description	MFG	P/N
22µF, 16V, X5R, 10%, 1206	Murata	GRM31CR61C226ME15
22µF, 16V, X5R, 20%, 1206	Taiyo Yuden	EMK316ABJ226ML-T

Output Capacitor Selection

As seen from Table 6, the EN2340QI has been optimized for use with either two 47µF/1206 or two 22µF/0805 output capacitors. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. Table 4 contains a list of recommended output capacitors.

Table 4. Recommended Output Capacitors

Description	MFG	P/N
47µF, 6.3V, X5R, 20%, 1206	Murata	GRM31CR60J476ME19L
47µF, 10V, X5R, 20%, 1206	Taiyo Yuden	LMK316BJ476ML-T
22µF, 10V, X5R, 20%, 0805	Panasonic	ECJ-2FB1A226M
22µF, 10V, X5R, 20%, 0805	Taiyo Yuden	LMK212BJ226MG-T

In some applications, extra bulk capacitance is required at the load. In this case, up to 1000µF of bulk capacitance may be used at the load as long as the minimum ESR between the device output and the bulk capacitance is maintained. Table 5 shows the recommended compensation components for applications that require bulk capacitance at the load.

Table 5. Minimum ESR for Bulk Capacitance at Load

PVIN (V)	VOUT (V)	Min. ESR	Compensation
4.5 to 14	≥2.5	4mΩ	C_{OUT} = 2x47µF/1206 Bulk Cap ≤ 1000µF C_A = 100pF R_A = 250kΩ R_{CA} = 5kΩ
≥10	0.6 to 1.5	9mΩ	
	1.5 to 2.5	7mΩ	
<10	0.6 to 1.5	12mΩ	
	1.5 to 2.5	9mΩ	

Output ripple voltage is determined by the aggregate output capacitor impedance. Capacitor impedance, denoted as Z, is comprised of capacitive reactance, effective series resistance, ESR, and effective series inductance, ESL reactance.

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

Table 6. R_A, C_A, and R_{CA} Values for Various PVIN/VOUT Combinations: Low V_{OUT} Ripple vs. Smallest Solution Size.

		Low V_{OUT} Ripple C_{IN} = 1 x 22µF/1206 C_{OUT} = 2 x 47µF/1206 R_A= 180/($V_{out}^{0.5}$) kΩ				Smallest Solution Size C_{IN} = 1 x 22µF/1206 C_{OUT} = 2 x 22µF/0805				
PVIN	**V_{OUT}**	**C_A (pF)**	**R_{CA} (kΩ)**	**Nominal Ripple (mV)**	**Nominal Deviation (mV)(7)**	**R_A (kΩ)**	**C_A (pF)**	**R_{CA} (kΩ)**	**Nominal Ripple (mV)**	**Nominal Deviation (mV)(7)**
14V	≤1.0V	10	30	≤5	≤47	75	27	0.1	≤10	≤34
	1.2V	12	27	6	48	43	39	0.1	13	33
	1.5V	15	27	5	53	56	39	0.1	15	38
	1.8V	22	27	6	54	56	39	0.1	18	41
	2.5V	27	24	8	55	51	39	0.1	26	59
	3.3V	39	18	11	63	51	33	0.1	35	63
	5.0V	47	8.2	18	97	75	22	5.1	42	115
12V	≤1.0V	18	22	≤4	≤48	27	47	0.1	≤10	≤35
	1.2V	22	22	5	49	75	47	0.1	13	37
	1.5V	27	20	5	53	75	47	0.1	15	38
	1.8V	33	20	6	54	75	47	0.1	17	44
	2.5V	47	18	7	54	56	47	0.1	25	59
	3.3V	56	15	10	66	51	39	0.1	32	63
	5.0V	56	10	16	99	75	22	5.1	39	128
10V	≤1.0V	33	18	≤3	≤45	27	82	0.1	≤9	≤35
	1.2V	39	18	4	46	30	100	0.1	13	39
	1.5V	47	18	5	54	30	100	0.1	14	43
	1.8V	56	16	6	56	30	100	0.1	17	50
	2.5V	68	12	7	57	75	56	0.1	26	70
	3.3V	82	10	9	68	56	47	0.1	30	83
	5.0V	100	4.3	14	98	75	33	5.1	33	140
8.0V	≤1.0V	100	8.2	≤3	≤51	100	100	0.1	≤10	≤41
	1.2V	100	8.2	4	51	100	100	0.1	12	43
	1.5V	100	8.2	4	54	100	100	0.1	14	46
	1.8V	100	8.2	5	57	100	100	0.1	16	53
	2.5V	100	8.2	6	64	91	82	0.1	23	71
	3.3V	100	8.2	8	70	75	56	0.1	25	85
	5.0V	100	8.2	10	110	75	56	5.1	30	127
6.6V	≤1.0V	100	8.2	≤3	≤60	100	100	0.1	≤9	≤46
	1.2V	100	8.2	4	63	100	100	0.1	12	51
	1.5V	100	8.2	4	65	100	100	0.1	14	56
	1.8V	100	8.2	5	68	100	100	0.1	16	61
	2.5V	100	8.2	5	75	100	100	0.1	19	83
	3.3V	100	8.2	6	85	91	82	0.1	22	106
5V	≤1.0V	100	8.2	≤3	≤73	100	100	0.1	≤9	≤56
	1.2V	100	8.2	3	75	100	100	0.1	11	63
	1.5V	100	8.2	4	76	100	100	0.1	13	70
	1.8V	100	8.2	4	80	100	100	0.1	13	78
	2.5V	100	8.2	4	88	100	100	0.1	14	98

Note: See Figure 11. Use the equation in Figure 11 to calculate R_B (for low V_{OUT} ripple option).

(7) Nominal Deviation is for a 2A load transient step.

(8) For compensation values of output voltage in between the specified output voltages, choose compensation values of the lower output voltage setting.

THERMAL CONSIDERATIONS

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. Intel Enpirion PowerSoC helps alleviate some of those concerns.

Intel Enpirion EN2340QI DC-DC converter is packaged in an 8x11x3mm 68-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 160°C.

The EN2340QI is guaranteed to support the full 4A output current up to 85°C ambient temperature. The following example and calculations illustrate the thermal performance of the EN2340QI.

Example:

V_{IN} = 12V

V_{OUT} = 3.3V

I_{OUT} = 4A

First calculate the output power.

P_{OUT} = 3.3V x 4A = 13.2W

Next, determine the input power based on the efficiency (η) shown in Figure 12.

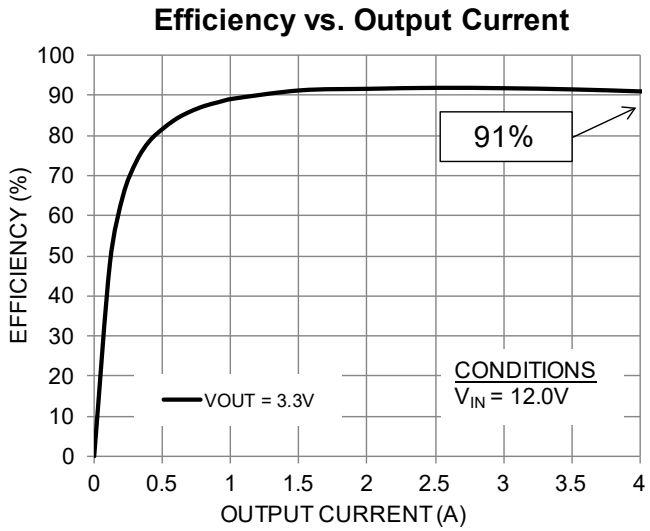


Figure 12. Efficiency vs. Output Current

For V_{IN} = 12V, V_{OUT} = 3.3V at 4A, η ≈ 91%

η = P_{OUT} / P_{IN} = 91% = 0.91

P_{IN} = P_{OUT} / η

P_{IN} ≈ 13.2W / 0.9 ≈ 14.51W

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

P_D = P_{IN} – P_{OUT}

≈ 14.51W – 13.2W ≈ 1.31W

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN2340QI has a θ_{JA} value of 18 °C/W without airflow.

Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

ΔT = P_D x θ_{JA}

ΔT ≈ 1.31W x 18°C/W = 23.5°C ≈ 24°C

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

T_J = T_A + ΔT

T_J ≈ 25°C + 24°C ≈ 49°C

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

T_{AMAX} = T_{JMAX} – P_D x θ_{JA}

≈ 125°C – 24°C ≈ 101°C

The maximum ambient temperature the device can reach is 101°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

ENGINEERING SCHEMATIC

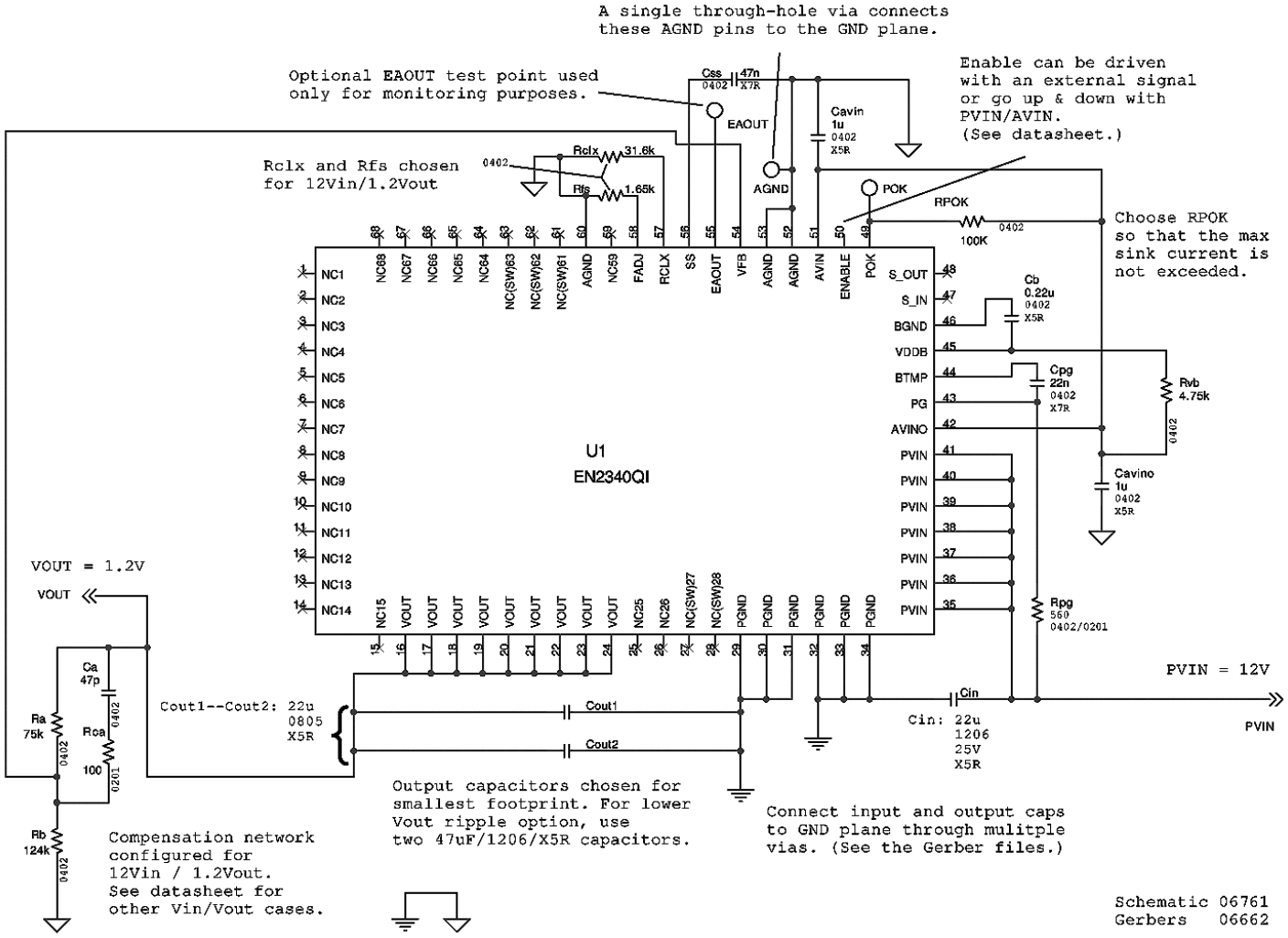


Figure 13. Engineering Schematic with Engineering Notes

LAYOUT RECOMMENDATIONS

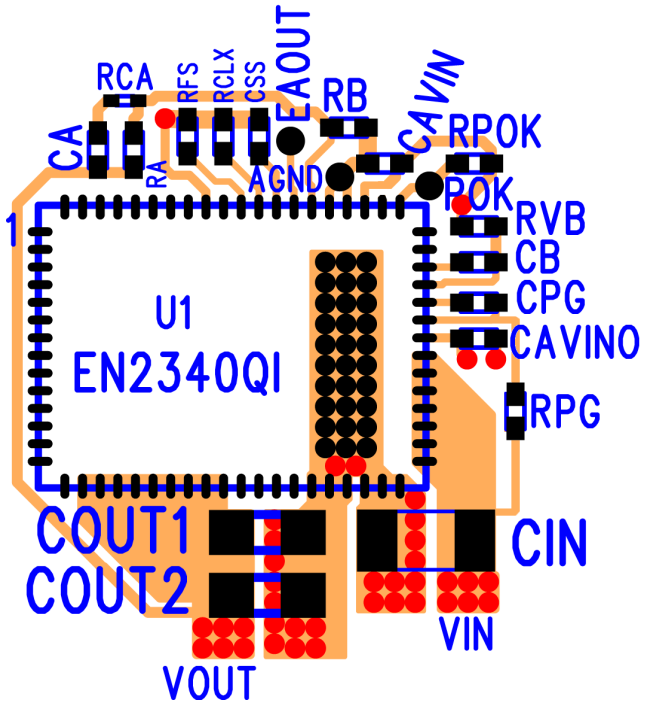


Figure 14. Top Layout with Critical Components Only (Top View)

See Figure 13 for corresponding schematic. This layout only shows the critical components and top layer traces for minimum footprint in single-supply mode. Alternate circuit configurations & other low-power pins need to be connected and routed according to customer application. Please see the Gerber files at http://www.intel.com/enpirion for details on all layers.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN2340QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN2340QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The PGND connections for the input and output capacitors on layer 1 need to have a slit between them in order to provide some separation between input and output current loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

Recommendation 4: The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input

and output current loops. If vias cannot be placed under the capacitors, then place them on both sides of the slit in the top layer PGND copper.

Recommendation 6: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 14 this connection is made at the input capacitor.

Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure 14. Refer to the section regarding Exposed Metal on Bottom of Package. As with any switch-mode DC-DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 8: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node. Contact Intel MySupport for any remote sensing applications.

Recommendation 9: Keep R_A, C_A, R_B, and R_{CA} close to the VFB pin (Refer to Figure 14). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pins 52 and 53 instead of going through the GND plane.

Recommendation 10: Follow all the layout recommendations as close as possible to optimize performance. Intel Enpirion provides schematic and layout reviews for all customer designs.

DESIGN CONSIDERATIONS FOR LEAD-FRAME BASED MODULES

Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 15.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN2340QI should be clear of any metal (copper pours, traces, or vias) except for the thermal pad. The “shaded-out” area in Figure 15 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by soldermask.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package. Please consult the Enpirion Manufacturing Application Note for more details and recommendations.

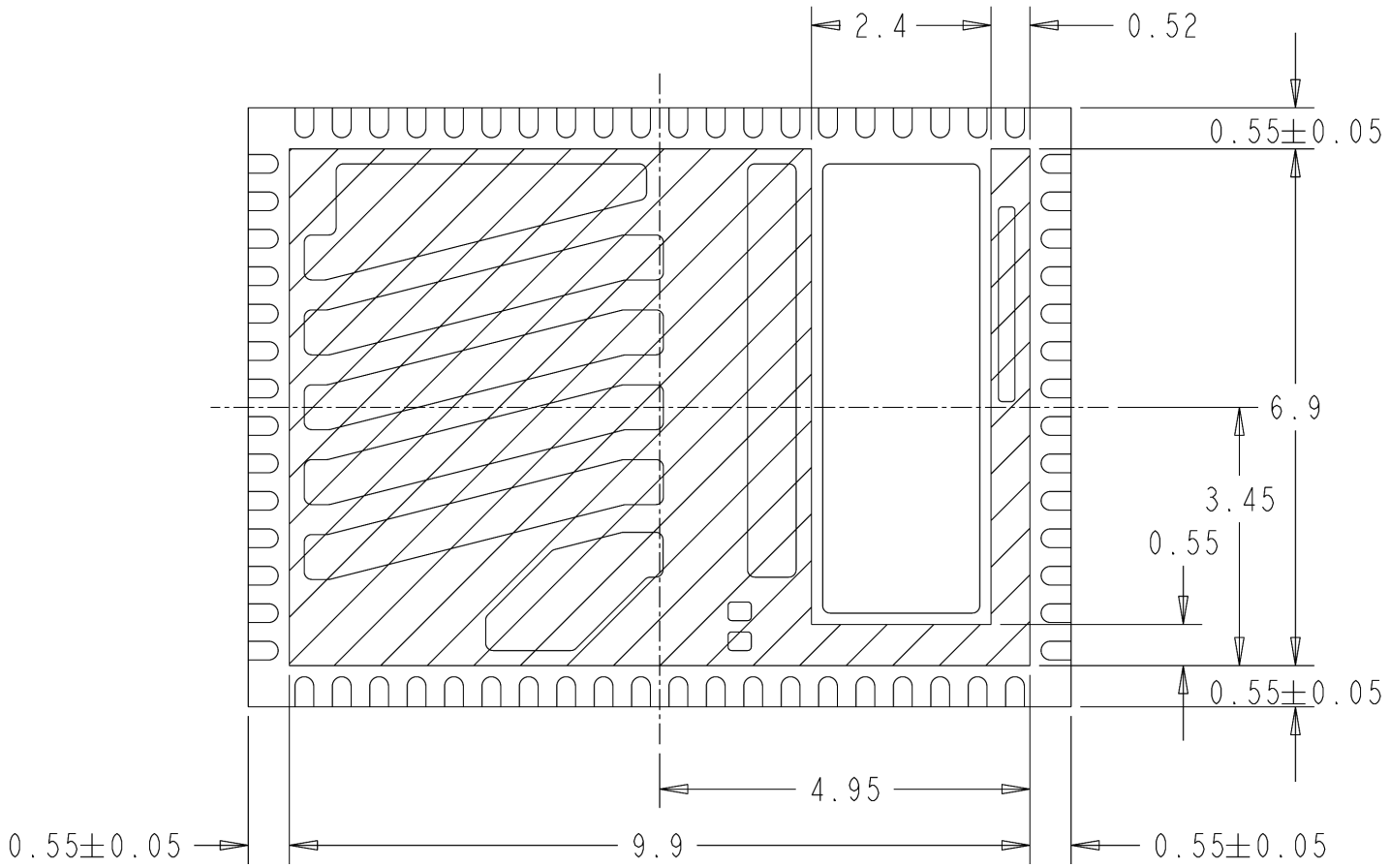


Figure 15. Lead-Frame exposed metal (Bottom View)

Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

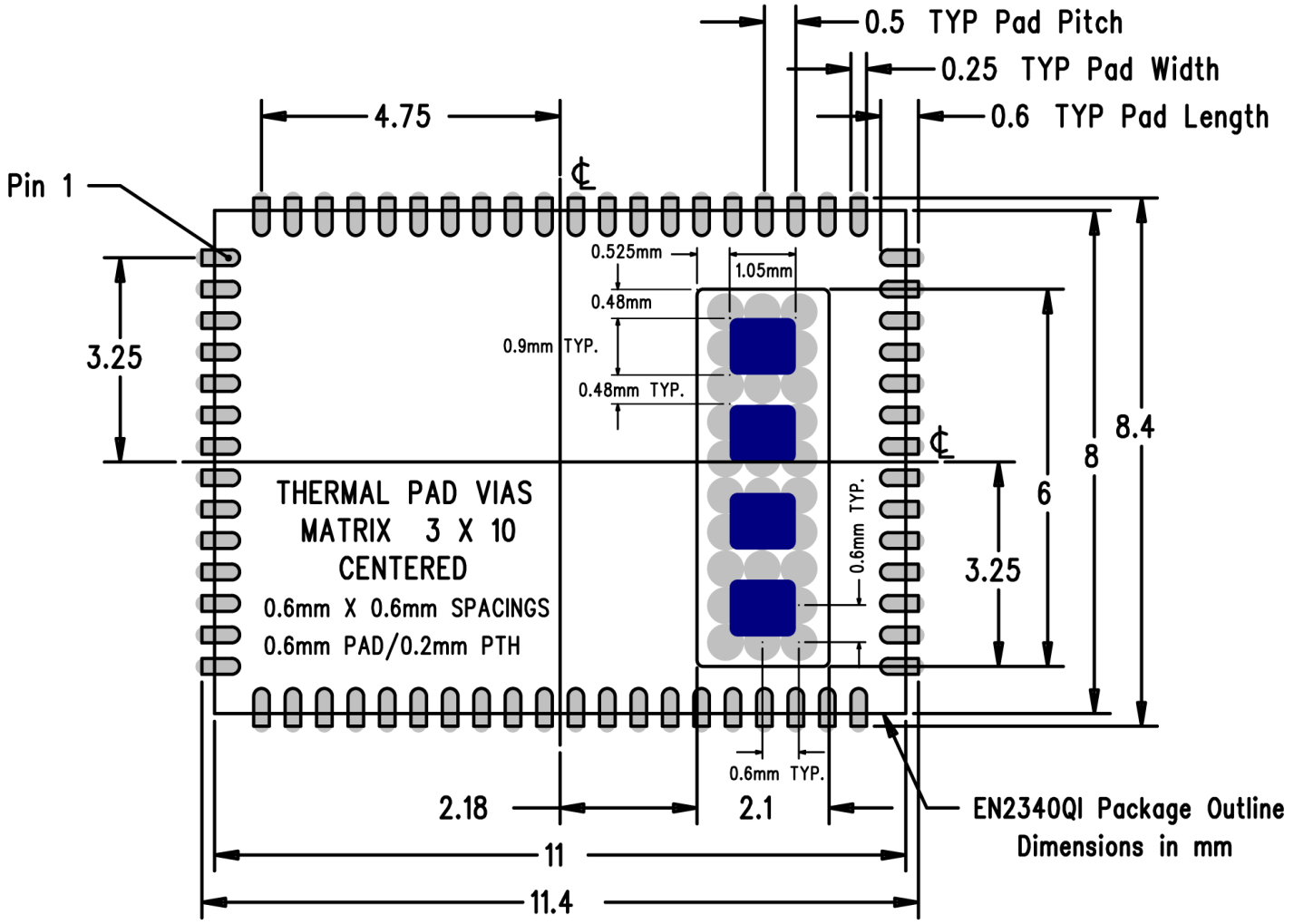


Figure 16. EN2340QI PCB Footprint (Top View)

The solder stencil aperture for the thermal pad is shown in blue and is based on Enpirion power product manufacturing specifications.

PACKAGE DIMENSIONS

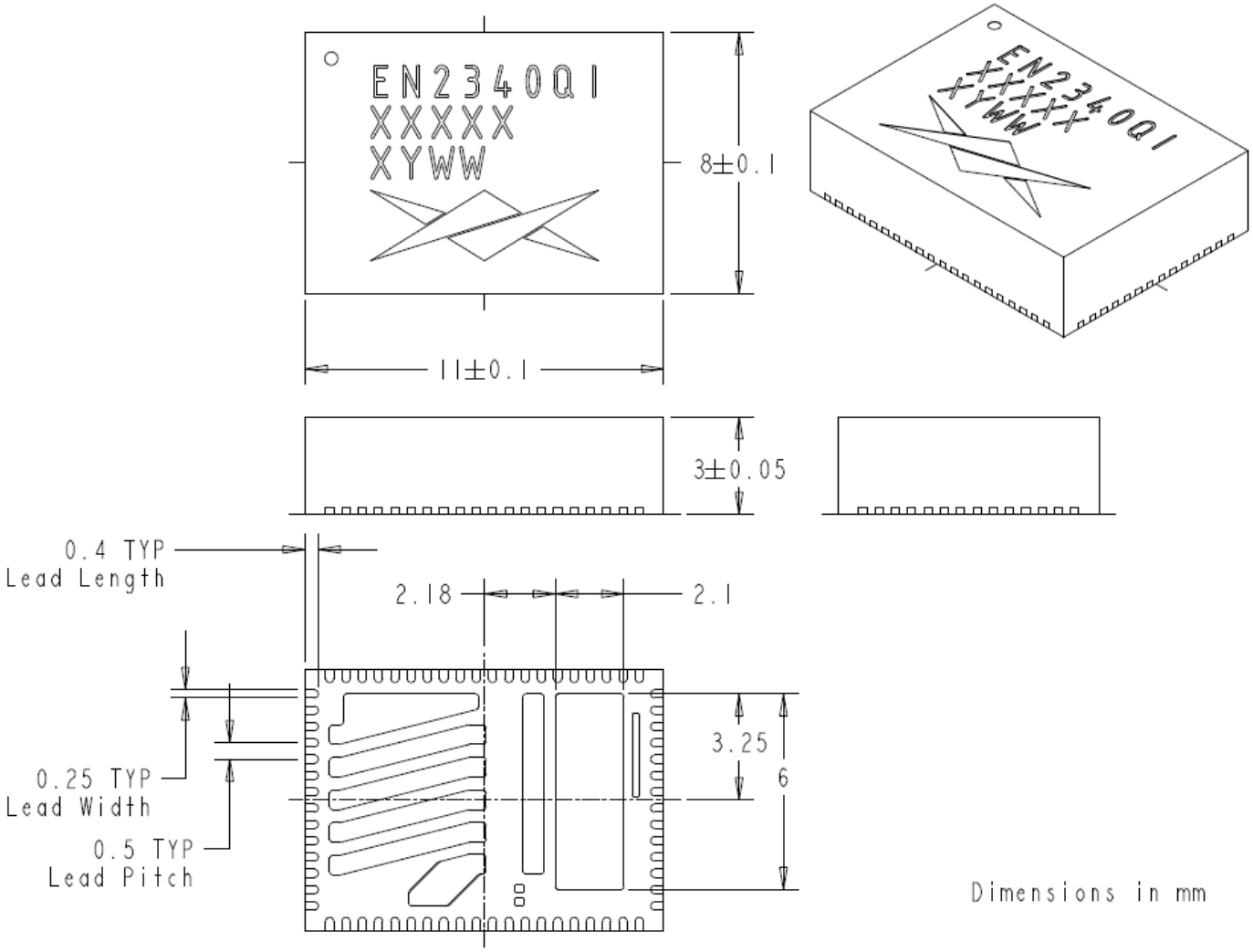


Figure 17. EN2340QI Package Dimensions (Bottom View)

Packing and Marking Information: https://www.intel.com/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
F	July 2019	Changed datasheet into Intel format

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

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