THE DATASHEET OF

AN15851A

Structure	Silicon Monolithic Bipolar IC
Appearance	36-USO Pin Plastic Package (USONF-36D)
Application	IC for Color TV
Function	4-Input AV Switch IC with RGB-YUV Converter

A	Absolute Maximum Ratings				
No.	Item	Symbol	Ratings	Unit	Note
1	Storage Temperature	Tstg	-55 ~ +150	°C	1
2	Operating Ambient Temperature	Topr	-20 ~ +70	°C	1
3	Operating Ambient Pressure	Popr	$1.013 \times 10^5 \pm 0.61 \times 10^5$	Pa	
4	Operating Constant Acceleration	Gopr	9810	m / s^2	
5	Operating Shock	Sopr	4900	m / s^2	
6	Power Supply Voltage	Vcc	14	V	
7	Power Supply Current	Icc	60	mA	
8	Power Dissipation	P_D	840	mW	

Operating Supply Voltage Range	Vcc	8.1V ~ 9.9V

Note 1) The temperature of all items shall be Ta = 25°C except storage temperature and operating ambient temperature.

B Electrical Characteristics
(Vcc=9V, unless otherwise specified, the ambient temperature is 25°C±2°C)

No.	Item	Symbol	Test Cct.	Condition		Limit Min	Limit Typ	Limit Max	Unit	Note
1	Quiescent Current	I_{CQ}	1	No input		38	46	52	mA	
	[VIDEO BLOCK]									
2	Video Gain (OUT1)	$Gv_{1/6}$	1	Select : 6dB f =15kHz, Vin=0.5Vp-p		5.0	5.7	6.4	dB	
		$Gv_{1CV/6}$			RGB → YUV	4.5	5.7	6.9		
		$Gv_{1/4}$	1	Select : 4.4dB f =15kHz, Vin=0.5Vp-p		3.4	4.1	4.8		
		$Gv_{1CV/4}$			RGB → YUV	2.9	4.1	5.3		
	Video Gain (OUT2)	$Gv_{2/6}$	1	Select : 6dB f =15kHz, Vin=0.5Vp-p		5.0	5.7	6.4	dB	
		$Gv_{2CV/6}$			RGB → YUV	4.5	5.7	6.9		
		$Gv_{2MX/6}$			YCmix NON RGB → YUV	4.5	5.7	6.9		1
		$Gv_{2/0}$	1	Select : 0dB f =15kHz, Vin=0.5Vp-p		-1.0	-0.3	0.4	dB	
		$Gv_{2CV/0}$			RGB → YUV	-1.5	-0.3	0.9		
		$Gv_{2MX/0}$			YCmix NON RGB → YUV	-1.5	-0.3	0.9		2
3	Video Frequency Characteristics	f_Y	1	f=100kHz, Vin=0.5Vp-p as reference 0dB, measure the frequency at output -3dB point.		20	30	-	MHz	
		f_{UV}				10	20	-		
		f_{CONV}				10	20	-		
		f_{MIX}				10	20	-		
4	Input Dynamic Range	V_{DYUV}	1	f = 20kHz, maximum input when output at THD < 2.0%.		2.0	2.4	-	Vp-p	
		V_{DYCONV}				2.0	2.4	-		
		V_{DYMIX}				1.9	2.3	-		
5	Video Crosstalk	C_M	1	f=5MHz, Vin=1Vp-p		50	60	-	dB	
	Y and U Crosstalk	C_{YU}				35	40	-		
	Y and V Crosstalk	C_{YV}				35	40	-		
	U and V Crosstalk	C_{UV}				35	40	-		
6	Mute Ratio(V/SY OUT1)	MR	1	Vin=0.5Vp-p, f=15kHz		40	50	-	dB	

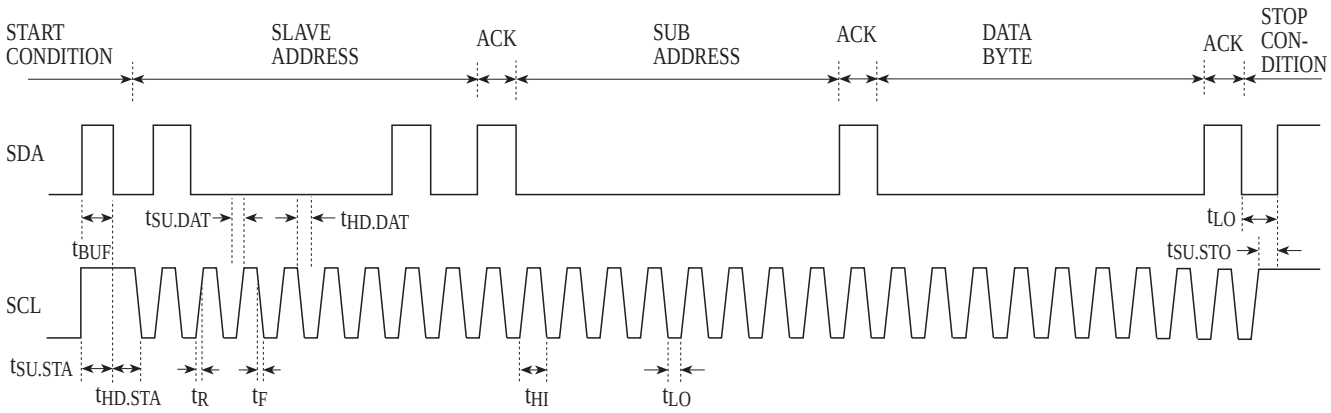
Note 1 : SELECT GAIN (U/SC & V/SY = 6dB ; Y/SY/CV = 0dB; Both input U/SC & V/SY)
Note 2 : SELECT GAIN (U/SC & V/SY = 0dB ; Y/SY/CV = 0dB; Both input U/SC & V/SY)

B	Electrical Characteristics			(Vcc=9V, unless otherwise specified, the ambient temperature is 25°C ± 2°C)					
No	Item	Symbol	Test Cir-cuit	Conditions	Limits			Unit	Note
					min	typ	max		
	[AUDIO BLOCK]								
7	Audio Gain	G_A	1	f=1kHz, 1Vp-p	-0.5	0	0.5	dB	
8	Audio Frequency Characteristics	f_A	1	f=1kHz, Vin=1Vp-p as reference 0dB, measure the frequency at output -3dB point.	36	41	-	kHz	
9	Input Dynamic Range	V_{DYA}	1	f=1kHz, maximum input when output at THD < 1.5%	2.8	2.9	-	Vrms	
10	Source Crosstalk	C_A	1	f=1kHz, Vin=1Vp-p Din Audio	80	85	-	dB	
	Channel Crosstalk	C_{LR}			80	85	-		
	[IIC Interface]								
11	Suction current during ACK	I_{ACK}	1	Max. suction current value of Pin 36 at 0.4V.	3.0	10	-	mA	
12	SCL, SDA signal input high level	V_{IHI}	1		3.0	-	5.5	V	
13	SCL, SDA signal input low level	V_{ILO}	1		0	-	1.5	V	
14	Max. frequency allowable to input	f_{imax}	1		-	-	100	kbit/s	

B Electrical Characteristics

(V_{CC}=9V, unless otherwise specified, the ambient temperature is 25°C ± 2°C)

No	Item	Symbol	Test Circuit	Conditions	Limits min	Limits typ	Limits max	Unit	Note
	[IIC Interface]								
1	Bus free before start	t_{BUF}			4.0	-	-	µs	
2	Start condition set-up time	$t_{SU, STA}$			4.0	-	-	µs	
3	Start condition hold time	$t_{HD, STA}$			4.0	-	-	µs	
4	Low period SCL, SDA	t_{LO}			4.0	-	-	µs	
5	High period SCL	t_{HI}			4.0	-	-	µs	
6	Rise time SCL, SDA	t_R			-	-	1.0	µs	
7	Fall time SCL, SDA	t_F			-	-	0.35	µs	
8	Data set-up time (write)	$t_{SU, DAT}$			0.25	-	-	µs	
9	Data hold time (write)	$t_{HD, DAT}$			0	-	-	µs	
10	Acknowledge set-up time	$t_{SU, ACK}$			-	-	3.5	µs	
11	Acknowledge hold time	$t_{HD, ACK}$			0	-	-	µs	
12	Stop condition set-up time	$t_{SU, STO}$			4.0	-	-	µs	

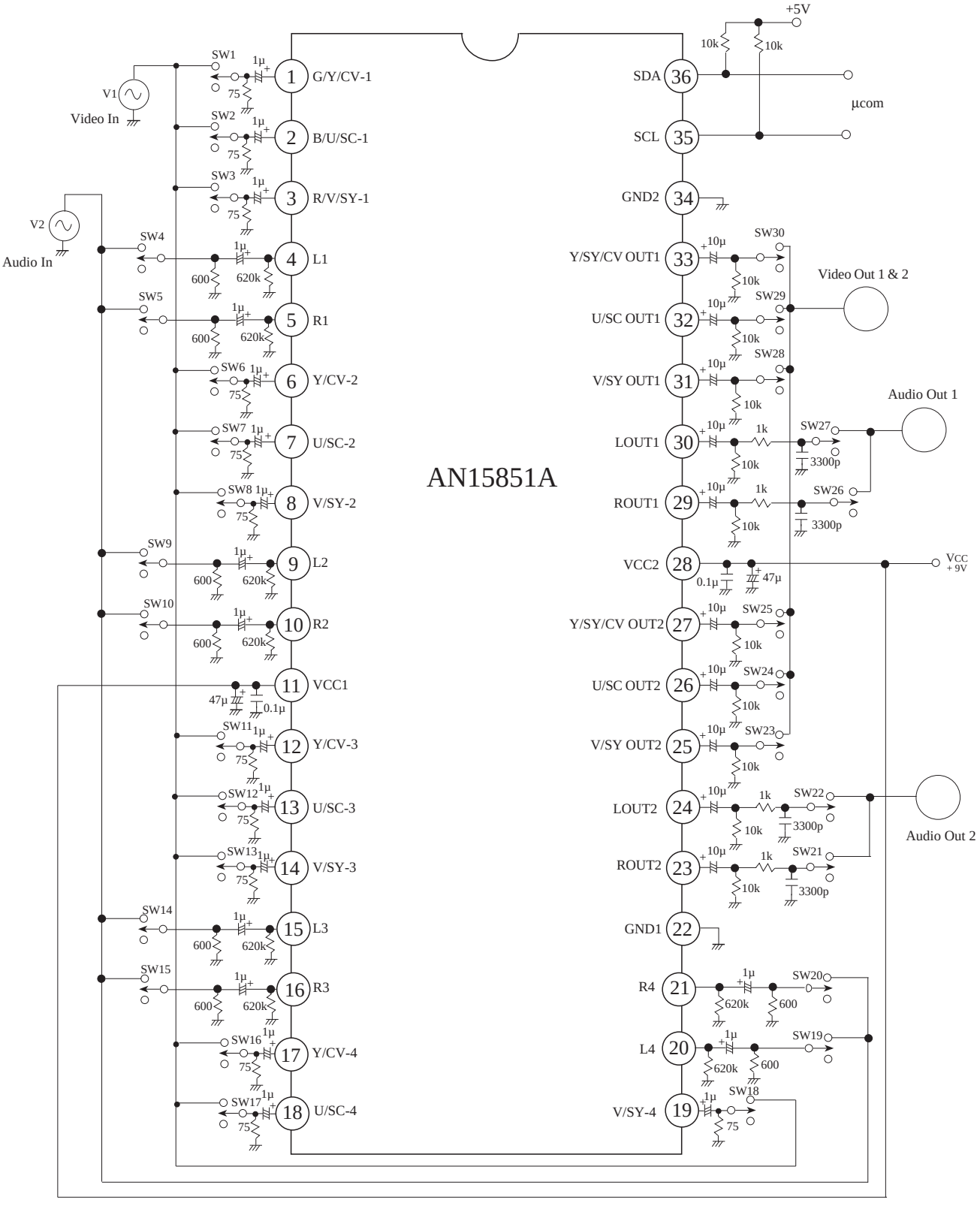


Note) The above characteristics are reference values on IC designing and not guaranteed by shipping inspection.

Eff. Date	Eff. Date	Eff. Date	Eff. Date
18 JAN 2002	6 MAR 2002	10 APR 2002	

B	Electrical Characteristics	(VCC=9V, unless otherwise specified, the ambient temperature is 25°C ± 2°C)							
No	Item	Symbol	Test Cir-cuit	Conditions	Limits			Unit	Note
					min	typ	max		
	[Video Block]								
13	Total Harmonic Distortion 1	THD_V	1	Vin=0.5Vp-p, f=20kHz	-	0.4	1.0	%	
	[Audio Block]								
14	Total Harmonic Distortion 2	THD_A	1	Vin=1Vrms, f=1kHz Din Audio	-	0.1	0.3	%	

Test Circuit 1



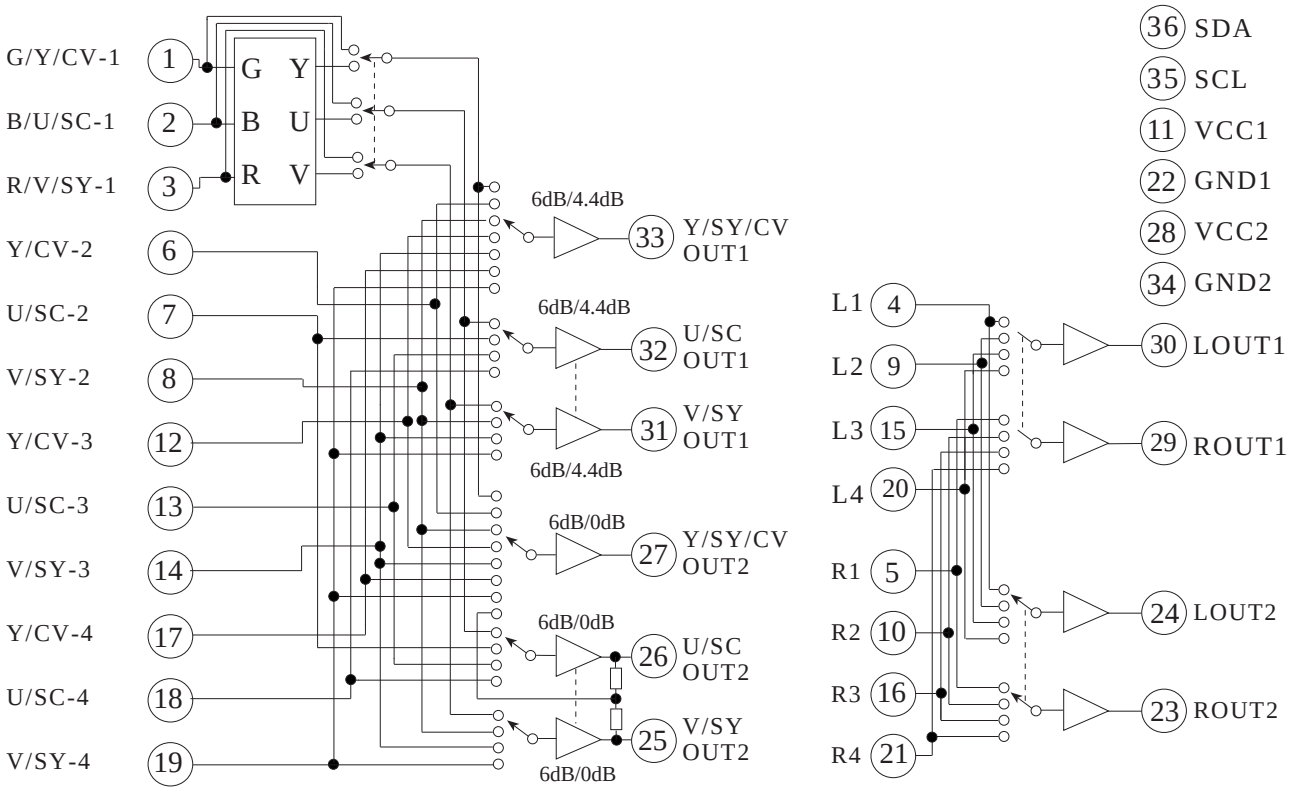
Note : The above circuit is used for Latchup Testing

Eff. Date	Eff. Date	Eff. Date	Eff. Date	Eff. Date
18 JAN 2002	6 MAR 2002	10 APR 2002		

Circuit Function Block Diagram

(Video)

(Audio)

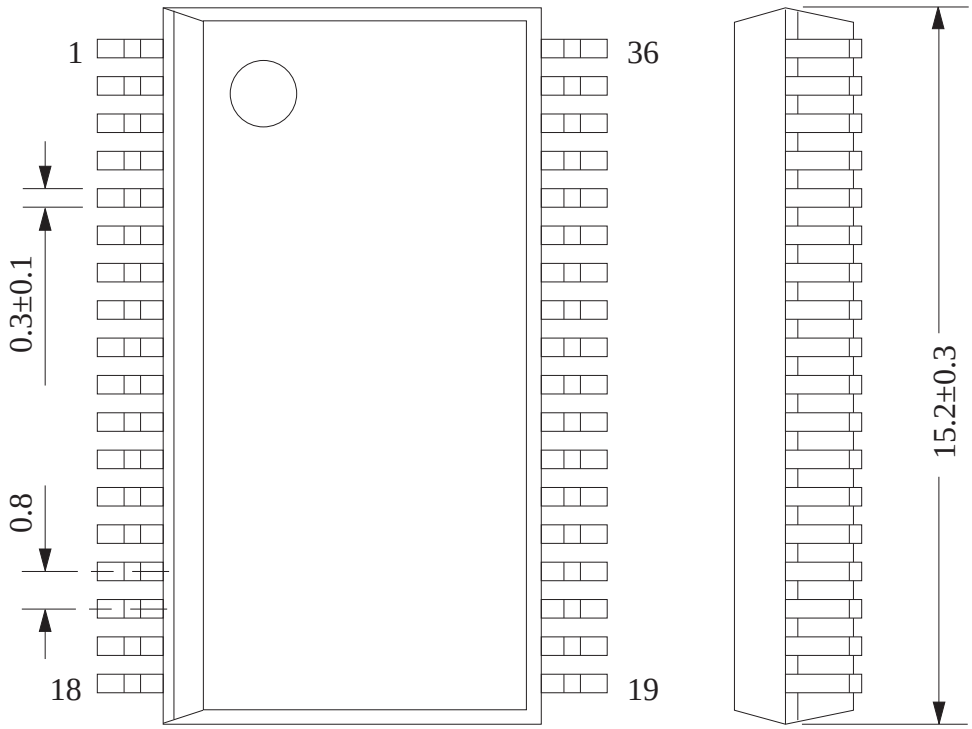


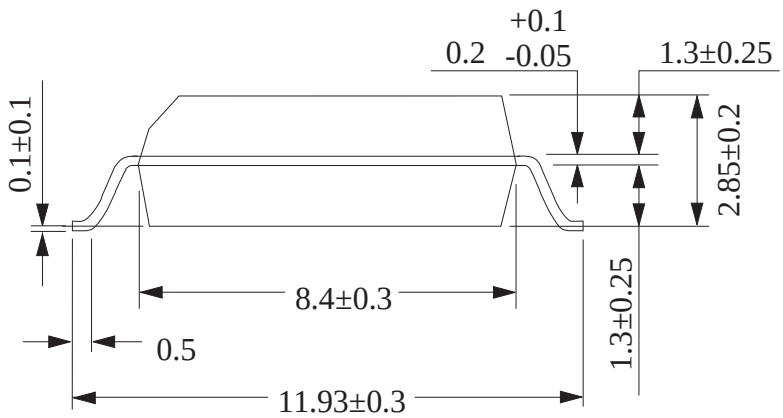
Pin Descriptions

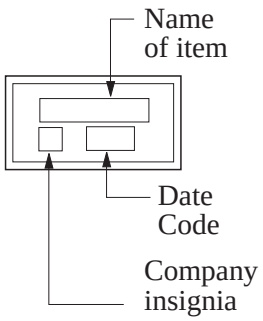
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	G/Y/CV-1 Input	13	U/SC-3 Input	25	V/SY OUT2
2	B/U/SC-1 Input	14	V/SY-3 Input	26	U/SC OUT2
3	R/V/SY-1 Input	15	L3 Input	27	Y/SY/CV OUT2
4	L1 Input	16	R3 Input	28	VCC2
5	R1 Input	17	Y/CV-4 Input	29	ROUT1
6	Y/CV-2 Input	18	U/SC-4 Input	30	LOUT1
7	U/SC-2 Input	19	V/SY-4 Input	31	V/SY OUT1
8	V/SY-2 Input	20	L4 Input	32	U/SC OUT1
9	L2 Input	21	R4 Input	33	Y/SY/CV OUT1
10	R2 Input	22	GND1	34	GND2
11	VCC1	23	ROUT2	35	SCL
12	Y/CV-3 Input	24	LOUT2	36	SDA

Package Name	USONF-36D

Unit : mm





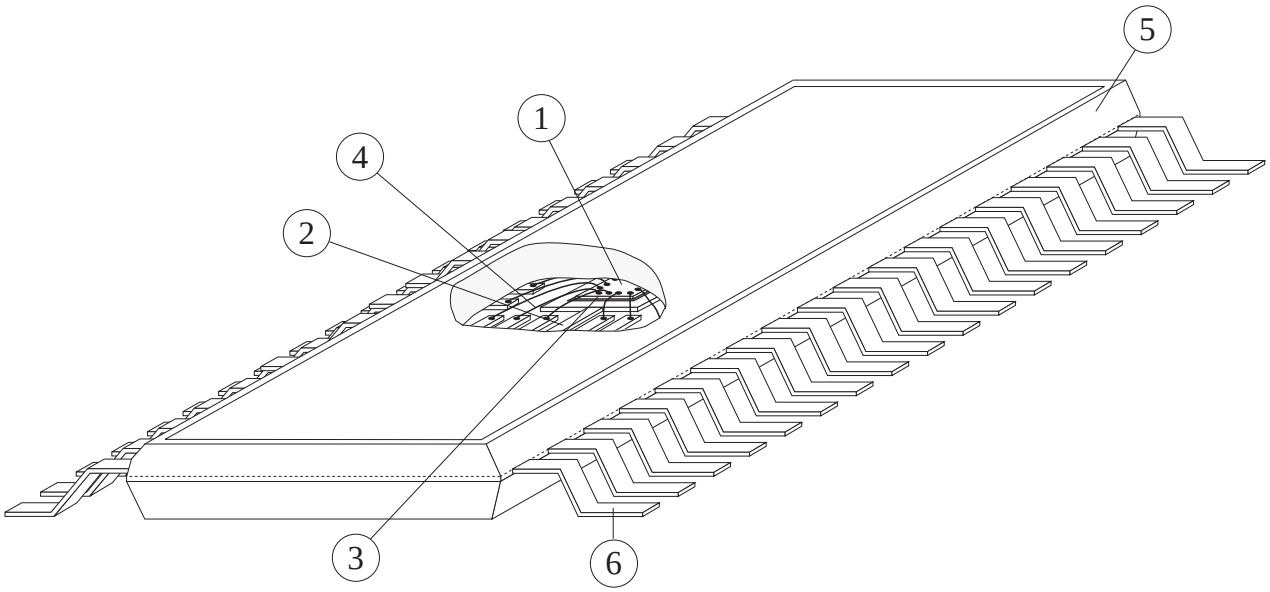


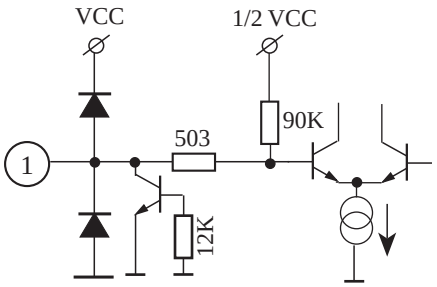
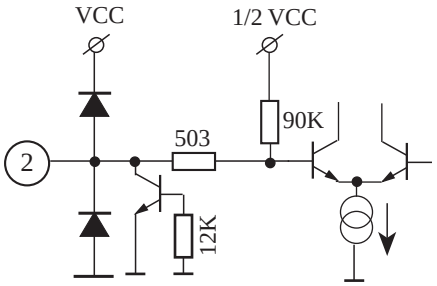
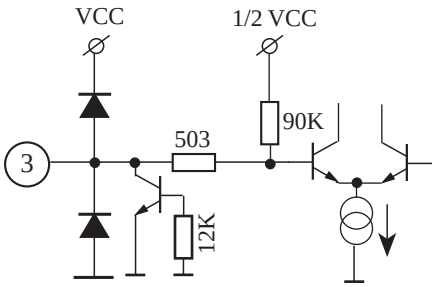
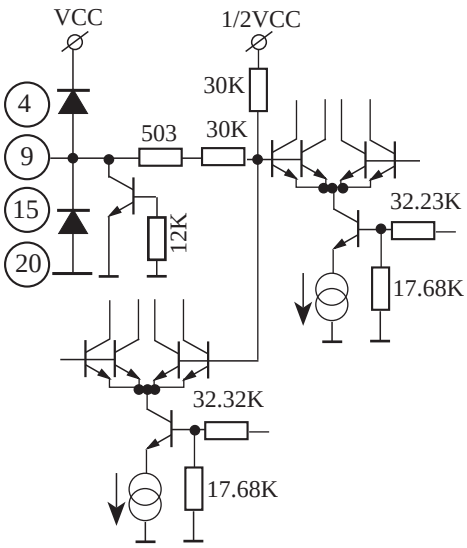
Eff. Date	Eff. Date	Eff. Date	Eff. Date
18 JAN 2002	6 MAR 2002	10 APR 2002	

(Structure Description)

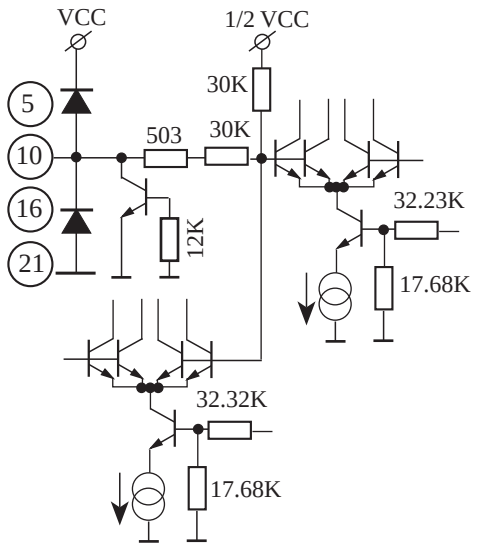
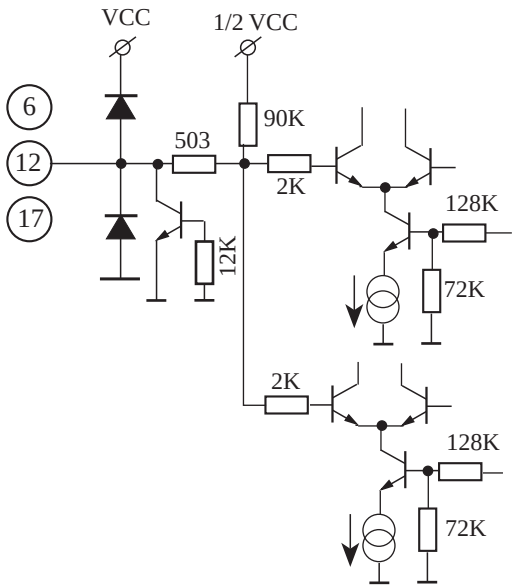
Chip surface passivation	[SiN,] PSG, Others ( )	(1)
Lead frame material	Fe group, [Cu group,] Others ( )	(2), (6)
Inner lead surface process	[Ag plating,] Au plating, Others ( )	(2)
Outer lead surface process	[Solder plating,] Solder dip, Others ( )	(6)
Chip mounting method	[Ag paste,] Au-Si alloy, Solder, Others ( )	(3)
Wire bonding method	[Ultrasonic heat bonding,] Others ( )	(4)
Wire material	[Au,] Diameter 24 μm Others ( )	(4)
Mold material	[Epoxy,] Others ( )	(5)
Molding method	Transfer mold, [Multiplunger mold,] Others ( )	(5)

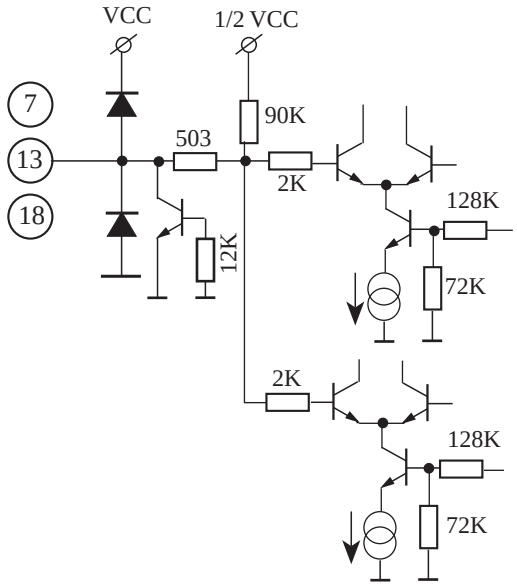
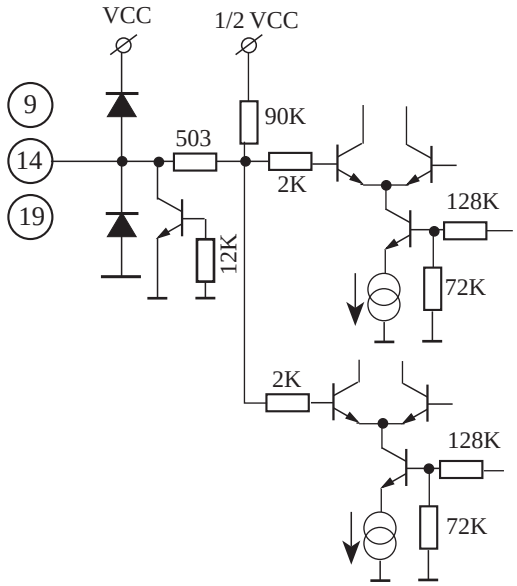
Package USONF-36D

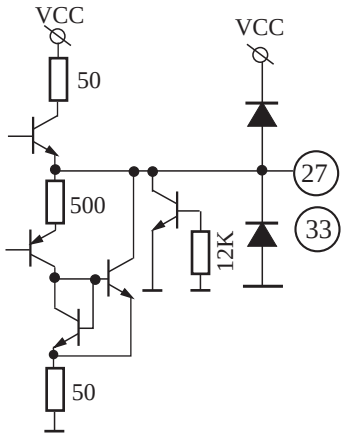
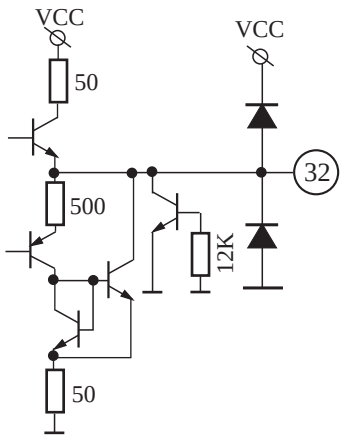
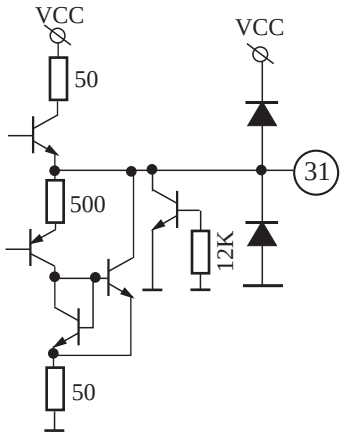


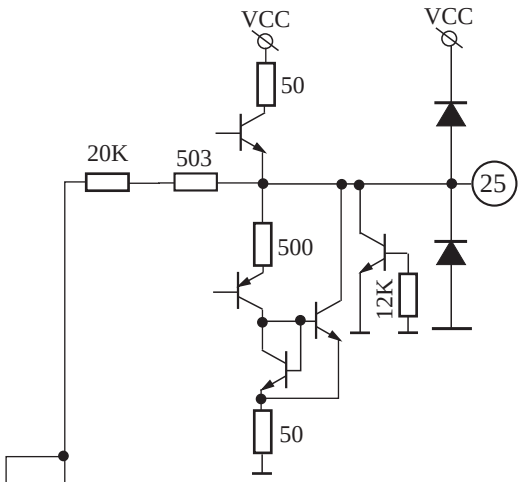
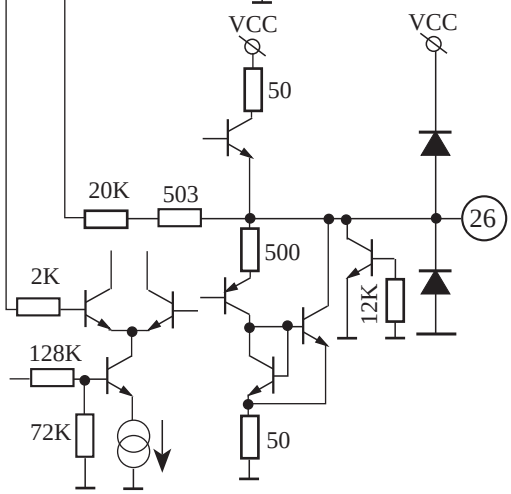
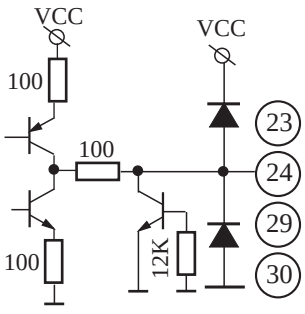
Pin No.	Pin Name	Pin Voltage	Description	Equivalent Circuit
1	G/Y/CV-1	4.5V	● Video signal input. ● Can be G, Y or Composite Video signal. ● Selectively controlled by IIC Bus to convert RGB to YUV.	
2	B/U/SC-1	4.5V	● Video signal input. ● Can be B, U or S-Video Chrominance (SC). ● Selectively controlled by IIC Bus to convert RGB to YUV.	
3	R/V/SY-1	4.5V	● Video signal input. ● Can be R, V or S-Video Luminance (SY). ● Selectively controlled by IIC Bus to convert RGB to YUV.	
4 9 15 20	L1 L2 L3 L4	4.7V	● Audio signal inputs.	

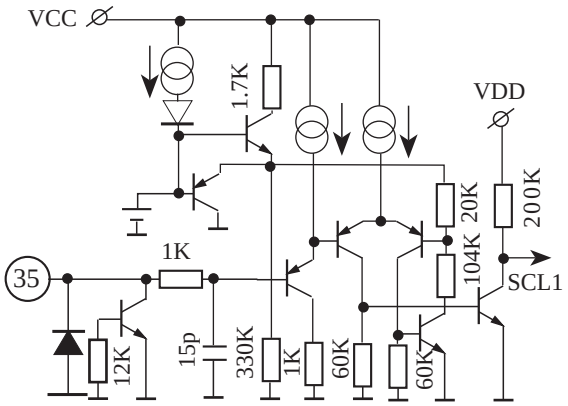
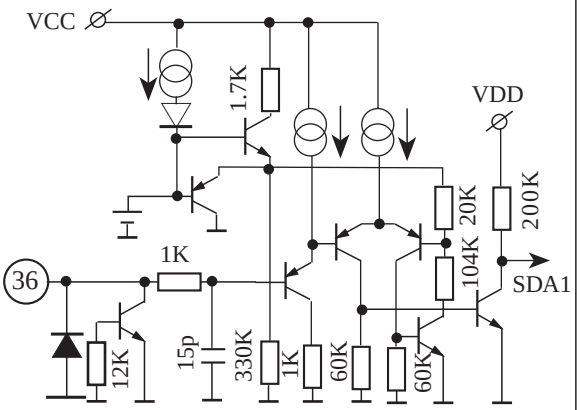
Note : Y = Component Video luminance
U = Component Video B-Y
V = Component Video R-Y

Pin No.	Pin Name	Pin Voltage	Description	Equivalent Circuit
5 10 16 21	R1 R2 R3 R4	4.7V	● Audio signal inputs.	
6 12 17	Y/CV-2 Y/CV-3 Y/CV-4	4.5V	● Video signal inputs. ● Can be Y or Composite Video.	

Pin No.	Pin Name	Pin Voltage	Description	Equivalent Circuit
7 13 18	U/SC-2 U/SC-3 U/SC-4	4.5V	• Video signal inputs. • Can be U or S-Video Chrominance (SC).	
8 14 19	V/SY-2 V/SY-3 V/SY-4	4.5V	• Video signal inputs. • Can be V or S-Video Luminance (SY).	

Pin No.	Pin Name	Pin Voltage	Description	Equivalent Circuit
27 33	Y/SY/CV OUT1 Y/SY/CV OUT2	4.5V	● Video signal output. ● Can be Y, S -Video Luminance (SY) or Composite Video depend on the input signal. ● Y/SY/CV OUT1 Video Gain of 4.4dB or 6dB selectively controlled by IIC Bus. ● Y/SY/CV OUT2 Video Gain of 4.4dB or 6dB selectively controlled by IIC Bus. ● Y/SY/CV OUT2 has additional feature of converting S- Video inputs to Composite Video selectively controlled by IIC Bus.	
32	U/SC OUT1	4.5V	● Video signal output. ● Can be U or S-Video Chrominance (SC) depend on the input signal. ● Video Gain of 4.4dB or 6dB selectively controlled by IIC Bus.	
31	V/SY OUT1	4.5V	● Video signal output. ● Can be V or S-Video Luminance (SY) depend on the input. ● Video Gain of 4.4dB or 6dB selectively controlled by IIC Bus. ● Video signal Mute selectively controlled by IIC Bus.	

Pin No.	Pin Name	Pin Voltage	Description	Equivalent Circuit
26	U/SC OUT2	4.5V	● Video signal output. ● Can be U or S-Video Chrominance (SC) output signal depend on the input signal. ● Video Gain of 0dB or 6dB selectively controlled by IIC Bus.	
25	V/SY OUT2	4.5V	● Video signal output. ● Can be V or S-Video Luminance (SY) output signal depend on the input signal. ● Video Gain of 0dB or 6dB selectively controlled by IIC Bus.	
23 24 29 30	ROUT2 LOUT2 ROUT1 LOUT1	4.7V	● Audio signal output.	

Pin No.	Pin Name	Pin Voltage	Description	Equivalent Circuit
35	SCL	-	● IIC Bus Clock input.	
36	SDA	-	● IIC Bus Data input.	

[I^2C BUS]

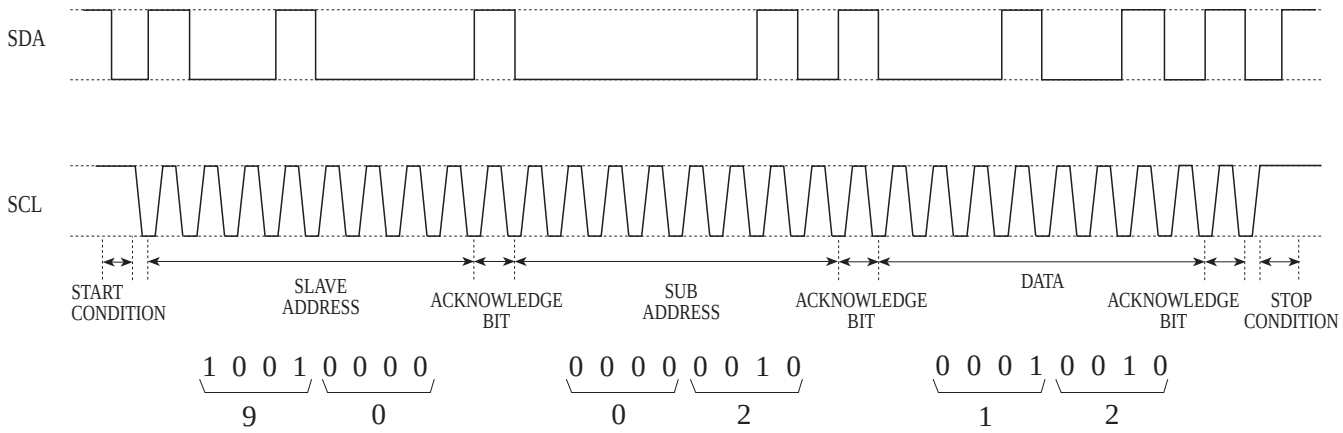


Fig.1 Example of transmission message

For transmission messages, both SCL and SDA are transferred in the form of synchronized serial transmission. SCL is a clock of a specific frequency, and SDA indicates address data for controlling the receiving side and is transferred in parallel, being synchronized with SCL. Data is transferred in principle in 3 octets (bytes), and each one octet (one octet = 8bits) includes one acknowledge bit. Frame structure is described below.

(a) Start Condition	The receiver becomes possible to receive data when SDA changes from HI to LO while SCL is HI.
(b) Stop Condition	The receiver halts receiving when SDA changes from LO to HI while SCL is HI.
(c) Slave Address	This is an address which is determined for each device. If other device address is sent, receiving will be halted.
(d) Sub Address	This is an address which is determined for each function.
(e) Data	This is control data.
(f) Acknowledge Bit	This is a bit by which the master acknowledges that data was successfully received in each octet. Master sends the HI signal and the receiver sends back the LO signal as shown in Figure1 with dotted line, causing the master to acknowledge the reception by the receiver. If the LO signal is not returned, communication will be halted.

Except Start and Stop conditions, SDA does not change while SCL is HI.

[I²C BUS ADDRESSING]

(1) This contains 12 SWs

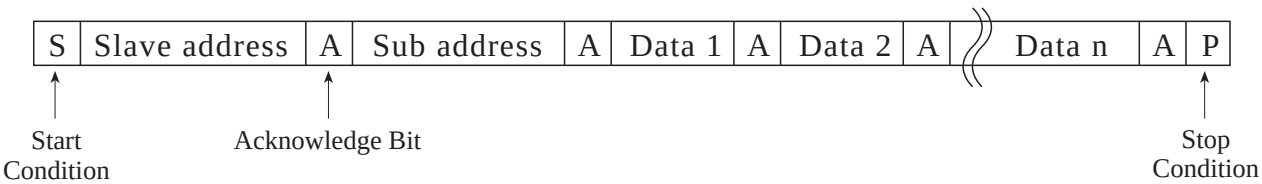
(2) Auto-increment function present :

- Sub address 0✱✱✱✱✱✱✱ : Auto-Increment Mode
  (When the data is sent in consecutive order, the Sub-address will be changed in consecutive order, as data is input.)
- Sub address 1✱✱✱✱✱✱✱ :Data Update Mode
  (When the data is sent consecutively, it is sent to the same Sub-address)

(3) I²C BUS PROTOCOL

- Slave address : 10010000 (90H)
- Format (Usual)

- Auto-Increment Mode/Data Update Mode



(4) Sub address byte and data byte format

Sub Address	Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
SLAVE	1	0	0	1	0	0	0	0
00	← V/SY OUT1 →		← U/SC OUT1 →		RGB/YUV SEL	← Y/SY/CV OUT1 →		
01	← V/SY OUT2 →		← U/SC OUT2 →		Mute V/SYOUT1	← Y/SY/CV OUT2 →		
02	← Gain Video OUT2 →		← Gain Video OUT1 →		← Audio OUT2 →		← Audio OUT1 →	

SUB-ADDRESS : 00

D2	D1	D0	Y/SY/CV OUT1
0	0	0	G/Y/CV-1 INPUT
0	0	1	Y/CV-2 INPUT
0	1	0	V/SY-2 INPUT
0	1	1	Y/CV-3 INPUT
1	0	0	V/SY-3 INPUT
1	0	1	Y/CV-4 INPUT
1	1	0	V/SY-4 INPUT
1	1	1	G/Y/CV-1 INPUT

SUB-ADDRESS : 00

D3	RGB/YUV SEL
1	Direct
0	RGB→YUV Converter

SUB-ADDRESS : 01

D2	D1	D0	Y/SY/CV OUT2
0	0	0	G/Y/CV-1 INPUT
0	0	1	Y/CV-2 INPUT
0	1	0	V/SY-2 INPUT
0	1	1	Y/CV-3 INPUT
1	0	0	V/SY-3 INPUT
1	0	1	Y/CV-4 INPUT
1	1	0	V/SY-4 INPUT
1	1	1	U/SC OUT2 + V/SY OUT2

SUB-ADDRESS : 01

D3	Mute V/SYOUT1
0	OFF
1	ON

SUB-ADDRESS : 00

D5	D4	U/SC OUT1
0	0	B/U/SC-1 INPUT
0	1	U/SC-2 INPUT
1	0	U/SC-3 INPUT
1	1	U/SC-4 INPUT

SUB-ADDRESS : 00

D7	D6	V/SY OUT1
0	0	R/V/SY-1 INPUT
0	1	V/SY-2 INPUT
1	0	V/SY-3 INPUT
1	1	V/SY-4 INPUT

SUB-ADDRESS : 01

D5	D4	U/SC OUT2
0	0	B/U/SC-1 INPUT
0	1	U/SC-2 INPUT
1	0	U/SC-3 INPUT
1	1	U/SC-4 INPUT

SUB-ADDRESS : 01

D7	D6	V/SY OUT2
0	0	R/V/SY-1 INPUT
0	1	V/SY-2 INPUT
1	0	V/SY-3 INPUT
1	1	V/SY-4 INPUT

SUB-ADDRESS : 02

D1	D0	LOUT1/ROUT1
0	0	LIN1, RIN1
0	1	LIN2, RIN2
1	0	LIN3, RIN3
1	1	LIN4, RIN4

SUB-ADDRESS : 02

D3	D2	LOUT2/ROUT2
0	0	LIN1, RIN1
0	1	LIN2, RIN2
1	0	LIN3, RIN3
1	1	LIN4, RIN4

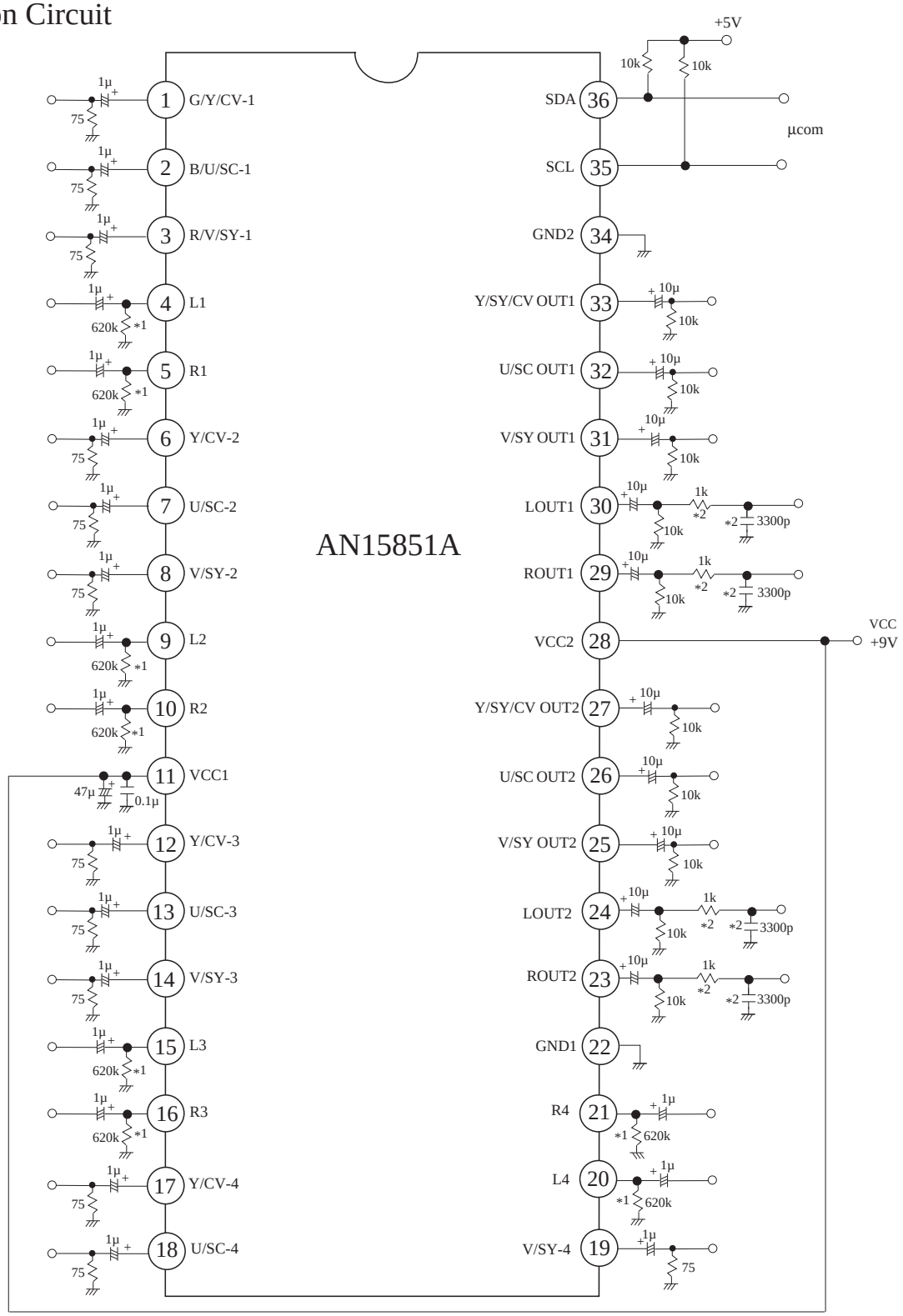
SUB-ADDRESS : 02

Gain Video OUT1		1	0
D4	Y/SY/CV OUT1	6.0dB	4.4dB
D5	U/SC and V/SY OUT1	4.4dB	6.0dB

SUB-ADDRESS : 02

Gain Video OUT2		1	0
D6	Y/SY/CV OUT2	6.0dB	0dB
D7	U/SC and V/SY OUT2	0dB	6.0dB

Application Circuit



Note : 1) The 620kΩ (*1) resistors are to improve Audio Input Dyanamic Range.
2) The 1kΩ resistors (*2) and 3300pF capacitors (*2) are for oscillation prevention.

Eff. Date	Eff. Date	Eff. Date	Eff. Date	Eff. Date
18 JAN 2002	6 MAR 2002	10 APR 2002		

(Precautions for use)

Make sure that the IC is not reverse mounted or pin shifted. The IC will be damaged under such conditions.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View AN15851A on WIN SOURCE
- Panasonic Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management