



**THE DATASHEET OF  
TPS65190RHDR**



## 10-Channel Level Shifter and VCOM Buffer

### FEATURES

- 10-Channel Level Shifter, Organized as Two Groups of 8 + 2 Channels
- Separate Positive Supplies ( $V_{GH}$ ) for Each Group
- $V_{GH}$  Levels up to 38V
- $V_{GL}$  Levels down to -13V
- Logic Level Inputs
- High Peak Output Currents
- High-Speed  $V_{COM}$  Buffer
- 28-Pin 5x5 mm QFN Package

### APPLICATIONS

- Large Format LCD Displays using GIP Technology

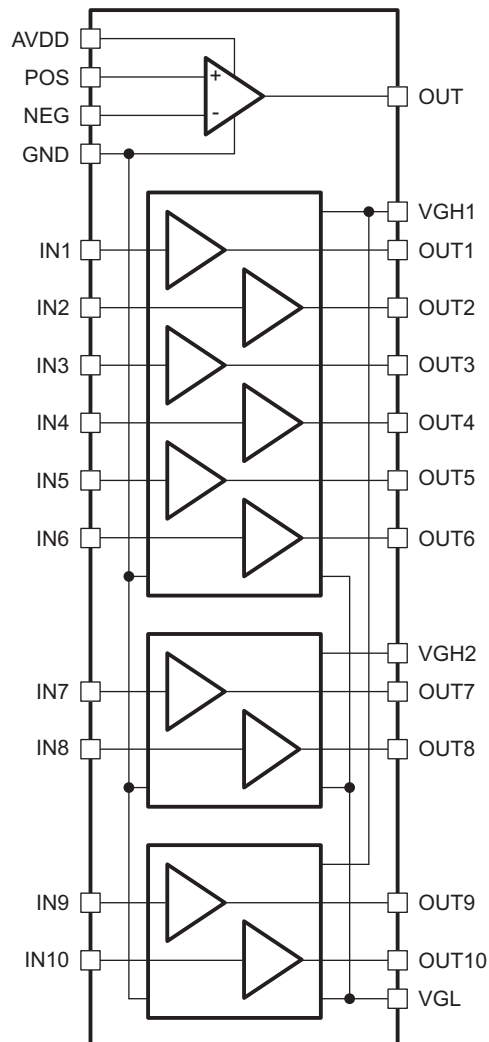
### DESCRIPTION

The TPS65190 is a combined multi-channel level-shifter and  $V_{COM}$  buffer intended for use in large format LCD display applications such as TVs and monitors. The device converts the logic-level signals generated by the Timing Controller (T-CON) to the high-level gate drive signals used by the display panel and amplifies/buffers an externally generated  $V_{COM}$  voltage.

The 10 level shifter channels are organized as 2 groups, each with its own positive supply. Channels 1-6 and 9-10 are supplied by  $V_{GH1}$  and channels 7-8 are supplied by  $V_{GH2}$ . The two positive supplies can be tied together if one positive supply voltage is used for all level shifter channels. Both level shifter groups use the same negative supply  $V_{GL}$ .

The level-shifters feature low impedance output stages that achieve fast rise and fall times even when driving significant capacitive loads.

The uncommitted high-speed operational amplifier features a high slew rate and high peak current capability that make it particularly suitable for driving the panel's common rail ( $V_{COM}$ ).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	ORDERING	PACKAGE	PACKAGE MARKING
-40 to 85°C	TPS65190RHDR	28-Pin QFN	TPS65190

(1) The device is supplied taped and reeled, with 3000 devices per reel.

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	VALUE	UNIT
Voltage on VGH1, VGH2 <sup>(2)</sup>	45	V
Voltage on VGL <sup>(2)</sup>	-15	V
Voltage on AVDD <sup>(2)</sup>	20	V
Voltage on IN1 through IN10 <sup>(2)</sup>	-0.3 to 7.0	V
Voltage on POS, NEG <sup>(2)</sup>	-0.3 to V <sub>AVDD</sub> + 0.3	V
Differential voltage between POS and NEG	±V <sub>AVDD</sub>	V
ESD Rating HBM	2	kV
ESD Rating MM	200	V
ESD Rating CDM	700	V
Continuous power dissipation	See Dissipation Rating Table	
T <sub>A</sub> Operating ambient temperature range	-40 to 85	°C
T <sub>J</sub> Operating junction temperature range	-40 to 150	°C
T <sub>STG</sub> Storage temperature range	-65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Voltage values are with respect to the GND pin

**DISSIPATION RATINGS**

PACKAGE	θ <sub>JA</sub>	T <sub>A</sub> ≤ 25°C POWER RATING	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
28-Pin QFN <sup>(1)</sup>	35 °C/W	3.57 W	2.29 W	1.86 W

(1) Refer to application section on how to improve thermal resistance θ<sub>JA</sub>.

**RECOMMENDED OPERATING CONDITIONS**

		MIN	TYP	MAX	UNIT
V <sub>GH1</sub>	Positive supply voltage range	12	30	38	V
V <sub>GH2</sub>		12	30	38	
V <sub>GL</sub>	Negative supply voltage range	-2	-6.2	-13	V
V <sub>IN</sub>	Level shifter input voltage range	3	3.3	5	V
V <sub>AVDD</sub>	Operational amplifier positive supply voltage range	8	15	20	V
V <sub>POS</sub> , V <sub>NEG</sub>	Operational amplifier common-mode input voltage range	1	0.5 x V <sub>AVDD</sub> -1		V
T <sub>A</sub>	Operating ambient temperature	-40		85	°C
T <sub>J</sub>	Operating junction temperature	-40		125	°C

**ELECTRICAL CHARACTERISTICS**
 $V_{GH1} = V_{GH2} = 30\text{ V}$ ;  $V_{GL} = -6.2\text{ V}$ ;  $V_{AVDD} = 15\text{ V}$ ;  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ ; typical values are at  $25\text{ }^\circ\text{C}$  unless otherwise noted.

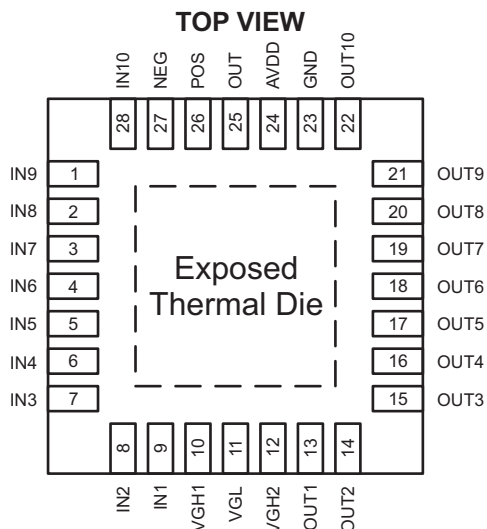
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LEVEL SHIFTER</b>						
$I_{GH1}$	$V_{GH1}$ Supply current	IN1 to IN10 = GND		0.18	1	mA
$I_{GH2}$	$V_{GH2}$ Supply current	IN1 to IN10 = GND		0.012	0.1	mA
$I_{GL}$	$V_{GL}$ Supply current	IN1 to IN10 = GND		0.015	0.1	mA
$I_{OUTX}$	Peak output current	Channels 1-8, sourcing		490		mA
		Channels 1-8, sinking		850		
		Channels 9-10, sourcing		250		
		Channels 9-10, sinking		450		
$I_{INX}$	Input current	Channels 1-10, inputs connected to GND		-0.003	$\pm 1$	$\mu\text{A}$
		Channels 1-10, inputs connected to 3.3 V		-0.002	$\pm 1$	
$V_{IH}$	High level input threshold	Channels 1 through 10			2.0	V
$V_{IL}$	Low level input threshold	Channels 1 through 10	0.5			V
$V_{DROPH}$	Output voltage drop high	Channels 1 through 8, $I_{OUT} = 10\text{ mA}$		0.19	0.4	V
		Channels 9 and 10, $I_{LOAD} = 10\text{ mA}$		0.36	1	
$V_{DROPL}$	Output voltage drop low	Channels 1 through 8, $I_{OUT} = -10\text{ mA}$		0.06	0.4	V
		Channels 9 and 10, $I_{OUT} = -10\text{ mA}$		0.11	1	
$t_R$	Rise time	Channels 1 through 8, $C_{OUT} = 4.7\text{ nF}^{(1)}$		404	600	ns
		Channels 9 and 10, $C_{OUT} = 4.7\text{ nF}^{(1)}$		740	950	
$t_F$	Fall time	Channels 1 through 8, $C_{OUT} = 4.7\text{ nF}^{(1)}$		192	370	ns
		Channels 9 and 10, $C_{OUT} = 4.7\text{ nF}^{(1)}$		377	700	
$t_{PH}$	Propagation delay	Rising edge, $C_{OUT} = 150\text{ pF}$		27		ns
$t_{PL}$		Falling edge, $C_{OUT} = 150\text{ pF}$		40		
<b>OPERATIONAL AMPLIFIER</b>						
$I_{AVDD}$	Supply current	$V_{CM} = 7.5\text{ V}$ , unity gain, no load		5.4		mA
$V_{OS}$	Input offset voltage	$V_{CM} = 7.5\text{ V}$		1	$\pm 20$	mV
$I_{IB}$	Input bias current	$V_{CM} = 7.5\text{ V}$		0.001	$\pm 0.1$	$\mu\text{A}$
$V_{CM}$	Common-mode input voltage range	$V_{AVDD} = 8\text{ V}$ to $20\text{ V}$	1		$V_{AVDD} - 1$	V
CMRR	Common mode rejection ratio	$V_{CM} = 1\text{ V}$ to $14\text{ V}$ , $1\text{ Hz}$ , no load		93		dB
$A_{VOL}$	Open loop gain	$V_{OUT} = 0.5\text{ V}$ to $14.5\text{ V}$ , no load		88		dB
$V_{DROPL}$	Output voltage drop low	$I_O = -10\text{ mA}$		52	200	mV
$V_{DROPH}$	Output voltage drop high	$I_O = 10\text{ mA}$		85	200	mV
PSRR	Power supply rejection ratio	Measured at $1\text{ Hz}$		90		dB
BW	Small signal unity gain bandwidth	$-3\text{ dB}$ , $V_{IN} = 100\text{ mV}_{PP}$		76		MHz
SR	Slew rate, rising	$A_V = 1$ , $V_{CM} = 7.5\text{ V}$ , $V_{IN} = 2\text{ V}_{PP}$		66		V/ $\mu\text{s}$
	Slew rate, falling			53		
$I_O$	Output current	Peak, $V_{CM} = 7.5\text{ V}$	$\pm 200$	$\pm 450$		mA
		$V_{OUT} = 13\text{ V}$ , sourcing	100	225		
		$V_{OUT} = 2\text{ V}$ , sinking	-100	317		
$I_{SC}$	Short circuit current	OUT shorted to GND or AVDD <sup>(2)</sup>	$\pm 250$	$\pm 498$	$\pm 900$	mA

(1) Rise and fall times are measured between 10% and 90% of the waveform's maximum amplitude.

(2) To prevent overheating, short-circuit conditions must not be allowed to persist indefinitely. The maximum allowable duration of short-circuit conditions will be determined by the IC's junction-to-ambient thermal resistance ( $\theta_{JA}$ ) and the ambient temperature of the application.

## DEVICE INFORMATION

### PIN ASSIGNMENT



### PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
IN9	1	I	Level shifter channel 9 input
IN8	2	I	Level shifter channel 8 input
IN7	3	I	Level shifter channel 7 input
IN6	4	I	Level shifter channel 6 input
IN5	5	I	Level shifter channel 5 input
IN4	6	I	Level shifter channel 4 input
IN3	7	I	Level shifter channel 3 input
IN2	8	I	Level shifter channel 2 input
IN1	9	I	Level shifter channel 1 input
VGH1	10	P	Positive supply for level shifter channels 1-6 and 9-10
VGL	11	P	Negative supply voltage for all level shifter channels
VGH2	12	P	Positive supply for level shifter channels 7-8
OUT1	13	O	Level shifter channel 1 output
OUT2	14	O	Level shifter channel 2 output
OUT3	15	O	Level shifter channel 3 output
OUT4	16	O	Level shifter channel 4 output
OUT5	17	O	Level shifter channel 5 output
OUT6	18	O	Level shifter channel 6 output
OUT7	19	O	Level shifter channel 7 output
OUT8	20	O	Level shifter channel 8 output
OUT9	21	O	Level shifter channel 9 output
OUT10	22	O	Level shifter channel 10 output
GND	23	P	Ground connection for level shifter and operational amplifier.
AVDD	24	P	Operational amplifier positive supply
OUT	25	O	Operational amplifier output
NEG	26	I	Operational amplifier inverting input
POS	27	I	Operational amplifier non-inverting input

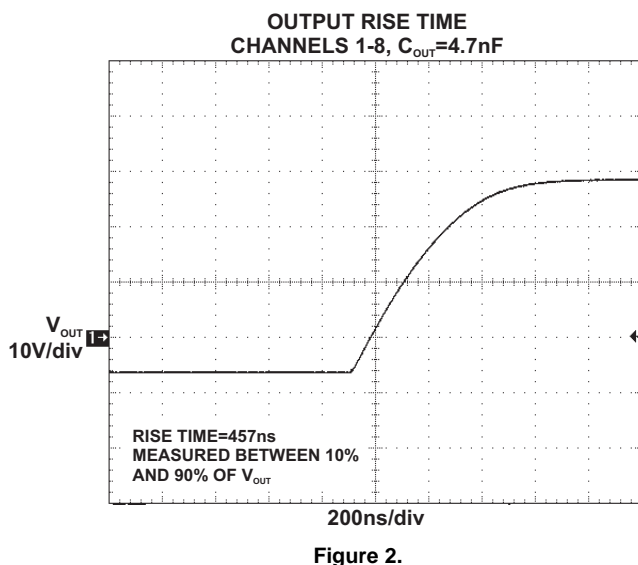
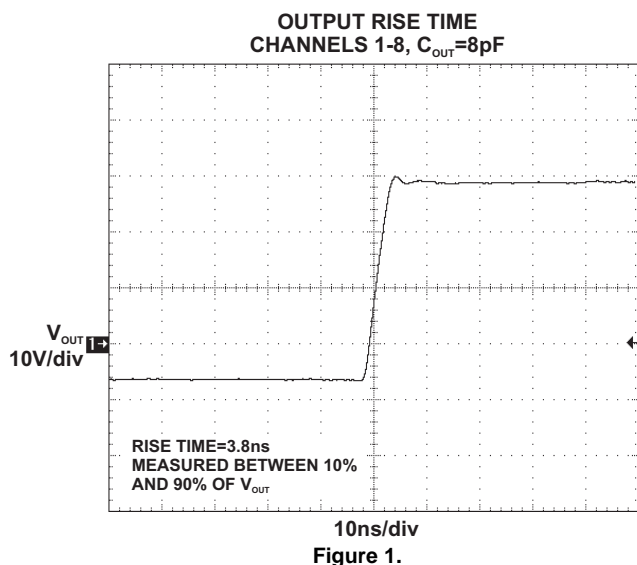
PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
IN10	28	I	Level shifter channel 10 input
Exposed Thermal Die		P	Connect to the system $V_{GL}$ connection.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

LEVEL SHIFTER		
Rise time	Channels 1-8, $C_{OUT} = 8 \text{ pF}$	Figure 1
	Channels 1-8, $C_{OUT} = 4.7 \text{ nF}$	Figure 2
	Channels 9-10, $C_{OUT} = 8 \text{ pF}$	Figure 3
	Channels 9-10, $C_{OUT} = 4.7 \text{ nF}$	Figure 4
Fall time	Channels 1-8, $C_{OUT} = 8 \text{ pF}$	Figure 5
	Channels 1-8, $C_{OUT} = 4.7 \text{ nF}$	Figure 6
	Channels 9-10, $C_{OUT} = 8 \text{ pF}$	Figure 7
	Channels 9-10, $C_{OUT} = 4.7 \text{ nF}$	Figure 8
Propagation delay, channels 1 to 8	Channels 1-8, rising, $C_{OUT} = 8 \text{ pF}$	Figure 9
	Channels 1-8, falling, $C_{OUT} = 8 \text{ pF}$	Figure 10
	Channels 9-10, rising, $C_{OUT} = 8 \text{ pF}$	Figure 11
	Channels 9-10, falling, $C_{OUT} = 8 \text{ pF}$	Figure 12
Peak output current	Channels 1-8, $C_{OUT} = 10 \text{ nF}$	Figure 13
	Channels 9-10, $C_{OUT} = 10 \text{ nF}$	Figure 14
Output voltage drop	Output low	Figure 15
	Output high	Figure 16
OPERATIONAL AMPLIFIER		
Small signal frequency response	$V_{CM} = 7.5 \text{ V}$ , $V_{IN} = 100 \text{ mV}_{PP}$	Figure 17
Output voltage drop		Figure 18
Slew rate	Output rising, $C_{OUT} = 150 \text{ pF}$	Figure 19
	Output falling, $C_{OUT} = 150 \text{ pF}$	Figure 20



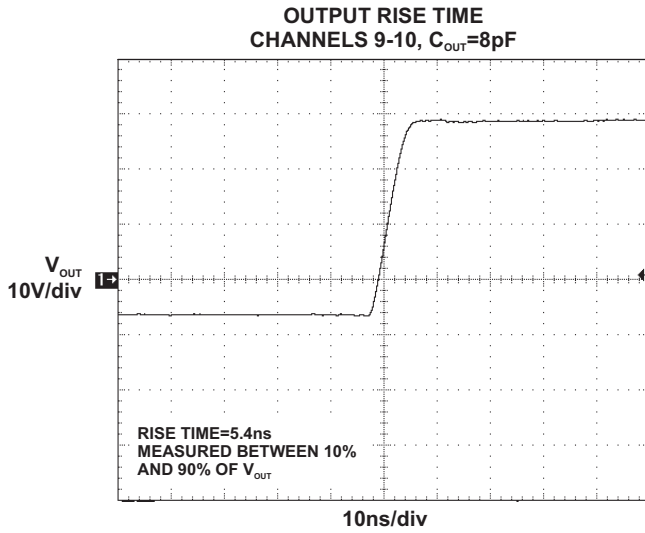


Figure 3.

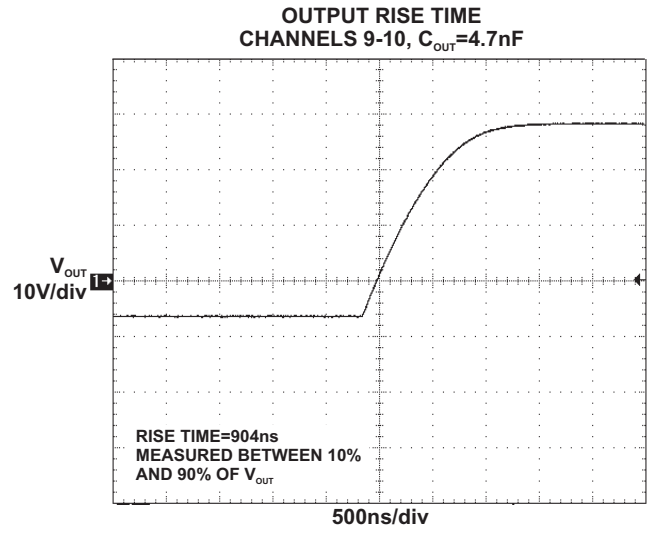


Figure 4.

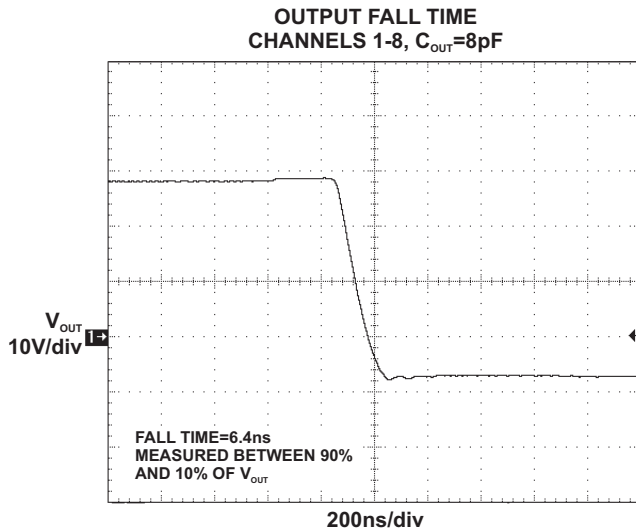


Figure 5.

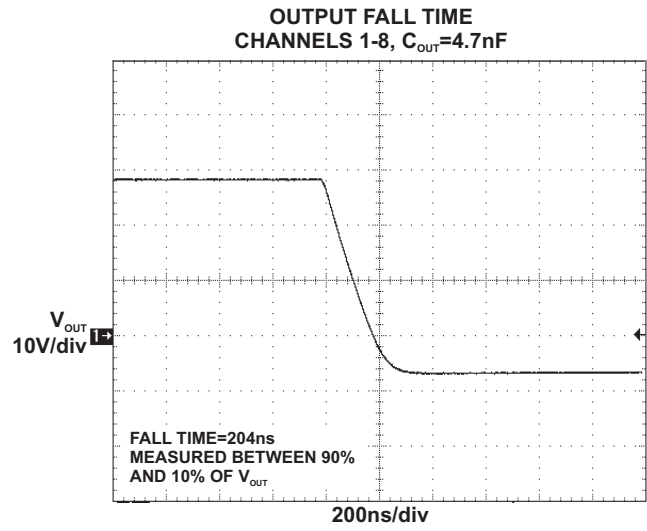


Figure 6.

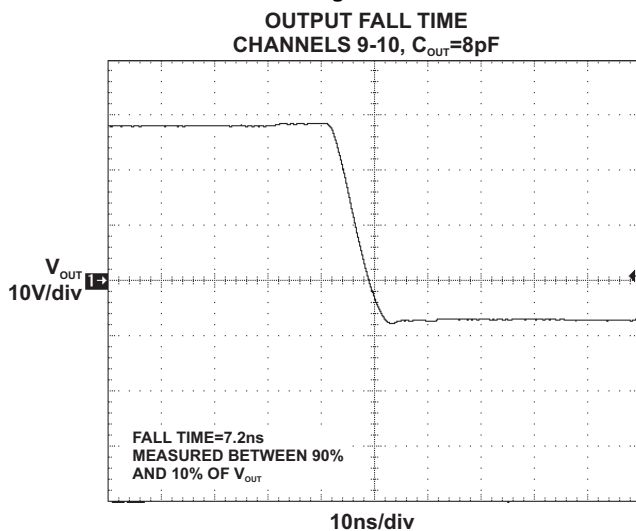


Figure 7.

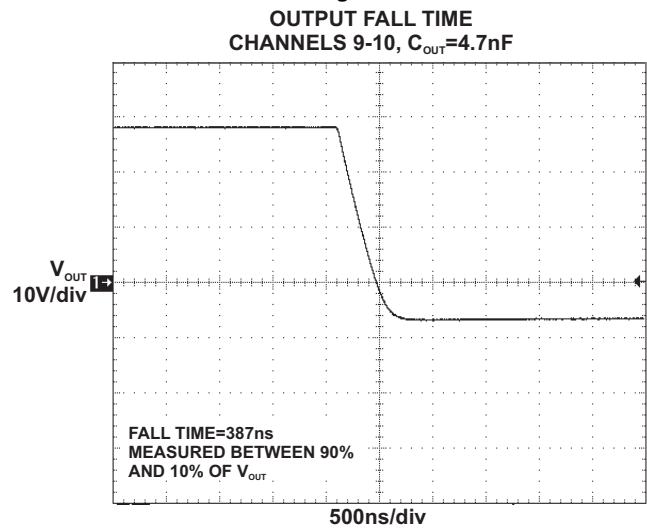
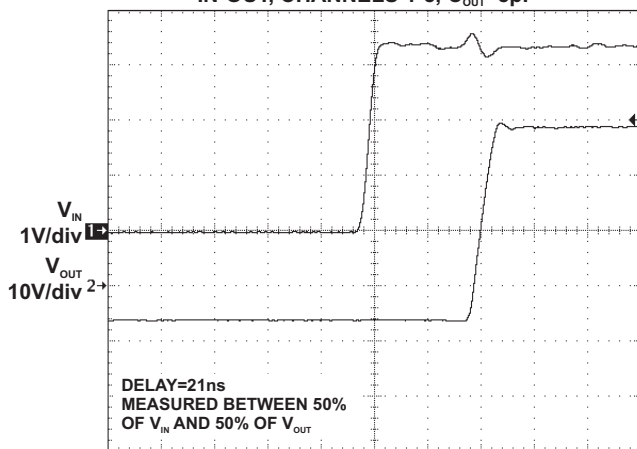


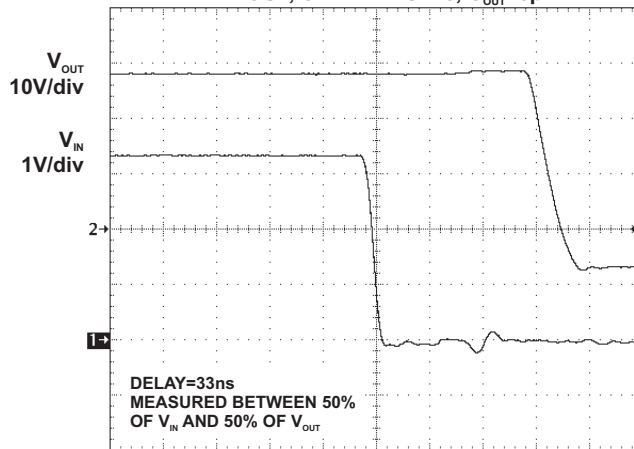
Figure 8.

PROPAGATION DELAY – RISING  
IN-OUT, CHANNELS 1-8,  $C_{OUT}=8pF$



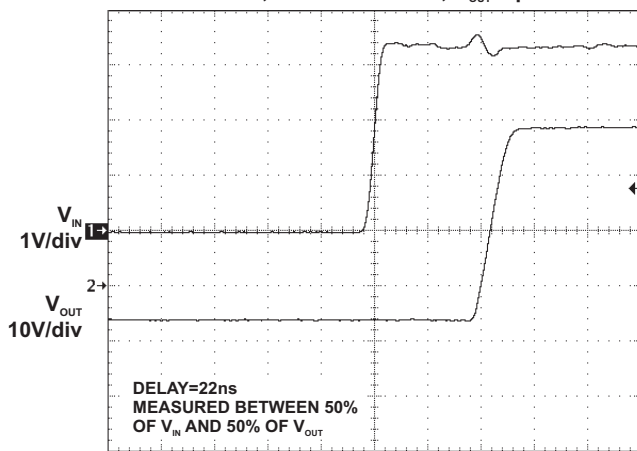
10ns/div  
Figure 9.

PROPAGATION DELAY – FALLING  
IN-OUT, CHANNELS 1-8,  $C_{OUT}=8pF$



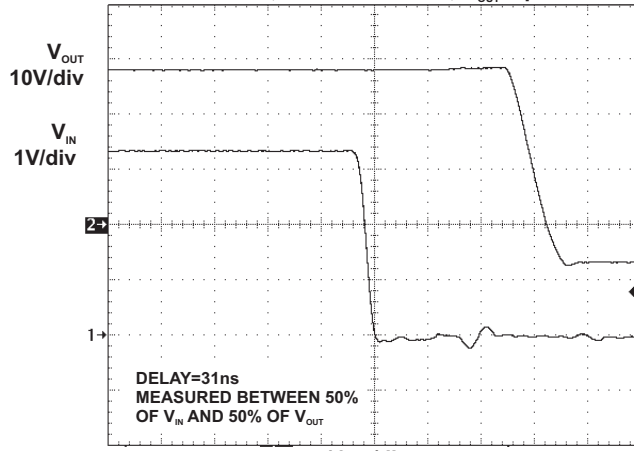
10ns/div  
Figure 10.

PROPAGATION DELAY – RISING  
IN-OUT, CHANNELS 9-10,  $C_{OUT}=8pF$



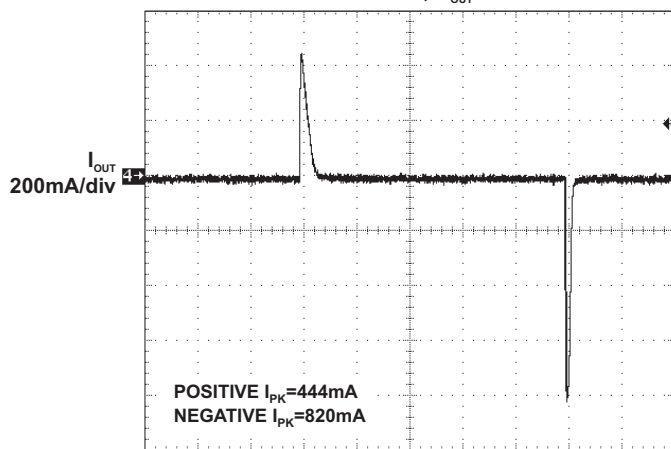
10ns/div  
Figure 11.

PROPAGATION DELAY – FALLING  
IN-OUT, CHANNELS 9-10,  $C_{OUT}=8pF$



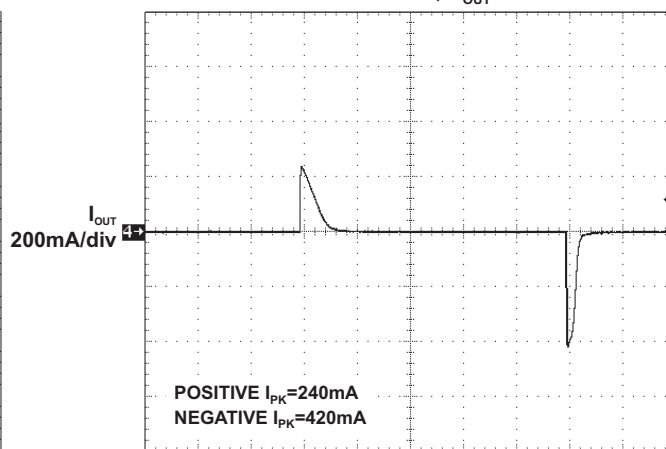
10ns/div  
Figure 12.

PEAK OUTPUT CURRENT  
CHANNELS 1-8,  $C_{OUT}=10nF$



5μs/div  
Figure 13.

PEAK OUTPUT CURRENT  
CHANNELS 9-10,  $C_{OUT}=10nF$



5μs/div  
Figure 14.

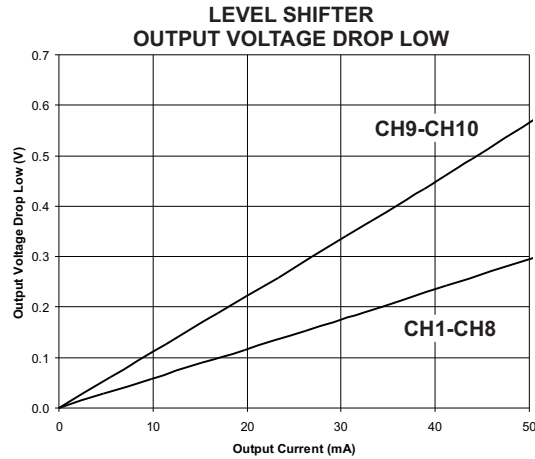


Figure 15.

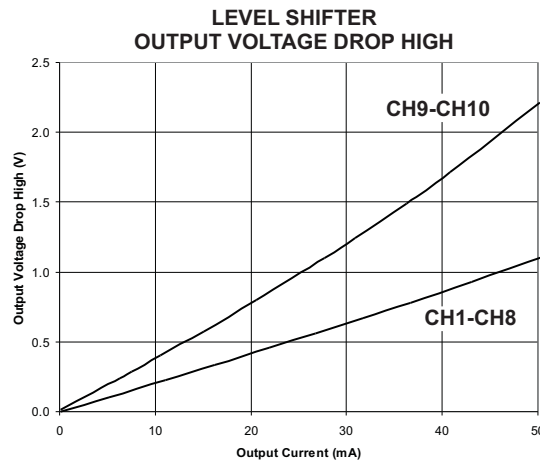


Figure 16.

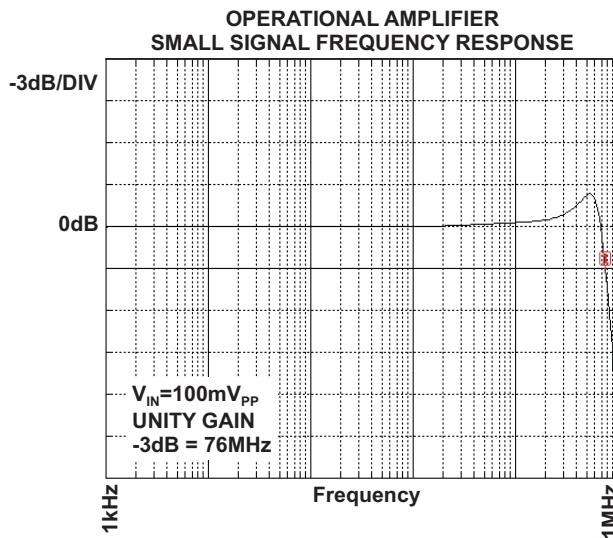


Figure 17.

OPERATIONAL AMPLIFIER  
OUTPUT VOLTAGE DROP

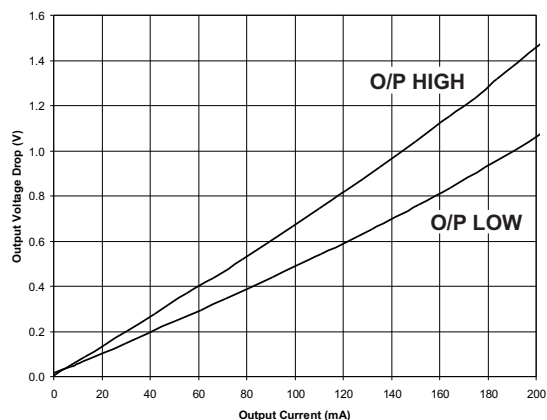


Figure 18.

OPERATIONAL AMPLIFIER  
POSITIVE SLEW RATE,  $C_{OUT}=150pF$

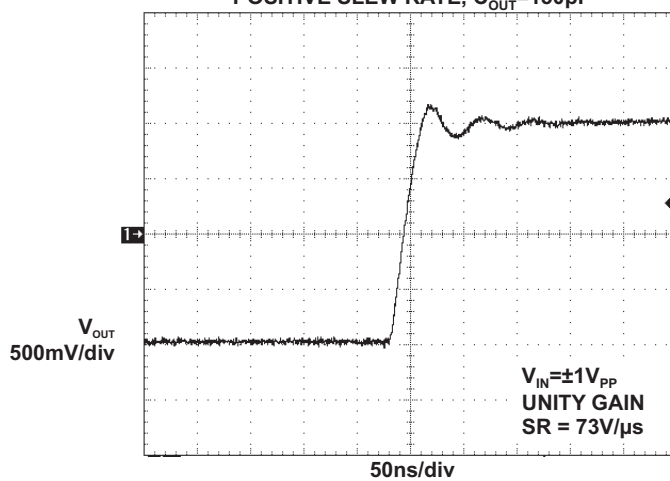


Figure 19.

OPERATIONAL AMPLIFIER  
NEGATIVE SLEW RATE,  $C_{OUT}=150pF$

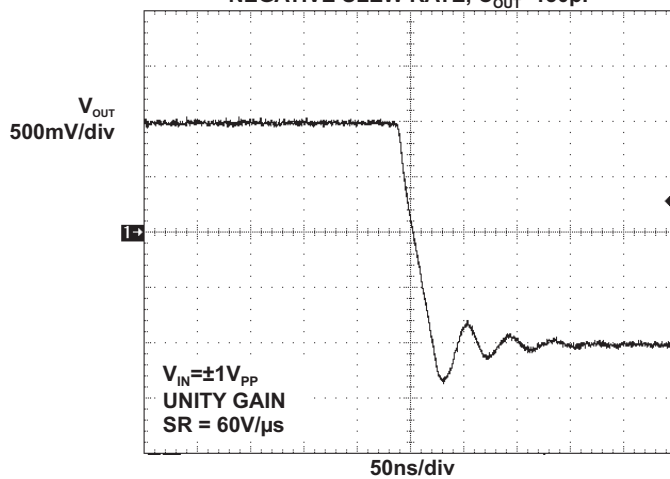


Figure 20.

## DETAILED DESCRIPTION

The TPS65190 contains 10 level shifter channels and one high-speed operational amplifier.

The 10 level shifter channels are organized in two groups: the first group, comprising channels 1-6 and 9-10 is powered from  $V_{VGH1}$  and  $V_{VGL}$ ; the second group, comprising channels 7 and 8 is powered from  $V_{VGH2}$  and  $V_{VGL}$ . Channels 1 to 8 are optimized for high speed operation while channels 9 and 10 operate a little slower.

All level shifter channels feature the same input circuitry and are compatible with the standard logic-level signals generated by timing controllers in typical applications. The output circuitry has been designed to achieve high rise and fall times when driving the capacitive loads typically encountered in LCD display applications

The input and output stages of the operational amplifier extend close to both supply rails and the output stage has been optimized to supply the fast transient currents typical in  $V_{COM}$  applications.

## APPLICATION INFORMATION

It is recommended to use high quality ceramic capacitors to decouple each supply pin. In typical applications 10  $\mu\text{F}$  is recommended for  $V_{VGH1}$  and  $V_{VGL}$ , while 1  $\mu\text{F}$  is normally sufficient for  $V_{VGH2}$ .

Use level shifter channels 1 to 8 for high-speed clock signals and use channels 9 to 10 for lower-speed signals (see Figure 14). The inputs of any unused level shifter channels should be tied to GND. The outputs of any unused level shifter channels should be left floating.

It is recommended to use low-value feedback resistors with the VCOM buffer to minimize the effects of stray capacitance at its inverting input. Using high value feedback resistors can cause excessive peaking in the amplifier's gain response (caused by pole formed by the feedback resistor and the stray capacitance). If the VCOM buffer is used in a unity gain configuration, the flattest gain response is achieved using a direct connection between the amplifier's output and inverting input.

If the VCOM buffer is not used, tie AVDD, its inverting and non-inverting inputs, and its output to GND.

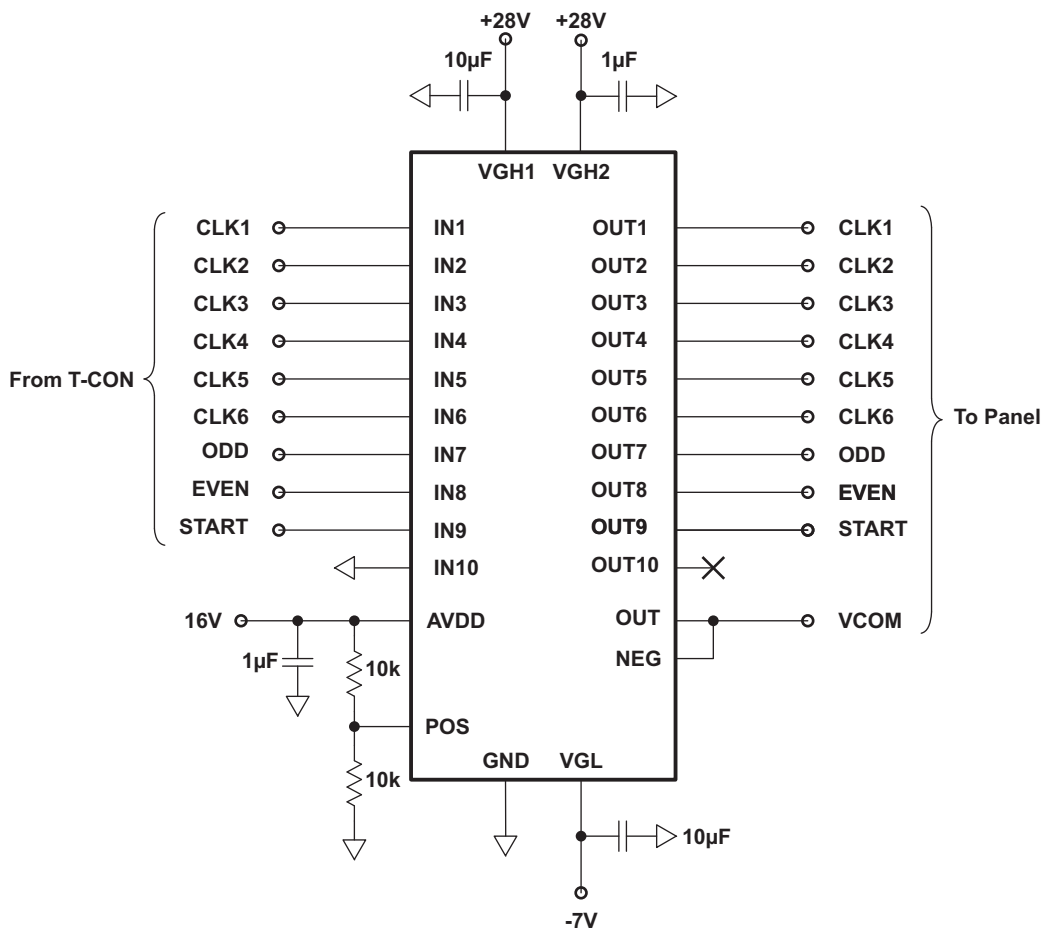


Figure 21. Typical Application Circuit

## PCB LAYOUT

Proper PCB layout is essential if the TPS65190's specified performance is to be achieved, and the following basic steps should be followed as a minimum:

1. Use high quality ceramic decoupling capacitors, placed as close as possible to the IC pins they are decoupling
2. Use short, wide tracks to route power to the IC
3. Ensure that the PCB's thermal design is adequate to dissipate power away from the IC

The TPS65190 is supplied in a 28-Pin QFN thermally enhanced package designed to eliminate the use of bulky heat sinks and slugs. In order to benefit from these superior thermal properties PCB layout and manufacturing should follow the guidelines contained in the following application reports, available for free download from <http://www.ti.com>.

- Application Report – QFN Layout Guidelines ([SLOA122](#))
- Application Report – QFN/SON PCB Attachment ([SLUA271A](#))

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS65190RHDR	ACTIVE	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65190	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65190RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65190RHDR	VQFN	RHD	28	3000	367.0	367.0	35.0

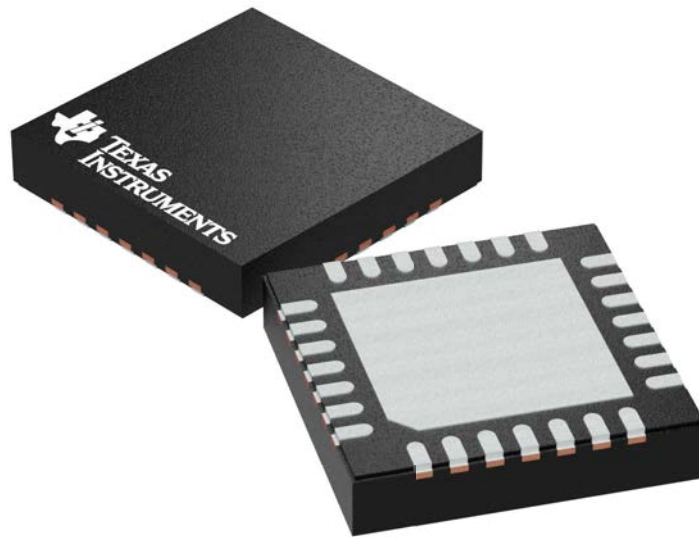
**GENERIC PACKAGE VIEW**

**RHD 28**

**VQFN - 1 mm max height**

**5 x 5 mm, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD



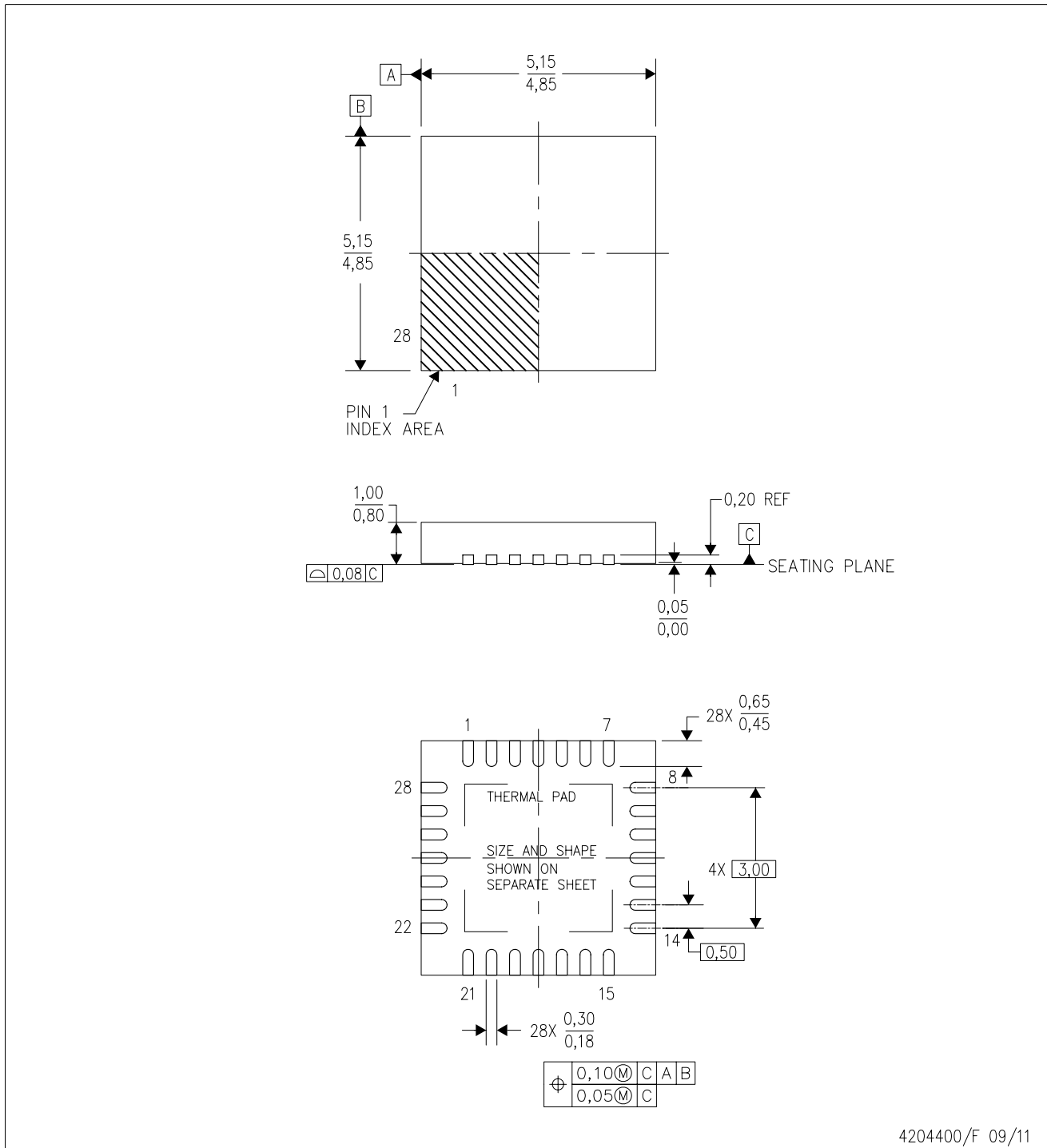
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204400/G

# MECHANICAL DATA

RHD (S-PVQFN-N28)

PLASTIC QUAD FLATPACK NO-LEAD



4204400/F 09/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) Package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-220.

## THERMAL PAD MECHANICAL DATA

RHD (S-PVQFN-N28)

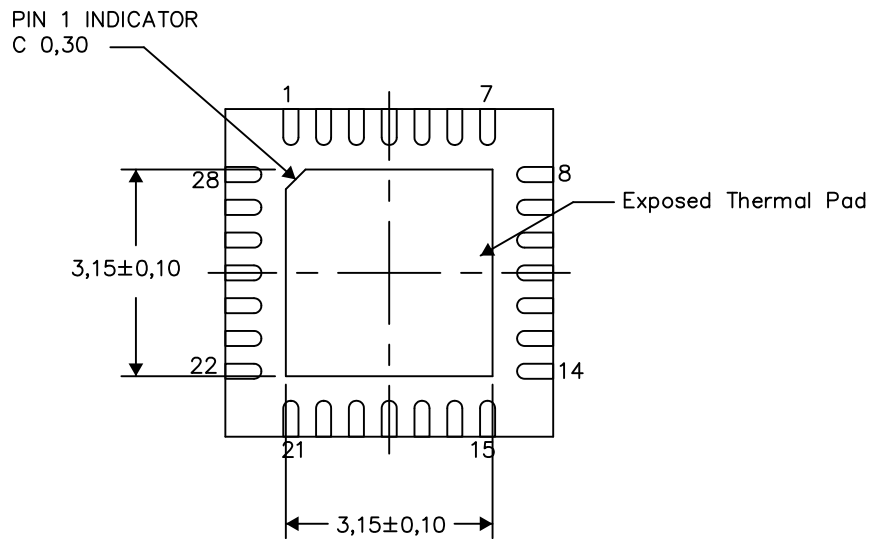
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206358-2/L 05/15

NOTE: All linear dimensions are in millimeters



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