



**THE DATASHEET OF  
MC100LVEL92DW**



# MC100LVEL92

## 5 V Triple PECL Input to LVPECL Output Translator

### Description

The MC100LVEL92 is a triple PECL input to LVPECL output translator. The device receives standard PECL signals and translates them to differential LVPECL output signals.

To accomplish the PECL to LVPECL level translation, the MC100LVEL92 requires three power rails. The  $V_{CC}$  supply is to be connected to the standard 5 V PECL supply, the  $LV_{CC}$  supply is to be connected to the 3.3 V LVPECL supply, and Ground is connected to the system ground plane. Both the  $V_{CC}$  and  $LV_{CC}$  should be bypassed to ground with 0.01  $\mu$ F capacitors.

The PECL  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

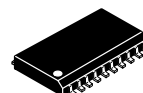
### Features

- 500 ps Propagation Delays
- 5 V and 3.3 V Supplies Required
- ESD Protection: Human Body Model; > 2 kV, Machine Model; > 200 V
- The 100 Series Contains Temperature Compensation
- LVPECL Operating Range:  $LV_{CC} = 3.0$  V to 3.8 V
- PECL Operating Range:  $V_{CC} = 4.5$  V to 5.5 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or < GND + 1.3 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity: Level 3 (Pb-Free)  
For Additional Information, see Application Note [AND8003/D](#)
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index 28 to 34
- Transistor Count = 247 devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



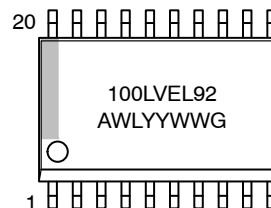
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SOIC-20 WB  
DW SUFFIX  
CASE 751D

### MARKING DIAGRAM\*



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

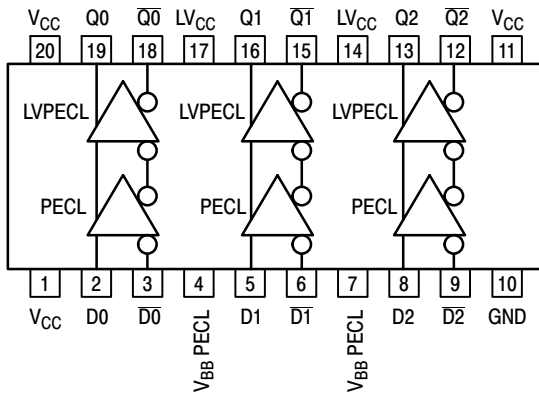
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

Device	Package	Shipping†
MC100LVEL92DWG	SOIC-20 WB (Pb-Free)	38 Units/Tube
MC100LVEL92DWR2G	SOIC-20 WB (Pb-Free)	1000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MC100LEVEL92



**Table 1. PIN DESCRIPTION**

PIN	FUNCTION
Dn, $\overline{Dn}$	PECL Inputs
Qn, $\overline{Qn}$	LVPECL Outputs
PECL $V_{BB}$	PECL Reference Voltage Output
LVCC	LVPECL Power Supply
VCC	PECL Power Supply
GND	Common Ground Rail

Warning: All V<sub>CC</sub>, LV<sub>CC</sub>, and GND pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. Logic Diagram and Pinout: SO-20 WB (Top View)**

**Table 2. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Power Supply	GND = 0 V		8 to 0	V
LV <sub>CC</sub>	LVPECL Power Supply	GND = 0 V		8 to 0	V
V <sub>I</sub>	PECL Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	6 to 0	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA
I <sub>BB</sub>	PECL V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-20 WB	90 60	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-20 WB	30 to 35	°C/W
T <sub>sol</sub>	Wave Solder (Pb-Free)	< 2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

# MC100LEVEL92

**Table 3. PECL INPUT DC CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ;  $LV_{CC} = 3.3\text{ V}$ ;  $GND = 0\text{ V}$  Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{V_{CC}}$	PECL Power Supply Current			12			12			12	mA
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3190		3515	3190		3525	3190		3525	mV
PECL $V_{BB}$	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 2)										V
	$V_{pp} < 500\text{ mV}$	1.3		4.8	1.2		4.8	1.2		4.8	
	$V_{pp} \geq 500\text{ mV}$	1.5		4.8	1.4		4.8	1.4		4.8	
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current										$\mu\text{A}$
	D	0.5			0.5			0.5			
	$\bar{D}$	-600			-600			-600			

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input parameters vary 1:1 with  $V_{CC}$ .  $V_{CC}$  can vary 4.5 V to 5.5 V.
2.  $V_{IHCMR}$  min varies 1:1 with GND.  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1.0 V.

**Table 4. LVPECL OUTPUT DC CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ;  $LV_{CC} = 3.3\text{ V}$ ;  $GND = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{LV_{CC}}$	LVPECL Power Supply Current			20			20			21	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
$V_{OL}$	Output LOW Voltage (Note 2)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Output parameters vary 1:1 with  $LV_{CC}$ .  $V_{CC}$  can vary 3.0 V to 3.8 V.
2. Outputs are terminated through a 50  $\Omega$  resistor to  $LV_{CC} - 2.0\text{ V}$ .

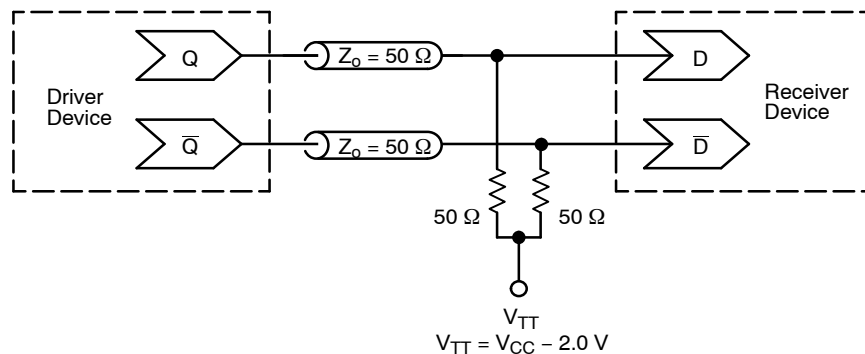
# MC100LEVEL92

**Table 5. AC CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ;  $LV_{CC} = 3.3\text{ V}$ ;  $GND = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay Diff D to Q S.E.	490 440	590 590	690 740	510 460	610 610	710 760	530 480	630 630	730 780	ps
$t_{SKEW}$	Skew Output-to-Output (Note 2) Part-to-Part (Diff) (Note 2) Duty Cycle (Diff) (Note 3)		20 20 25	100 200		20 20 25	100 200		20 20 25	100 200	ps
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$V_{PP}$	Input Swing (Note 4)	150		1000	150		1000	150		1000	mV
$t_r$ $t_f$	Output Rise/Fall Times Q (20% – 80%)	270		530	270		530	270		530	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1.  $LV_{CC}$  can vary 3.0 V to 3.8 V;  $V_{CC}$  can vary 4.5 V to 5.5 V. Outputs are terminated through a 50  $\Omega$  resistor to  $LV_{CC} - 2.0\text{ V}$ .
2. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.
3. Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.
4.  $V_{PP}(\min)$  is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of  $\approx 40$ .

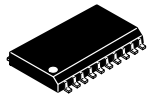


**Figure 2. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

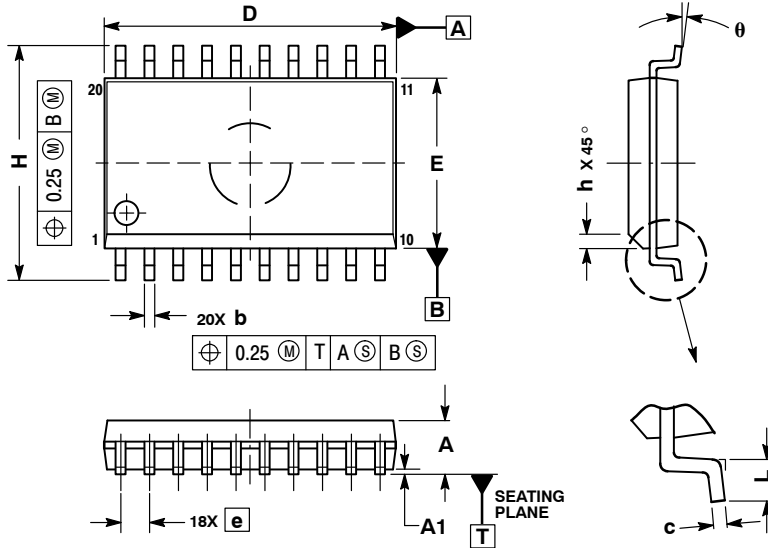
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015

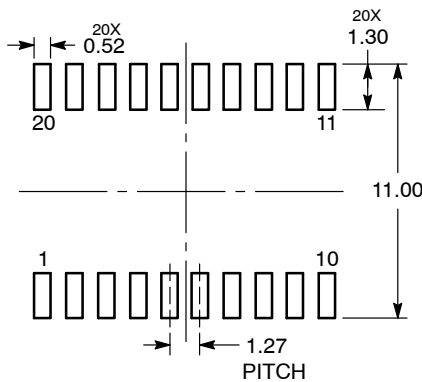


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

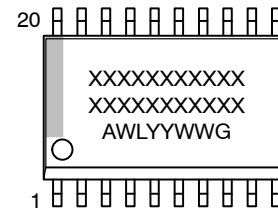
RECOMMENDED  
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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