

OPA188 Precision, Low-Noise, Rail-to-Rail Output, 36-V, Zero-Drift Operational Amplifier

1 Features

- Low offset voltage: 25 μV (maximum)
- Zero drift: 0.03 $\mu\text{V}/^\circ\text{C}$
- Low noise: 8.8 $\text{nV}/\sqrt{\text{Hz}}$
 - 0.1-Hz to 10-Hz Noise: 0.25 μV_{PP}
- Excellent dc precision:
 - PSRR: 142 dB
 - CMRR: 146 dB
 - Open-loop gain: 136 dB
- Gain bandwidth: 2 MHz
- Quiescent current: 510 μA (Maximum)
- Wide supply range: $\pm 2\text{ V}$ to $\pm 18\text{ V}$
- Rail-to-rail output
- Input includes negative rail
- RFI filtered inputs
- *MicroSIZE* packages

2 Applications

- [Weight scale](#)
- [Analog input module](#)
- [Flow transmitter](#)
- [Battery test](#)
- [DC power supply, ac source, electronic load](#)
- [Data acquisition \(DAQ\)](#)
- [Semiconductor test](#)

3 Description

The OPA188 operational amplifier uses TI's proprietary auto-zeroing techniques to provide low offset voltage (25- μV maximum) and near [zero-drift](#) over time and temperature. This miniature, high-precision, low-quiescent current amplifier offers high input impedance and rail-to-rail output swing within 15 mV of the rails. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range from 4 V to 36 V ($\pm 2\text{ V}$ to $\pm 18\text{ V}$).

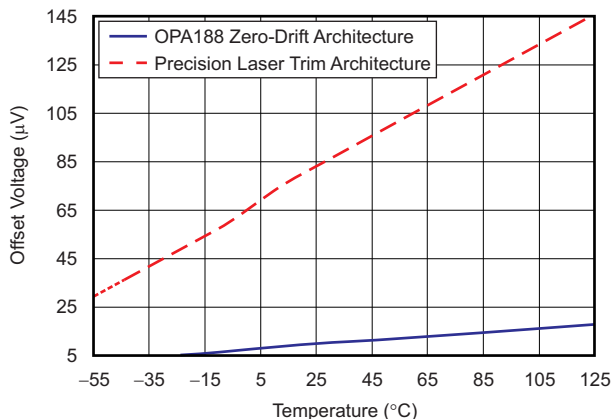
The single version is available in the *MicroSIZE* SOT-23-5, MSOP-8, and SO-8 packages. All versions are specified for operation from -40°C to $+125^\circ\text{C}$.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA188	SOIC (8)	4.90 mm x 3.91 mm
	SOT-23 (5)	2.90 mm x 1.60 mm
	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Auto-Zero Technology Provides Ultra-Low Temperature Drift



5 Device Comparison Table

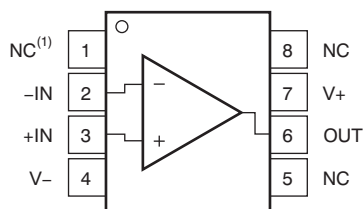
5.1 Portfolio Comparison

Table 1. Zero-Drift Amplifier Portfolio

VERSION	PRODUCT	OFFSET VOLTAGE (μV , maximum)	OFFSET VOLTAGE DRIFT ($\mu\text{V}/^\circ\text{C}$, maximum)	BANDWIDTH (MHz)	INPUT VOLTAGE NOISE (μV_{PP} , $f = 0.1 \text{ Hz to } 10 \text{ Hz}$)
Single	OPA188 (4 V to 36 V)	± 25	± 0.085	2	0.25
	OPA333 (5 V)	± 10	± 0.05	0.35	1.1
	OPA378 (5 V)	± 50	± 0.25	0.9	0.4
	OPA735 (12 V)	± 5	± 0.05	1.6	2.5
Dual	OPA2188 (4 V to 36 V)	± 25	± 0.085	2	0.25
	OPA2333 (5 V)	± 10	± 0.05	0.35	1.1
	OPA2378 (5 V)	± 50	± 0.25	0.9	0.4
	OPA2735 (12 V)	± 5	± 0.05	1.6	2.5
Quad	OPA4330 (5 V)	± 50	± 0.25	0.35	1.1

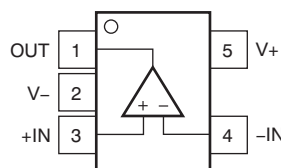
6 Pin Configuration and Functions

OPA188 D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



(1) NC = no connection.

OPA188 DBV Package
5-Pin SOT-23
Top View



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	D, DGK	DBV		
+IN	3	3	I	Noninverting input
-IN	2	4	I	Inverting input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V+	7	5	—	Positive (highest) power supply
V-	4	2	—	Negative (lowest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Voltage	Supply	Split supply	±20		V
		Single supply	40		
	Signal input pins ⁽²⁾		(V-) - 0.5	(V+) + 0.5	
		Differential	±0.7		
Current	Signal input pins ⁽²⁾		±10		mA
	Output short-circuit ⁽³⁾		Continuous		
Temperature	Operating ⁽⁴⁾ , T _A		-55	150	°C
	Junction, T _J			150	
	Storage, T _{stg}		-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.
- (3) Short-circuit to ground, V-, or V+.
- (4) Provided device does not exceed maximum junction temperature (T_J) at any time.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _S	Operating voltage range	Split supply	±2		±18	V
		Single supply	4		36	
T _A	Specified temperature range		-40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		OPA188			UNIT
		D (SO)	DBV (SOT23)	DGK (MSOP)	
		8 PINS	5 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	122.0	158.8	180.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	68.5	60.7	67.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	63.5	44.8	102.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	13.7	1.6	10.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	62.8	44.2	100.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics: High-Voltage Operation

at $T_A = +25^\circ\text{C}$, $V_S = \pm 4\text{ V}$ to $\pm 18\text{ V}$ ($V_S = 8\text{ V}$ to 36 V), $R_L = 10\text{ k}\Omega$ connected to $V_S / 2^{(1)}$, and $V_{CM} = V_{OUT} = V_S / 2^{(1)}$ (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			± 6	± 25	μV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 0.03	± 0.085	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 4\text{ V}$ to 36 V , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 0.075	± 0.3	$\mu\text{V}/\text{V}$
	Long-term stability ⁽²⁾			4		μV
INPUT BIAS CURRENT						
I_B	Input bias current	$V_{CM} = V_S / 2$		± 160	± 1400	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 18	nA
I_{OS}	Input offset current			± 320	± 2800	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 6	nA
NOISE						
e_n	Input voltage noise	$f = 0.1\text{ Hz}$ to 10 Hz		250		nV _{PP}
		$f = 0.1\text{ Hz}$ to 10 Hz		40		nV _{rms}
	Input voltage noise density	$f = 1\text{ kHz}$		8.8		nV/ $\sqrt{\text{Hz}}$
i_n	Input current noise density	$f = 1\text{ kHz}$		7		fA/ $\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	V^-		$(V^+) - 1.5$	V
CMRR	Common-mode rejection ratio	$(V^-) < V_{CM} < (V^+) - 1.5\text{ V}$	120	134		dB
		$(V^-) + 0.5\text{ V} < V_{CM} < (V^+) - 1.5\text{ V}$, $V_S = \pm 18\text{ V}$	130	146		dB
		$(V^-) + 0.5\text{ V} < V_{CM} < (V^+) - 1.5\text{ V}$, $V_S = \pm 18\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	120	126		dB
INPUT IMPEDANCE						
Z_{ID}	Differential			100 6		M Ω pF
Z_{IC}	Common-mode			6 9.5		$10^{12}\ \Omega$ pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$(V^-) + 0.5\text{ V} < V_O < (V^+) - 0.5\text{ V}$	130	136		dB
		$(V^-) + 0.5\text{ V} < V_O < (V^+) - 0.5\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	120	126		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			2		MHz
SR	Slew rate	$G = +1$		0.8		V/ μs
t_S	Settling time	0.1%	$V_S = \pm 18\text{ V}$, $G = 1$, 10-V step	20		μs
		0.01%	$V_S = \pm 18\text{ V}$, $G = 1$, 10-V step	27		μs
t_{OR}	Overload recovery time	$V_{IN} \times G = V_S$		1		μs
THD+N	Total harmonic distortion + noise	1 kHz, $G = 1$, $V_{OUT} = 1\text{ V}_{rms}$		0.0001%		
OUTPUT						
Voltage output swing from rail		No load		6	15	mV
		$R_L = 10\text{ k}\Omega$		220	250	mV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		310	350	mV
I_{SC}	Short-circuit current	Sinking		-18		mA
		Sourcing		16		mA
R_O	Open-loop output resistance	$f = 1\text{ MHz}$, $I_O = 0$		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
I_Q	Quiescent current (per amplifier)	$V_S = \pm 4\text{ V}$ to $V_S = \pm 18\text{ V}$		450	510	μA
		$I_O = 0\text{ mA}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			600	μA

(1) $V_S / 2 = \text{midsupply}$.

(2) 1000-hour life test at 125°C demonstrated randomly distributed variation in the range of measurement limits—approximately $4\ \mu\text{V}$.

7.6 Electrical Characteristics: Low-Voltage Operation

at $T_A = 25^\circ\text{C}$, $V_S = \pm 2\text{ V}$ to $< \pm 4\text{ V}$ ($V_S = 4\text{ V}$ to $< 8\text{ V}$), $R_L = 10\text{ k}\Omega$ connected to $V_S / 2^{(1)}$, and $V_{CM} = V_{OUT} = V_S / 2^{(1)}$ (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			± 6	± 25	μV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 0.03	± 0.085	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 4\text{ V}$ to 36 V , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.075	0.3	$\mu\text{V}/\text{V}$
	Long-term stability ⁽²⁾			4		μV
INPUT BIAS CURRENT						
I_B	Input bias current			± 160	± 1400	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 18	nA
I_{OS}	Input offset current			± 320	± 2800	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 6	nA
NOISE						
e_n	Input voltage noise	$f = 0.1\text{ Hz}$ to 10 Hz		250		nV_{PP}
		$f = 0.1\text{ Hz}$ to 10 Hz		40		nV_{rms}
	Input voltage noise density	$f = 1\text{ kHz}$		8.8		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input current noise density	$f = 1\text{ kHz}$		7		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	V^-		$(V^+) - 1.5$	V
CMRR	Common-mode rejection ratio	$(V^-) < V_{CM} < (V^+) - 1.5\text{ V}$	106	114		dB
		$(V^-) + 0.5\text{ V} < V_{CM} < (V^+) - 1.5\text{ V}$, $V_S = \pm 2\text{ V}$	114	120		dB
		$(V^-) + 0.5\text{ V} < V_{CM} < (V^+) - 1.5\text{ V}$, $V_S = \pm 2\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	110	120		dB
INPUT IMPEDANCE						
Z_{ID}	Differential			$100 \parallel 6$		$\text{M}\Omega \parallel \text{pF}$
Z_{IC}	Common-mode			$6 \parallel 9.5$		$10^{12}\ \Omega \parallel \text{pF}$
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$(V^-) + 0.5\text{ V} < V_O < (V^+) - 0.5\text{ V}$, $R_L = 5\text{ k}\Omega$	110	120		dB
		$(V^-) + 0.5\text{ V} < V_O < (V^+) - 0.5\text{ V}$	120	130		dB
		$(V^-) + 0.5\text{ V} < V_O < (V^+) - 0.5\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	110	120		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			2		MHz
SR	Slew rate	$G = +1$		0.8		$\text{V}/\mu\text{s}$
t_{OR}	Overload recovery time	$V_{IN} \times G = V_S$		1		μs
THD+N	Total harmonic distortion + noise	1 kHz, $G = 1$, $V_{OUT} = 1\text{ V}_{rms}$		0.0001%		
OUTPUT						
	Voltage output swing from rail	No load		6	15	mV
		$R_L = 10\text{ k}\Omega$		220	250	mV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		310	350	mV
I_{SC}	Short-circuit current	Sinking		-18		mA
		Sourcing		16		mA
R_O	Open-loop output resistance	$f = 1\text{ MHz}$, $I_O = 0$		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
I_Q	Quiescent current (per amplifier)	$V_S = \pm 2\text{ V}$ to $V_S = \pm 4\text{ V}$		425	485	μA
		$I_O = 0\text{ mA}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			575	μA

(1) $V_S / 2 = \text{midsupply}$.

(2) 1000-hour life test at 125°C demonstrated randomly distributed variation in the range of measurement limits—approximately $4\ \mu\text{V}$.

7.7 Typical Characteristics: Table of Graphs

7.7.1 Table of Graphs

Table 2. Typical Characteristic Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature	Figure 3
Offset Voltage vs Common-Mode Voltage	Figure 4, Figure 5
Offset Voltage vs Power Supply	Figure 6
Open-Loop Gain and Phase vs Frequency	Figure 7
Closed-Loop Gain vs Frequency	Figure 8
I_B and I_{OS} vs Common-Mode Voltage	Figure 9
Input Bias Current vs Temperature	Figure 10
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 11
CMRR and PSRR vs Frequency (Referred-to-Input)	Figure 12
CMRR vs Temperature	Figure 13, Figure 14
PSRR vs Temperature	Figure 15
0.1-Hz to 10-Hz Noise	Figure 16
Input Voltage Noise Spectral Density vs Frequency	Figure 17
THD+N Ratio vs Frequency	Figure 18
THD+N vs Output Amplitude	Figure 19
Quiescent Current vs Supply Voltage	Figure 20
Quiescent Current vs Temperature	Figure 21
Open-Loop Gain vs Temperature	Figure 22
Open-Loop Output Impedance vs Frequency	Figure 23
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 24, Figure 25
No Phase Reversal	Figure 26
Positive Overload Recovery	Figure 27
Negative Overload Recovery	Figure 28
Small-Signal Step Response (100 mV)	Figure 29, Figure 30
Large-Signal Step Response	Figure 31, Figure 32
Large-Signal Settling Time (10-V Positive Step)	Figure 33
Large-Signal Settling Time (10-V Negative Step)	Figure 34
Short-Circuit Current vs Temperature	Figure 35
Maximum Output Voltage vs Frequency	Figure 36
EMIRR IN+ vs Frequency	Figure 37

7.8 Typical Characteristics

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

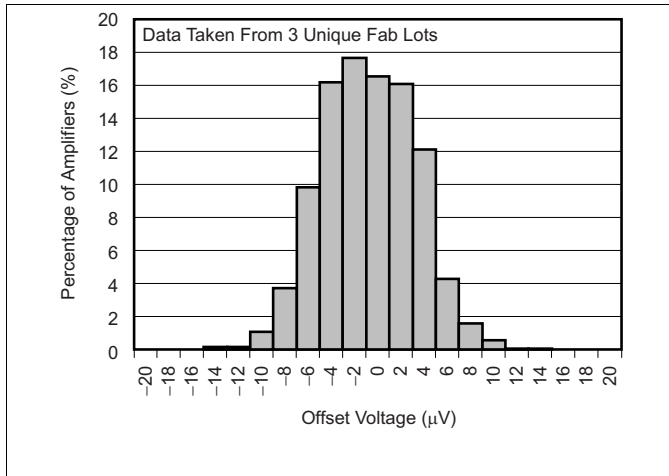


Figure 1. Offset Voltage Production Distribution

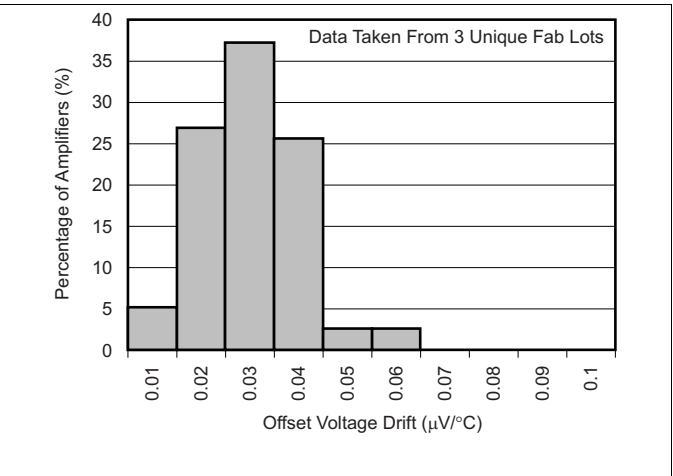


Figure 2. Offset Voltage Drift Distribution

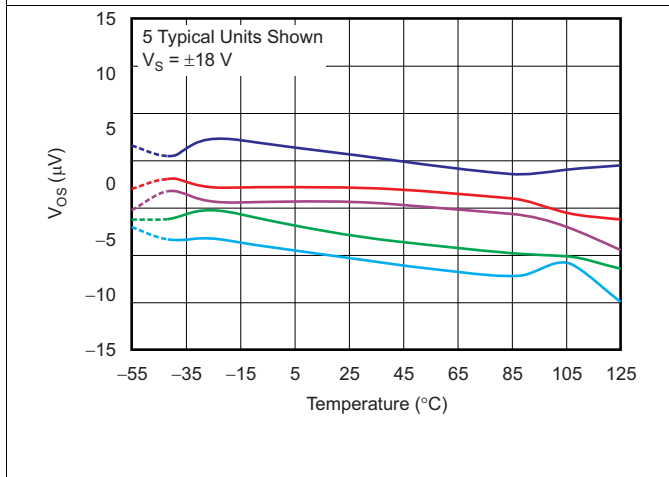


Figure 3. Offset Voltage vs Temperature

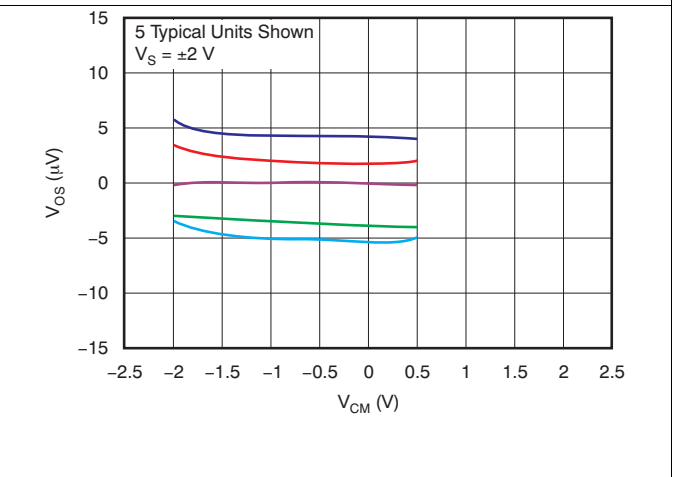


Figure 4. Offset Voltage vs Common-Mode Voltage

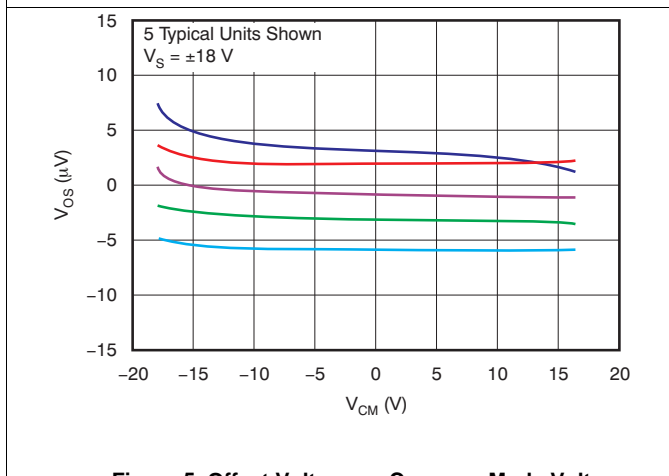


Figure 5. Offset Voltage vs Common-Mode Voltage

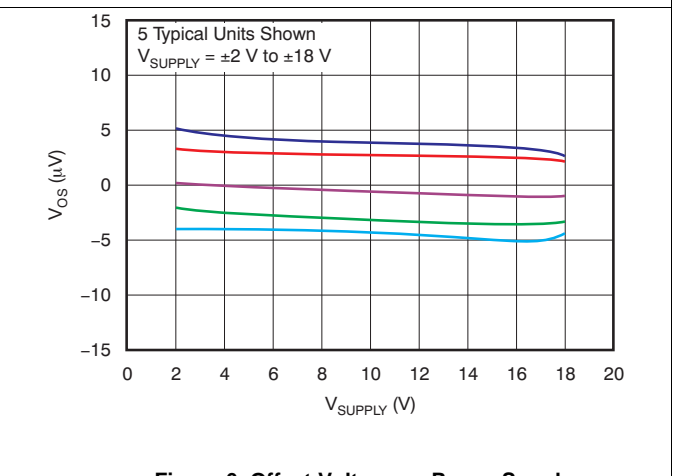


Figure 6. Offset Voltage vs Power Supply

Typical Characteristics (continued)

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

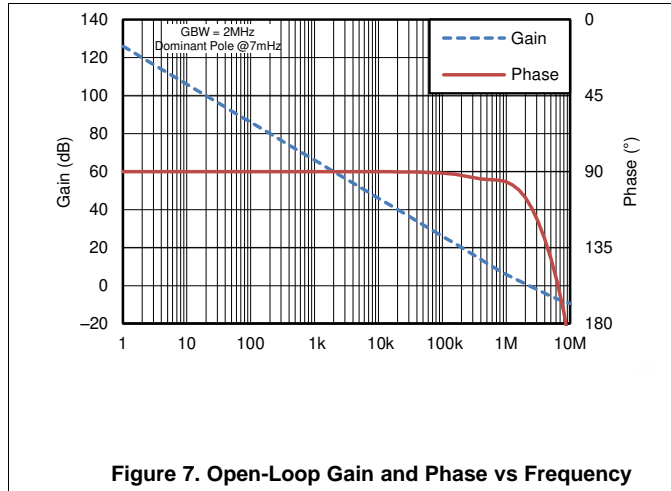


Figure 7. Open-Loop Gain and Phase vs Frequency

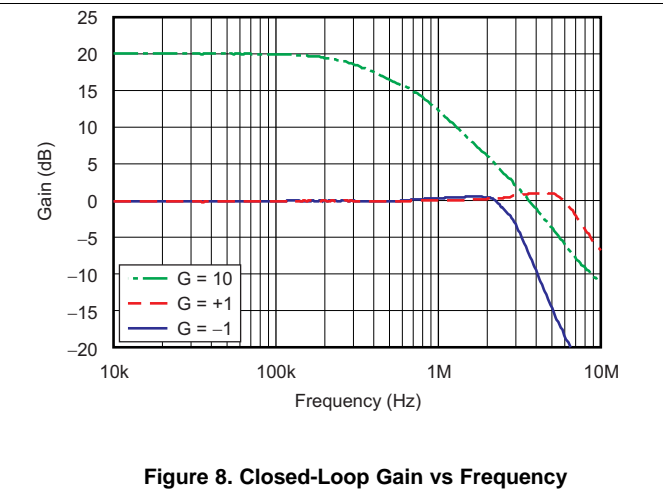


Figure 8. Closed-Loop Gain vs Frequency

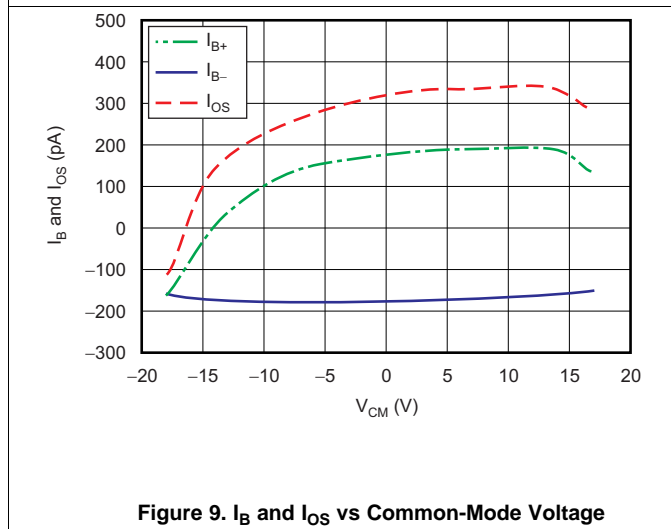


Figure 9. I_B and I_{OS} vs Common-Mode Voltage

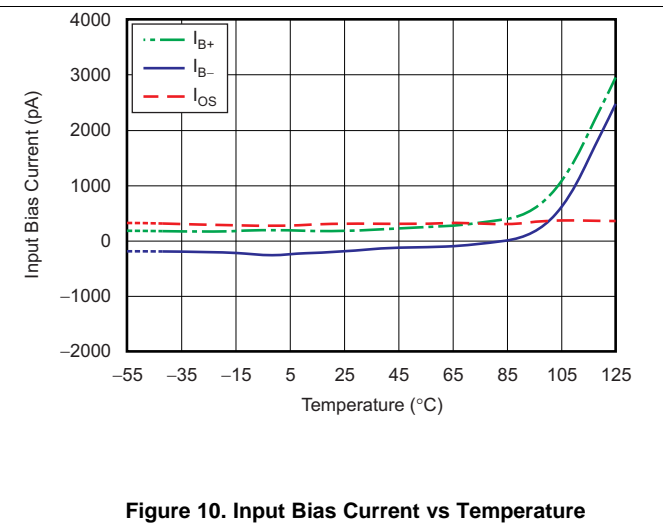


Figure 10. Input Bias Current vs Temperature

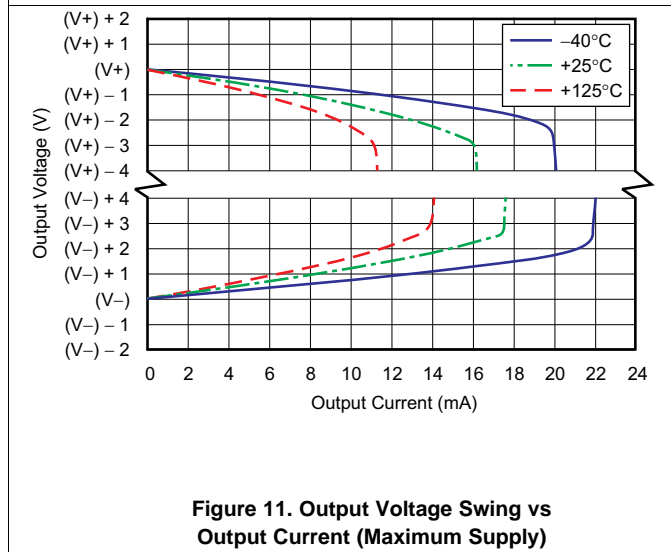


Figure 11. Output Voltage Swing vs Output Current (Maximum Supply)

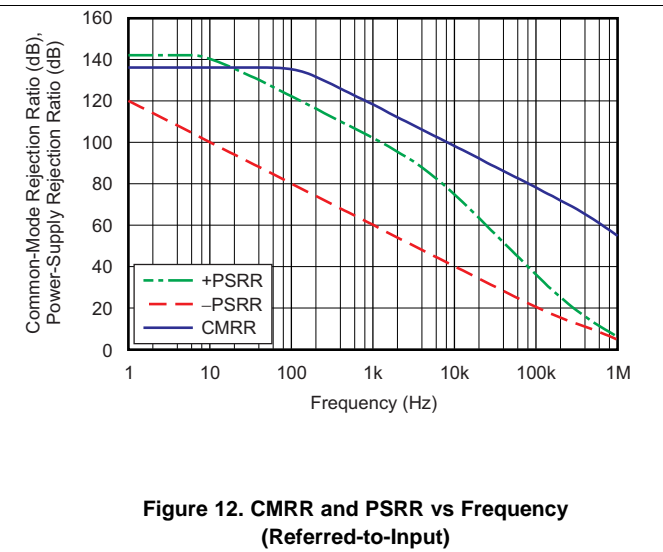


Figure 12. CMRR and PSRR vs Frequency (Referred-to-Input)

Typical Characteristics (continued)

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

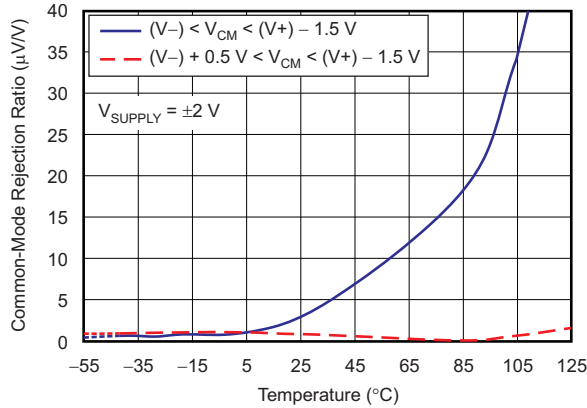


Figure 13. CMRR vs Temperature

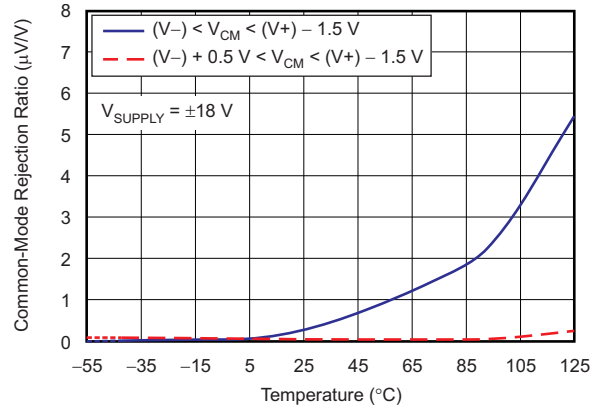


Figure 14. CMRR vs Temperature

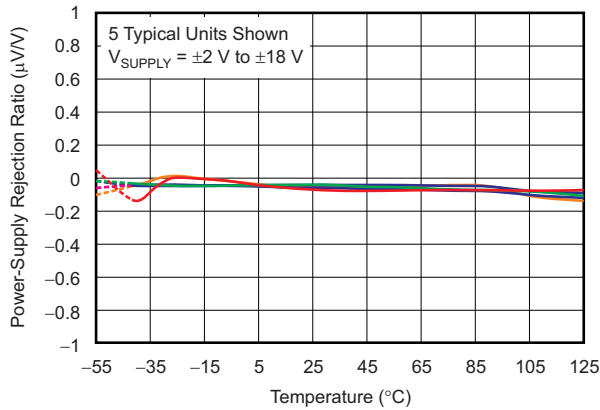


Figure 15. PSRR vs Temperature

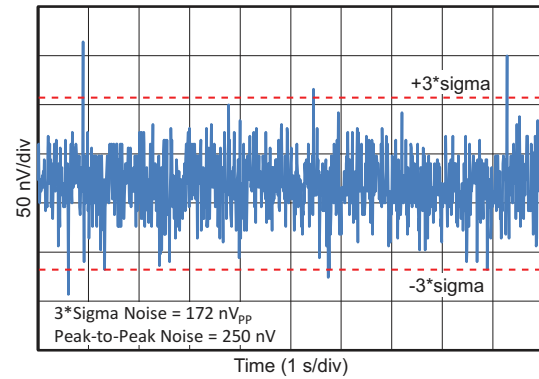


Figure 16. 0.1-Hz to 10-Hz Noise

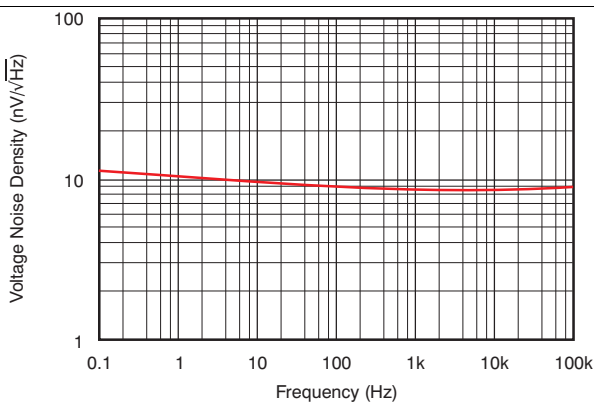


Figure 17. Input Voltage Noise Spectral Density vs Frequency

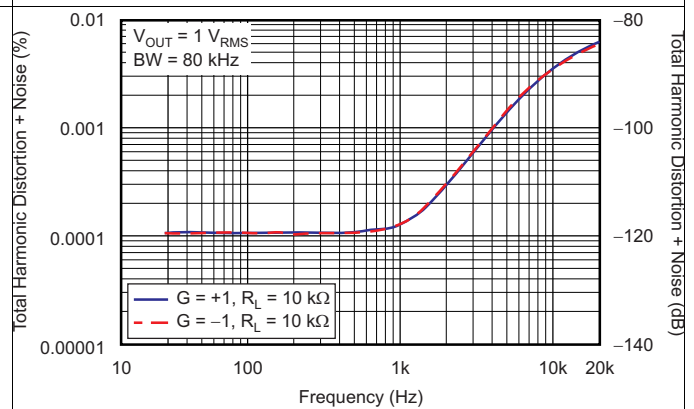


Figure 18. THD+N Ratio vs Frequency

Typical Characteristics (continued)

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

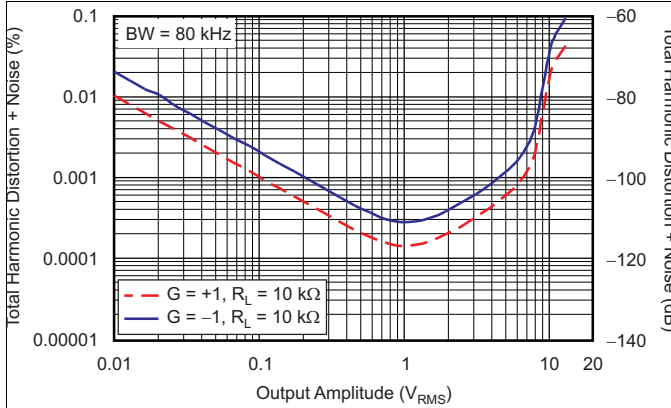


Figure 19. THD+N vs Output Amplitude

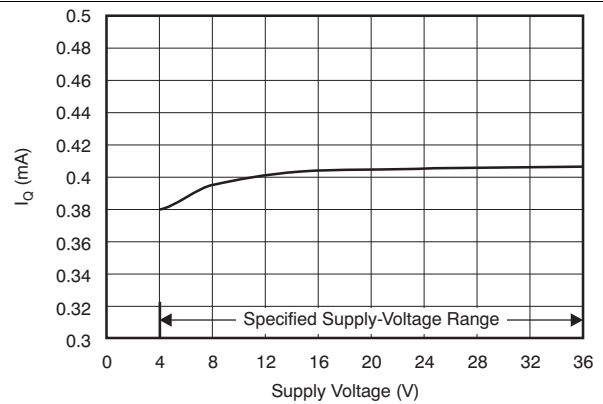


Figure 20. Quiescent Current vs Supply Voltage

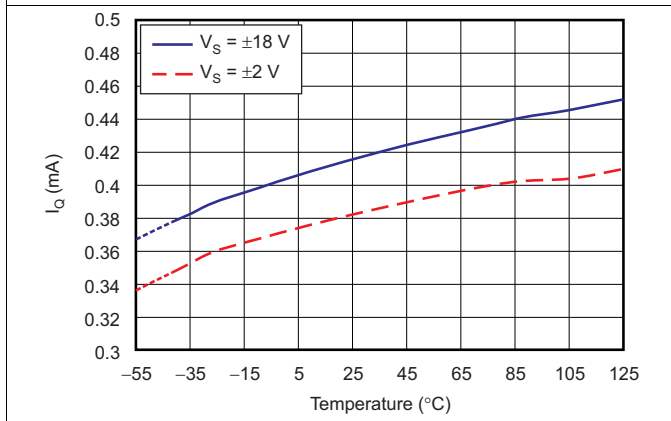


Figure 21. Quiescent Current vs Temperature

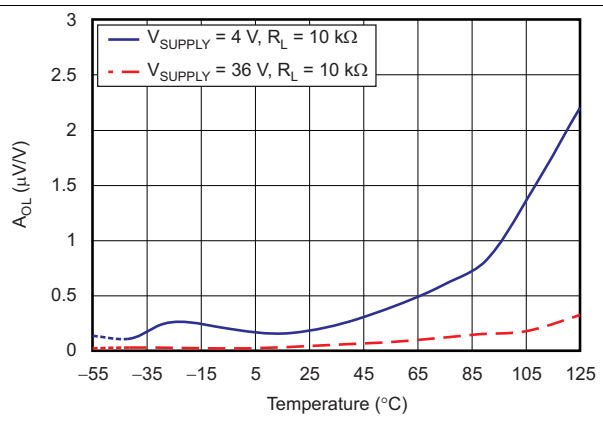


Figure 22. Open-Loop Gain vs Temperature

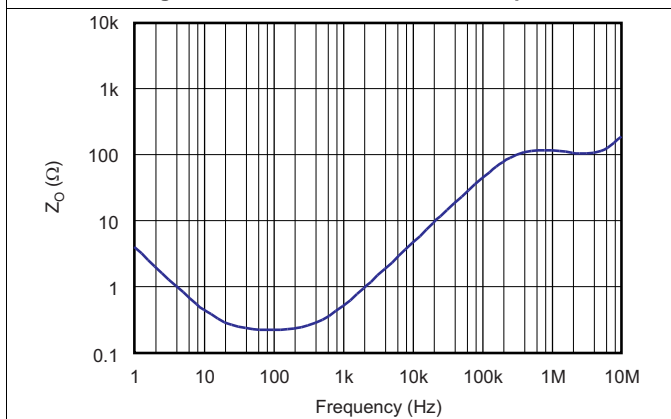


Figure 23. Open-Loop Output Impedance vs Frequency

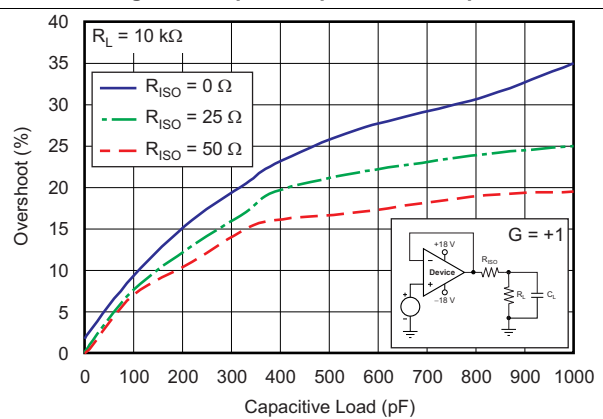


Figure 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

Typical Characteristics (continued)

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

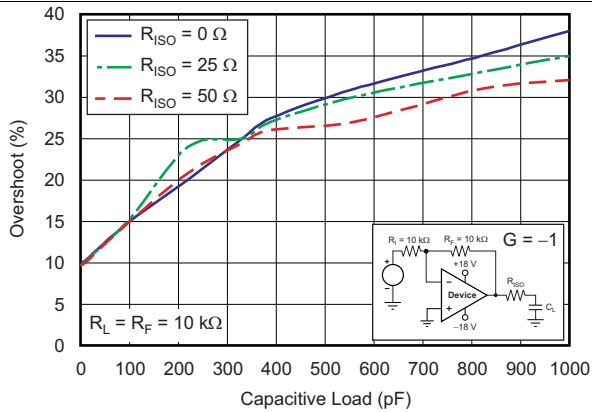


Figure 25. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

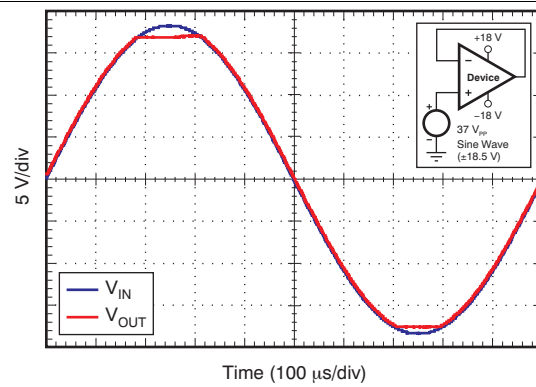


Figure 26. No Phase Reversal

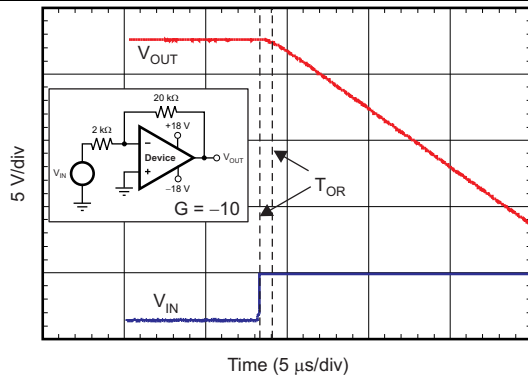


Figure 27. Positive Overload Recovery

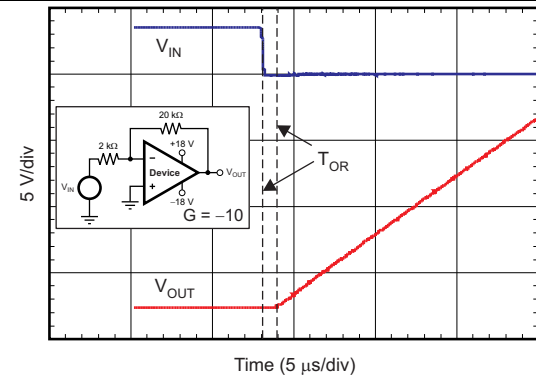


Figure 28. Negative Overload Recovery

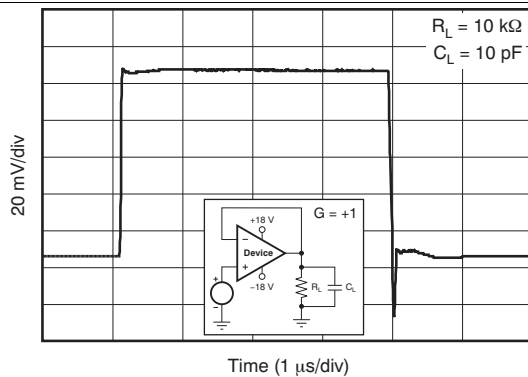


Figure 29. Small-Signal Step Response (100 mV)

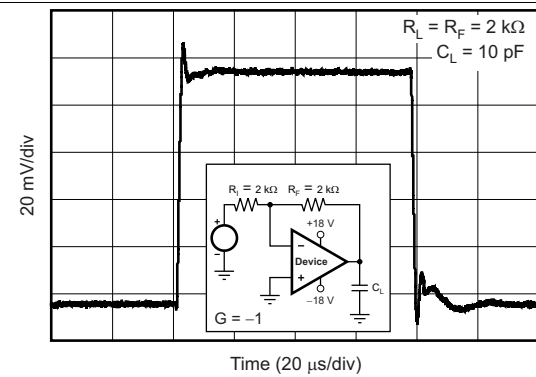
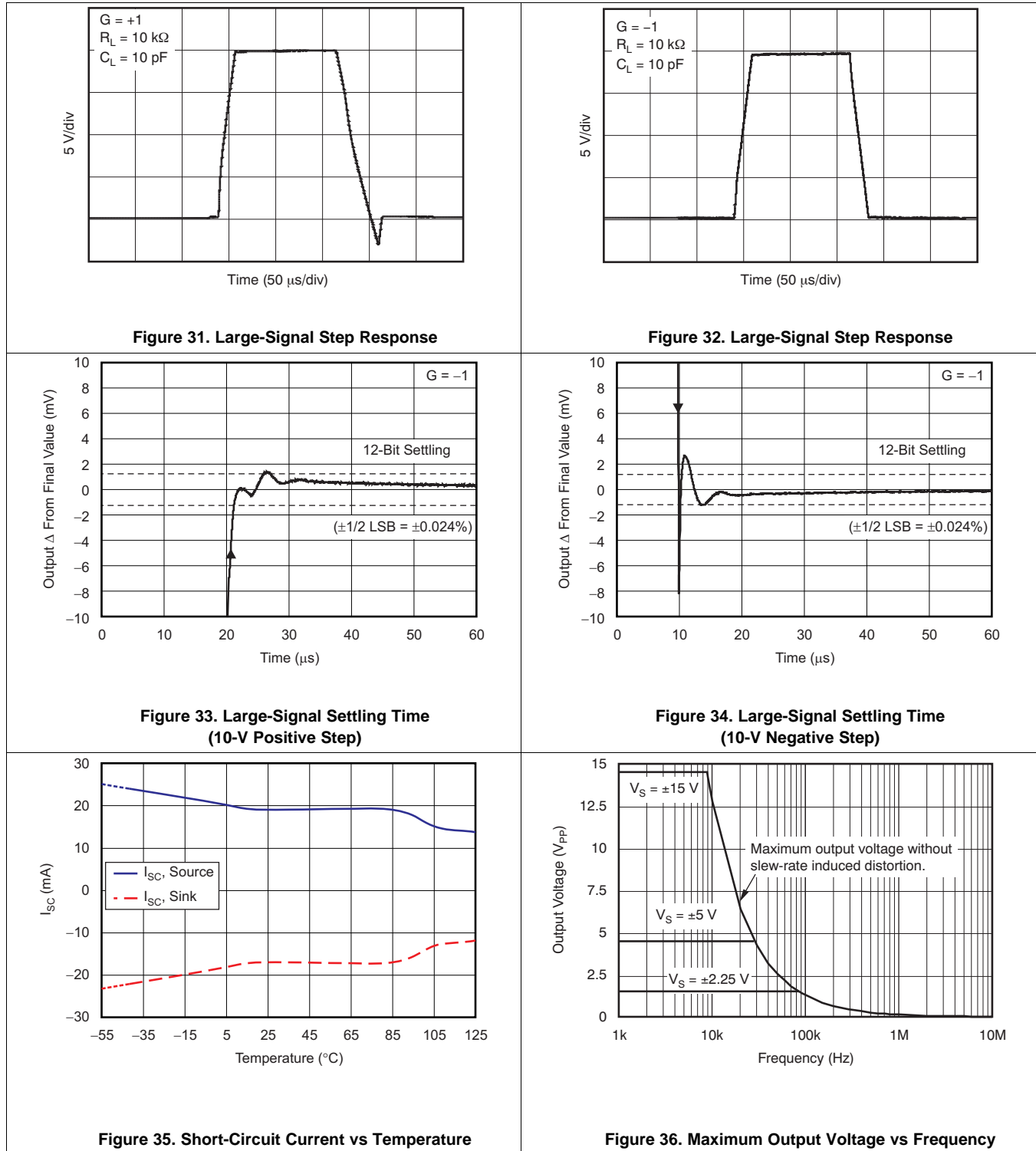


Figure 30. Small-Signal Step Response (100 mV)

Typical Characteristics (continued)

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)



Typical Characteristics (continued)

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

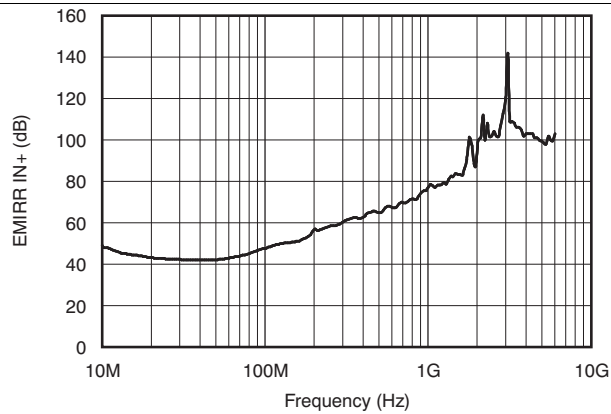


Figure 37. EMIRR IN+ vs Frequency

8 Detailed Description

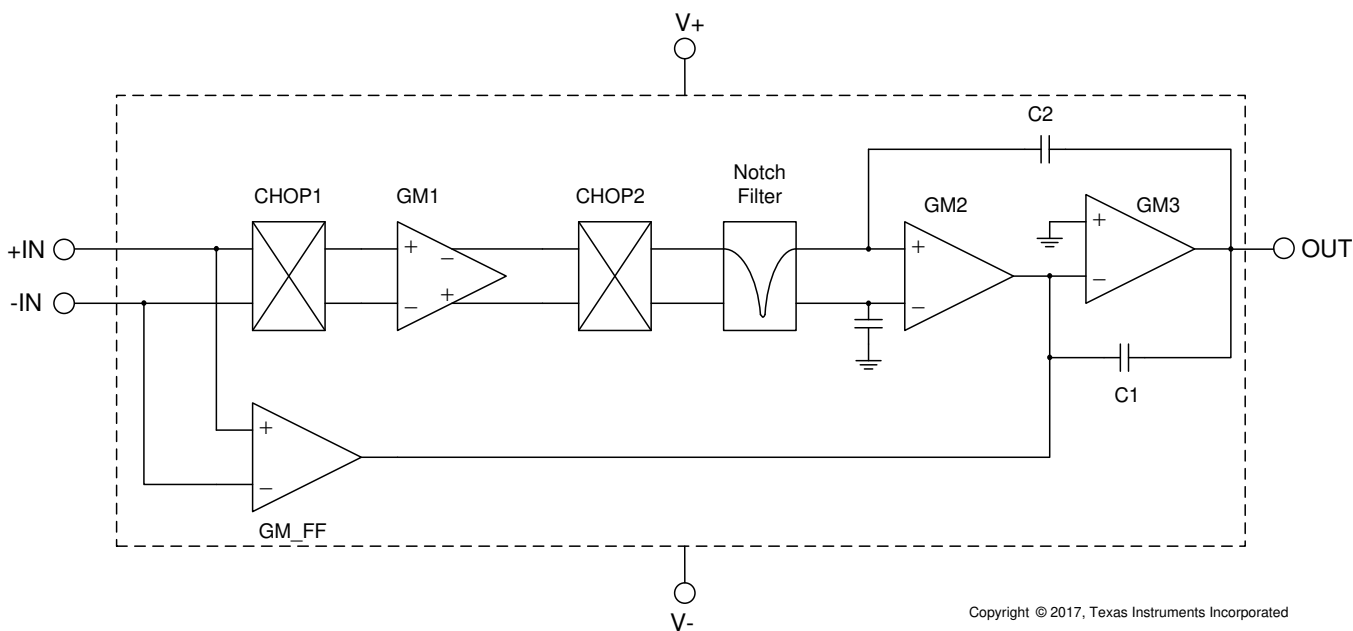
8.1 Overview

The OPA188 operational amplifier combines precision offset and drift with excellent overall performance, making this device an excellent choice for many precision applications. The precision offset drift of only $0.085 \mu\text{V}/^\circ\text{C}$ provides stability over the entire temperature range. In addition, this device offers excellent overall performance with high CMRR, PSRR, and A_{OL} . As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, $0.1\text{-}\mu\text{F}$ capacitors are adequate.

The OPA188 device is part of a family of zero-drift, low-power, rail-to-rail output operational amplifiers. These devices operate from 4 V to 36 V , are unity-gain stable, and are designed for a wide range of general-purpose applications. The zero-drift architecture provides ultra-low input offset voltage and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as ultra-low broadband noise and zero flicker noise.

8.2 Functional Block Diagram

Figure 38 shows a representation of the proprietary OPA188 architecture. Table 3 lists the active and passive component counts for this device. The component count allows for accurate reliability calculations.



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Figure 38. Functional Block Diagram

Table 3. Component Count

COMPONENT	COUNT
Transistors	636
Diodes	5
Resistors	41
Capacitors	72

8.3 Feature Description

The OPA188 is unity-gain stable and free from unexpected output phase reversal. This device uses a proprietary, periodic zero-drift technique to provide low input offset voltage and very low input offset voltage drift over temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by ensuring the potentials are equal on both input pins. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield the operational amplifier and input circuitry from air currents, such as cooling fans.

Follow these guidelines to reduce the likelihood of junctions being at different temperatures, which may cause thermoelectric voltages of 0.1 $\mu\text{V}/^\circ\text{C}$ or higher, depending on the materials used.

8.3.1 Operating Characteristics

The OPA188 is specified for operation from 4 V to 36 V (± 2 V to ± 18 V). Many specifications apply from -40°C to $+125^\circ\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in [Typical Characteristics](#).

8.3.2 Phase-Reversal Protection

The OPA188 has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPA188 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail; [Figure 39](#) shows this performance.

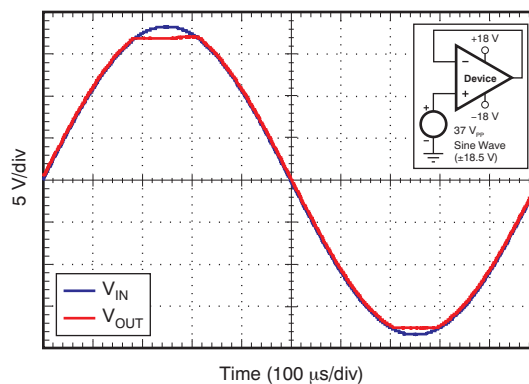


Figure 39. No Phase Reversal

8.3.3 Input Bias Current Clock Feedthrough

Zero-drift amplifiers (such as the OPA188) use switching on the inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce very short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents the device from being amplified. However, the devices may be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter such as an RC network.

8.3.4 Internal Offset Correction

The OPA188 op amp uses an auto-calibration technique with a time-continuous 750-kHz op amp in the signal path. This amplifier is zero-corrected every 3 μs using a proprietary technique. Upon power up, the amplifier requires approximately 100 μs to achieve the specified V_{OS} accuracy. This design has no aliasing or flicker noise.

Feature Description (continued)

8.3.5 EMI Rejection

The OPA188 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the benefits from these design improvements. Texas Instruments™ has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 40 shows the results of this testing on the OPA188. Table 4 lists the EMIRR IN+ values for the OPA188 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 4 may be centered on or operated near the particular frequency shown. Detailed information can also be found in *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.

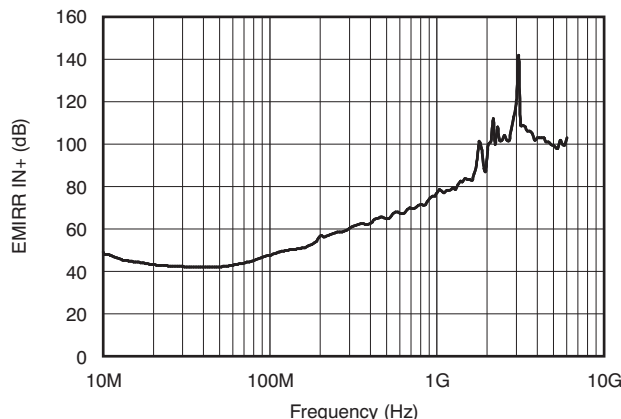


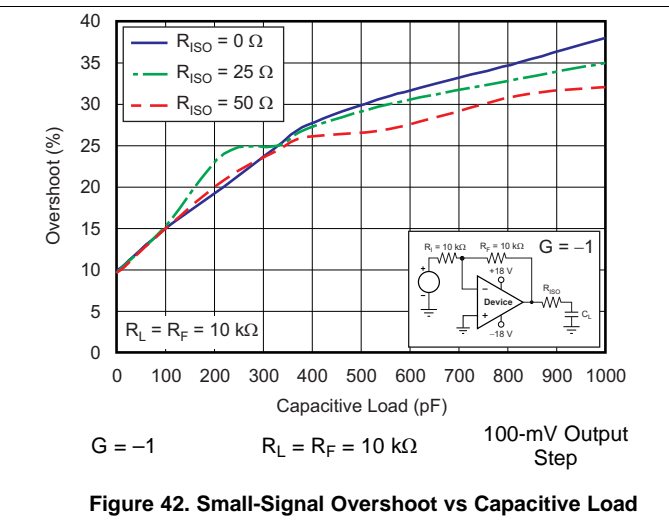
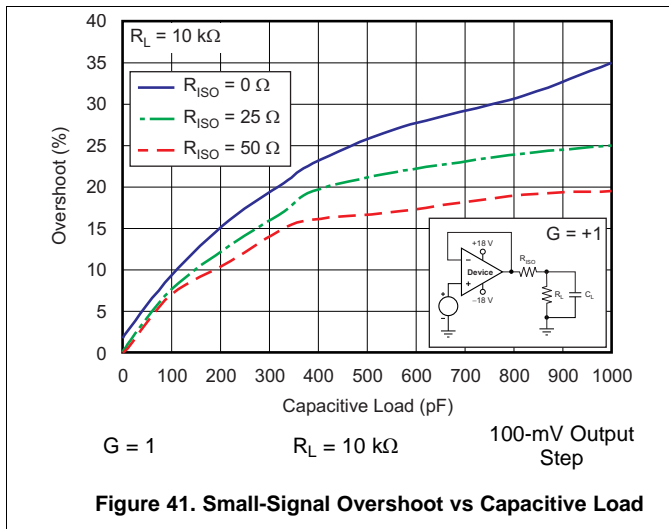
Figure 40. EMIRR Testing

Table 4. OPA188 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	62.2 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	74.7 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	100.7 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	102.4 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	104.8 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	100.3 dB

8.3.6 Capacitive Load and Stability

The device dynamic characteristics are optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the amplifier phase margin and can lead to gain peaking or oscillations. As a result, larger capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 41 and Figure 42 show graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. For details of analysis techniques and application circuits, see *Feedback Plots Define Op Amp AC Performance*, available for download from www.ti.com.



8.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See Figure 43 for an illustration of the ESD circuits contained in the OPA188 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an internal absorption device of the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA188 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

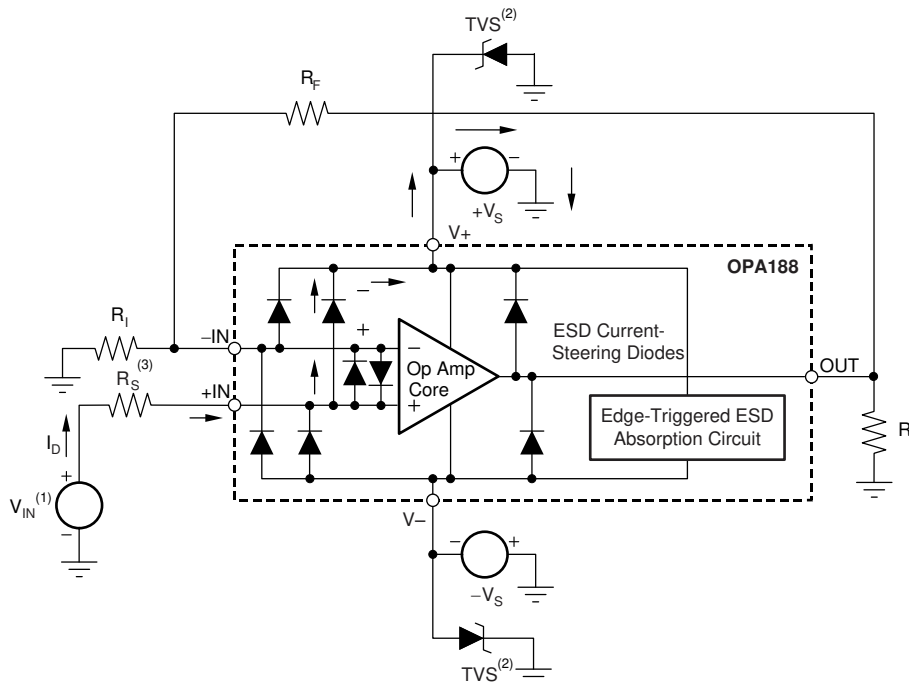
When the operational amplifier connects into a circuit (such as Figure 43 shows), the ESD protection components are intended to remain inactive and do not become involved in the operation of the application circuit. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits may be biased on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 43 shows a specific example where the input voltage, V_{IN} , exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper-input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN} . As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the absolute maximum ratings of the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies ($+V_S$ or $-V_S$) are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current-steering diodes. This state is not a normal bias condition; the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins, as shown in Figure 43. The zener voltage must be selected such that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



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- (1) $V_{IN} = +V_S + 500 \text{ mV}$.
- (2) TVS: $+V_{S(max)} > V_{TVSBR(min)} > +V_S$.
- (3) Suggested value is approximately 1 k Ω .

Figure 43. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

The OPA188 input terminals are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 43. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain and $G = 1$ circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA188. Figure 43 shows an example configuration that implements a current-limiting feedback resistor.

8.4 Device Functional Modes

The OPA188 has a single functional mode, and is operational when the power-supply voltage is greater than 4.5 V ($\pm 2.25 \text{ V}$). The maximum power supply voltage for the OPA188 is 36 V ($\pm 18 \text{ V}$).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

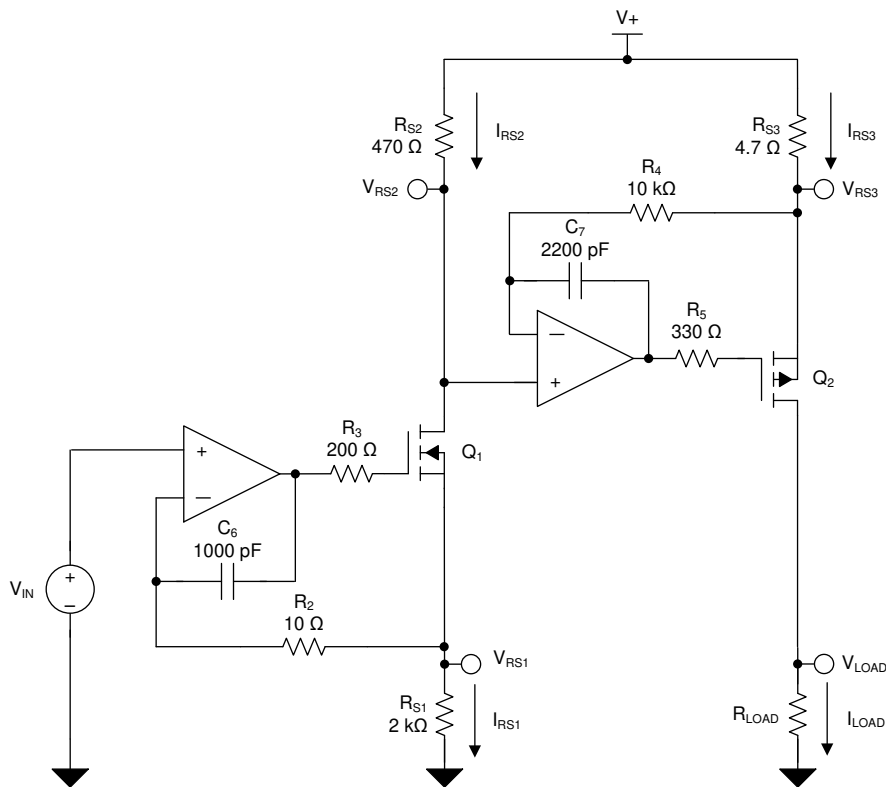
The OPA188 operational amplifier combines precision offset and drift with excellent overall performance, making this device an excellent choice for many precision applications. The precision offset drift of only $0.085 \mu\text{V}/^\circ\text{C}$ provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and A_{OL} dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, $0.1\text{-}\mu\text{F}$ capacitors are adequate.

The following application examples highlight only a few of the circuits where the OPA188 can be used.

9.2 Typical Applications

9.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in [Figure 44](#) is a high-side voltage-to-current (V-I) converter. The converter translates an input voltage of 0 V to 2 V to an output current of 0 mA to 100 mA. [Figure 45](#) shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA188 facilitate excellent dc accuracy for the circuit.



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Figure 44. High-Side Voltage-to-Current (V-I) Converter

Typical Applications (continued)

9.2.1.1 Design Requirements

The design requirements are:

- Supply voltage: 5 V dc
- Input: 0 V to 2 V dc
- Output: 0 mA to 100 mA dc

9.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN} , and the three current sensing resistors, R_{S1} , R_{S2} , and R_{S3} . The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3} .

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPA188 CMOS operational amplifier is a high-precision, ultra-low offset, ultra-low drift amplifier, optimized for low-voltage, single-supply operation, with an output swing to within 15 mV of the positive rail. The devices in the OPA188 family use chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making this device appropriate for precise dc control. The rail-to-rail output stage of the OPA188 makes sure that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in reference design TIPD102, a step-by-step process to design a [High-Side Voltage-to-Current \(V-I\) Converter](#).

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to [Precision Design Guide TIPD102, High-Side Voltage-to-Current \(V-I\) Converter](#).

9.2.1.3 Application Curves

Figure 45 shows the measured transfer function for the high-side voltage-to-current converter shown in Figure 44 .

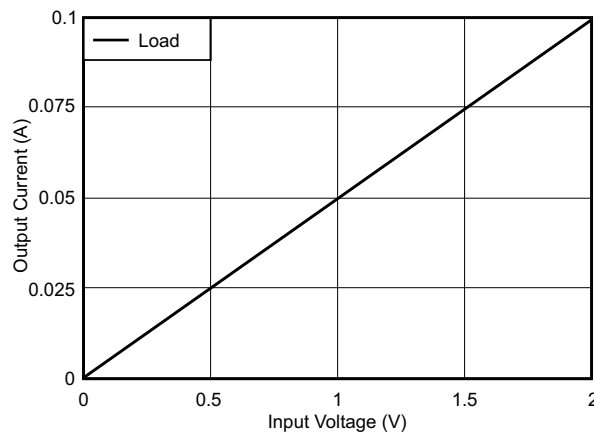


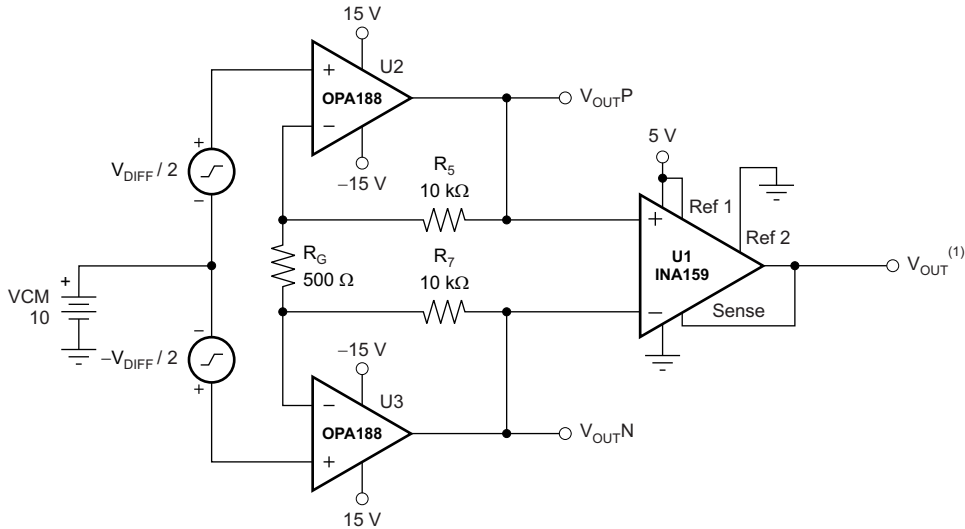
Figure 45. Measured Transfer Function for High-Side V-I Converter

9.2.2 Discrete INA + Attenuation for ADC With 3.3-V Supply

NOTE

The TINA-TI files shown in the following sections require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

Figure 46 shows an example of how the OPA188 is used as a high-voltage, high-impedance front-end for a precision, discrete instrumentation amplifier with attenuation. The INA159 provides the attenuation that allows this circuit to easily interface with 3.3-V or 5-V analog-to-digital converters (ADCs). Click the following link to download the TINA-TI file: [Discrete INA](#).

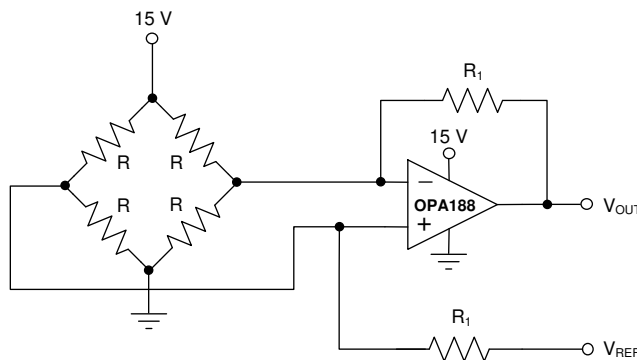


(1) $V_{OUT} = V_{DIFF} \times (41 / 5) + (Ref\ 1) / 2.$

Figure 46. Discrete INA + Attenuation for ADC With 3.3-V Supply

9.2.3 Bridge Amplifier

Figure 47 shows the basic configuration for a bridge amplifier. Click the following link to download the TINA-TI file: [Bridge Amplifier Circuit](#).



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Figure 47. Bridge Amplifier

9.2.4 Low-Side Current Monitor

Figure 48 shows the OPA188 configured in a low-side current-sensing application. The load current (I_{LOAD}) creates a voltage drop across the shunt resistor (R_{SHUNT}). This voltage is amplified by the OPA188, with a gain of 201. The load current is set from 0 A to 500 mA, which corresponds to an output voltage range from 0 V to 10 V. The output range can be adjusted by changing the shunt resistor or gain of the configuration. Click the following link to download the TINA-TI file: [Current-Sensing Circuit](#).

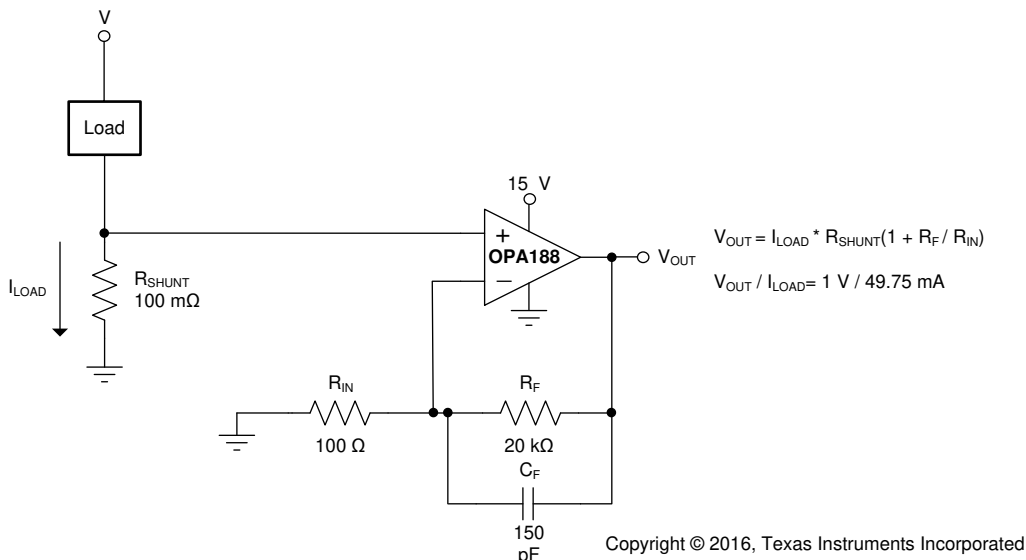


Figure 48. Low-Side Current Monitor

9.2.5 Programmable Power Supply

Figure 49 shows the OPA188 configured as a precision programmable power supply using the 16-bit, voltage output DAC8581 and the OPA548 high-current amplifier. This application amplifies the digital-to-analog converter (DAC) voltage by a value of five, and handles a large variety of capacitive and current loads. The OPA188 in the front-end provides precision and low drift across a wide range of inputs and conditions. Click the following link to download the TINA-TI file: [Programmable Power-Supply Circuit](#).

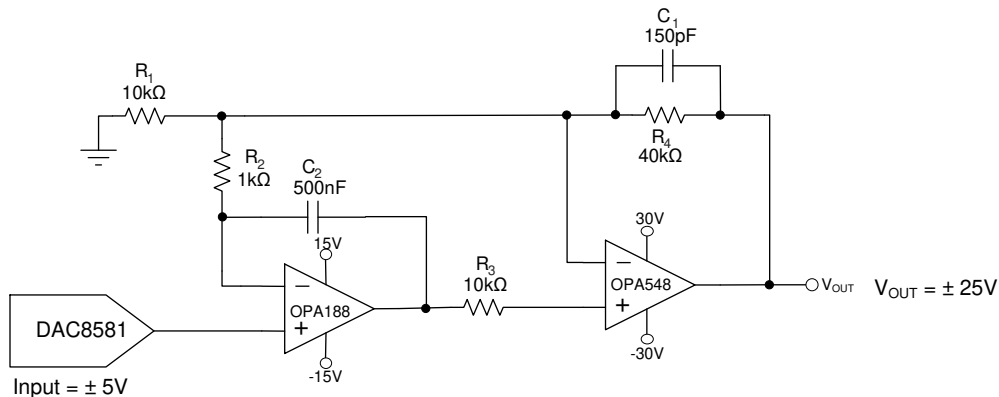
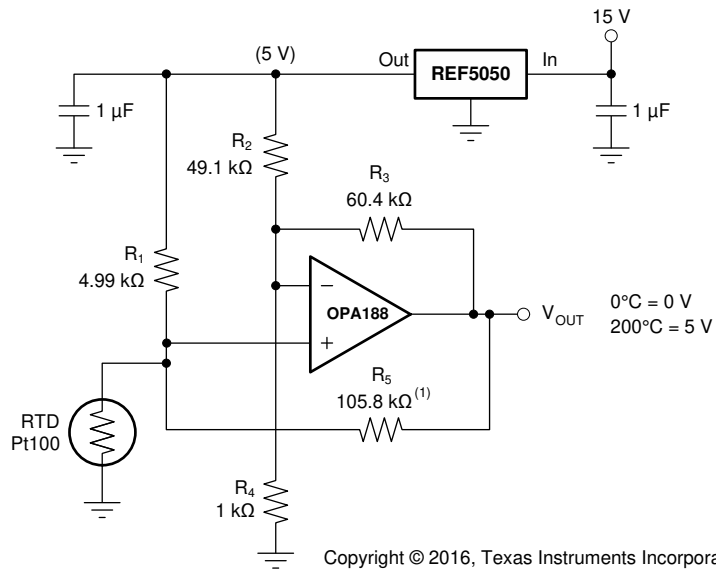


Figure 49. Programmable Power Supply

9.2.6 RTD Amplifier With Linearization

See [Analog Linearization Of Resistance Temperature Detectors](#) for an in-depth analysis of [Figure 50](#) . Click the following link to download the TINA-TI file: [RTD Amplifier with Linearization](#).



- (1) R_5 provides positive-varying excitation to linearize output.

Figure 50. RTD Amplifier With Linearization

10 Power Supply Recommendations

The OPA188 is specified for operation from 4 V to 36 V (± 2 V to ± 18 V); many specifications apply from -40°C to $+125^{\circ}\text{C}$. *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 40 V can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Layout](#).

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Connect Low-ESR, 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply lines as possible.
- Use a ground plane to help distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

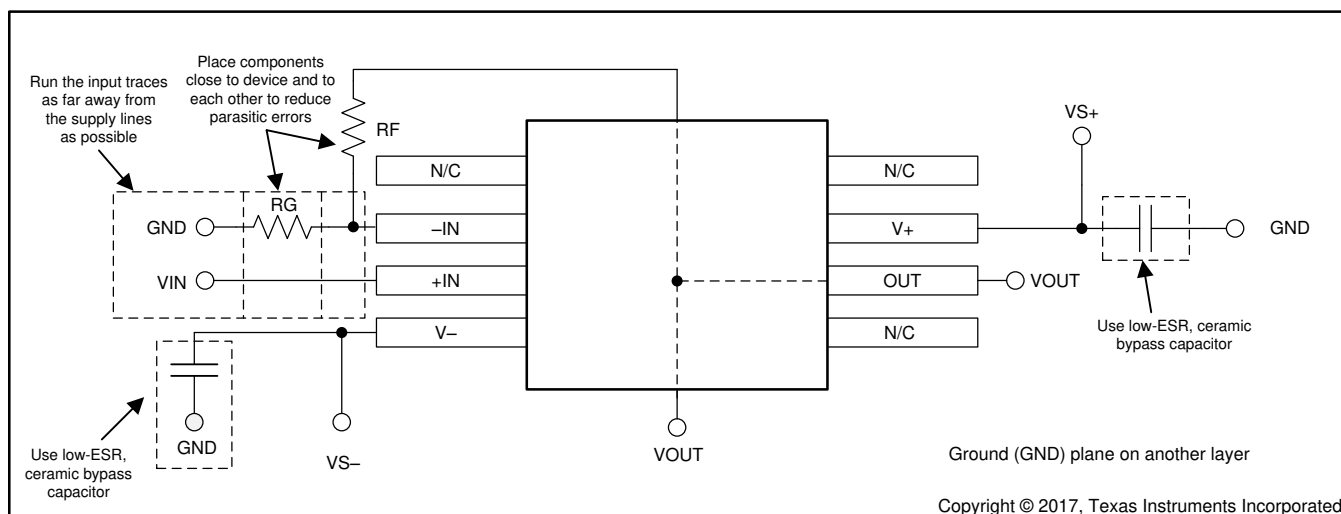
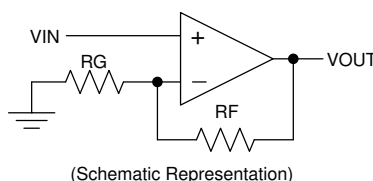


Figure 51. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Download Software)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE as well as additional design capabilities.

Available as a free download, [TINA-TI](#) offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers application report](#)
- Texas Instruments, [Feedback Plots Define Op Amp AC Performance application report](#)
- Texas Instruments, [Analog Linearization Of Resistance Temperature Detectors technical brief](#)
- Texas Instruments, [High-Side Voltage-to-Current \(V-I\) Converter design guide](#)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA188AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA188	Samples
OPA188AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXZ	Samples
OPA188AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXZ	Samples
OPA188AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXX	Samples
OPA188AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXX	Samples
OPA188AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA188	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA188 :

- Automotive: [OPA188-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

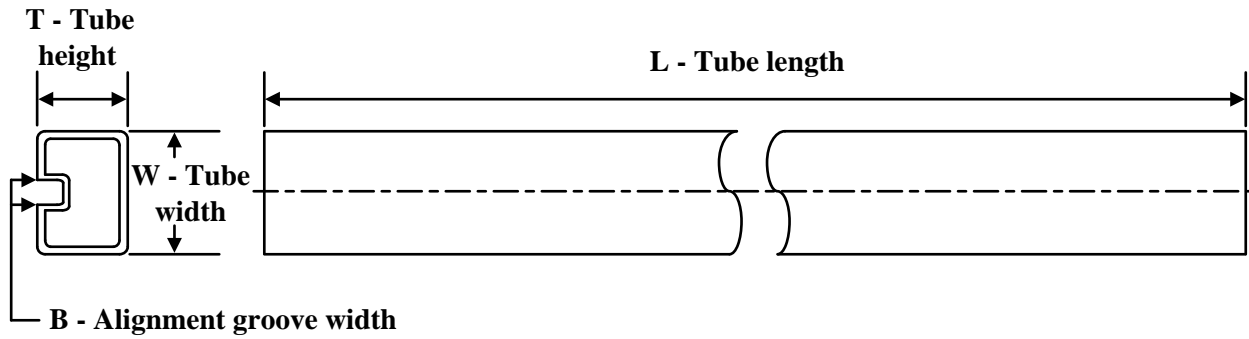

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA188AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA188AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA188AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA188AIDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA188AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA188AIDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
OPA188AIDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
OPA188AIDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
OPA188AIDGKT	VSSOP	DGK	8	250	202.0	201.0	28.0
OPA188AIDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA188AID	D	SOIC	8	75	506.6	8	3940	4.32

EXAMPLE BOARD LAYOUT

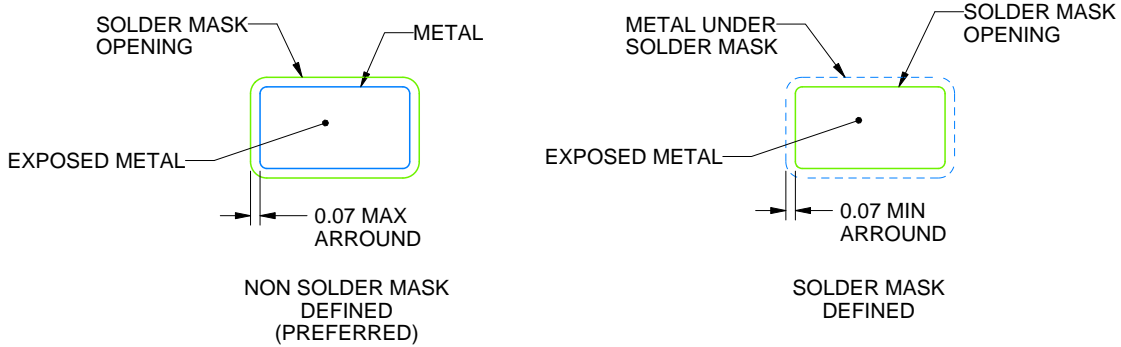
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



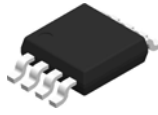
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

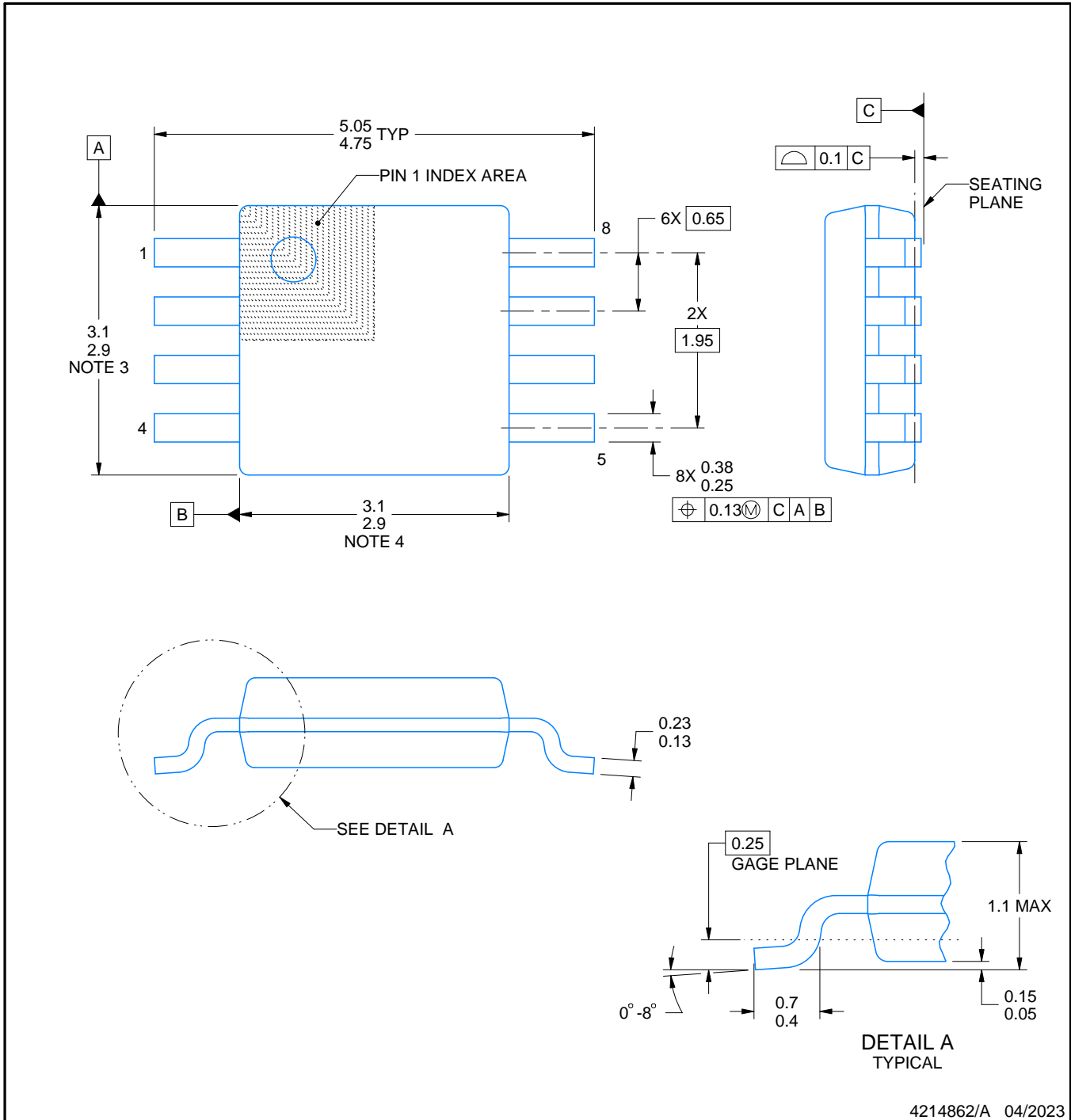
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

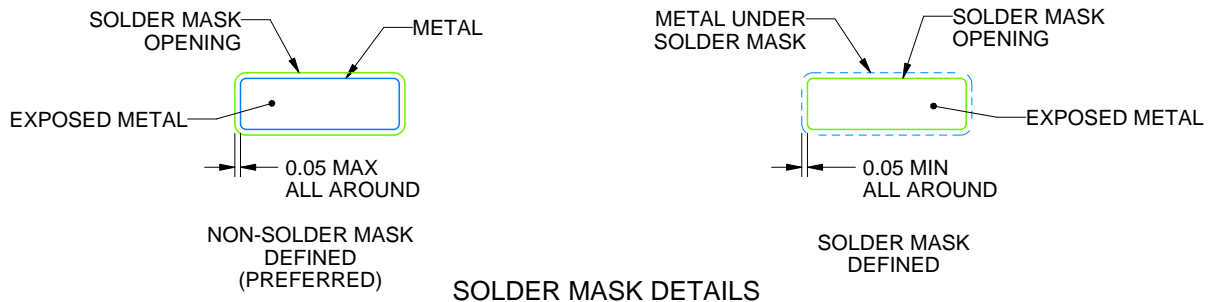
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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