THE DATASHEET OF

XRT83SL314IB

www.win-source.net 0086-755-83957316

14-CHANNEL T1/E1/J1 SHORT-HAUL LINE INTERFACE UNIT

MARCH 2005 *REV. 1.0.1*

GENERAL DESCRIPTION

The XRT83SL314 is a fully integrated 14-channel short-haul line interface unit (LIU) that operates from a single 3.3V power supply. Using internal termination, the LIU provides one bill of materials to operate in T1, E1, or J1 mode independently on a per channel basis with minimum external components. The LIU features are programmed through a standard microprocessor interface. EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays.

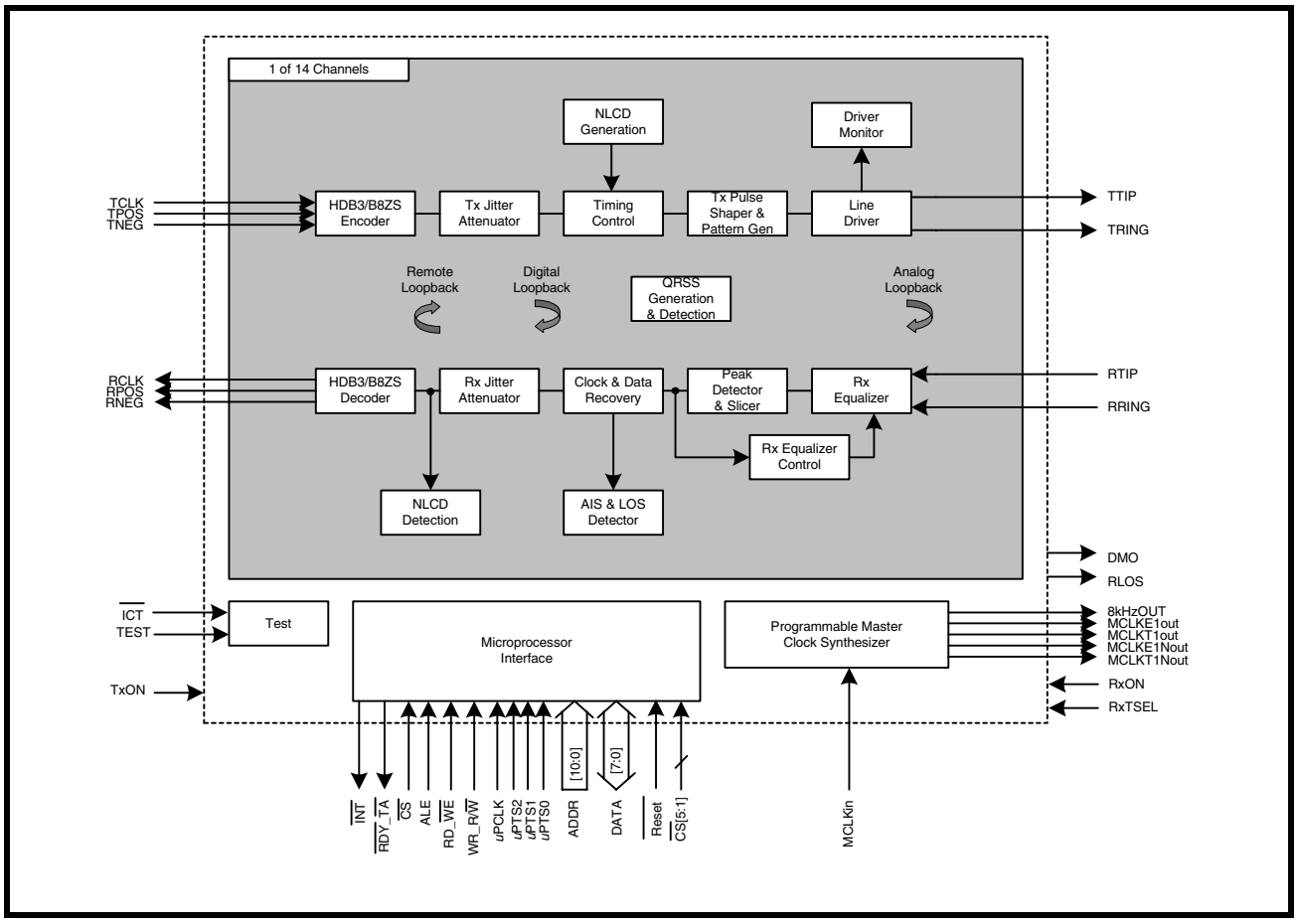
The on-chip clock synthesizer generates T1/E1/J1 clock rates from a selectable external clock frequency and has five output clock references that can be used for external timing (8kHz, 1.544Mhz, 2.048Mhz, nxT1/J1, nxE1).

Additional features include RLOS, a 16-bit LCV counter for each channel, AIS, QRSS generation/ detection, Network Loop Code generation/detection, TAOS, DMO, and diagnostic loopback modes.

APPLICATIONS

- T1 Digital Cross Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public Switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks
- Integrated Multi-Service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse Multiplexing for ATM (IMA)
- Wireless Base Stations

FIGURE 1. BLOCK DIAGRAM OF THE XRT83SL314



FEATURES

- Fully integrated 14-Channel short haul transceivers for T1/J1 (1.544MHz) and E1 (2.048MHz) applications.
- T1/E1/J1 short haul and clock rate are per port selectable through software without changing components.
- Internal Impedance matching on both receive and transmit for 75Ω (E1), 100Ω (T1), 110Ω (J1), and 120Ω (E1) applications are per port selectable through software without changing components.
- Power down on a per channel basis with independent receive and transmit selection.
- Five pre-programmed transmit pulse settings for T1 short haul applications.
- Arbitrary Pulse Generators for both T1 and E1 modes.
- On-Chip transmit short-circuit protection and limiting protects line drivers from damage on a per channel basis.
- Independent Crystal-Less digital jitter attenuators (JA) with 32-Bit or 64-Bit FIFO for the receive and transmit paths
- On-Chip frequency multiplier generates T1 or E1 master clocks from a variety of external clock sources (8, 16, 56, 64, 128, 256kHz and 1X, 2X, 4X, 8X T1 or E1)
- Driver failure monitor output (DMO) alerts of possible system or external component problems.
- Transmit outputs and receive inputs may be "High" impedance for protection or redundancy applications on a per channel basis.
- Support for automatic protection switching.
- 1:1 and 1+1 protection without relays.
- Receive monitor mode handles 0 to 29dB resistive attenuation (flat loss) along with 0 to 6dB cable loss for both T1 and E1.
- Receiver line attenuation indication output in 1dB steps.
- Loss of signal (RLOS) according to ITU-T G.775/ ETS300233 (E1) and ANSI T1.403 (T1/J1).
- Programmable receive slicer threshold (45%, 50%, 55%, or 68%) for improved receiver interference immunity.
- Programmable data stream muting upon RLOS detection.
- On-Chip HDB3/B8ZS encoder/decoder with an internal 16-bit LCV counter for each channel.
- On-Chip digital clock recovery circuit for high input jitter tolerance.
- QRSS pattern generator and detection for testing and monitoring.
- Error and bipolar violation insertion and detection.
- Transmit all ones (TAOS) and in-band network loop up and loop down code generation.
- Automatic loop code detection for remote loopback activation.
- Supports local analog, remote, digital, and dual loopback modes.
- Low Power dissipation: 170mW per channel (50% density).
- 250mW per channel maximum power dissipation (100% density).
- Single 3.3V supply operation (3V to 5V I/O tolerant).
- 304-Pin TBGA package
- -40°C to +85°C Temperature Range
- Supports gapped clocks for mapper/multiplexer applications.

PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT83SL314IB	304 Lead TBGA	-40°C to +85°C

PIN OUT OF THE XRT83SL314

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC
1	unnamed.12	unnamed.11	RGND_5	RRING_5	RTIP_5	RVDD_4	RTIP_4	RRING_4	RGND_4	unnamed.10	unnamed.10	RGND_3	RRING_3	RTIP_3	RVDD_3	RTIP_2	RRING_2	RGND_2	RRING_1	RTIP_1	unnamed.9	RLOS	unnamed.0
2	ICTB	DGND_DRV	TRING_5	TVDD_5	RVDD_5	RCLK_5	RCLK_4	TRING_4	DVDD_3_4_5	unnamed.14	DGND_3_4_5	TRING_3	TVDD_3	RCLK_3	RCLK_2	RVDD_2	TRING_2	DVDD_1_2	RGND_1	RVDD_1	RCLK_1	UPCLK	DVDD_DRV
3	TCLK_5	INTB	DVDD_PRE	unnamed.13	TTIP_5	RNEG_5	RNEG_4	TTIP_4	TVDD_4	DVDD_DRV	AGND_BIAS	TTIP_3	RNEG_3	RNEG_2	TTIP_2	TVDD_2	DGND_DRV	TRING_1	TTIP_1	RNEG_1	RDY_DTACK#	D[6]	D[5]
4	MCLKE1xN	TPOS_4	TPOS_5	TEST	unnamed.11	TGND_5	RPOS_5	RPOS_4	TGND_4	AVDD_BIAS	DGND_PRE	TGND_3	RPOS_3	RPOS_2	TGND_2	DGND_1_2	TVDD_1	TGND_1	RPOS_1	DMO	D[7]	D[2]	D[1]
5	MCLKOUT_E1	TCLK_4	TNEG_4	TNEG_5																DVDD_PRE	D[4]	D[0]	TCLK_1
6	MCLKIN	TCLK_3	TNEG_3	TPOS_3																D[3]	TPOS_1	TPOS_2	TCLK_2
7	MCLKOUT_T1	TPOS_6	TNEG_6	TCLK_6																TNEG_1	TNEG_2	TNEG_0	TCLK_0
8	RVDD_6	MCLKT1xN	GNDPLL_21	EIGHT_KHZ																TPOS_0	DGND_DRV	DGND_PRE	GNDPLL_11
9	RTIP_6	RCLK_6	GNDPLL_22	DVDD_DRV																GNDPLL_12	RCLK_0	RVDD_0	RTIP_0
10	RRING_6	TVDD_6	RNEG_6	RPOS_6																RPOS_0	RNEG_0	TVDD_0	RRING_0
11	RGND_6	TRING_6	TTIP_6	TGND_6																TGND_0	TTIP_0	TRING_0	RGND_0
12	RGND_7	TRING_7	DGND_6_7	DVDD_6_7																DGND_13_0	DVDD_13_0	TRING_13	RGND_13
13	RRING_7	TVDD_7	TTIP_7	TGND_7																TGND_13	TTIP_13	TVDD_13	RRING_13
14	RTIP_7	RCLK_7	RNEG_7	RPOS_7																RPOS_13	RNEG_13	RCLK_13	RTIP_13
15	RVDD_7	VDDPLL_21	VDDPLL_22	DGND_PRE																RXTSEL	DVDD_UP	DGND_UP	RVDD_13
16	DGND_DRV	TCLK_7	TNEG_7	TCLK_10																TCLK_13	DVDD_DRV	VDDPLL_12	VDDPLL_11
17	TPOS_7	TNEG_10	TCLK_9	TPOS_9																TCLK_12	TNEG_11	TPOS_13	TNEG_13
18	TPOS_10	TNEG_9	TNEG_8	RDB_DSB																A[7]	TPOS_12	TPOS_11	TCLK_11
19	TCLK_8	TPOS_8	ALE_AS	CSB2																A[1]	A[6]	RXOFF	TNEG_12
20	WRB_RWB	CSB5	CSB3	DVDD_PRE	A[9]	TGND_8	RPOS_8	RPOS_9	TGND_9	unnamed.4	DGND_PRE	TGND_10	RPOS_10	RPOS_11	TGND_11	TRING_11	DGND_11_12	TGND_12	RPOS_12	DVDD_PRE	A[2]	A[5]	TXOFF
21	CSB4	CSB1	DVDD_DRV	unnamed.7	TVDD_8	TTIP_8	RNEG_8	RNEG_9	TTIP_9	unnamed.3	DGND_DRV	TTIP_10	RNEG_10	RNEG_11	TTIP_11	TVDD_11	DVDD_11_12	TVDD_12	TTIP_12	RNEG_12	UPTS0	A[3]	A[4]
22	CSB	RESETB	A[8]	TRING_8	RVDD_8	RCLK_8	RCLK_9	TVDD_9	TRING_9	unnamed.1	unnamed.6	TRING_10	TVDD_10	RCLK_10	RCLK_11	RVDD_11	DVDD_DRV	TRING_12	RGND_12	RCLK_12	unnamed.5	UPTS1	A[0]
23	A[10]	unnamed.2	RGND_8	RRING_8	RTIP_8	RVDD_9	RTIP_9	RRING_9	RGND_9	DVDD_8_9_10	DGND_8_9_10	RGND_10	RRING_10	RTIP_10	RVDD_10	RTIP_11	RRING_11	RGND_11	RRING_12	RTIP_12	RVDD_12	DGND_DRV	UPTS2

Bottom View

TABLE OF CONTENTS

GENERAL DESCRIPTION 1
APPLICATIONS 1
FIGURE 1. BLOCK DIAGRAM OF THE XRT83SL314 1
FEATURES 2
PRODUCT ORDERING INFORMATION 2
PIN OUT OF THE XRT83SL314 3
TABLE OF CONTENTS I
PIN DESCRIPTIONS BY FUNCTION 4
MICROPROCESSOR 4
RECEIVER SECTION 5
TRANSMITTER SECTION 8
CONTROL FUNCTION 10
CLOCK SECTION 10
POWER AND GROUND 11
NO CONNECTS 13
1.0 CLOCK SYNTHESIZER 14
TABLE 1: INPUT CLOCK SOURCE SELECT 14
FIGURE 2. SIMPLIFIED BLOCK DIAGRAM OF THE CLOCK SYNTHESIZER 15
1.1 ALL T1/E1 MODE 15
2.0 RECEIVE PATH LINE INTERFACE 15
FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH 15
2.1 LINE TERMINATION (RTIP/RRING) 16
2.1.1 CASE 1: INTERNAL TERMINATION 16
TABLE 2: SELECTING THE INTERNAL IMPEDANCE 16
FIGURE 4. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION 16
2.1.2 CASE 2: INTERNAL TERMINATION WITH ONE EXTERNAL FIXED RESISTOR FOR ALL MODES 17
TABLE 3: SELECTING THE VALUE OF THE EXTERNAL FIXED RESISTOR 17
FIGURE 5. TYPICAL CONNECTION DIAGRAM USING ONE EXTERNAL FIXED RESISTOR 17
2.2 EQUALIZER CONTROL 18
FIGURE 6. SIMPLIFIED BLOCK DIAGRAM OF THE EQUALIZER AND PEAK DETECTOR 18
2.3 CABLE LOSS INDICATOR 18
FIGURE 7. SIMPLIFIED BLOCK DIAGRAM OF THE CABLE LOSS INDICATOR 18
2.4 EQUALIZER ATTENUATION FLAG 19
FIGURE 8. SIMPLIFIED BLOCK DIAGRAM OF THE EQUALIZER ATTENUATION FLAG 19
2.5 PEAK DETECTOR AND SLICER 19
TABLE 4: SELECTING THE SLICER LEVEL FOR THE PEAK DETECTOR 19
2.6 CLOCK AND DATA RECOVERY 20
FIGURE 9. RECEIVE DATA UPDATED ON THE RISING EDGE OF RCLK 20
FIGURE 10. RECEIVE DATA UPDATED ON THE FALLING EDGE OF RCLK 20
TABLE 5: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG 21
2.6.1 RECEIVE SENSITIVITY 21
FIGURE 11. TEST CONFIGURATION FOR MEASURING RECEIVE SENSITIVITY 21
2.6.2 INTERFERENCE MARGIN 22
FIGURE 12. TEST CONFIGURATION FOR MEASURING INTERFERENCE MARGIN 22
2.6.3 GENERAL ALARM DETECTION AND INTERRUPT GENERATION 22
FIGURE 13. INTERRUPT GENERATION PROCESS BLOCK 22
2.6.3.1 RLOS (RECEIVER LOSS OF SIGNAL) 22
FIGURE 14. ANALOG RECEIVE LOS OF SIGNAL FOR T1/E1/J1 23
TABLE 6: ANALOG RLOS DECLARE/CLEAR (TYPICAL VALUES) FOR T1/E1 23
2.6.3.2 EXLOS (EXTENDED LOSS OF SIGNAL) 23
2.6.3.3 AIS (ALARM INDICATION SIGNAL) 23
2.6.3.4 NLCD (NETWORK LOOP CODE DETECTION) 24
FIGURE 15. PROCESS BLOCK FOR AUTOMATIC LOOP CODE DETECTION 24
2.6.3.5 FLSD (FIFO LIMIT STATUS DETECTION) 25
2.6.3.6 LCVD (LINE CODE VIOLATION DETECTION) 25
2.7 RECEIVE JITTER ATTENUATOR 25
2.8 HDB3/B8ZS DECODER 25
2.9 RPOS/RNEG/RCLK 26
FIGURE 16. SINGLE RAIL MODE WITH A FIXED REPEATING "0011" PATTERN 26
FIGURE 17. DUAL RAIL MODE WITH A FIXED REPEATING "0011" PATTERN 26

2.10 RXMUTE (RECEIVER LOS WITH DATA MUTING) 26
FIGURE 18. SIMPLIFIED BLOCK DIAGRAM OF THE RXMUTE FUNCTION 26
3.0 T1/E1 APPLICATIONS 27
3.1 LOOPBACK DIAGNOSTICS 27
3.1.1 LOCAL ANALOG LOOPBACK 27
FIGURE 19. SIMPLIFIED BLOCK DIAGRAM OF LOCAL ANALOG LOOPBACK 27
3.1.2 REMOTE LOOPBACK 27
FIGURE 20. SIMPLIFIED BLOCK DIAGRAM OF REMOTE LOOPBACK 27
3.1.3 DIGITAL LOOPBACK 28
FIGURE 21. SIMPLIFIED BLOCK DIAGRAM OF DIGITAL LOOPBACK 28
3.1.4 DUAL LOOPBACK 28
FIGURE 22. SIMPLIFIED BLOCK DIAGRAM OF DUAL LOOPBACK 28
3.2 84-CHANNEL T1/E1 MULTIPLEXER/MAPPER APPLICATIONS 29
FIGURE 23. SIMPLIFIED BLOCK DIAGRAM OF AN 84-CHANNEL APPLICATION 29
TABLE 7: CHIP SELECT ASSIGNMENTS 29
3.3 LINE CARD REDUNDANCY 30
3.3.1 1:1 AND 1+1 REDUNDANCY WITHOUT RELAYS 30
3.3.2 TRANSMIT INTERFACE WITH 1:1 AND 1+1 REDUNDANCY 30
FIGURE 24. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR 1:1 AND 1+1 REDUNDANCY 30
3.3.3 RECEIVE INTERFACE WITH 1:1 AND 1+1 REDUNDANCY 30
FIGURE 25. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR 1:1 AND 1+1 REDUNDANCY 31
3.3.4 N+1 REDUNDANCY USING EXTERNAL RELAYS 31
3.3.5 TRANSMIT INTERFACE WITH N+1 REDUNDANCY 32
FIGURE 26. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR N+1 REDUNDANCY 32
3.3.6 RECEIVE INTERFACE WITH N+1 REDUNDANCY 33
FIGURE 27. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR N+1 REDUNDANCY 33
3.4 POWER FAILURE PROTECTION 34
3.5 OVERVOLTAGE AND OVERCURRENT PROTECTION 34
3.6 NON-INTRUSIVE MONITORING 34
FIGURE 28. SIMPLIFIED BLOCK DIAGRAM OF A NON-INTRUSIVE MONITORING APPLICATION 34
4.0 TRANSMIT PATH LINE INTERFACE 35
FIGURE 29. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT PATH 35
4.1 TCLK/TPOS/TNEG DIGITAL INPUTS 35
FIGURE 30. TRANSMIT DATA SAMPLED ON FALLING EDGE OF TCLK 35
FIGURE 31. TRANSMIT DATA SAMPLED ON RISING EDGE OF TCLK 35
TABLE 8: TIMING SPECIFICATIONS FOR TCLK/TPOS/TNEG 36
4.2 HDB3/B8ZS ENCODER 36
TABLE 9: EXAMPLES OF HDB3 ENCODING 36
TABLE 10: EXAMPLES OF B8ZS ENCODING 36
4.3 TRANSMIT JITTER ATTENUATOR 37
TABLE 11: MAXIMUM GAP WIDTH FOR MULTIPLEXER/MAPPER APPLICATIONS 37
4.4 TAOS (TRANSMIT ALL ONES) 37
FIGURE 32. TAOS (TRANSMIT ALL ONES) 37
4.5 TRANSMIT DIAGNOSTIC FEATURES 37
4.5.1 ATAOS (AUTOMATIC TRANSMIT ALL ONES) 38
FIGURE 33. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION 38
4.5.2 NETWORK LOOP UP CODE 38
FIGURE 34. NETWORK LOOP UP CODE GENERATION 38
4.5.3 NETWORK LOOP DOWN CODE 38
FIGURE 35. NETWORK LOOP DOWN CODE GENERATION 38
4.5.4 QRSS GENERATION 39
TABLE 12: RANDOM BIT SEQUENCE POLYNOMIALS 39
4.6 TRANSMIT PULSE SHAPER AND FILTER 39
4.6.1 T1 SHORT HAUL LINE BUILD OUT (LBO) 40
TABLE 13: SHORT HAUL LINE BUILD OUT 40
4.6.2 ARBITRARY PULSE GENERATOR FOR T1 AND E1 40
FIGURE 36. ARBITRARY PULSE SEGMENT ASSIGNMENT 40
4.7 DMO (DIGITAL MONITOR OUTPUT) 40
4.8 LINE TERMINATION (TTIP/TRING) 41
FIGURE 37. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION 41
5.0 MICROPROCESSOR INTERFACE BLOCK 42
TABLE 14: SELECTING THE MICROPROCESSOR INTERFACE MODE 42
FIGURE 38. SIMPLIFIED BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK 42
5.1 THE MICROPROCESSOR INTERFACE BLOCK SIGNALS 43

TABLE 15: XRT84L314 MICROPROCESSOR INTERFACE SIGNALS THAT EXHIBIT CONSTANT ROLES IN BOTH INTEL AND MOTOROLA MODES43
TABLE 16: INTEL MODE: MICROPROCESSOR INTERFACE SIGNALS 43
TABLE 17: MOTOROLA MODE: MICROPROCESSOR INTERFACE SIGNALS 44
5.2 INTEL MODE PROGRAMMED I/O ACCESS (ASYNCHRONOUS) 45
FIGURE 39. INTEL µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS 46
TABLE 18: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS 46
5.3 MOTOROLA MODE PROGRAMMED I/O ACCESS (SYNCHRONOUS) 47
FIGURE 40. MOTOROLA POWER PC µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS 48
TABLE 19: MOTOROLA POWER PC MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS 48
FIGURE 41. MOTOROLA 68K µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS 49
TABLE 20: MOTOROLA 68K MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS 49
TABLE 21: MICROPROCESSOR REGISTER ADDRESS (ADDR[7:0]) 50
TABLE 22: MICROPROCESSOR REGISTER CHANNEL DESCRIPTION 50
TABLE 23: MICROPROCESSOR REGISTER GLOBAL DESCRIPTION 51
TABLE 24: MICROPROCESSOR REGISTER 0X00H BIT DESCRIPTION 52
TABLE 25: EQUALIZER CONTROL AND TRANSMIT LINE BUILD OUT 52
TABLE 26: MICROPROCESSOR REGISTER 0X01H BIT DESCRIPTION 53
TABLE 27: MICROPROCESSOR REGISTER 0X02H BIT DESCRIPTION 54
TABLE 28: MICROPROCESSOR REGISTER 0X03H BIT DESCRIPTION 55
TABLE 29: MICROPROCESSOR REGISTER 0X04H BIT DESCRIPTION 56
TABLE 30: MICROPROCESSOR REGISTER 0X05H BIT DESCRIPTION 57
TABLE 31: MICROPROCESSOR REGISTER 0X06H BIT DESCRIPTION 59
TABLE 32: MICROPROCESSOR REGISTER 0X07H BIT DESCRIPTION 60
TABLE 33: MICROPROCESSOR REGISTER 0X08H BIT DESCRIPTION 60
TABLE 34: MICROPROCESSOR REGISTER 0X09H BIT DESCRIPTION 61
TABLE 35: MICROPROCESSOR REGISTER 0X0AH BIT DESCRIPTION 61
TABLE 36: MICROPROCESSOR REGISTER 0X0BH BIT DESCRIPTION 61
TABLE 37: MICROPROCESSOR REGISTER 0X0CH BIT DESCRIPTION 61
TABLE 38: MICROPROCESSOR REGISTER 0X0DH BIT DESCRIPTION 62
TABLE 39: MICROPROCESSOR REGISTER 0X0EH BIT DESCRIPTION 62
TABLE 40: MICROPROCESSOR REGISTER 0X0FH BIT DESCRIPTION 62
TABLE 41: MICROPROCESSOR REGISTER 0XE0H BIT DESCRIPTION 63
TABLE 42: MICROPROCESSOR REGISTER 0XE1H BIT DESCRIPTION 64
TABLE 43: MICROPROCESSOR REGISTER 0XE2H BIT DESCRIPTION 64
TABLE 44: MICROPROCESSOR REGISTER 0XE3H BIT DESCRIPTION 65
TABLE 45: MICROPROCESSOR REGISTER 0XE4H BIT DESCRIPTION 66
TABLE 46: MICROPROCESSOR REGISTER 0XE5H BIT DESCRIPTION 66
TABLE 47: MICROPROCESSOR REGISTER 0XE6H BIT DESCRIPTION 67
TABLE 48: MICROPROCESSOR REGISTER 0XE7H BIT DESCRIPTION 68
TABLE 49: MICROPROCESSOR REGISTER 0XE8H BIT DESCRIPTION 69
CLOCK SELECT REGISTER 70
FIGURE 42. REGISTER 0XE9H SUB REGISTERS 70
TABLE 50: MICROPROCESSOR REGISTER 0XE9H BIT DESCRIPTION 70
TABLE 51: MICROPROCESSOR REGISTER 0XEAH BIT DESCRIPTION 72
TABLE 52: MICROPROCESSOR REGISTER 0XEBH BIT DESCRIPTION 72
TABLE 53: E1 ARBITRARY SELECT 73
TABLE 54: MICROPROCESSOR REGISTER 0XFFH BIT DESCRIPTION 74
ELECTRICAL CHARACTERISTICS 75
TABLE 55: ABSOLUTE MAXIMUM RATINGS 75
TABLE 56: DC DIGITAL INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS 75
TABLE 57: AC ELECTRICAL CHARACTERISTICS 75
TABLE 58: POWER CONSUMPTION 76
TABLE 59: E1 RECEIVER ELECTRICAL CHARACTERISTICS 76
TABLE 60: T1 RECEIVER ELECTRICAL CHARACTERISTICS 77
TABLE 61: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS 78
TABLE 62: T1 TRANSMITTER ELECTRICAL CHARACTERISTICS 78
ORDERING INFORMATION 79
PACKAGE DIMENSIONS (DIE DOWN) 79
REVISION HISTORY 80

PIN DESCRIPTIONS BY FUNCTION

MICROPROCESSOR

NAME	PIN	TYPE	DESCRIPTION
$\overline{CS}$	A22	I	**Chip Select Input** Active low signal. This signal enables the microprocessor interface by pulling chip select "Low". The microprocessor interface is disabled when the chip select signal returns "High".
ALE_TS	C19	I	**Address Latch Enable Input (Transfer Start)** See the Microprocessor section of this datasheet for a description.
$\overline{WR}$_R/$\overline{W}$	A20	I	**Write Strobe Input (Read/Write)** See the Microprocessor section of this datasheet for a description.
$\overline{RD}$_$\overline{WE}$	D18	I	**Read Strobe Input (Write Enable)** See the Microprocessor section of this datasheet for a description.
$\overline{RDY}$_$\overline{TA}$	AA3	O	**Ready Output (Transfer Acknowledge)** See the Microprocessor section of this datasheet for a description.
$\overline{INT}$	B3	O	**Interrupt Output** Active low signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". GIE (Global Interrupt Enable) must be set "High" in the appropriate global register to enable interrupt generation. ***NOTE:*** *This pin is internally pulled "High" with a 50KΩ resistor.*
µPCLK	AB2	I	**Micro Processor Clock Input** In a synchronous microprocessor interface, µPCLK is used as the internal timing reference for programming the LIU.
ADDR10 ADDR9 ADDR8 ADDR7 ADDR6 ADDR5 ADDR4 ADDR3 ADDR2 ADDR1 ADDR0	A23 E20 C22 Y18 AA19 AB20 AC21 AB21 AA20 Y19 AC22	I	**Address Bus Input** ADDR[10:8] is used as a chip select decoder. The LIU has 5 chip select output pins for enabling up to 5 additional devices for accessing internal registers. The LIU has the option to select itself (master device), up to 5 additional devices, or all 6 devices simultaneously by setting the ADDR[10:8] pins specified below. ADDR[7:0] is a direct address bus for permitting access to the internal registers. **ADDR[10:8]** 000 = Master Device 001 = Chip Select Output 1 (Pin B21) 010 = Chip Select Output 2 (Pin D19) 011 = Chip Select Output 3 (Pin C20) 100 = Chip Select Output 4 (Pin A21) 101 = Chip Select Output 5 (Pin B20) 110 = Reserved 111 = All Chip Selects Active Including the Master Device

MICROPROCESSOR

NAME	PIN	TYPE	DESCRIPTION
DATA7 DATA6 DATA5 DATA4 DATA3 DATA2 DATA1 DATA0	AA4 AB3 AC3 AA5 Y6 AB4 AC4 AB5	I/O	**Bi-directional Data Bus** DATA[7:0] is a bi-directional data bus used for read and write operations.
µPTS2 µPTS1 µPTS0	AC23 AB22 AA21	I	**Microprocessor Type Select Input** µPTS[2:0] are used to select the microprocessor type interface. 000 = Intel 68HC11, 8051, 80C188 (Asynchronous) 001 = Motorola 68K (Asynchronous) 111 = Motorola MPC8260, MPC860 Power PC (Synchronous)
$\overline{\text{Reset}}$	B22	I	**Hardware Reset Input** Active low signal. When this pin is pulled "Low" for more than 10µS, the internal registers are set to their default state. See the register description for the default values. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*
$\overline{\text{CS5}}$ $\overline{\text{CS4}}$ $\overline{\text{CS3}}$ $\overline{\text{CS2}}$ $\overline{\text{CS1}}$	B20 A21 C20 D19 B21	O	**Chip Select Output** The XRT83SL314 can be used to provide the necessary chip selects for up to 5 additional devices by using the 3 MSBs ADDR[10:8] from the 11-Bit address bus. The LIU allows up to 84-channel applications with only using one chip select. See the ADDR[10:0] definition in the pin description.

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RxON	AB19	I	**Receive On/Off Input** Upon power up, the receivers are powered off. Turning the receivers On or Off can be selected through the microprocessor interface by programming the appropriate channel register if the hardware pin is pulled "High". If the hardware pin is pulled "Low", all channels are automatically turned off. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*
RxTSEL	Y15	I	**Receive Termination Control** Upon power up, the receivers are in "High" impedance. Switching to internal termination can be selected through the microprocessor interface by programming the appropriate channel register. However, to switch control to the hardware pin, RxTCNTL must be programmed to "1" in the appropriate global register. Once control has been granted to the hardware pin, it must be pulled "High" to switch to internal termination. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RLOS	AB1	O	**Receive Loss of Signal (Global Pin for All 14-Channels)** When a receive loss of signal occurs for any one of the 14-channels according to ITU-T G.775, the RLOS pin will go "High" for a minimum of one RCLK cycle. RLOS will remain "High" until the loss of signal condition clears. See the Receive Loss of Signal section of this datasheet for more details. ***NOTE:*** *This pin is for redundancy applications to initiate an automatic switch to the backup card. For individual channel RLOS, see the register map.*
RCLK13 RCLK12 RCLK11 RCLK10 RCLK9 RCLK8 RCLK7 RCLK6 RCLK5 RCLK4 RCLK3 RCLK2 RCLK1 RCLK0	AB14 Y22 R22 P22 G22 F22 B14 B9 F2 G2 P2 R2 AA2 AA9	O	**Receive Clock Output** RCLK is the recovered clock from the incoming data stream. If the incoming signal is absent or RxON is pulled "Low", RCLK maintains its timing by using an internal master clock as its reference. RPOS/RNEG data can be updated on either edge of RCLK selected by RCLKE in the appropriate global register. ***NOTE:*** *RCLKE is a global setting that applies to all 14 channels.*
RPOS13 RPOS12 RPOS11 RPOS10 RPOS9 RPOS8 RPOS7 RPOS6 RPOS5 RPOS4 RPOS3 RPOS2 RPOS1 RPOS0	Y14 W20 P20 N20 H20 G20 D14 D10 G4 H4 N4 P4 W4 Y10	O	**RPOS/RDATA Output** Receive digital output pin. In dual rail mode, this pin is the receive positive data output. In single rail mode, this pin is the receive non-return to zero (NRZ) data output.

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RNEG13 RNEG12 RNEG11 RNEG10 RNEG9 RNEG8 RNEG7 RNEG6 RNEG5 RNEG4 RNEG3 RNEG2 RNEG1 RNEG0	AA14 Y21 P21 N21 H21 G21 C14 C10 F3 G3 N3 P3 Y3 AA10	O	**RNEG/LCV_OF Output** In dual rail mode, this pin is the receive negative data output. In single rail mode, this pin is a Line Code Violation / Counter Overflow indicator. If LCV is selected by programming the appropriate global register and if a line code violation, a bi-polar violation, or excessive zeros occur, the LCV pin will pull "High" for a minimum of one RCLK cycle. LCV will remain "High" until there are no more violations. However, if OF is selected the LCV pin will pull "High" if the internal LCV counter is saturated. The LCV pin will remain "High" until the LCV counter is reset.
RTIP13 RTIP12 RTIP11 RTIP10 RTIP9 RTIP8 RTIP7 RTIP6 RTIP5 RTIP4 RTIP3 RTIP2 RTIP1 RTIP0	AC14 Y23 T23 P23 G23 E23 A14 A9 E1 G1 P1 T1 Y1 AC9	I	**Receive Differential Tip Input** RTIP is the positive differential input from the line interface. Along with the RRING signal, these pins should be coupled to a 1:1 transformer for proper operation.
RRING13 RRING12 RRING11 RRING10 RRING9 RRING8 RRING7 RRING6 RRING5 RRING4 RRING3 RRING2 RRING1 RRING0	AC13 W23 U23 N23 H23 D23 A13 A10 D1 H1 N1 U1 W1 AC10	I	**Receive Differential Ring Input** RRING is the negative differential input from the line interface. Along with the RTIP signal, these pins should be coupled to a 1:1 transformer for proper operation.

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TxON	AC20	I	**Transmit On/Off Input** Upon power up, the transmitters are powered off. Turning the transmitters On or Off is selected through the microprocessor interface by programming the appropriate channel register if this pin is pulled "High". If the TxON pin is pulled "Low", all 14 transmitters are powered off. ***NOTE:*** *TxON is ideal for redundancy applications. See the Redundancy Applications Section of this datasheet for more details. Internally pulled "Low" with a 50KΩ resistor.*
DMO	Y4	O	**Digital Monitor Output (Global Pin for All 14-Channels)** When no transmit output pulse is detected for more than 128 TCLK cycles on one of the 14-channels, the DMO pin will go "High" for a minimum of one TCLK cycle. DMO will remain "High" until the transmitter sends a valid pulse. ***NOTE:*** *This pin is for redundancy applications to initiate an automatic switch to the backup card. For individual channel DMO, see the register map.*
TCLK13 TCLK12 TCLK11 TCLK10 TCLK9 TCLK8 TCLK7 TCLK6 TCLK5 TCLK4 TCLK3 TCLK2 TCLK1 TCLK0	Y16 Y17 AC18 D16 C17 A19 B16 D7 A3 B5 B6 AC6 AC5 AC7	I	**Transmit Clock Input** TCLK is the input facility clock used to sample the incoming TPOS/TNEG data. If TCLK is absent, pulled "Low", or pulled "High", the transmitter outputs at TTIP/TRING can be selected to send an all ones or an all zero signal by programming TCLKCNL in the appropriate global register. TPOS/TNEG data can be sampled on either edge of TCLK selected by TCLKE in the appropriate global register. ***NOTE:*** *TCLKE is a global setting that applies to all 14 channels.*
TPOS13 TPOS12 TPOS11 TPOS10 TPOS9 TPOS8 TPOS7 TPOS6 TPOS5 TPOS4 TPOS3 TPOS2 TPOS1 TPOS0	AB17 AA18 AB18 A18 D17 B19 A17 B7 C4 B4 D6 AB6 AA6 Y8	I	**TPOS/TDATA Input** Transmit digital input pin. In dual rail mode, this pin is the transmit positive data input. In single rail mode, this pin is the transmit non-return to zero (NRZ) data input. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TNEG13 TNEG12 TNEG11 TNEG10 TNEG9 TNEG8 TNEG7 TNEG6 TNEG5 TNEG4 TNEG3 TNEG2 TNEG1 TNEG0	AC17 AC19 AA17 B17 B18 C18 C16 C7 D5 C5 C6 AA7 Y7 AB7	I	**Transmit Negative Data Input** In dual rail mode, this pin is the transmit negative data input. In single rail mode, this pin can be left unconnected. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*
TTIP13 TTIP12 TTIP11 TTIP10 TTIP9 TTIP8 TTIP7 TTIP6 TTIP5 TTIP4 TTIP3 TTIP2 TTIP1 TTIP0	AA13 W21 R21 M21 J21 F21 C13 C11 E3 H3 M3 R3 W3 AA11	O	**Transmit Differential Tip Output** TTIP is the positive differential output to the line interface. Along with the TRING signal, these pins should be coupled to a 1:2 step up transformer for proper operation.
TRING13 TRING12 TRING11 TRING10 TRING9 TRING8 TRING7 TRING6 TRING5 TRING4 TRING3 TRING2 TRING1 TRING0	AB12 V22 T20 M22 J22 D22 B12 B11 C2 H2 M2 U2 V3 AB11	O	**Transmit Differential Ring Output** TRING is the negative differential output to the line interface. Along with the TTIP signal, these pins should be coupled to a 1:2 step up transformer for proper operation.

CONTROL FUNCTION

NAME	PIN	TYPE	DESCRIPTION
TEST	D4	I	**Factory Test Mode** For normal operation, the TEST pin should be tied to ground. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{\text{ICT}}$	A2	I	**In Circuit Testing** When this pin is tied "Low", all output pins are forced to "High" impedance for in circuit testing. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*

CLOCK SECTION

NAME	PIN	TYPE	DESCRIPTION
MCLKin	A6	I	**Master Clock Input** The master clock input can accept a wide range of inputs that can be used to generate T1 or E1 clock rates on a per channel basis. See the register map for details.
8kHzOUT	D8	O	**8kHz Output Clock**
MCLKE1out	A5	O	**2.048MHz Output Clock**
MCLKE1Nout	A4	O	**2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz Output Clock** See the register map for programming details.
MCLKT1out	A7	O	**1.544MHz Output Clock**
MCLKT1Nout	B8	O	**1.544MHz, 3.088MHz, 6.176MHz, or 12.352MHz Output Clock** See the register map for programming details.

POWER AND GROUND

NAME	PIN	TYPE	DESCRIPTION
TVDD13 TVDD12 TVDD11 TVDD10 TVDD9 TVDD8 TVDD7 TVDD6 TVDD5 TVDD4 TVDD3 TVDD2 TVDD1 TVDD0	AB13 V21 T21 N22 H22 E21 B13 B10 D2 J3 N2 T3 U4 AB10	PWR	**Transmit Analog Power Supply (3.3V ±5%)** TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
RVDD13 RVDD12 RVDD11 RVDD10 RVDD9 RVDD8 RVDD7 RVDD6 RVDD5 RVDD4 RVDD3 RVDD2 RVDD1 RVDD0	AC15 AA23 T22 R23 F23 E22 A15 A8 E2 F1 R1 T2 Y2 AB9	PWR	**Receive Analog Power Supply (3.3V ±5%)** RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
DVDD DVDD DVDD DVDD DVDD DVDD	J2 V2 D12 AA12 U21 K23	PWR	**Digital Power Supply (3.3V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.
DVDD_DRV DVDD_DRV DVDD_DRV DVDD_DRV DVDD_DRV DVDD_DRV DVDD_PRE DVDD_PRE DVDD_PRE DVDD_PRE DVDD_UP	C21 AC2 K3 D9 AA16 U22 C3 Y5 D20 Y20 AA15	PWR	**Digital Power Supply (3.3V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.

POWER AND GROUND

NAME	PIN	TYPE	DESCRIPTION
AVDD_BIAS AVDD_PLL22 AVDD_PLL21 AVDD_PLL12 AVDD_PLL11	K4 C15 B15 AB16 AC16	PWR	**Analog Power Supply (3.3V ±5%)** AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1μF capacitor.
TGND13 TGND12 TGND11 TGND10 TGND9 TGND8 TGND7 TGND6 TGND5 TGND4 TGND3 TGND2 TGND1 TGND0	Y13 V20 R20 M20 J20 F20 D13 D11 F4 J4 M4 R4 V4 Y11	GND	**Transmit Analog Ground** It's recommended that all ground pins of this device be tied together.
RGND13 RGND12 RGND11 RGND10 RGND9 RGND8 RGND7 RGND6 RGND5 RGND4 RGND3 RGND2 RGND1 RGND0	AC12 W22 V23 M23 J23 C23 A12 A11 C1 J1 M1 V1 W2 AC11	GND	**Receive Analog Ground** It's recommended that all ground pins of this device be tied together.
DGND DGND DGND DGND DGND DGND	L2 T4 C12 Y12 U20 L23	GND	**Digital Ground** It's recommended that all ground pins of this device be tied together.

POWER AND GROUND

NAME	PIN	TYPE	DESCRIPTION
DGND_DRV	B2	GND	**Digital Ground**
DGND_DRV	U3		It's recommended that all ground pins of this device be tied together.
DGND_DRV	A16		
DGND_DRV	AA8		
DGND_DRV	L21		
DGND_DRV	AB23		
DGND_PRE	L4		
DGND_PRE	D15		
DGND_PRE	AB8		
DGND_PRE	L20		
DGND_UP	AB15		
AGND_BIAS	L3	GND	**Analog Ground**
AGND_PLL22	C9		It's recommended that all ground pins of this device be tied together.
AGND_PLL21	C8		
AGND_PLL12	Y9		
AGND_PLL11	AC8		

NO CONNECTS

NAME	PIN	TYPE	DESCRIPTION
NC	A1	NC	**No Connect**
NC	B1		This pin can be left floating or tied to ground.
NC	K1		
NC	L1		
NC	AA1		
NC	AC1		
NC	K2		
NC	D3		
NC	E4		
NC	K20		
NC	D21		
NC	K21		
NC	K22		
NC	L22		
NC	AA22		
NC	B23		

1.0 CLOCK SYNTHESIZER

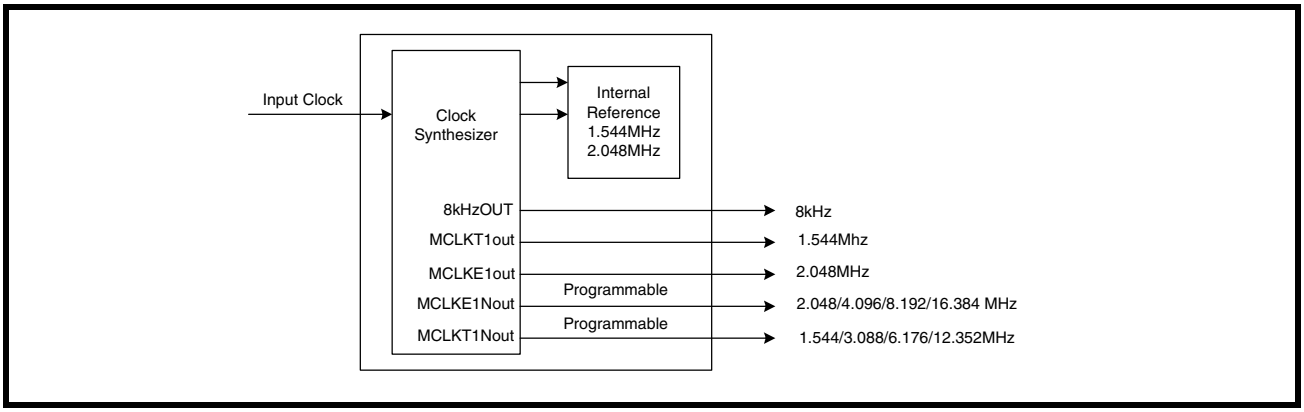
In system design, fewer clocks on the network card could reduce noise and interference. Common clock references such as 8kHz are readily available to network designers. Network cards that support both T1 and E1 modes must be able to produce 1.544MHz and 2.048MHz transmission data. The XRT83SL314 has a built in clock synthesizer that requires only one input clock reference by programming CLKSEL[3:0] in the appropriate global register. A list of the input clock options is shown in Table 1.

TABLE 1: INPUT CLOCK SOURCE SELECT

CLKSEL[3:0]	INPUT CLOCK REFERENCE
0h (0000)	2.048 MHz
1h (0001)	1.544MHz
2h (0010)	8 kHz
3h (0011)	16 kHz
4h (0100)	56 kHz
5h (0101)	64 kHz
6h (0110)	128 kHz
7h (0111)	256 kHz
8h (1000)	4.096 MHz
9h (1001)	3.088 MHz
Ah (1010)	8.192 MHz
Bh (1011)	6.176 MHz
Ch (1100)	16.384 MHz
Dh (1101)	12.352 MHz
Eh (1110)	2.048 MHz
Fh (1111)	1.544 MHz

The single input clock reference is used to generate multiple timing references. The first objective of the clock synthesizer is to generate 1.544MHz and 2.048MHz for each of the 14 channels. This allows each channel to operate in either T1 or E1 mode independent from the other channels. The state of the equalizer control bits in the appropriate channel registers determine whether the LIU operates in T1 or E1 mode. The second objective is to generate additional output clock references for system use. The available output clock references are shown in Figure 2.

FIGURE 2. SIMPLIFIED BLOCK DIAGRAM OF THE CLOCK SYNTHESIZER



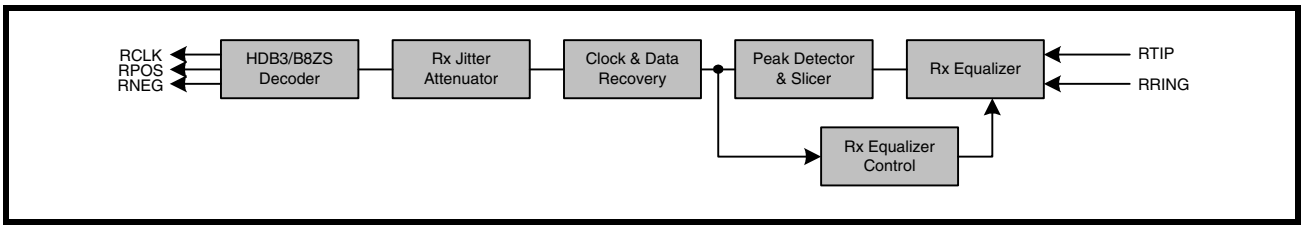
1.1 ALL T1/E1 Mode

To reduce system noise and power consumption, the XRT83SL314 offers an ALL T1/E1 mode. Since most line card designs are configured to operate in T1 or E1 only, the LIU can be selected to shut off the timing references for the mode not being used by programming the appropriate global register. By default the ALL T1/E1 mode is enabled (ALLT1/E1 bit = "0"). If the LIU is configured for T1, all E1 clock references and the 8kHz reference are shut off internally to the chip. This reduces the amount of internal clocks switching within the LIU, hence reducing noise and power consumption. In E1 mode, the T1 clock references are internally shut off, however the 8kHz reference is available. To disable this feature, the ALLT1/E1 bit must be set to a "1" in the appropriate global register.

2.0 RECEIVE PATH LINE INTERFACE

The receive path of the XRT83SL314 LIU consists of 14 independent T1/E1/J1 receivers. The following section describes the complete receive path from RTIP/RRING inputs to RCLK/RPOS/RNEG outputs. A simplified block diagram of the receive path is shown in Figure 3.

FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH



2.1 Line Termination (RTIP/RRING)

2.1.1 CASE 1: Internal Termination

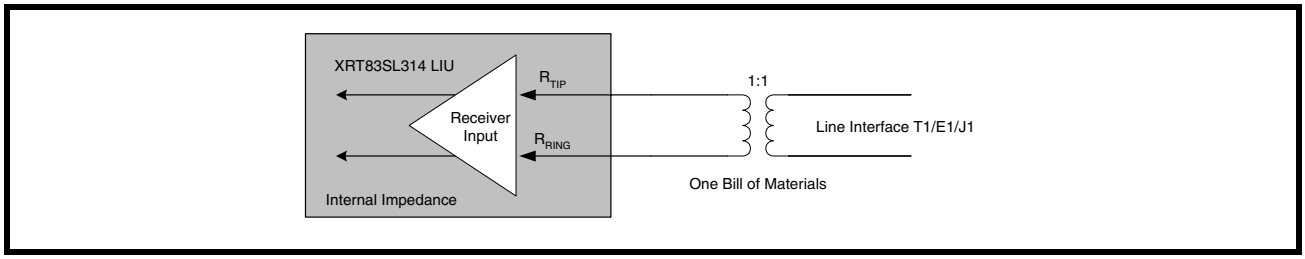
The input stage of the receive path accepts standard T1/E1/J1 twisted pair or E1 coaxial cable inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The receive termination (along with the transmit termination) impedance is selected by programming TERSEL[1:0] to match the line impedance. Selecting the internal impedance is shown in Table 2.

TABLE 2: SELECTING THE INTERNAL IMPEDANCE

TERSEL[1:0]	RECEIVE TERMINATION
0h (00)	100Ω
1h (01)	110Ω
2h (10)	75Ω
3h (11)	120Ω

The XRT83SL314 has the ability to switch the internal termination to "High" impedance by programming RxTSEL in the appropriate channel register. For internal termination, set RxTSEL to "1". By default, RxTSEL is set to "0" ("High" impedance). For redundancy applications, a dedicated hardware pin (RxTSEL) is also available to control the receive termination for all channels simultaneously. This hardware pin takes priority over the register setting if RxTCNTL is set to "1" in the appropriate global register. If RxTCNTL is set to "0", the state of this pin is ignored. See Figure 4 for a typical connection diagram using the internal termination.

FIGURE 4. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



2.1.2 CASE 2: Internal Termination With One External Fixed Resistor for All Modes

Along with the internal termination, a high precision external fixed resistor can be used to optimize the return loss. This external resistor can be used for all modes of operation ensuring one bill of materials. There are three resistor values that can be used by setting the RxRES[1:0] bits in the appropriate channel register. Selecting the value for the external fixed resistor is shown in Table 3.

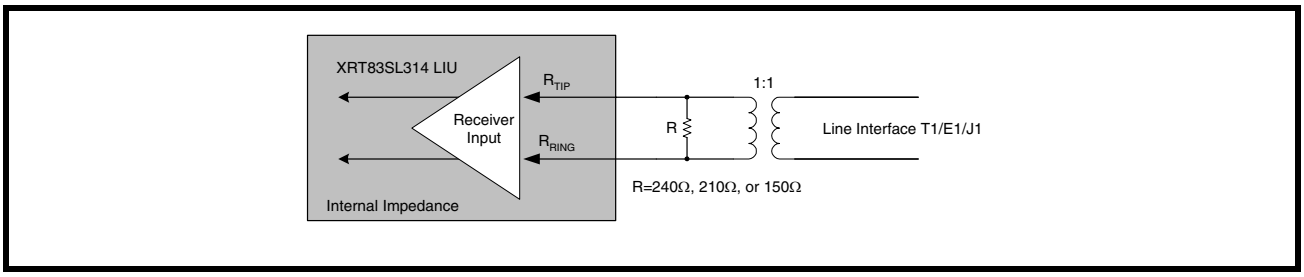
TABLE 3: SELECTING THE VALUE OF THE EXTERNAL FIXED RESISTOR

RxRES[1:0]	EXTERNAL FIXED RESISTOR
0h (00)	None
1h (01)	240Ω
2h (10)	210Ω
3h (11)	150Ω

By default, RxRES[1:0] is set to "None" for no external fixed resistor. If an external fixed resistor is used, the XRT83SL314 uses the parallel combination of the external fixed resistor and the internal termination as the input impedance. See Figure 5 for a typical connection diagram using the external fixed resistor.

NOTE: *Without the external resistor, the XRT83SL314 meets all return loss specifications. This mode was created to add flexibility for optimizing return loss by using a high precision external resistor.*

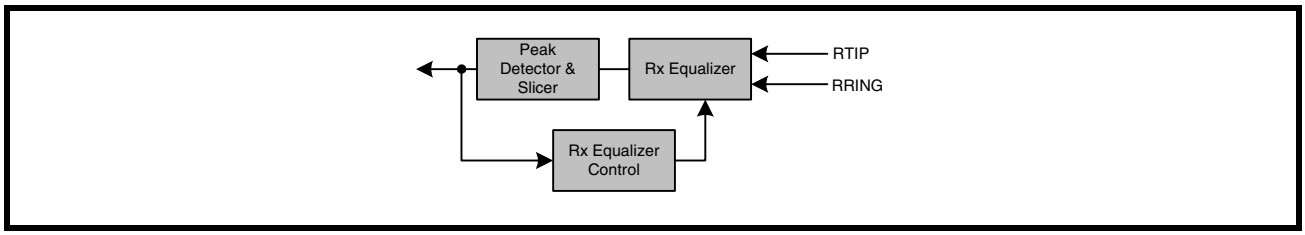
FIGURE 5. TYPICAL CONNECTION DIAGRAM USING ONE EXTERNAL FIXED RESISTOR



2.2 Equalizer Control

The main objective of the equalizer is to amplify an input attenuated signal to a pre-determined amplitude that is acceptable to the peak detector circuit. Using feedback from the peak detector, the equalizer will gain the input up to the maximum value specified by the equalizer control bits, in the appropriate channel register, normalizing the signal. Once the signal has reached the pre-determined amplitude, the signal is then processed within the peak detector and slicer circuit. A simplified block diagram of the equalizer and peak detector is shown in Figure 6.

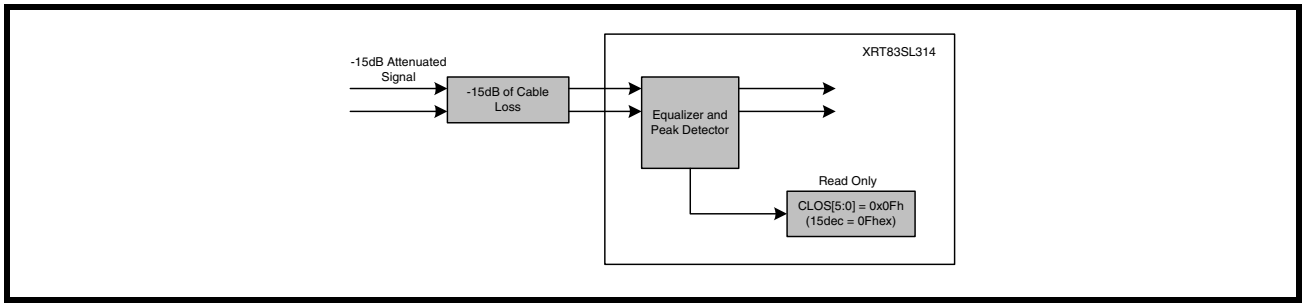
FIGURE 6. SIMPLIFIED BLOCK DIAGRAM OF THE EQUALIZER AND PEAK DETECTOR



2.3 Cable Loss Indicator

The ability to monitor the cable loss attenuation of the receiver inputs is a valuable feature. The XRT83SL314 contains a per channel, read only register for cable loss indication. CLOS[5:0] is a 6-Bit binary word that reports the value of cable loss in 1dB steps. An example of -15dB cable loss attenuation is shown in Figure 7.

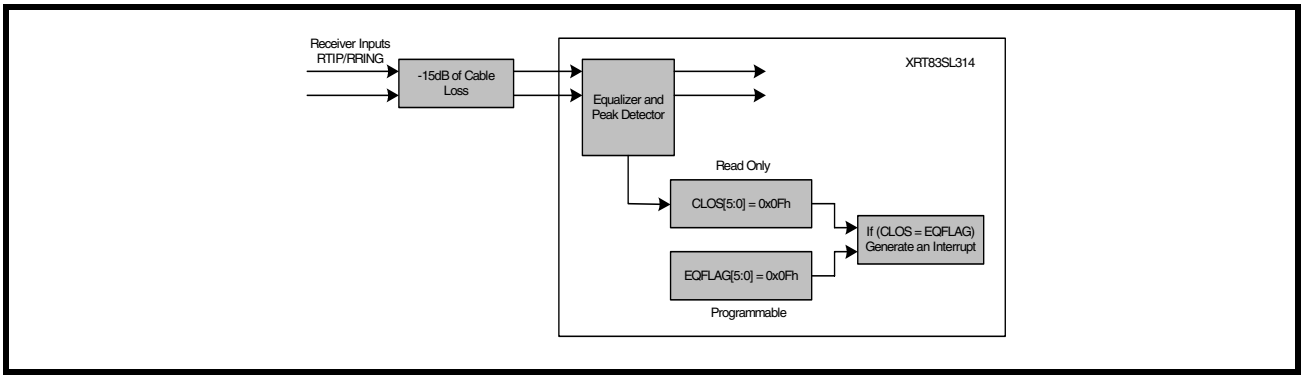
FIGURE 7. SIMPLIFIED BLOCK DIAGRAM OF THE CABLE LOSS INDICATOR



2.4 Equalizer Attenuation Flag

The ability to detect the amount of cable loss on the receiver inputs is enhanced by having the ability to generate an interrupt by programming a pre-determined value for cable loss into the EQFLAG[5:0] global register. This is particularly useful in applications where it is necessary for the LIU to generate an interrupt for a cable loss which is lower than the declaration of the RLOS feature (see the RLOS section in this datasheet). If the contents of the EQFLAG[5:0] register bits are equal to or less than the contents in the cable loss indicator bits CLOS[5:0] for a given channel, an interrupt will be generated (if enabled in the appropriate channel register and GIE is to "1"). Using the same example in Figure 7, a simplified block diagram of the equalizer flag is shown in Figure 8.

FIGURE 8. SIMPLIFIED BLOCK DIAGRAM OF THE EQUALIZER ATTENUATION FLAG



2.5 Peak Detector and Slicer

The peak detector provides feedback to the equalizer control circuit until the amplitude of the incoming signal is at an appropriate level. Once this level is obtained, the slicer identifies the incoming signal as a "1" and passes the raw data to the clock and data recovery circuit. The slicer threshold is selected by programming SL[1:0] in the appropriate global register. Selecting the slicer level is shown in Table 4.

TABLE 4: SELECTING THE SLICER LEVEL FOR THE PEAK DETECTOR

SL[1:0]	SLICER LEVEL
0h (00)	50%
1h (01)	45%
2h (10)	55%
3h (11)	68%

2.6 Clock and Data Recovery

The receive clock (RCLK) is recovered by the clock and data recovery circuitry. An internal PLL locks on the incoming data stream and outputs a clock that's in phase with the incoming signal. This allows for multi-channel T1/E1/J1 signals to arrive from different timing sources and remain independent. In the absence of an incoming signal, RCLK maintains its timing by using the internal master clock as its reference. The recovered data can be updated on either edge of RCLK. By default, data is updated on the rising edge of RCLK. To update data on the falling edge of RCLK, set RCLKE to "1" in the appropriate global register. Figure 9 is a timing diagram of the receive data updated on the rising edge of RCLK. Figure 10 is a timing diagram of the receive data updated on the falling edge of RCLK. The timing specifications are shown in Table 5.

FIGURE 9. RECEIVE DATA UPDATED ON THE RISING EDGE OF RCLK

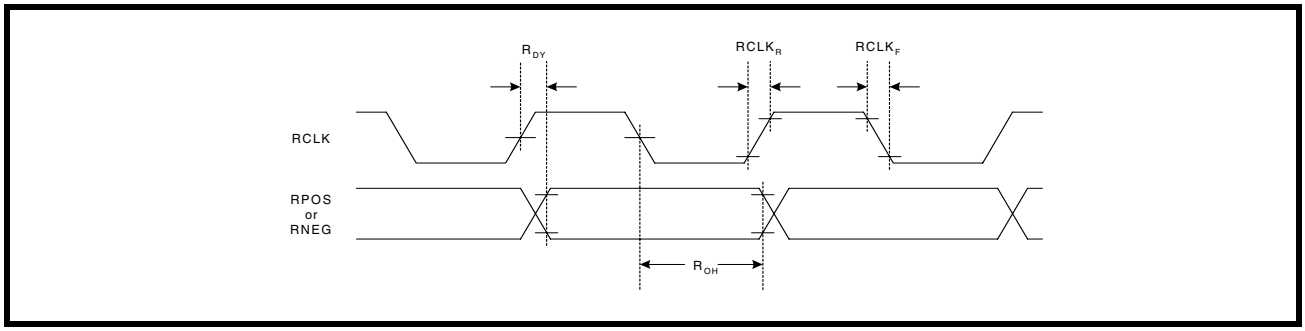


FIGURE 10. RECEIVE DATA UPDATED ON THE FALLING EDGE OF RCLK

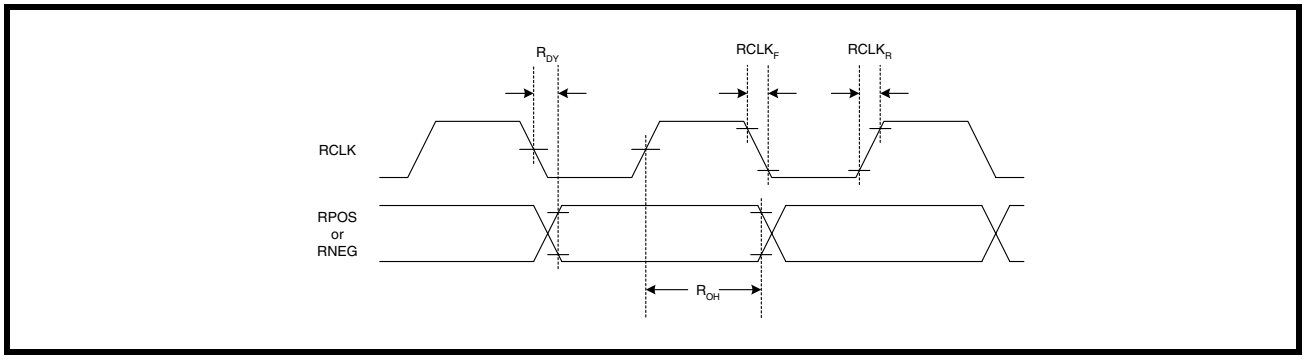


TABLE 5: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG

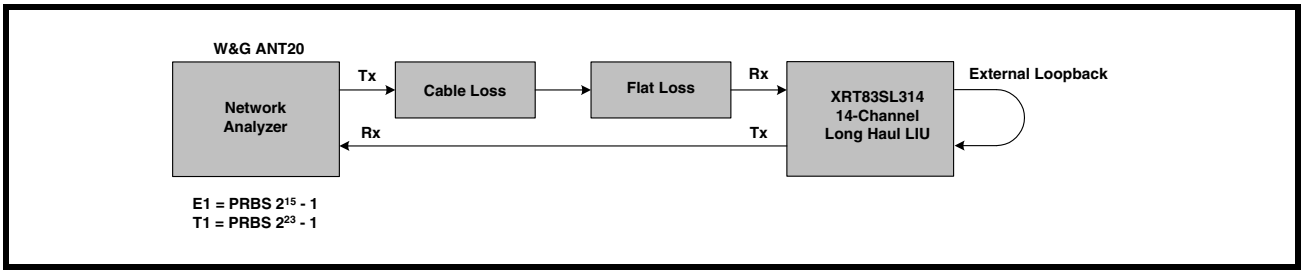
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RCLK Duty Cycle	R_{CDU}	45	50	55	%
Receive Data Setup Time	R_{SU}	150	-	-	ns
Receive Data Hold Time	R_{HO}	150	-	-	ns
RCLK to Data Delay	R_{DY}	-	-	40	ns
RCLK Rise Time (10% to 90%) with 25pF Loading	$RCLK_R$	-	-	40	ns
RCLK Fall Time (90% to 10%) with 25pF Loading	$RCLK_F$	-	-	40	ns

NOTE: *VDD=3.3V ±5%, T_A=25°C, Unless Otherwise Specified*

2.6.1 Receive Sensitivity

To meet short haul requirements, the XRT83SL314 can accept T1/E1/J1 signals that have been attenuated by 12dB of flat loss in E1 mode or by 655 feet of cable loss along with 6dB of flat loss in T1 mode. However, the XRT83SL314 can tolerate cable loss and flat loss beyond the industry specifications. The receive sensitivity in the short haul mode is approximately 4,000 feet without experiencing bit errors, LOF, pattern synchronization, etc. Although data integrity is maintained, the RLOS function (if enabled) will report an RLOS condition according to the receiver loss of signal section in this datasheet. The test configuration for measuring the receive sensitivity is shown in Figure 11.

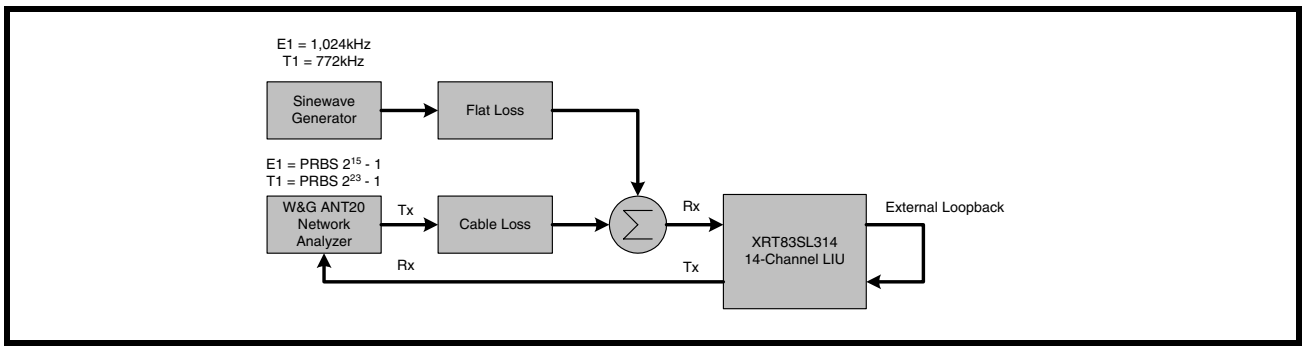
FIGURE 11. TEST CONFIGURATION FOR MEASURING RECEIVE SENSITIVITY



2.6.2 Interference Margin

The interference margin for the XRT83SL314 will be added when the first revision of silicon arrives. The test configuration for measuring the interference margin is shown in Figure 12.

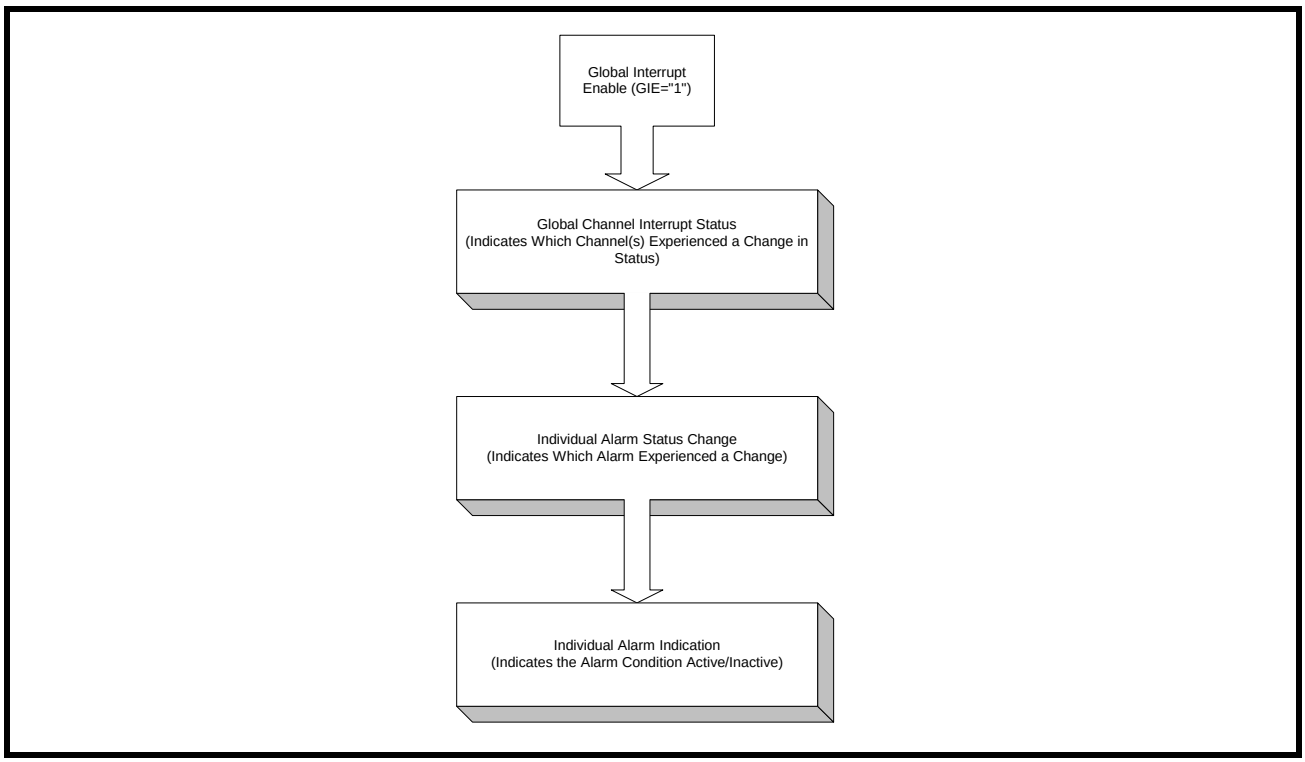
FIGURE 12. TEST CONFIGURATION FOR MEASURING INTERFERENCE MARGIN



2.6.3 General Alarm Detection and Interrupt Generation

The receive path detects EQFLAG, RLOS, AIS, QRPD, NCLD, and FLS. These alarms can be individually masked to prevent the alarm from triggering an interrupt. To enable interrupt generation, the Global Interrupt Enable (GIE) bit must be set "High" in the appropriate global register. Any time a change in status occurs (it the alarms are enabled), the interrupt pin will pull "Low" to indicate an alarm has occurred. Once the status registers have been read, the INT pin will return "High". The status registers are Reset Upon Read (RUR). The interrupts are categorized in a hierarchical process block. Figure 13 is a simplified block diagram of the interrupt generation process.

FIGURE 13. INTERRUPT GENERATION PROCESS BLOCK



NOTE: *The interrupt pin is internally pulled "High" with a 50KΩ resistor.*

2.6.3.1 RLOS (Receiver Loss of Signal)

In T1 mode, RLOS is declared if an incoming signal has no transitions over a period of 175 +/-75 contiguous pulse intervals. However, the XRT83SL314 LIU has a built in analog RLOS so that the user can be notified when the amplitude of the incoming signal has been attenuated -9dB below the equalizer gain setting. For example: In T1 or E1 short haul mode, the equalizer gain setting is 15dB. Once the input reaches an amplitude of -24dB below nominal, the LIU will declare RLOS. The RLOS circuitry clears when the input reaches +3dB relative to where it was declared. This +3dB value is a pre-determined hysteresis so that transients will not cause the RLOS to clear. In E1 mode, RLOS is declared if an incoming signal has no transitions for N consecutive pulse intervals, where 10≤N≤255. According to G.775, no transitions in E1 mode is defined between -9dB and -35dB below nominal. Figure 14 is a simplified block diagram of the analog RLOS function. Table 6 summarizes the analog RLOS values for the different equalizer gain settings.

FIGURE 14. ANALOG RECEIVE LOS OF SIGNAL FOR T1/E1/J1

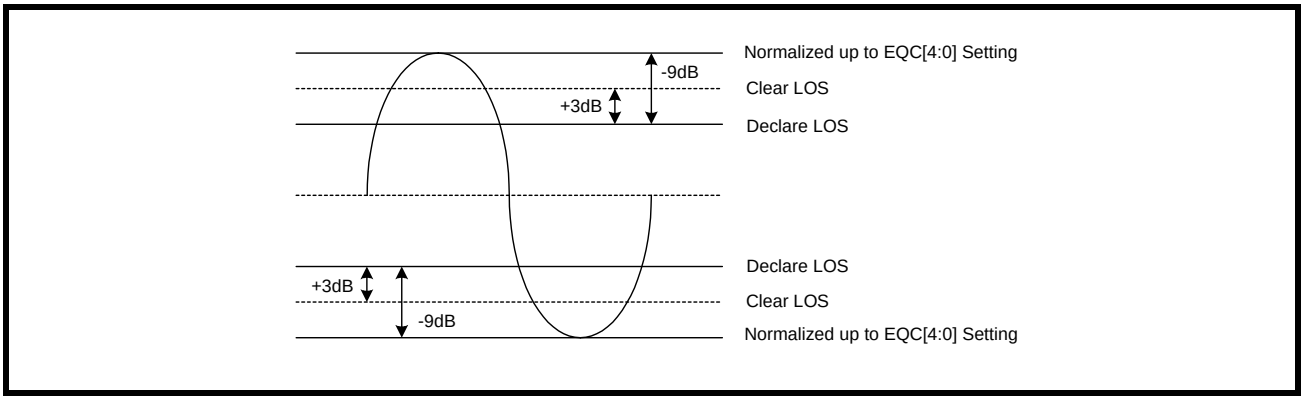


TABLE 6: ANALOG RLOS DECLARE/CLEAR (TYPICAL VALUES) FOR T1/E1

GAIN SETTING	DECLARE	CLEAR
15dB (Short Haul Mode)	-24dB	-21dB
29dB (Monitoring Gain Mode)	-38dB	-35dB

NOTE: *For programming the equalizer gain setting on a per channel basis, see the microprocessor register map for details.*

2.6.3.2 EXLOS (Extended Loss of Signal)

By enabling the extended loss of signal by programming the appropriate channel register, the digital RLOS is extended to count 4,096 consecutive zeros before declaring RLOS in T1 and E1 mode. By default, EXLOS is disabled and RLOS operates in normal mode.

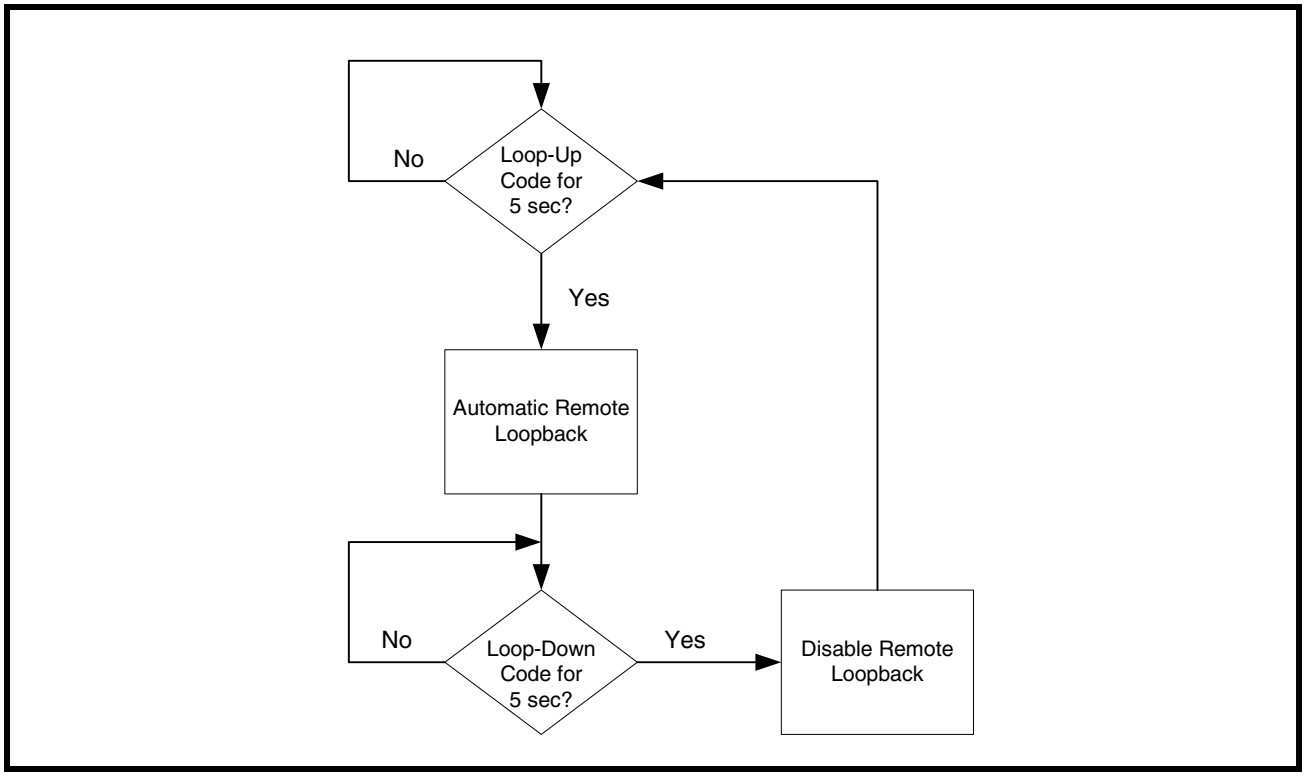
2.6.3.3 AIS (Alarm Indication Signal)

The XRT83SL314 adheres to the ITU-T G.775 specification for an all ones pattern. The alarm indication signal is set to "1" if an all ones pattern (at least 99.9% ones density) is present for T, where T is 3ms to 75ms in T1 mode. AIS will clear when the ones density is not met within the same time period T. In E1 mode, the AIS is set to "1" if the incoming signal has 2 or less zeros in a 512-bit window. AIS will clear when the incoming signal has 3 or more zeros in the 512-bit window.

2.6.3.4 NLCD (Network Loop Code Detection)

The Network Loop Code Detection can be programmed to detect a Loop-Up, Loop-Down, or Automatic Loop Code. If the network loop code detection is programmed for Loop-Up, the NLCD will be set "High" if a repeating pattern of "00001" occurs for more than 5 seconds. If the network loop code detection is programmed for Loop-Down, the NLCD will be set "High" if a repeating pattern of "001" occurs for more than 5 seconds. If the network loop code detection is programmed for automatic loop code, the LIU is configured to detect a Loop-Up code. If a Loop-Up code is detected for more than 5 seconds, the XRT83SL314 will automatically program the channel into a remote loopback mode. The LIU will remain in remote loopback even if the Loop-Up code disappears. The channel will continue in remote loop back until a Loop-Down code is detected for more than 5 seconds (or, if the automatic loop code is disabled) and then automatically return to normal operation with no loop back. The process of the automatic loop code detection is shown in Figure 15.

FIGURE 15. PROCESS BLOCK FOR AUTOMATIC LOOP CODE DETECTION



2.6.3.5 FLSD (FIFO Limit Status Detection)

The purpose of the FIFO limit status is to indicate when the Read and Write FIFO pointers are within a pre-determined range (over-flow or under-flow indication). The FLSD is set to "1" if the FIFO Read and Write Pointers are within ±3-Bits.

2.6.3.6 LCVD (Line Code Violation Detection)

The LIU contains 14 independent, 16-bit LCV counters. When the counters reach full-scale, they remain saturated at FFFFh until they are reset globally or on a per channel basis. For performance monitoring, the counters can be updated globally or on a per channel basis to place the contents of the counters into holding registers. The LIU uses an indirect address bus to access a counter for a given channel. Once the contents of the counters have been placed in holding registers, they can be individually read out from register 0xE8h 8-bits at a time according to the BYTEsel bit in the appropriate global register. By default, the LSB is in register 0xE8h until the BYTEsel is pulled "High" where upon the MSB will be placed in the register for read back. Once both bytes have been read, the next channel may be selected for read back.

By default, the LVC/OFD will be set to a "1" if the receiver is currently detecting line code violations or excessive zeros for HDB3 (E1 mode) or B8ZS (T1 mode). In AMI mode, the LCVD will be set to a "1" if the receiver is currently detecting bipolar violations or excessive zeros. However, if the LIU is configured to monitor the 16-bit LCV counter by programming the appropriate global register, the LCV/OFD will be set to a "1" if the counter saturates.

2.7 Receive Jitter Attenuator

The receive path has a dedicated jitter attenuator that reduces phase and frequency jitter in the recovered clock. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth of 32-bit or 64-bit. If the LIU is used for line synchronization (loop timing systems), the JA should be enabled. When the Read and Write pointers of the FIFO are within 2-Bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this condition occurs, the jitter attenuator will not attenuate input jitter until the Read/Write pointer's position is outside the 2-Bit window. In T1 mode, the bandwidth of the JA is always set to 3Hz. In E1 mode, the bandwidth is programmable to either 10Hz or 1.5Hz (1.5Hz automatically selects the 64-Bit FIFO depth). The JA has a clock delay equal to ½ of the FIFO bit depth.

NOTE: *If the LIU is used in a multiplexer/mapper application where stuffing bits are typically removed, the transmit path has a dedicated jitter attenuator to smooth out the gapped clock. See the Transmit Section of this datasheet.*

2.8 HDB3/B8ZS Decoder

In single rail mode, RPOS can decode AMI or HDB3/B8ZS signals. For E1 mode, HDB3 is defined as any block of 4 successive zeros replaced with OOOV or BOOV, so that two successive V pulses are of opposite polarity to prevent a DC component. In T1 mode, 8 successive zeros are replaced with OOOVBOVB. If the HDB3/B8ZS decoder is selected, the receive path removes the V and B pulses so that the original data is output to RPOS.

2.9 RPOS/RNEG/RCLK

The digital output data can be programmed to either single rail or dual rail formats. Figure 16 is a timing diagram of a repeating "0011" pattern in single-rail mode. Figure 17 is a timing diagram of the same fixed pattern in dual rail mode.

FIGURE 16. SINGLE RAIL MODE WITH A FIXED REPEATING "0011" PATTERN

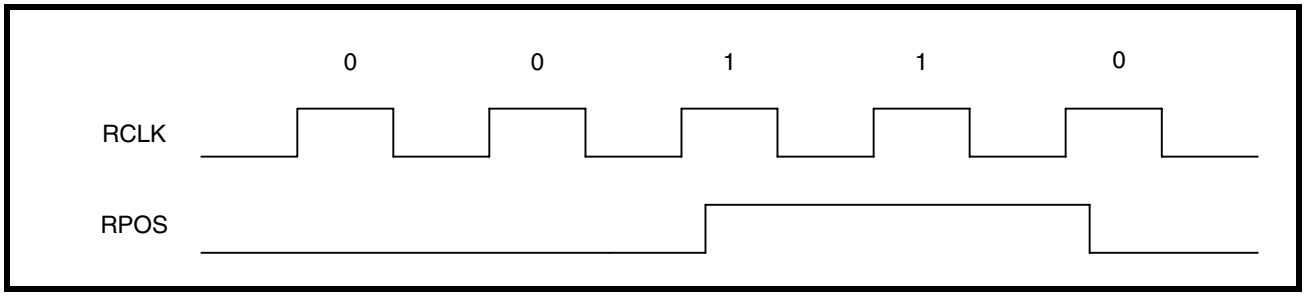
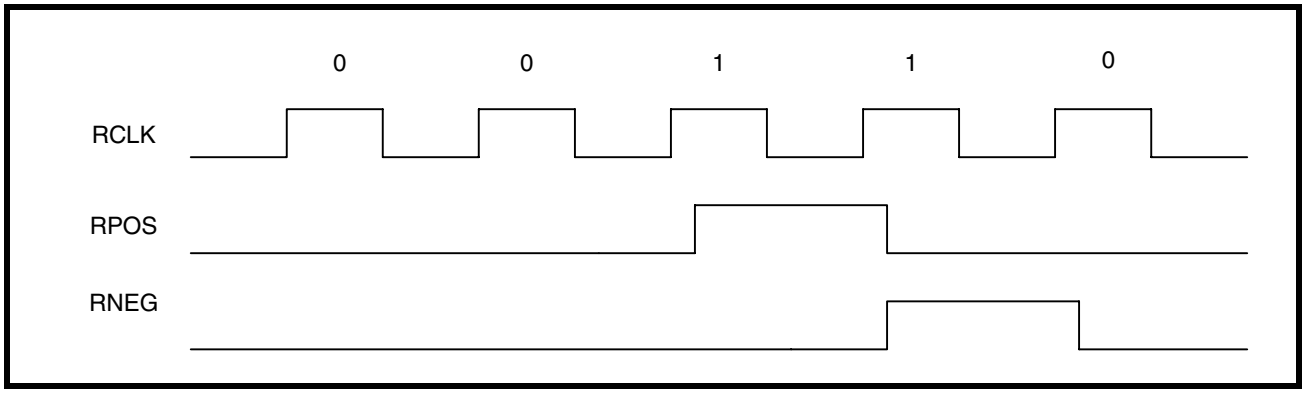


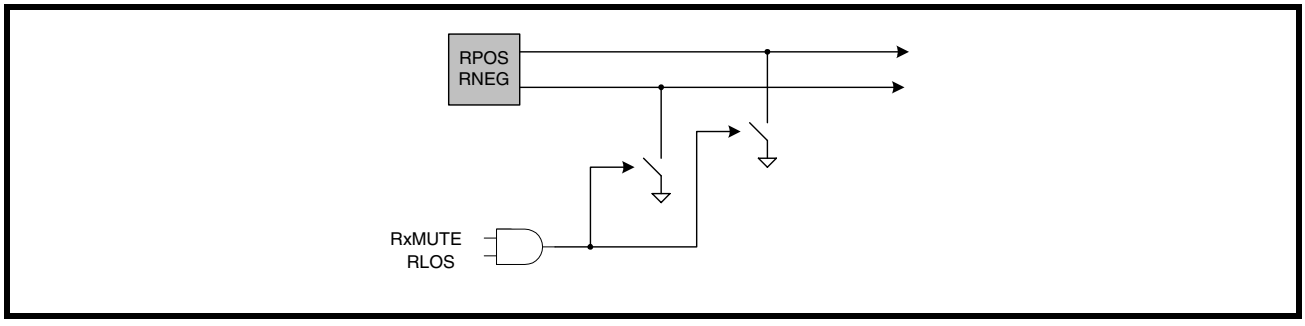
FIGURE 17. DUAL RAIL MODE WITH A FIXED REPEATING "0011" PATTERN



2.10 RxMUTE (Receiver LOS with Data Muting)

The receive muting function can be selected by setting RxMUTE to "1" in the appropriate global register. If selected, any channel that experiences an RLOS condition will automatically pull RPOS and RNEG "Low" to prevent data chattering. If RLOS does not occur, the RxMUTE will remain inactive until an RLOS on a given channel occurs. The default setting for RxMUTE is "0" which is disabled. A simplified block diagram of the RxMUTE function is shown in Figure 18.

FIGURE 18. SIMPLIFIED BLOCK DIAGRAM OF THE RXMUTE FUNCTION



3.0 T1/E1 APPLICATIONS

This applications section describes common T1/E1 system considerations along with references to application notes available for reference where applicable.

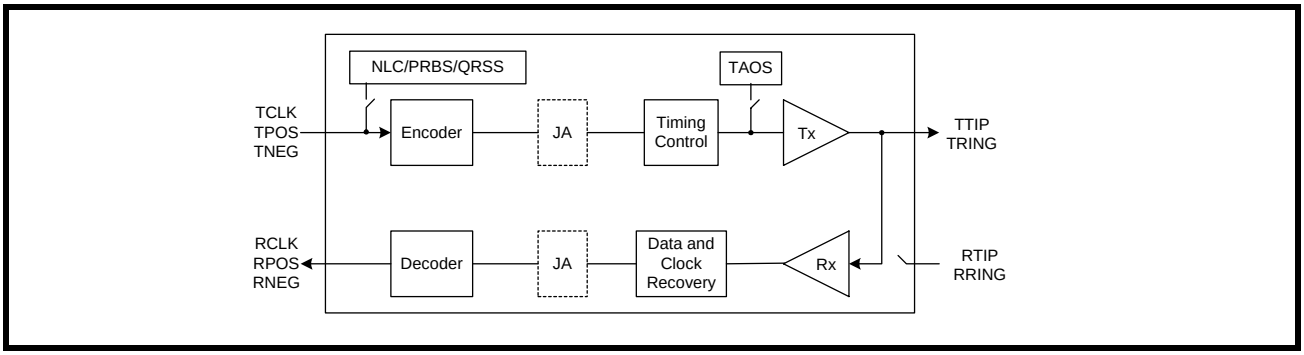
3.1 Loopback Diagnostics

The XRT83SL314 supports several loopback modes for diagnostic testing. The following section describes the local analog loopback, remote loopback, digital loopback, and dual loopback modes.

3.1.1 Local Analog Loopback

With local analog loopback activated, the transmit output data at TTIP/TRING is internally looped back to the analog inputs at RTIP/RRING. External inputs at RTIP/RRING are ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of local analog loopback is shown in Figure 19.

FIGURE 19. SIMPLIFIED BLOCK DIAGRAM OF LOCAL ANALOG LOOPBACK

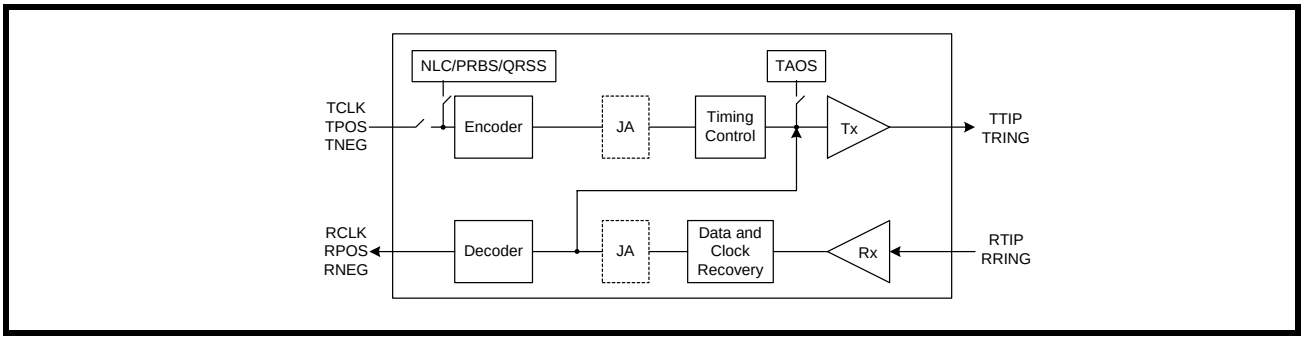


NOTE: *The transmit diagnostic features such as TAOS, NLC generation, and QRSS take priority over the transmit input data at TCLK/TPOS/TNEG.*

3.1.2 Remote Loopback

With remote loopback activated, the receive input data at RTIP/RRING is internally looped back to the transmit output data at TTIP/TRING. The remote loopback includes the Receive JA (if enabled). The transmit input data at TCLK/TPOS/TNEG are ignored while valid receive output data continues to be sent to the system. A simplified block diagram of remote loopback is shown in Figure 20.

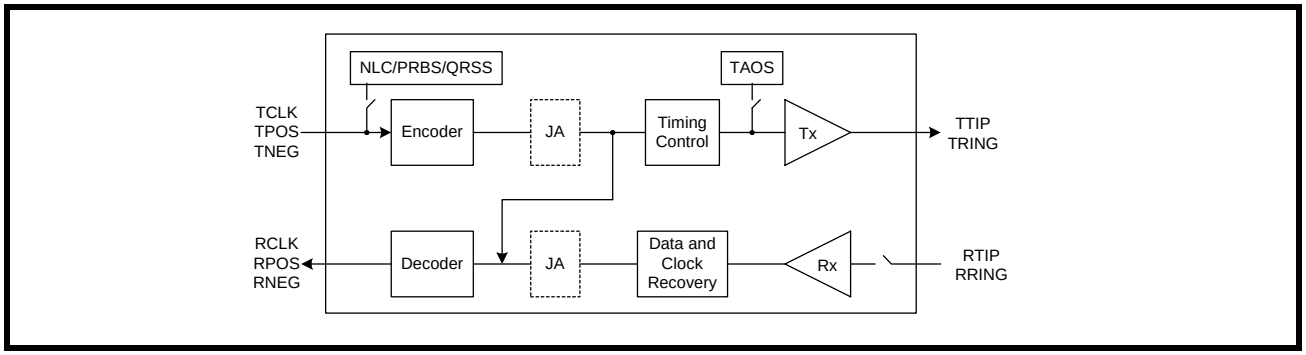
FIGURE 20. SIMPLIFIED BLOCK DIAGRAM OF REMOTE LOOPBACK



3.1.3 Digital Loopback

With digital loopback activated, the transmit input data at TCLK/TPOS/TNEG is looped back to the receive output data at RCLK/RPOS/RNEG. The digital loopback mode includes the Transmit JA (if enabled). The receive input data at RTIP/RRING is ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of digital loopback is shown in Figure 21.

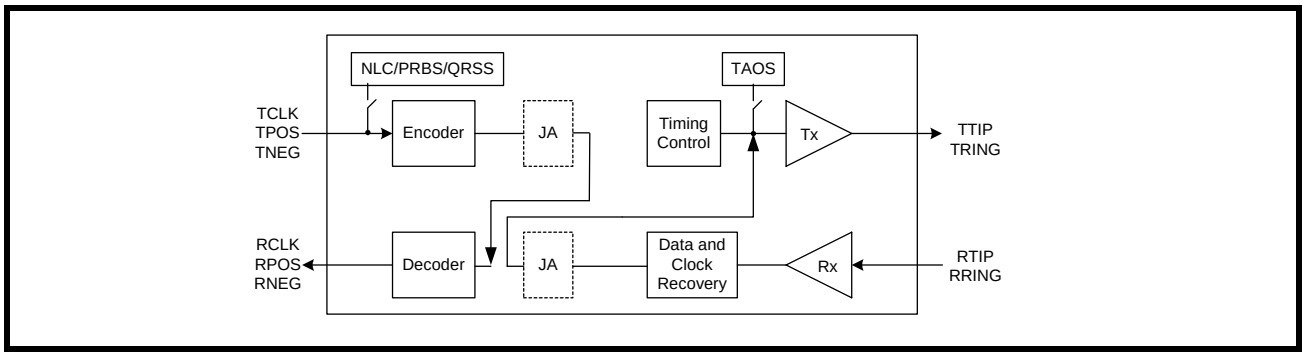
FIGURE 21. SIMPLIFIED BLOCK DIAGRAM OF DIGITAL LOOPBACK



3.1.4 Dual Loopback

With dual loopback activated, the remote loopback is combined with the digital loopback. A simplified block diagram of dual loopback is shown in Figure 22.

FIGURE 22. SIMPLIFIED BLOCK DIAGRAM OF DUAL LOOPBACK



3.2 84-Channel T1/E1 Multiplexer/Mapper Applications

The XRT83SL314 has the capability of providing the necessary chip selects for multiple 14-channel LIU devices. The LIU is responsible for selecting itself, up to 5 additional LIU devices, or all 6 devices simultaneously for permitting access to internal registers. The state of the chip select output pins is determined by a chip select decoder controlled by the 3 MSBs of the address bus ADDR[10:8]. Only one LIU (Master) requires the ADDR[10:8]. The other 5 LIU devices use the 8 LSBs for the direct address bus ADDR[7:0]. Figure 23 is a simplified block diagram of connecting six 14-channel LIU devices for 84-channel applications. Selection of the chip select outputs using ADDR[10:8] is shown in Table 7.

FIGURE 23. SIMPLIFIED BLOCK DIAGRAM OF AN 84-CHANNEL APPLICATION

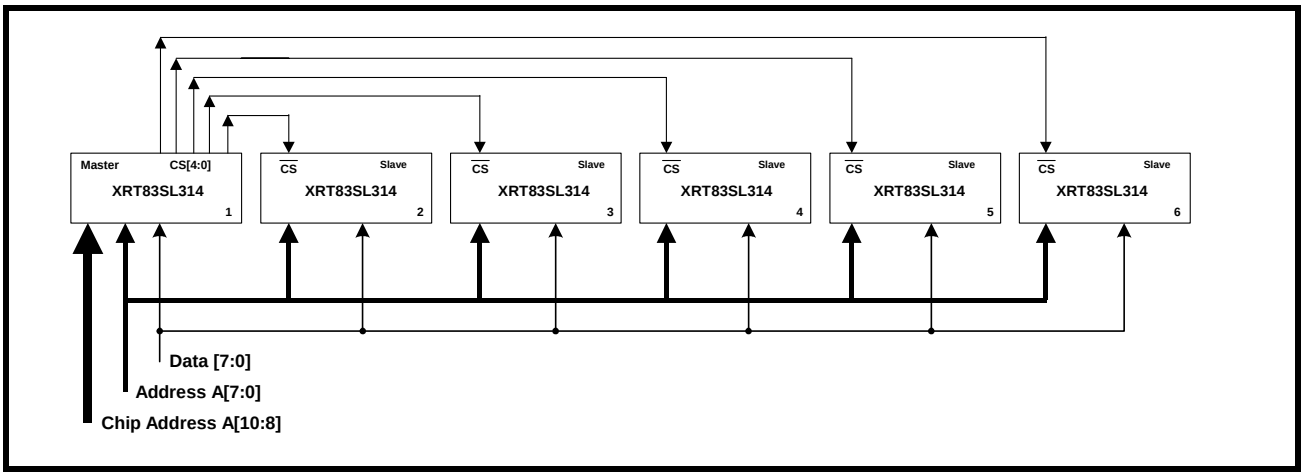


TABLE 7: CHIP SELECT ASSIGNMENTS

ADDR[10:8]	ACTIVE CHIP SELECT
0h (000)	Current Device (Master)
1h (001)	Chip 1
2h (010)	Chip 2
3h (011)	Chip 3
4h (100)	Chip 4
5h (101)	Chip 5
6h (110)	Reserved
7h (111)	All Devices Active

3.3 Line Card Redundancy

Telecommunication system design requires signal integrity and reliability. When a T1/E1 primary line card has a failure, it must be swapped with a backup line card while maintaining connectivity to a backplane without losing data. System designers can achieve this by implementing common redundancy schemes with the XRT83SL314 LIU. EXAR offers features that are tailored to redundancy applications while reducing the number of components and providing system designers with solid reference designs.

RLOS and DMO

If an RLOS or DMO condition occurs, the XRT83SL314 reports the alarm to the individual status registers on a per channel basis. However, for redundancy applications, an RLOS or DMO alarm can be used to initiate an automatic switch to the back up card. For this application, two global pins RLOS and DMO are used to indicate that one of the 14-channels has an RLOS or DMO condition.

Typical Redundancy Schemes

- 1:1 One backup card for every primary card (Facility Protection)
- 1+1 One backup card for every primary card (Line Protection)
- ·N+1 One backup card for N primary cards

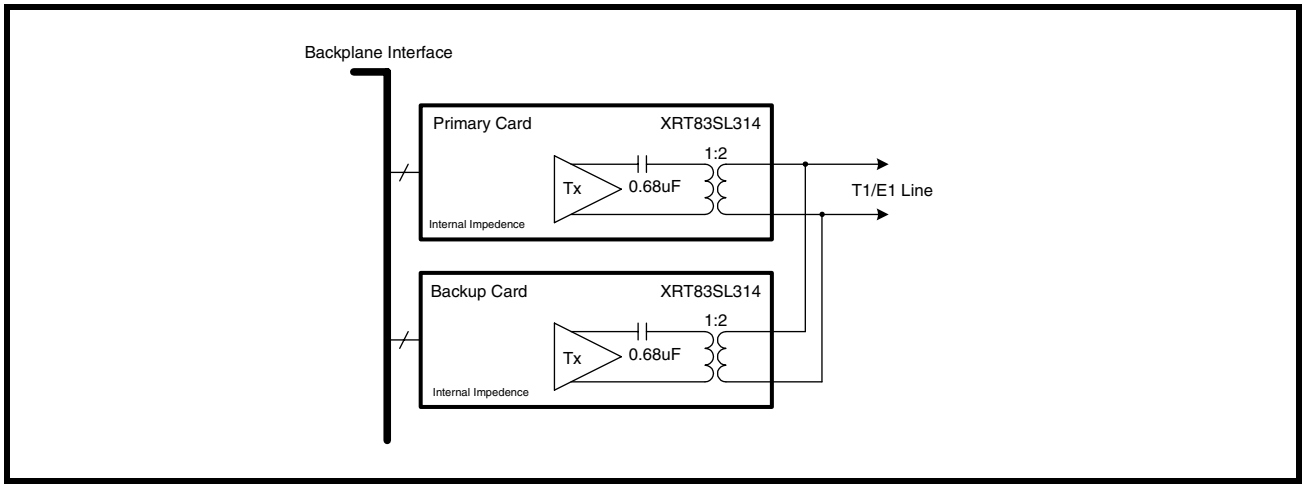
3.3.1 1:1 and 1+1 Redundancy Without Relays

The 1:1 facility protection and 1+1 line protection have one backup card for every primary card. When using 1:1 or 1+1 redundancy, the backup card has its transmitters tri-stated and its receivers in high impedance. This eliminates the need for external relays and provides one bill of materials for all interface modes of operation. For 1+1 line protection, the receiver inputs on the backup card have the ability to monitor the line for bit errors while in high impedance. The transmit and receive sections of the LIU device are described separately.

3.3.2 Transmit Interface with 1:1 and 1+1 Redundancy

The transmitters on the backup card should be tri-stated. Select the appropriate impedance for the desired mode of operation, T1/E1/J1. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See Figure 24. for a simplified block diagram of the transmit section for a 1:1 and 1+1 redundancy.

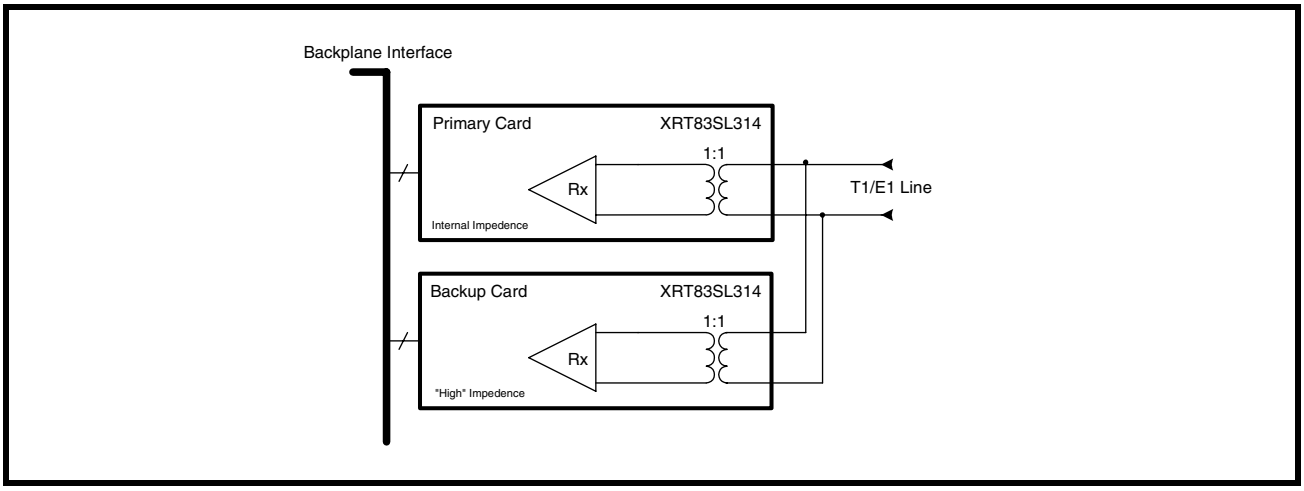
FIGURE 24. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR 1:1 AND 1+1 REDUNDANCY



3.3.3 Receive Interface with 1:1 and 1+1 Redundancy

The receivers on the backup card should be programmed for "High" impedance. Since there is no external resistor in the circuit, the receivers on the backup card will not load down the line interface. This key design feature eliminates the need for relays and provides one bill of materials for all interface modes of operation. Select the impedance for the desired mode of operation, T1/E1/J1. To swap the primary card, set the backup card to internal impedance, then the primary card to "High" impedance. See Figure 25. for a simplified block diagram of the receive section for a 1:1 redundancy scheme.

FIGURE 25. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR 1:1 AND 1+1 REDUNDANCY



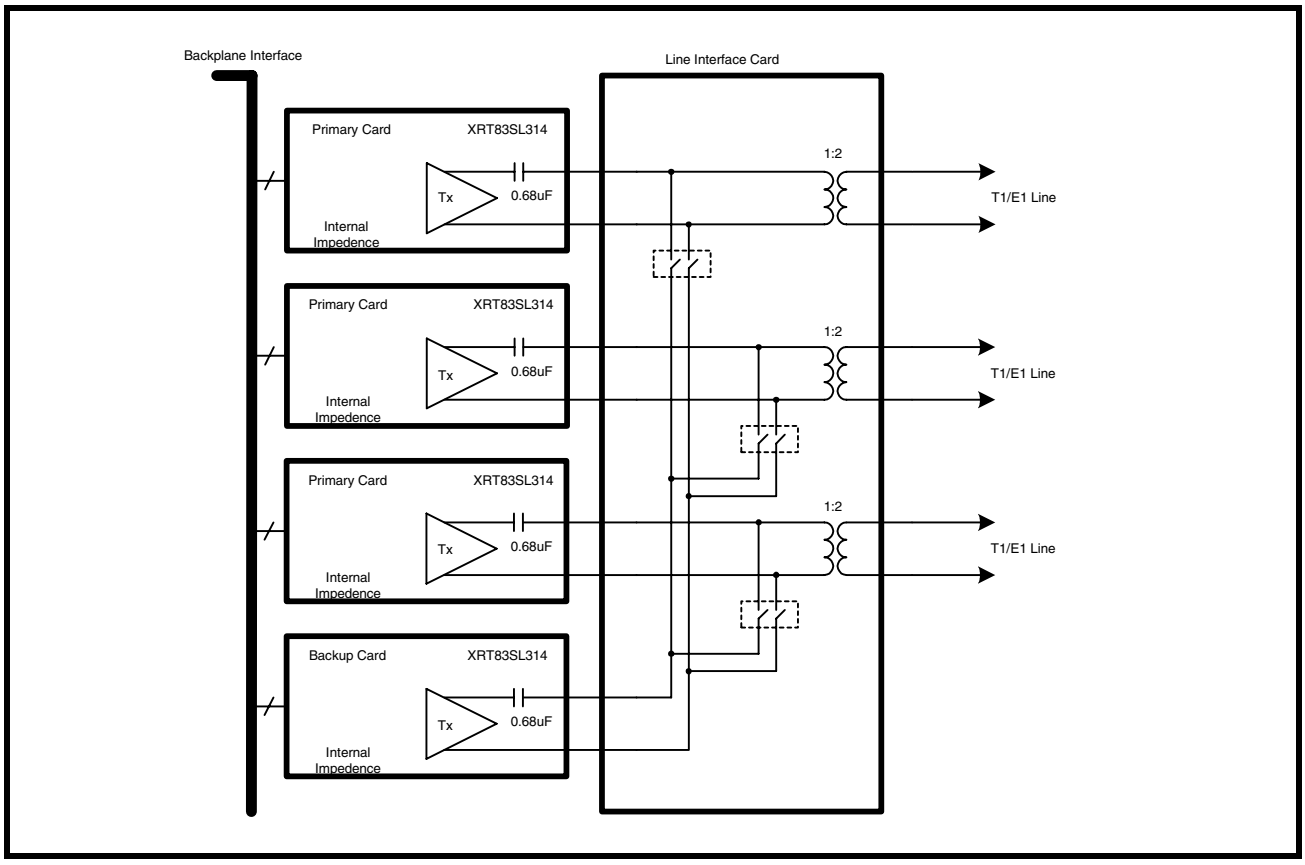
3.3.4 N+1 Redundancy Using External Relays

N+1 redundancy has one backup card for N primary cards. Due to impedance mismatch and signal contention, external relays are necessary when using this redundancy scheme. The relays create complete isolation between the primary cards and the backup card. This allows all transmitters and receivers on the primary cards to be configured in internal impedance, providing one bill of materials for all interface modes of operation. The transmit and receive sections of the LIU device are described separately.

3.3.5 Transmit Interface with N+1 Redundancy

For N+1 redundancy, the transmitters on all cards should be programmed for internal impedance. The transmitters on the backup card do not have to be tri-stated. To swap the primary card, close the desired relays, and tri-state the transmitters on the failed primary card. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See Figure 26 for a simplified block diagram of the transmit section for an N+1 redundancy scheme.

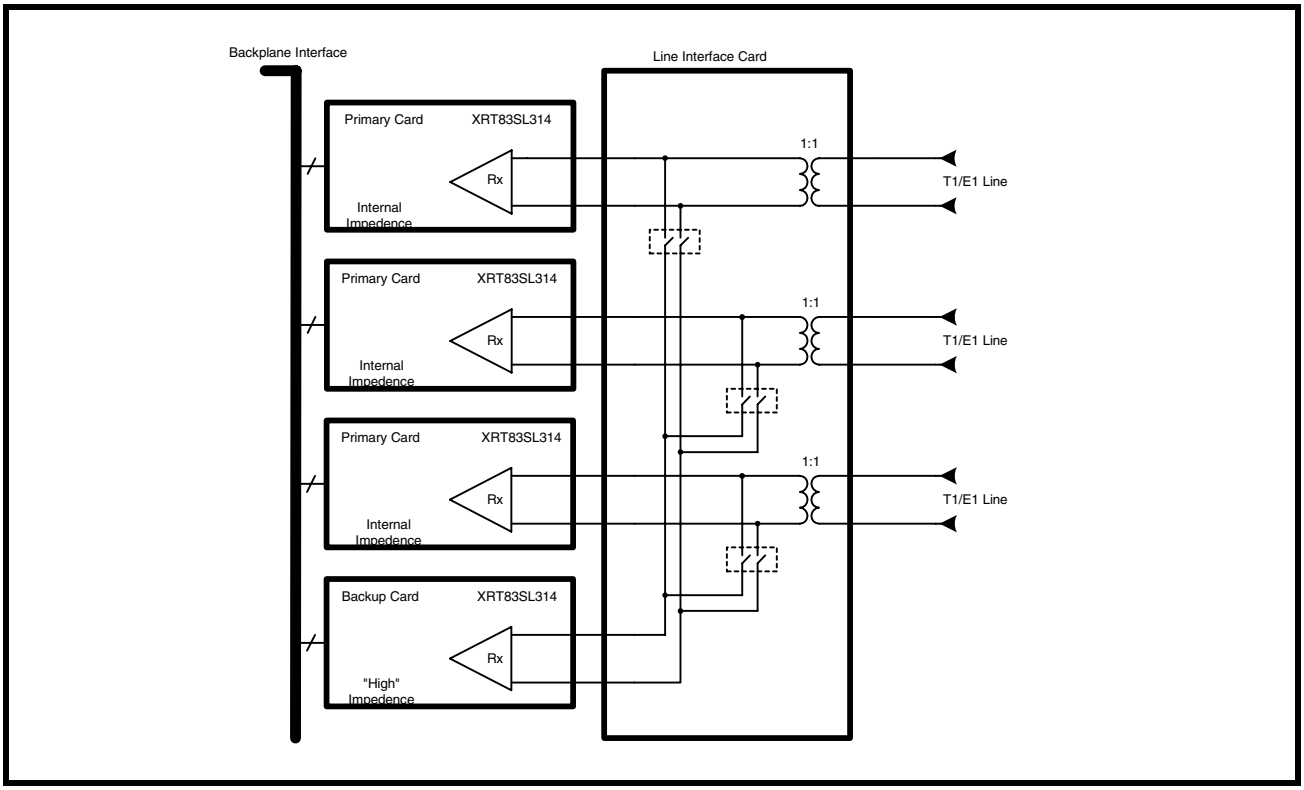
FIGURE 26. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR N+1 REDUNDANCY



3.3.6 Receive Interface with N+1 Redundancy

For N+1 redundancy, the receivers on the primary cards should be programmed for internal impedance. The receivers on the backup card should be programmed for "High" impedance mode. To swap the primary card, set the backup card to internal impedance, then the primary card to "High" impedance. See Figure 27 for a simplified block diagram of the receive section for a N+1 redundancy scheme.

FIGURE 27. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR N+1 REDUNDANCY



3.4 Power Failure Protection

For 1:1 or 1+1 line card redundancy in T1/E1 applications, power failure could cause a line card to change the characteristics of the line impedance, causing a degradation in system performance. The XRT83SL314 was designed to ensure reliability during power failures. The LIU has patented high impedance circuits that allow the receiver inputs and the transmitter outputs to be in "High" impedance when the LIU experiences a power failure or when the LIU is powered off.

NOTE: *For power failure protection, a transformer must be used to couple to the line interface. See the TAN-56 application note for more details.*

3.5 Overvoltage and Overcurrent Protection

Physical layer devices such as LIUs that interface to telecommunications lines are exposed to overvoltage transients posed by environmental threats. An Overvoltage transient is a pulse of energy concentrated over a small period of time, usually under a few milliseconds. These pulses are random and exceed the operating conditions of CMOS transceiver ICs. Electronic equipment connecting to data lines are susceptible to many forms of overvoltage transients such as lightning, AC power faults and electrostatic discharge (ESD). There are three important standards when designing a telecommunications system to withstand overvoltage transients.

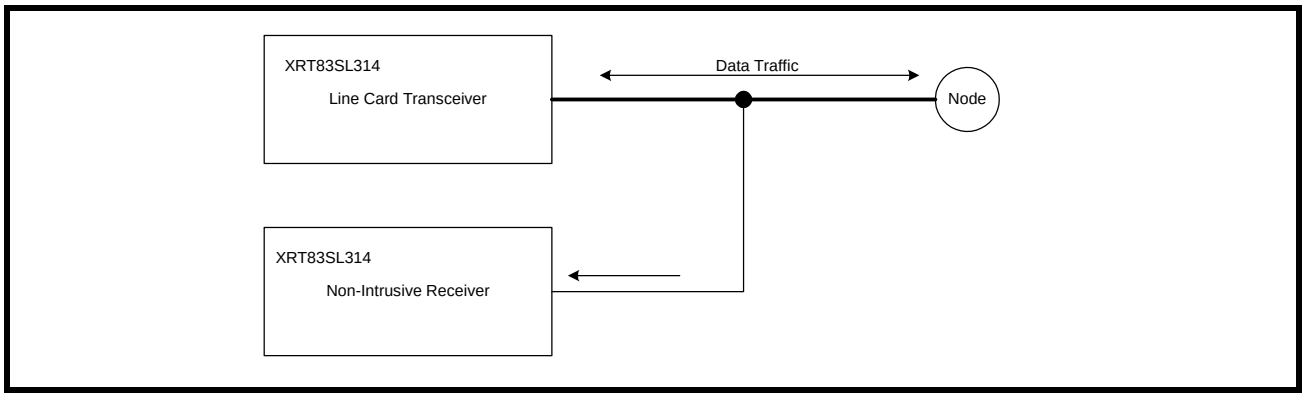
- UL1950 and FCC Part 68
- Telcordia (Bellcore) GR-1089
- ITU-T K.20, K.21 and K.41

NOTE: For a reference design and performance, *see the TAN-54 application note for more details.*

3.6 Non-Intrusive Monitoring

In non-intrusive monitoring applications, the transmitters are shut off by setting TxON "Low". The receivers must be actively receiving data without interfering with the line impedance. The XRT83SL314's internal termination ensures that the line termination meets T1/E1 specifications for 75Ω, 100Ω or 120Ω while monitoring the data stream. System integrity is maintained by placing the non-intrusive receiver in "High" impedance, equivalent to that of a 1+1 redundancy application. A simplified block diagram of non-intrusive monitoring is shown in Figure 28.

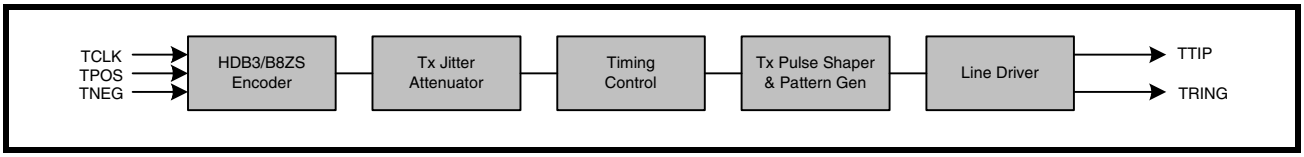
FIGURE 28. SIMPLIFIED BLOCK DIAGRAM OF A NON-INTRUSIVE MONITORING APPLICATION



4.0 TRANSMIT PATH LINE INTERFACE

The transmit path of the XRT83SL314 LIU consists of 14 independent T1/E1/J1 transmitters. The following section describes the complete transmit path from TCLK/TPOS/TNEG inputs to TTIP/TRING outputs. A simplified block diagram of the transmit path is shown in Figure 29.

FIGURE 29. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT PATH



4.1 TCLK/TPOS/TNEG Digital Inputs

In dual rail mode, TPOS and TNEG are the digital inputs for the transmit path. In single rail mode, TNEG has no function and can be left unconnected. The XRT83SL314 can be programmed to sample the inputs on either edge of TCLK. By default, data is sampled on the falling edge of TCLK. To sample data on the rising edge of TCLK, set TCLKE to "1" in the appropriate global register. Figure 30 is a timing diagram of the transmit input data sampled on the falling edge of TCLK. Figure 31 is a timing diagram of the transmit input data sampled on the rising edge of TCLK. The timing specifications are shown in Table 8.

FIGURE 30. TRANSMIT DATA SAMPLED ON FALLING EDGE OF TCLK

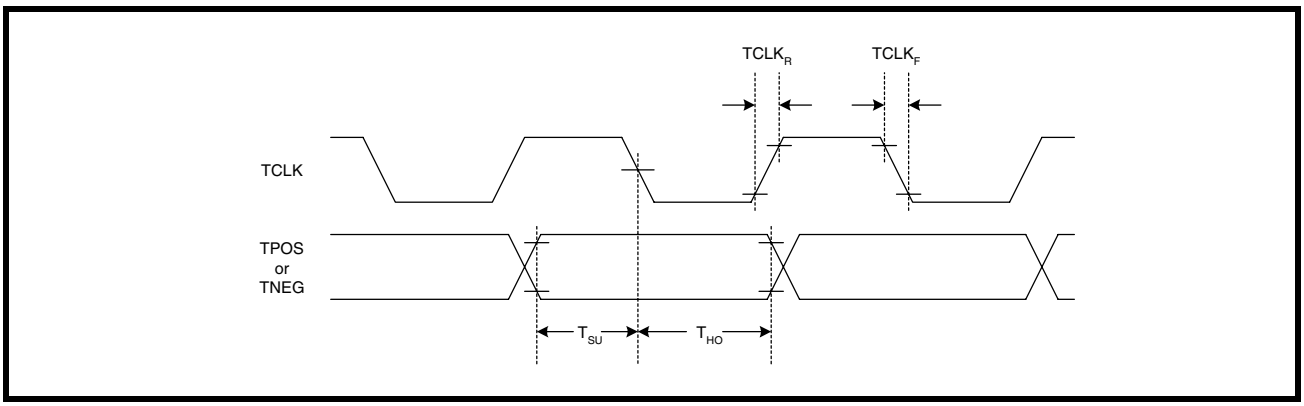


FIGURE 31. TRANSMIT DATA SAMPLED ON RISING EDGE OF TCLK

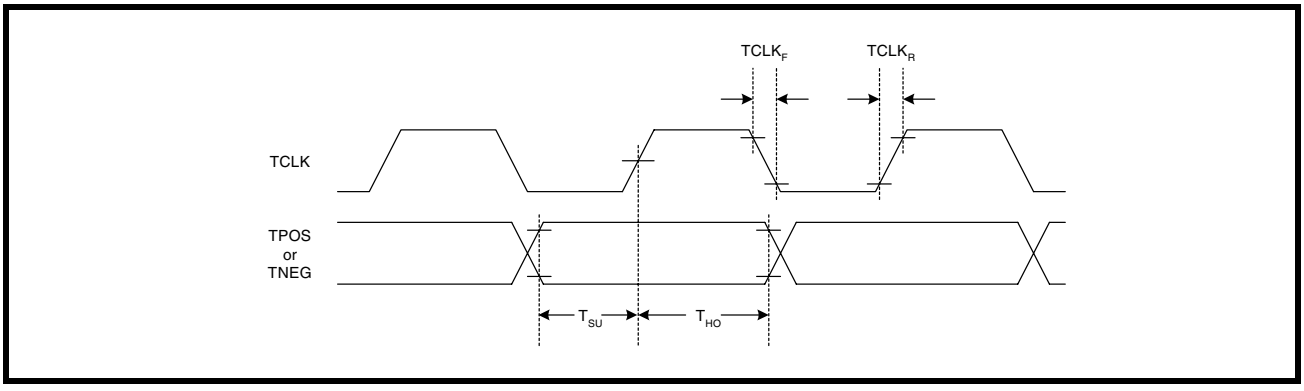


TABLE 8: TIMING SPECIFICATIONS FOR TCLK/TPOS/TNEG

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TCLK Duty Cycle	T_{CDU}	30	50	70	%
Transmit Data Setup Time	T_{SU}	50	-	-	ns
Transmit Data Hold Time	T_{HO}	30	-	-	ns
TCLK Rise Time (10% to 90%)	$TCLK_R$	-	-	40	ns
TCLK Fall Time (90% to 10%)	$TCLK_F$	-	-	40	ns

NOTE: *VDD=3.3V ±5%, T_A=25°C, Unless Otherwise Specified*

4.2 HDB3/B8ZS Encoder

In single rail mode, the LIU can encode the TPOS input signal to AMI or HDB3/B8ZS data. In E1 mode and HDB3 encoding selected, any sequence with four or more consecutive zeros in the input will be replaced with 000V or B00V, where "B" indicates a pulse conforming to the bipolar rule and "V" representing a pulse violating the rule. An example of HDB3 encoding is shown in Table 9. In T1 mode and B8ZS encoding selected, an input data sequence with eight or more consecutive zeros will be replaced using the B8ZS encoding rule. An example with Bipolar with 8 Zero Substitution is shown in Table 10.

TABLE 9: EXAMPLES OF HDB3 ENCODING

	NUMBER OF PULSES BEFORE NEXT 4 ZEROS	
Input		0000
HDB3 (Case 1)	Odd	000V
HDB3 (Case 2)	Even	B00V

TABLE 10: EXAMPLES OF B8ZS ENCODING

CASE 1	PRECEDING PULSE	NEXT 8 BITS
Input	+	00000000
B8ZS		000VB0VB
AMI Output	+	000+-0-+
Case 2		
Input	-	00000000
B8ZS		000VB0VB
AMI Output	-	000-+0+-

4.3 Transmit Jitter Attenuator

The XRT83SL314 LIU is ideal for multiplexer or mapper applications where the network data crosses multiple timing domains. As the higher data rates are de-multiplexed down to T1 or E1 data, stuffing bits are typically removed which can leave gaps in the incoming data stream. The transmit path has a dedicated jitter attenuator with a 32-Bit or 64-Bit FIFO that is used to smooth the gapped clock into a steady T1 or E1 output. The maximum gap width of the 14-Channel LIU is shown in Table 11.

TABLE 11: MAXIMUM GAP WIDTH FOR MULTIPLEXER/MAPPER APPLICATIONS

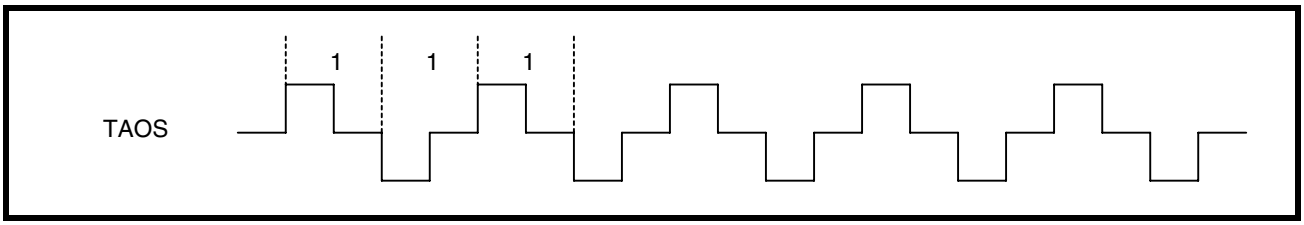
FIFO DEPTH	MAXIMUM GAP WIDTH
32-Bit	20 UI
64-Bit	50 UI

NOTE: *If the LIU is used in a loop timing system, the receive path has a dedicated jitter attenuator. See the Receive Section of this datasheet.*

4.4 TAOS (Transmit All Ones)

The XRT83SL314 has the ability to transmit all ones on a per channel basis by programming the appropriate channel register. This function takes priority over the digital data present on the TPOS/TNEG inputs. For example: If a fixed "0011" pattern is present on TPOS in single rail mode and TAOS is enabled, the transmitter will output all ones. In addition, if digital or dual loopback is selected, the data on the RPOS output will be equal to the data on the TPOS input. Figure 32 is a diagram showing the all ones signal at TTIP and TRING.

FIGURE 32. TAOS (TRANSMIT ALL ONES)



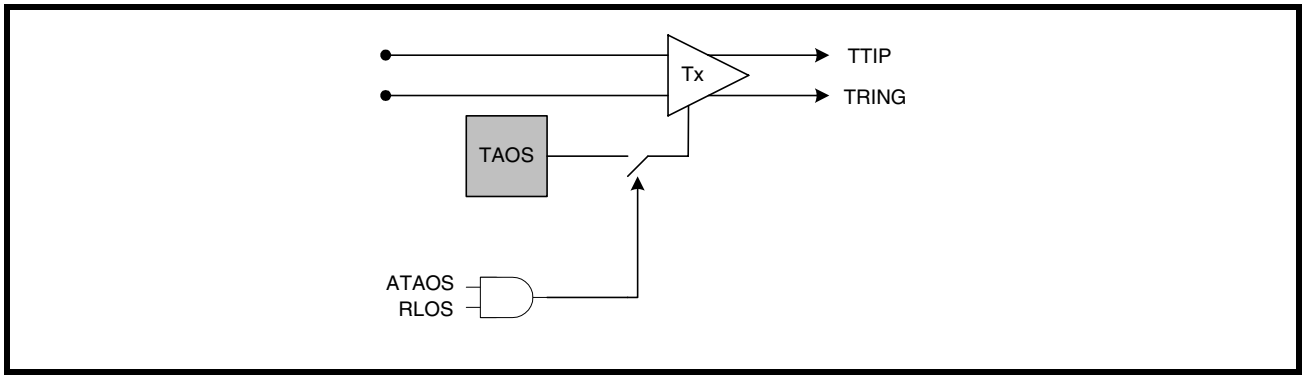
4.5 Transmit Diagnostic Features

In addition to TAOS, the XRT83SL314 offers multiple diagnostic features for analyzing network integrity such as ATAOS, Network Loop Code generation, and QRSS on a per channel basis by programming the appropriate registers. These diagnostic features take priority over the digital data present on TPOS/TNEG inputs. The transmitters will send the diagnostic code to the line and will be maintained in the digital loopback if selected. When the LIU is responsible for sending diagnostic patterns, the LIU is automatically placed in the single rail mode.

4.5.1 ATAOS (Automatic Transmit All Ones)

If ATAOS is selected by programming the appropriate global register, an AMI all ones signal will be transmitted for each channel that experiences an RLOS condition. If RLOS does not occur, the ATAOS will remain inactive until an RLOS on a given channel occurs. A simplified block diagram of the ATAOS function is shown in Figure 33.

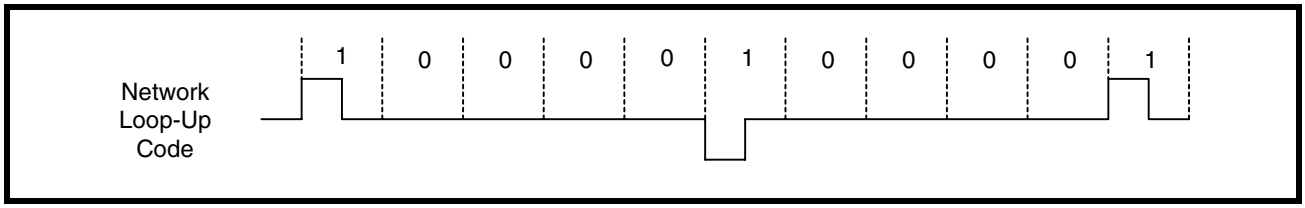
FIGURE 33. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION



4.5.2 Network Loop Up Code

By setting the LIU to generate a NLUC, the transmitters will send out a repeating "00001" pattern. The output waveform is shown in Figure 34.

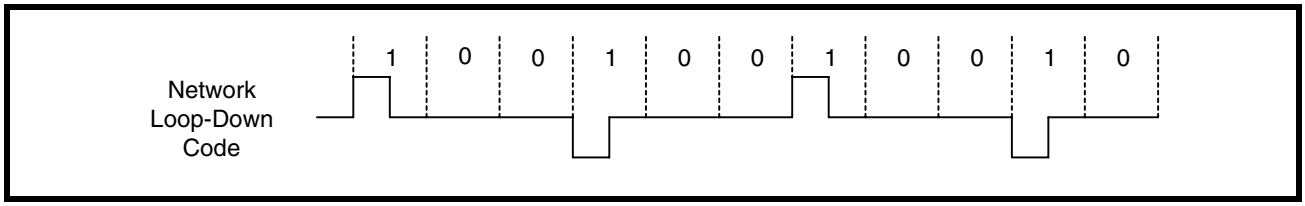
FIGURE 34. NETWORK LOOP UP CODE GENERATION



4.5.3 Network Loop Down Code

By setting the LIU to generate a NLDC, the transmitters will send out a repeating "001" pattern. The output waveform is shown in Figure 35.

FIGURE 35. NETWORK LOOP DOWN CODE GENERATION



4.5.4 QRSS Generation

The XRT83SL314 can transmit a QRSS random sequence to a remote location from TTIP/TRING. The polynomial is shown in Table 12.

TABLE 12: RANDOM BIT SEQUENCE POLYNOMIALS

RANDOM PATTERN	T1	E1
QRSS	$2^{20} - 1$	$2^{15} - 1$

4.6 Transmit Pulse Shaper and Filter

If TCLK is not present, pulled "Low", or pulled "High" the transmitter outputs at TTIP/TRING will automatically send an all ones or an all zero signal to the line by programming the appropriate global register. By default, the transmitters will send all zeros. To send all ones, the TCLKCNL bit must be set "High".

4.6.1 T1 Short Haul Line Build Out (LBO)

The short haul transmitter output pulses are generated using a 7-Bit internal DAC (6-Bit plus the MSB sign bit). The line build out can be set to interface to five different ranges of cable attenuation by programming the appropriate channel register. The pulse shape is divided into eight discrete time segments which are set to fixed values to comply with the pulse template. To program the eight segments individually to optimize a special line build out, see the arbitrary pulse section of this datasheet. The short haul LBO settings are shown in Table 13.

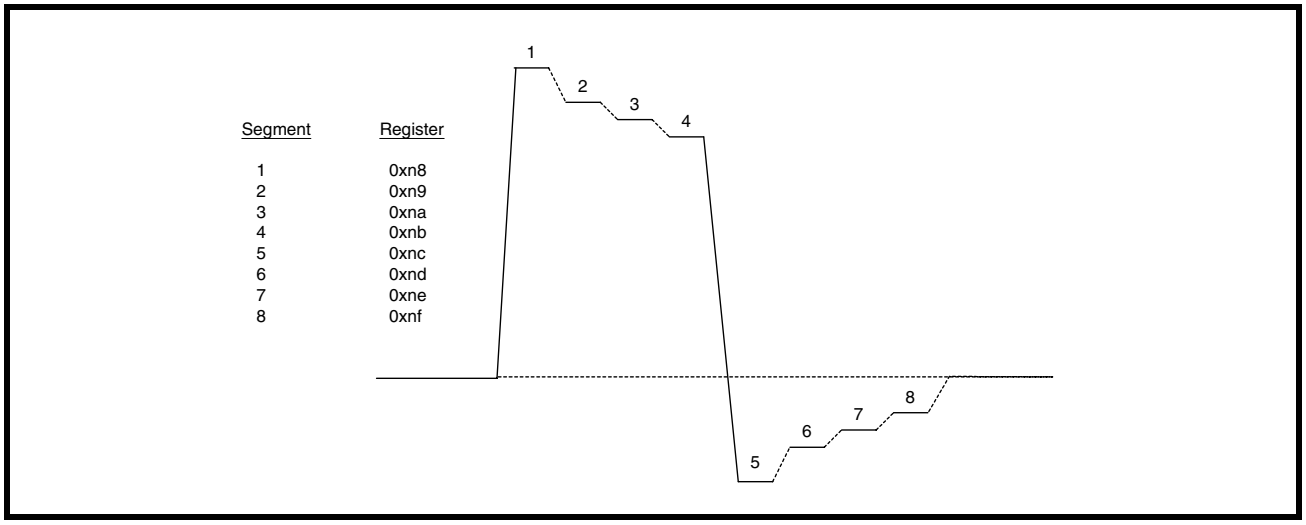
TABLE 13: SHORT HAUL LINE BUILD OUT

LBO SETTING EQC[4:0]	RANGE OF CABLE ATTENUATION
08h (01000)	0 - 133 Feet
09h (01001)	133 - 266 Feet
0Ah (01010)	266 - 399 Feet
0Bh (01011)	399 - 533 Feet
0Ch (01100)	533 - 655 Feet

4.6.2 Arbitrary Pulse Generator For T1 and E1

The arbitrary pulse generator divides the pulse into eight individual segments. Each segment is set by a 7-Bit binary word by programming the appropriate channel register. This allows the system designer to set the overshoot, amplitude, and undershoot for a unique line build out. The MSB (bit 7) is a sign-bit. If the sign-bit is set to "0", the segment will move in a positive direction relative to a flat line (zero) condition. If this sign-bit is set to "1", the segment will move in a negative direction relative to a flat line condition. The resolution of the DAC is typically 60mV per LSB. Thus, writing 7-bit = 1111111 will clamp the output at either voltage rail corresponding to a maximum amplitude. A pulse with numbered segments is shown in Figure 36.

FIGURE 36. ARBITRARY PULSE SEGMENT ASSIGNMENT



NOTE: *By default, the arbitrary segments are programmed to 0x00h. The transmitter outputs will result in an all zero pattern to the line interface.*

4.7 DMO (Digital Monitor Output)

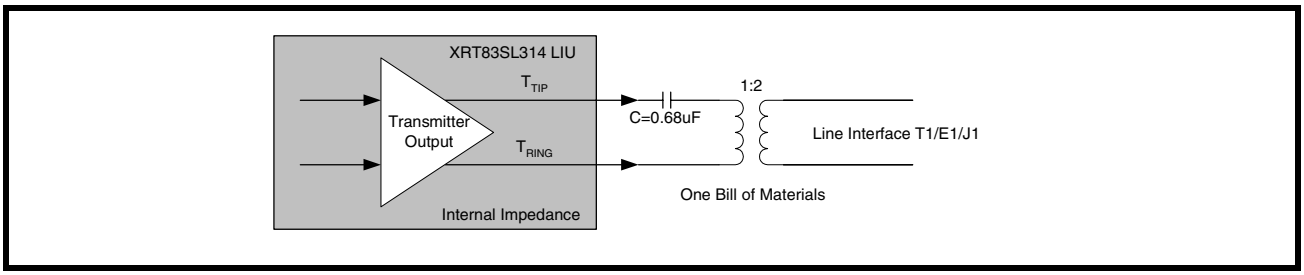
The driver monitor circuit is used to detect transmit driver failures by monitoring the activities at TTIP/TRING outputs. Driver failure may be caused by a short circuit in the primary transformer or system problems at the transmit inputs. If the transmitter of a channel has no output for more than 128 clock cycles, DMO goes "High" until a valid transmit pulse is detected. If the DMO interrupt is enabled, the change in status of DMO will cause

the interrupt pin to go "Low". Once the status register is read, the interrupt pin will return "High" and the status register will be reset (RUR).

4.8 Line Termination (TTIP/TRING)

The output stage of the transmit path generates standard return-to-zero (RZ) signals to the line interface for T1/E1/J1 twisted pair or E1 coaxial cable. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The transmitter outputs only require one DC blocking capacitor of 0.68μF. For redundancy applications (or simply to tri-state the transmitters), set TxTSEL to a "1" in the appropriate channel register. A typical transmit interface is shown in Figure 37.

FIGURE 37. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



5.0 MICROPROCESSOR INTERFACE BLOCK

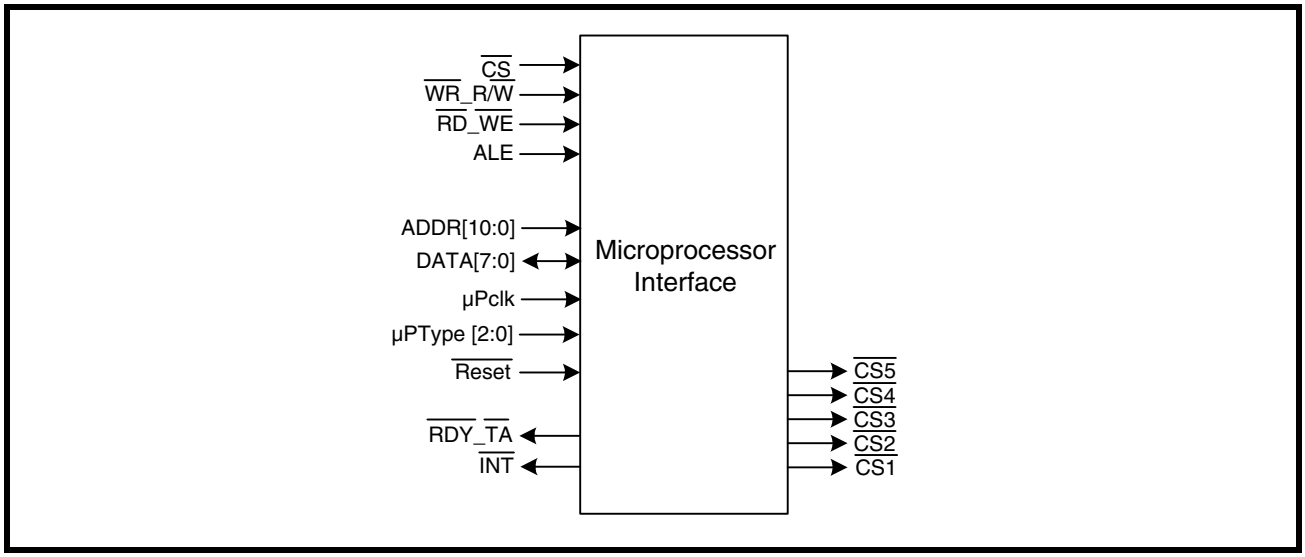
The Microprocessor Interface section supports communication between the local microprocessor (µP) and the LIU. The XRT83SL314 supports an Intel asynchronous interface, Motorola 68K asynchronous, and a Motorola Power PC interface. The microprocessor interface is selected by the state of the µPTS[2:0] input pins. Selecting the microprocessor interface is shown in Table 14.

TABLE 14: SELECTING THE MICROPROCESSOR INTERFACE MODE

µPTS[2:0]	MICROPROCESSOR MODE
0h (000)	Intel 68HC11, 8051, 80C188 (Asynchronous)
1h (001)	Motorola 68K (Asynchronous)
7h (111)	Motorola MPC8260, MPC860 Power PC (Synchronous)

The XRT83SL314 uses multipurpose pins to configure the device appropriately. The local µP configures the LIU by writing data into specific addressable, on-chip Read/Write registers. The microprocessor interface provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The microprocessor interface also supports polled and interrupt driven environments. A simplified block diagram of the microprocessor is shown in Figure 38.

FIGURE 38. SIMPLIFIED BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK



5.1 The Microprocessor Interface Block Signals

The LIU may be configured into different operating modes and have its performance monitored by software through a standard microprocessor using data, address and control signals. These interface signals are described below in Table 15, Table 16, and Table 17. The microprocessor interface can be configured to operate in Intel mode or Motorola mode. When the microprocessor interface is operating in Intel mode, some of the control signals function in a manner required by the Intel 80xx family of microprocessors. Likewise, when the microprocessor interface is operating in Motorola mode, then these control signals function in a manner as required by the Motorola Power PC family of microprocessors. (For using a Motorola 68K asynchronous processor, see Figure 41 and Table 20) Table 15 lists and describes those microprocessor interface signals whose role is constant across the two modes. Table 16 describes the role of some of these signals when the microprocessor interface is operating in the Intel mode. Likewise, Table 17 describes the role of these signals when the microprocessor interface is operating in the Motorola Power PC mode.

TABLE 15: XRT84L314 MICROPROCESSOR INTERFACE SIGNALS THAT EXHIBIT CONSTANT ROLES IN BOTH INTEL AND MOTOROLA MODES

PIN NAME	TYPE	DESCRIPTION
µPTS[2:0]	I	**Microprocessor Interface Mode Select Input pins** These three pins are used to specify the microprocessor interface mode. The relationship between the state of these three input pins, and the corresponding microprocessor mode is presented in Table 14.
DATA[7:0]	I/O	**Bi-Directional Data Bus for register "Read" or "Write" Operations.**
ADDR[10:8]	I	**Three-Bit Address Bus Inputs** The 3 MSBs of the address bits are used as a chip select decoder. The state of these 3 pins enable the Chip Selects for additional LIU devices. ***NOTE:*** *See the 84-Channel Application Section of this datasheet.*
ADDR[7:0]	I	**Eight-Bit Address Bus Inputs** The XRT83SL314 LIU microprocessor interface uses a direct address bus. This address bus is provided to permit the user to select an on-chip register for Read/Write access.
$\overline{CS}$	I	**Chip Select Input** This active low signal selects the microprocessor interface of the XRT83SL314 LIU and enables Read/Write operations with the on-chip register locations.

TABLE 16: INTEL MODE: MICROPROCESSOR INTERFACE SIGNALS

XRT83SL314 PIN NAME	INTEL EQUIVALENT PIN	TYPE	DESCRIPTION
ALE_TS	ALE	I	**Address-Latch Enable:** This active high signal is used to latch the contents on the address bus ADDR[7:0]. The contents of the address bus are latched into the ADDR[7:0] inputs on the falling edge of ALE.
$\overline{RD}$_$\overline{WE}$	$\overline{RD}$	I	**Read Signal:** This active low input functions as the read signal from the local µP. When this pin is pulled “Low” (if $\overline{CS}$ is “Low”) the LIU is informed that a read operation has been requested and begins the process of the read cycle.
$\overline{WR}$_R/$\overline{W}$	$\overline{WR}$	I	**Write Signal:** This active low input functions as the write signal from the local µP. When this pin is pulled “Low” (if $\overline{CS}$ is “Low”) the LIU is informed that a write operation has been requested and begins the process of the write cycle.
$\overline{RDY}$_$\overline{TA}$	$\overline{RDY}$	O	**Ready Output:** This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command.

TABLE 17: MOTOROLA MODE: MICROPROCESSOR INTERFACE SIGNALS

XRT83SL314 PIN NAME	MOTOROLA EQUIVALENT PIN	TYPE	DESCRIPTION
ALE_TS	TS	I	**Transfer Start:** This active high signal is used to latch the contents on the address bus ADDR[7:0]. The contents of the address bus are latched into the ADDR[7:0] inputs on the falling edge of TS.
$\overline{WR}$_R/$\overline{W}$	R/$\overline{W}$	I	**Read/Write:** This input pin from the local µP is used to inform the LIU whether a Read or Write operation has been requested. When this pin is pulled "High", $\overline{WE}$ will initiate a read operation. When this pin is pulled "Low", $\overline{WE}$ will initiate a write operation.
$\overline{RD}$_$\overline{WE}$	$\overline{WE}$	I	**Write Enable:** This active low input functions as the read or write signal from the local µP dependent on the state of R/$\overline{W}$. When $\overline{WE}$ is pulled "Low" (If $\overline{CS}$ is "Low") the LIU begins the read or write operation.
No Pin	$\overline{OE}$	I	**Output Enable:** This signal is not necessary for the XRT83SL314 to interface to the MPC8260 or MPC860 Power PCs.
µPCLK	CLKOUT	I	**Synchronous Processor Clock:** This signal is used as the timing reference for the Power PC synchronous mode.
$\overline{RDY}$_$\overline{TA}$	$\overline{TA}$	O	**Transfer Acknowledge:** This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command.

5.2 Intel Mode Programmed I/O Access (Asynchronous)

If the LIU is interfaced to an Intel type µP, then it should be configured to operate in the Intel mode. Intel type Read and Write operations are described below.

Intel Mode Read Cycle

Whenever an Intel-type µP wishes to read the contents of a register, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[10:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables further communication between the µP and the LIU microprocessor interface block.
3. Toggle the ALE input pin "High". This step enables the address bus input drivers, within the microprocessor interface block of the LIU.
4. The µP should then toggle the ALE pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
5. Next, the µP should indicate that this current bus cycle is a Read operation by toggling the $\overline{RD}$ input pin "Low". This action also enables the bi-directional data bus output drivers of the LIU.
6. After the µP toggles the Read signal "Low", the LIU will toggle the $\overline{RDY}$ output pin "Low". The LIU does this in order to inform the µP that the data is available to be read by the µP, and that it is ready for the next command.
7. After the µP detects the $\overline{RDY}$ signal and has read the data, it can terminate the Read Cycle by toggling the $\overline{RD}$ input pin "High".

NOTE: *$\overline{ALE}$ can be tied "High" if this signal is not available.*

The Intel Mode Write Cycle

Whenever an Intel type µP wishes to write a byte or word of data into a register within the LIU, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[10:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables further communication between the µP and the LIU microprocessor interface block.
3. Toggle the ALE input pin "High". This step enables the address bus input drivers, within the microprocessor interface block of the LIU.
4. The µP should then toggle the ALE pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
5. The µP should then place the byte or word that it intends to write into the target register, on the bi-directional data bus DATA[7:0].
6. Next, the µP should indicate that this current bus cycle is a Write operation by toggling the $\overline{WR}$ input pin "Low". This action also enables the bi-directional data bus input drivers of the LIU.
7. After the µP toggles the Write signal "Low", the LIU will toggle the $\overline{RDY}$ output pin "Low". The LIU does this in order to inform the µP that the data has been written into the internal register location, and that it is ready for the next command.

NOTE: *$\overline{ALE}$ can be tied "High" if this signal is not available.*

The Intel Read and Write timing diagram is shown in Figure 39. The timing specifications are shown in Table 18.

FIGURE 39. INTEL µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

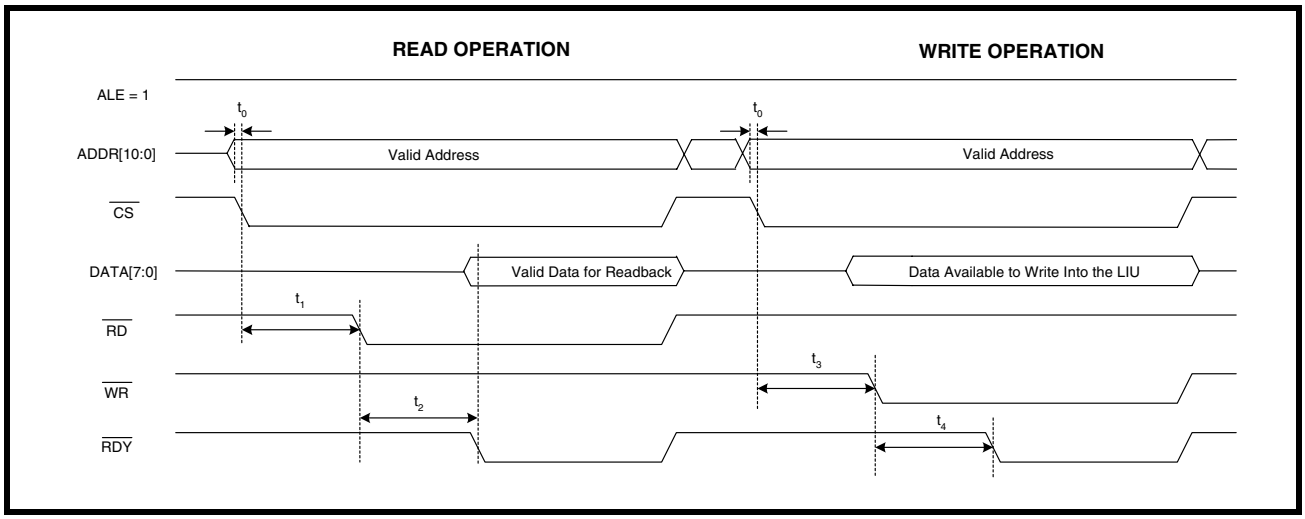


TABLE 18: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	30	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	150	ns
NA	$\overline{RD}$ Pulse Width (t_2)	150	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	30	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	150	ns
NA	$\overline{WR}$ Pulse Width (t_4)	150	-	ns

5.3 Motorola Mode Programmed I/O Access (Synchronous)

If the LIU is interfaced to a Motorola type µP, it should be configured to operate in the Motorola mode. Motorola type programmed I/O Read and Write operations are described below.

Motorola Mode Read Cycle

Whenever a Motorola type µP wishes to read the contents of a register, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[10:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables further communication between the µP and the LIU microprocessor interface block.
3. The µP should then toggle the TS pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
4. Next, the µP should indicate that this current bus cycle is a Read operation by pulling the R/$\overline{W}$ input pin "High".
5. Toggle the $\overline{WE}$ input pin "Low". This action enables the bi-directional data bus output drivers of the LIU.
6. After the µP toggles the $\overline{WE}$ signal "Low", the LIU will toggle the $\overline{TA}$ output pin "Low". The LIU does this in order to inform the µP that the data is available to be read by the µP, and that it is ready for the next command.
7. After the µP detects the $\overline{TA}$ signal and has read the data, it can terminate the Read Cycle by toggling the $\overline{WE}$ input pin "High".

Motorola Mode Write Cycle

Whenever a motorola type µP wishes to write a byte or word of data into a register within the LIU, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[10:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables further communication between the µP and the LIU microprocessor interface block.
3. The µP should then toggle the TS pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
4. Next, the µP should indicate that this current bus cycle is a Write operation by pulling the R/$\overline{W}$ input pin "Low".
5. Toggle the $\overline{WE}$ input pin "Low". This action enables the bi-directional data bus output drivers of the LIU.
6. After the µP toggles the $\overline{WE}$ signal "Low", the LIU will toggle the $\overline{TA}$ output pin "Low". The LIU does this in order to inform the µP that the data has been written into the internal register location, and that it is ready for the next command.
7. After the µP detects the $\overline{TA}$ signal and has read the data, it can terminate the Read Cycle by toggling the $\overline{WE}$ input pin "High".

The Motorola Read and Write timing diagram is shown in Figure 40. The timing specifications are shown in Table 19.

FIGURE 40. MOTOROLA POWER PC µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

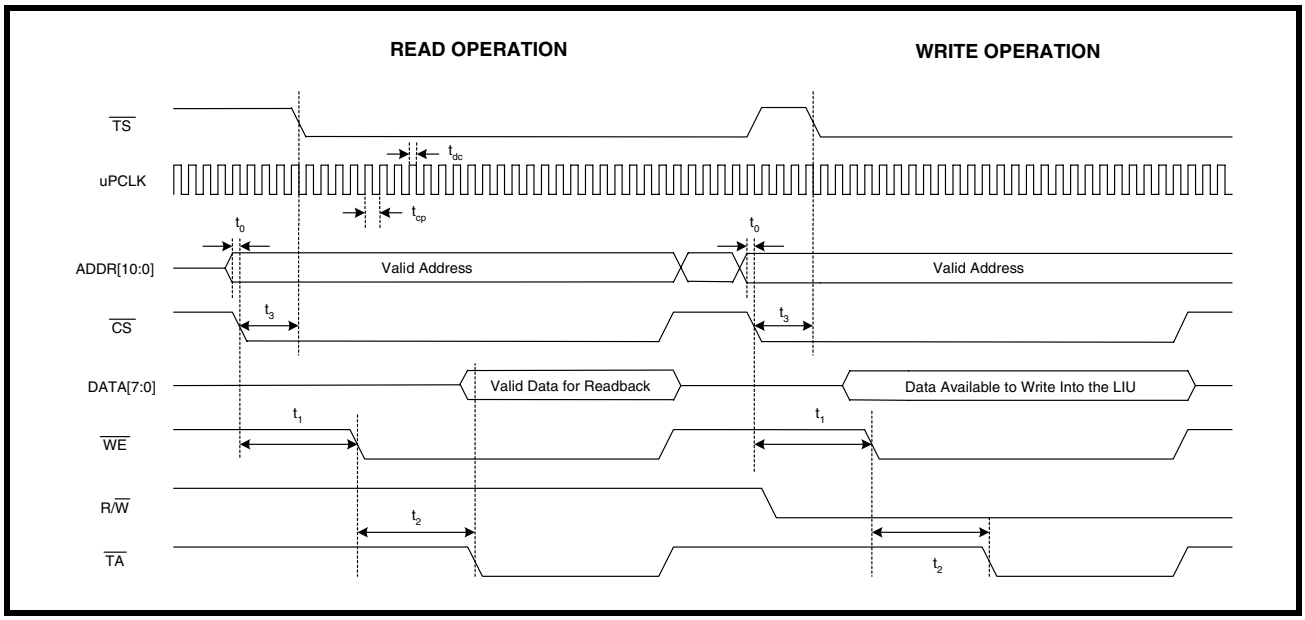


TABLE 19: MOTOROLA POWER PC MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{WE}$ Assert	0	-	ns
t_2	$\overline{WE}$ Assert to $\overline{TA}$ Assert	-	150	ns
NA	$\overline{WE}$ Pulse Width (t_2)	150	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{TS}$ Falling Edge	0	-	ns
t_{dc}	µPCLK Duty Cycle	40	60	%
t_{cp}	µPCLK Clock Period	20	-	ns

FIGURE 41. MOTOROLA 68K µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

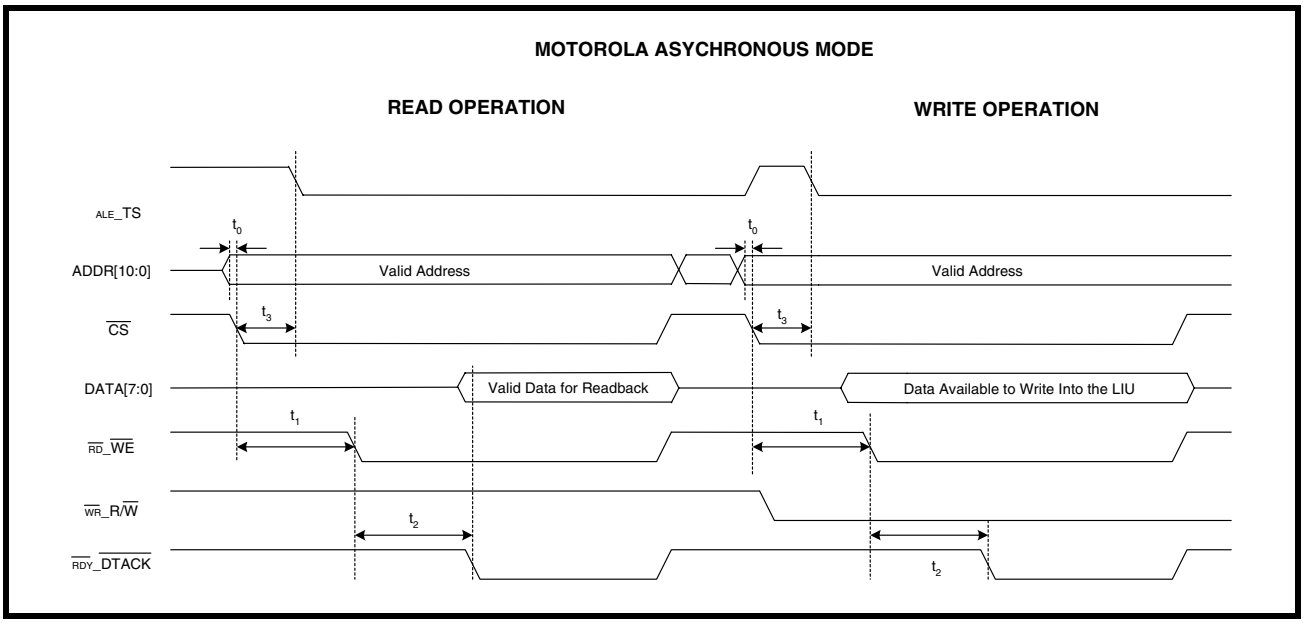


TABLE 20: MOTOROLA 68K MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{DS}$ (Pin $\overline{RD}_\overline{WE}$) Assert	30	-	ns
t_2	$\overline{DS}$ Assert to $\overline{DTACK}$ Assert	-	150	ns
NA	$\overline{DS}$ Pulse Width (t_2)	150	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{AS}$ (Pin ALE_TS) Falling Edge	0	-	ns

TABLE 21: MICROPROCESSOR REGISTER ADDRESS (ADDR[7:0])

REGISTER NUMBER	ADDRESS (HEX)	FUNCTION
0 - 15	0x00 - 0x0F	Channel 0 Control Registers
16 - 31	0x10 - 0x1F	Channel 1 Control Registers
32 - 47	0x20 - 0x2F	Channel 2 Control Registers
48 - 63	0x30 - 0x3F	Channel 3 Control Registers
64 - 79	0x40 - 0x4F	Channel 4 Control Registers
80 - 95	0x50 - 0x5F	Channel 5 Control Registers
96 - 111	0x60 - 0x6F	Channel 6 Control Registers
112 - 127	0x70 - 0x7F	Channel 7 Control Registers
128 - 143	0x80 - 0x8F	Channel 8 Control Registers
144 - 159	0x90 - 0x9F	Channel 9 Control Registers
160 - 175	0xA0 - 0xAF	Channel 10 Control Registers
176 - 191	0xB0 - 0xBF	Channel 11 Control Registers
192 - 207	0xC0 - 0xCF	Channel 12 Control Registers
208 - 223	0xD0 - 0xDF	Channel 13 Control Registers
224 - 227	0xE0 - 0xEB	Global Control Registers Applied to All 14 Channels
228 - 243	0xEC - 0xF3	R/W Registers Reserved for Testing
244	0xF4	E1 Arbitrary Select
245 - 253	0xF5 - 0xFD	R/W Registers Reserved for Testing
254	0xFE	Device "ID"
255	0xFF	Device "Revision ID"

TABLE 22: MICROPROCESSOR REGISTER CHANNEL DESCRIPTION

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
Channel 0 Control Registers (0x00 - 0x0F)										
0	0x00	R/W	QRSS/PRBS	Reserved	RxON	EQC4	EQC3	EQC2	EQC1	EQC0
1	0x01	R/W	RxTSEL	TxTSEL	TERSEL1	TERSEL0	RxJASEL	TxJASEL	JABW	FIFOS
2	0x02	R/W	INVQRSS	TxTEST2	TxTEST1	TxTEST0	TxON	LOOP2	LOOP1	LOOP0
3	0x03	R/W	NLCDE1	NLCDE0	CODES	RxRES1	RxRES0	INSBPV	INSBER	Reserved
4	0x04	R/W	EQFLAGE	DMOIE	FLSIE	LCVI/OFE	NLCDIE	AISDIE	RLOSIE	QRPDIE
5	0x05	RO	EQFLAG	DMO	FLS	LCV/OF	NLCD	AIS	RLOS	QRPD
6	0x06	RUR	EQFLAGS	DMOIS	FLSIS	LCV/OFIS	NLCDIS	AISIS	RLOSIS	QRPDIS

TABLE 22: MICROPROCESSOR REGISTER CHANNEL DESCRIPTION

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
7	0x07	RO	Reserved	FLSDET	CLOS5	CLOS4	CLOS3	CLOS2	CLOS1	CLOS0
8	0x08	R/W	Reserved	1SEG6	1SEG5	1SEG4	1SEG3	1SEG2	1SEG1	1SEG0
9	0x09	R/W	Reserved	2SEG6	2SEG5	2SEG4	2SEG3	2SEG2	2SEG1	2SEG0
10	0x0A	R/W	Reserved	3SEG6	3SEG5	3SEG4	3SEG3	3SEG2	3SEG1	3SEG0
11	0x0B	R/W	Reserved	4SEG6	4SEG5	4SEG4	4SEG3	4SEG2	4SEG1	4SEG0
12	0x0C	R/W	Reserved	5SEG6	5SEG5	5SEG4	5SEG3	5SEG2	5SEG1	5SEG0
13	0x0D	R/W	Reserved	6SEG6	6SEG5	6SEG4	6SEG3	6SEG2	6SEG1	6SEG0
14	0x0E	R/W	Reserved	7SEG6	7SEG5	7SEG4	7SEG3	7SEG2	7SEG1	7SEG0
15	0x0F	R/W	Reserved	8SEG6	8SEG5	8SEG4	8SEG3	8SEG2	8SEG1	8SEG0
Channel (1 - 13) Control Registers (0xN0 - 0xNF) See Channel 0										

TABLE 23: MICROPROCESSOR REGISTER GLOBAL DESCRIPTION

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
Global Control Registers for All 14 Channels										
224	0xE0	R/W	SR/DR	ATAOS	RCLKE	TCLKE	DATAP	Reserved	GIE	SRESET
225	0xE1	R/W	Reserved	Reserved	GAUGE1	GAUGE0	Reserved	RxMUTE	EXLOS	ICT
226	0xE2	R/W	Reserved	RxTCNTL	EQFLAG5	EQFLAG4	EQFLAG3	EQFLAG2	EQFLAG1	EQFLAG0
227	0xE3	R/W	Reserved	Reserved	Reserved	Reserved	SL1	SL0	EQG1	EQG0
228	0xE4	R/W	MCLKT1out1	MCLKT1out0	MCLKE1out1	MCLKE1out0	Reserved	Reserved	Reserved	Reserved
229	0xE5	R/W	LCV/OFLW	CNTRDEN	Reserved	Reserved	LCVCH3	LCVCH2	LCVCH1	LCVCH0
230	0xE6	R/W	Reserved	Reserved	Reserved	allRST	allUPDATE	BYTEsel	chUPDATE	chRST
231	0xE7	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
232	0xE8	RO	LCVCNT7	LCVCNT6	LCVCNT5	LCVCNT4	LCVCNT3	LCVCNT2	LCVCNT1	LCVCNT0
233	0xE9	R/W	Reserved	Reserved	ALLT1E1	TCLKCNL	CLKSEL3	CLKSEL2	CLKSEL1	CLKSEL0
234	0xEA	RUR	GCHIS7	GCHIS6	GCHIS5	GCHIS4	GCHIS3	GCHIS2	GCHIS1	GCHIS0
235	0xEB	RUR	Reserved	Reserved	GCHIS13	GCHIS12	GCHIS11	GCHIS10	GCHIS9	GCHIS8
244	0xF4	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	E1arben
R/W Registers Reserved for Testing (0xEC - 0xFD), Excluding 0xF4h										
254	0xFE	RO	**Device "ID"**							
255	0xFF	RO	**Device "Revision ID"**							

TABLE 24: MICROPROCESSOR REGISTER 0X00H BIT DESCRIPTION

CHANNEL 0-13 (0X00H-0XD0H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	QRSS/ PRBS	**QRSS/PRBS Select Bits** These bits are used to select between QRSS and PRBS. 0 = QRSS 1 = PRBS	R/W	0
D6	Reserved	This Register Bit is Not Used.		
D5	RxON	**Receiver ON/OFF** Upon power up, the receiver is powered OFF. RxON is used to turn the receiver ON or OFF if the hardware pin RxON is pulled "High". If the hardware pin is pulled "Low", all receivers are turned off. 0 = Receiver is Powered Off 1 = Receiver is Powered On	R/W	0
D4 D3 D2 D1 D0	EQC4 EQC3 EQC2 EQC1 EQC0	**Equalizer Control Bits** The equalizer control bits are shown in Table 25 below.	R/W	0 0 0 0 0

TABLE 25: EQUALIZER CONTROL AND TRANSMIT LINE BUILD OUT

EQC[4:0]	T1/E1 MODE/RECEIVE SENSITIVITY	TRANSMIT LBO	CABLE	CODING
0x08h	T1 Short Haul/15dB	0 to 133 feet (0.6dB)	100Ω TP	B8ZS
0x09h	T1 Short Haul/15dB	133 to 266 feet (1.2dB)	100Ω TP	B8ZS
0x0Ah	T1 Short Haul/15dB	266 to 399 feet (1.8dB)	100Ω TP	B8ZS
0x0Bh	T1 Short Haul/15dB	399 to 533 feet (2.4dB)	100Ω TP	B8ZS
0x0Ch	T1 Short Haul/15dB	533 to 655 feet (3.0dB)	100Ω TP	B8ZS
0x0Dh	T1 Short Haul/15dB	Arbitrary Pulse	100Ω TP	B8ZS
0x0Eh	T1 Gain Mode/29dB	0 to 133 feet (0.6dB)	100Ω TP	B8ZS
0x0Fh	T1 Gain Mode/29dB	133 to 266 feet (1.2dB)	100Ω TP	B8ZS
0x10h	T1 Gain Mode/29dB	266 to 399 feet (1.8dB)	100Ω TP	B8ZS
0x11h	T1 Gain Mode/29dB	399 to 533 feet (2.4dB)	100Ω TP	B8ZS
0x12h	T1 Gain Mode/29dB	533 to 655 feet (3.0dB)	100Ω TP	B8ZS
0x13h	T1 Gain Mode/29dB	Arbitrary Pulse	100Ω TP	B8ZS
0x1Ch	E1 Short Haul/15dB	ITU G.703	75Ω Coax	HDB3

TABLE 25: EQUALIZER CONTROL AND TRANSMIT LINE BUILD OUT

EQC[4:0]	T1/E1 MODE/RECEIVE SENSITIVITY	TRANSMIT LBO	CABLE	CODING
0x1Dh	E1 Short Haul/15dB	ITU G.703	120Ω TP	HDB3
0x1Eh	E1 Gain Mode/29dB	ITU G.703	75Ω Coax	HDB3
0x1Fh	E1 Gain Mode/29dB	ITU G.703	120Ω TP	HDB3

TABLE 26: MICROPROCESSOR REGISTER 0X01H BIT DESCRIPTION

CHANNEL 0-13 (0X01H-0XD1H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	RxTSEL	**Receive Termination Select** Upon power up, the receiver is in "High" impedance. RxTSEL is used to switch between the internal termination and "High" impedance. 0 = "High" Impedance 1 = Internal Termination	R/W	0
D6	TxTSEL	**Transmit Termination Select** Upon power up, the transmitter is in "High" impedance. TxTSEL is used to switch between the internal termination and "High" impedance. 0 = "High" Impedance 1 = Internal Termination	R/W	0
D5 D4	TERSEL1 TERSEL0	**Receive Line Impedance Select** TERSEL[1:0] are used to select the line impedance for T1/J1/E1. 00 = 100Ω 01 = 110Ω 10 = 75Ω 11 = 120Ω	R/W	0 0
D3	RxJASEL	**Receive Jitter Attenuator Select** RxJASEL is used to enable the receiver jitter attenuator. By default, RxJASEL is disabled. 0 = Disabled 1 = Enabled	R/W	0
D2	TxJASEL	**Transmit Jitter Attenuator Select** TxJASEL is used to enable the transmitter jitter attenuator. By default, TxJASEL is disabled. 0 = Disabled 1 = Enabled	R/W	0

TABLE 26: MICROPROCESSOR REGISTER 0X01H BIT DESCRIPTION

CHANNEL 0-13 (0X01H-0XD1H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D1	JABW	**Jitter Bandwidth (E1 Mode Only, T1 is permanently set to 3Hz)** The jitter bandwidth is a global setting that is applied to both the receiver and transmitter jitter attenuator. 0 = 10Hz 1 = 1.5Hz	R/W	0
D0	FIFOS	**FIFO Depth Select** The FIFO depth select is used to configure the part for a 32-bit or 64-bit FIFO (within the jitter attenuator blocks). The delay of the FIFO is equal to ½ the FIFO depth. This is a global setting that is applied to both the receiver and transmitter FIFO. 0 = 32-Bit 1 = 64-Bit	R/W	0

TABLE 27: MICROPROCESSOR REGISTER 0X02H BIT DESCRIPTION

CHANNEL 0-13 (0X02H-0XD2H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	INVQRSS	**QRSS inversion** INVQRSS is used to invert the transmit QRSS pattern set by the TxTEST[2:0] bits. By default, INVQRSS is disabled and the QRSS will be transmitted with normal polarity. 0 = Disabled 1 = Enabled	R/W	0
D6 D5 D4	TxTEST2 TxTEST1 TxTEST0	**Test Code Pattern** TxTEST[2:0] are used to select a diagnostic test pattern to the line (transmit outputs). 0XX = No Pattern 100 = Tx QRSS 101 = Tx TAOS 110 = Tx TLUC 111 = Tx TLDC	R/W	0 0 0

TABLE 27: MICROPROCESSOR REGISTER 0X02H BIT DESCRIPTION

CHANNEL 0-13 (0X02H-0XD2H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D3	TxOn	**Transmit ON/OFF** Upon power up, the transmitters are powered off. This bit is used to turn the transmitter for this channel On or Off if the TxON pin is pulled "High". If the TxON pin is pulled "Low", all 14 transmitters are powered off. 0 = Transmitter is Powered OFF 1 = Transmitter is Powered ON	R/W	0
D2 D1 D0	LOOP2 LOOP1 LOOP0	**Loopback Diagnostic Select** LOOP[2:0] are used to select the loopback mode. 0XX = No Loopback 100 = Dual Loopback 101 = Analog Loopback 110 = Remote Loopback 111 = Digital Loopback	R/W	0 0 0

TABLE 28: MICROPROCESSOR REGISTER 0X03H BIT DESCRIPTION

CHANNEL 0-13 (0X03H-0XD3H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7 D6	NLCDE1 NLCDE0	**Network Loop Code Detection Enable** NLCDE[1:0] are used to select the loop code detection. 00 = Disabled 01 = Detect Loop Up Code 10 = Detect Loop Down Code 11 = Automatic Loop Code Detection	R/W	0 0
D5	CODES	**Encoding/Decoding Select (Single Rail Mode Only)** 0 = HDB3 (E1), B8ZS (T1) 1 = AMI Coding	R/W	0
D4 D3	RxRES1 RxRES0	**Receive External Fixed Resistor** RxRES[1:0] are used to select the value for a high precision external resistor to improve return loss. 00 = None 01 = 240Ω 10 = 210Ω 11 = 150Ω	R/W	0 0

TABLE 28: MICROPROCESSOR REGISTER 0X03H BIT DESCRIPTION

CHANNEL 0-13 (0X03H-0XD3H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D2	INSBPV	**Insert Bipolar Violation** When this bit transitions from a "0" to a "1", a bipolar violation will be inserted in the transmitted QRSS/PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a "0" to this bit before writing a "1".	R/W	0
D1	INSBER	**Insert Bit Error** When this bit transitions from a "0" to a "1", a bit error will be inserted in the transmitted QRSS/PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a "0" to this bit before writing a "1".	R/W	0
D0	Reserved	This Register Bit is Not Used.		

TABLE 29: MICROPROCESSOR REGISTER 0X04H BIT DESCRIPTION

CHANNEL 0-13 (0X04H-0XD4H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	EQFLAGE	**Equalizer Attenuation Flag Enable** 0 = Masks the EQFLAG function 1 = Enables Interrupt Generation	R/W	0
D6	DMOIE	**Digital Monitor Output Interrupt Enable** 0 = Masks the DMO function 1 = Enables Interrupt Generation	R/W	0
D5	FLSIE	**FIFO Limit Status Interrupt Enable** 0 = Masks the FLS function 1 = Enables Interrupt Generation	R/W	0
D4	LCV/OFIE	**Line Code Violation / Counter Overflow Interrupt Enable** 0 = Masks the LCV/OF function 1 = Enables Interrupt Generation	R/W	0
D3	NLCDIE	**Network Loop Code Detection Interrupt Enable** 0 = Masks the NLCD function 1 = Enables Interrupt Generation	R/W	0
D2	AISIE	**Alarm Indication Signal Interrupt Enable** 0 = Masks the AIS function 1 = Enables Interrupt Generation	R/W	0

TABLE 29: MICROPROCESSOR REGISTER 0X04H BIT DESCRIPTION

CHANNEL 0-13 (0X04H-0XD4H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D1	RLOSIE	**Receiver Loss of Signal Interrupt Enable** 0 = Masks the RLOS function 1 = Enables Interrupt Generation	R/W	0
D0	QRPDIE	**Quasi Random Signal Source Interrupt Enable** 0 = Masks the QRPD function 1 = Enables Interrupt Generation	R/W	0

NOTE: *The GIE bit in the global register 0xE0h must be set to "1" in addition to the individual register bits to enable the interrupt pin.*

TABLE 30: MICROPROCESSOR REGISTER 0X05H BIT DESCRIPTION

CHANNEL 0-13 (0X05H-0XD5H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	EQFLAG	**Equalizer Attenuation Flag** The equalizer attenuation flag is always active regardless if the interrupt generation is disabled. This bit indicates the EQFLAG activity. An interrupt will not occur unless the EQFLAGE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. 0 = No Alarm 1 = Equalizer Attenuation Flag is Set	RO	0
D6	DMO	**Digital Monitor Output** The digital monitor output is always active regardless if the interrupt generation is disabled. This bit indicates the DMO activity. An interrupt will not occur unless the DMOIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. 0 = No Alarm 1 = Transmit output driver has failures	RO	0
D5	FLS	**FIFO Limit Status** The FIFO limit status is always active regardless if the interrupt generation is disabled. This bit indicates whether the RD/WR pointers are within 3-Bits. An interrupt will not occur unless the FLSIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. 0 = No Alarm 1 = RD/WR FIFO pointers are within ±3-Bits	RO	0

NOTE: The GIE bit in the global register 0xE0h must be set to "1" in addition to the individual register bits to enable the interrupt pin.

TABLE 30: MICROPROCESSOR REGISTER 0X05H BIT DESCRIPTION

CHANNEL 0-13 (0X05H-0XD5H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D4	LCV/OF	**Line Code Violation / Counter Overflow** This bit serves a dual purpose. By default, this bit monitors the line code violation activity. However, if bit 7 in register 0xE5h is set to a "1", this bit monitors the overflow status of the internal LCV counter. An interrupt will not occur unless the LCV/OFIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. 0 = No Alarm 1 = A line code violation, bipolar violation, or excessive zeros has occurred	RO	0
D3	NLCD	**Network Loop Code Detection** The network loop code detection is always active regardless if the interrupt generation is disabled. This bit indicates the NLCD activity. An interrupt will not occur unless the NLCDIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. 0 = No Alarm 1 = Network loop code detected according to the mode selected in channel register 0x03h	RO	0
D2	AISD	**Alarm Indication Signal** The alarm indication signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the AIS activity. An interrupt will not occur unless the AISIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. 0 = No Alarm 1 = An all ones signal is detected	RO	0
D1	RLOS	**Receiver Loss of Signal** The receiver loss of signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the RLOS activity. An interrupt will not occur unless the RLOSIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. 0 = No Alarm 1 = An RLOS condition is present	RO	0
D0	QRPD	**Quasi Random Pattern Detection** The quasi random pattern detection is always active regardless if the interrupt generation is disabled. This bit indicates that a QRPD has been detected. An interrupt will not occur unless the QRPDIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. 0 = No Alarm 1 = A QRP is detected	RO	0

TABLE 31: MICROPROCESSOR REGISTER 0X06H BIT DESCRIPTION

CHANNEL 0-13 (0X06H-0XD6H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	EQFLAGS	**Equalizer Attenuation Flag Status** 0 = No change 1 = Change in status occurred	RUR	0
D6	DMOIS	**Digital Monitor Output Status** 0 = No change 1 = Change in status occurred	RUR	0
D5	FLSIS	**FIFO Limit Status** 0 = No change 1 = Change in status occurred	RUR	0
D4	LCV/OFIS	**Line Code Violation / Overflow Status** 0 = No change 1 = Change in status occurred	RUR	0
D3	NLCDIS	**Network Loop Code Detection Status** 0 = No change 1 = Change in status occurred	RUR	0
D2	AISDIS	**Alarm Indication Signal Status** 0 = No change 1 = Change in status occurred	RUR	0
D1	RLOSIS	**Receiver Loss of Signal Status** 0 = No change 1 = Change in status occurred	RUR	0
D0	QRPDIS	**Quasi Random Pattern Detection Status** 0 = No change 1 = Change in status occurred	RUR	0

NOTE: *Any change in status will generate an interrupt (if enabled in channel register 0x04h and GIE is set to "1" in the global register 0xE0h). The status registers are reset upon read (RUR).*

TABLE 32: MICROPROCESSOR REGISTER 0X07H BIT DESCRIPTION

CHANNEL 0-13 (0X07H-0XD7H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used.		
D6	FLSDET	**FIFO LIMIT STATUS DETECT** The FLSDET is used to determine whether the receiver or transmitter FIFO has reached its limit status. If both FIFOs reach their limit capacity, this bit will be set to "1". 0 = Receive JA 1 = Transmit JA	RO	0
D5 D4 D3 D2 D1 D0	CLOS5 CLOS4 CLOS3 CLOS2 CLOS1 CLOS0	**Cable Loss Indication** This 6-Bit binary word indicates the cable attenuation on the receiver inputs RTIP/RRING within ±1dB with Bit 5 being the MSB.	RO	0

TABLE 33: MICROPROCESSOR REGISTER 0X08H BIT DESCRIPTION

CHANNEL 0-13 (0X08H-0XD8H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D6 D5 D4 D3 D2 D1 D0	1SEG6 1SEG5 1SEG4 1SEG3 1SEG2 1SEG1 1SEG0	**Arbitrary Pulse Generation** The transmit output pulse is divided into 8 individual segments. This register is used to program the first segment which corresponds to the overshoot of the pulse amplitude. There are four segments for the top portion of the pulse and four segments for the bottom portion of the pulse. Segment number 5 corresponds to the undershoot of the pulse. The MSB of each segment is the sign bit. Bit 6 = 0 = Negative Direction Bit 6 = 1 = Positive Direction	R/W	0 0 0 0 0 0 0

TABLE 34: MICROPROCESSOR REGISTER 0X09H BIT DESCRIPTION

CHANNEL 0-13 (0X09H-0XD9H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	2SEG[6:0]	**Segment Number Two, Same Description as Register 0x08h**	R/W	

TABLE 35: MICROPROCESSOR REGISTER 0X0AH BIT DESCRIPTION

CHANNEL 0-13 (0X0AH-0XDAH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	3SEG[6:0]	**Segment Number Three, Same Description as Register 0x08h**	R/W	

TABLE 36: MICROPROCESSOR REGISTER 0X0BH BIT DESCRIPTION

CHANNEL 0-13 (0X0BH-0XDBH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	4SEG[6:0]	**Segment Number Four, Same Description as Register 0x08h**	R/W	

TABLE 37: MICROPROCESSOR REGISTER 0X0CH BIT DESCRIPTION

CHANNEL 0-13 (0X0CH-0XDCH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	5SEG[6:0]	**Segment Number Five, Same Description as Register 0x08h**	R/W	

TABLE 38: MICROPROCESSOR REGISTER 0X0DH BIT DESCRIPTION

CHANNEL 0-13 (0X0DH-0XDDH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	6SEG[6:0]	**Segment Number Six, Same Description as Register 0x08h**	R/W	

TABLE 39: MICROPROCESSOR REGISTER 0X0EH BIT DESCRIPTION

CHANNEL 0-13 (0X0EH-0XDEH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	7SEG[6:0]	**Segment Number Seven, Same Description as Register 0x08h**	R/W	

TABLE 40: MICROPROCESSOR REGISTER 0X0FH BIT DESCRIPTION

CHANNEL 0-13 (0X0FH-0XDFH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	8SEG[6:0]	**Segment Number Eight, Same Description as Register 0x08h**	R/W	

TABLE 41: MICROPROCESSOR REGISTER 0XE0H BIT DESCRIPTION

GLOBAL REGISTER (0XE0H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	SR/DR	**Single Rail/Dual Rail Mode** This bit sets the LIU to receive and transmit digital data in a single rail or a dual rail format. 0 = Dual Rail Mode 1 = Single Rail Mode	R/W	0
D6	ATAOS	**Automatic Transmit All Ones** If ATAOS is selected, an all ones pattern will be transmitted on any channel that experiences an RLOS condition. If an RLOS condition does not occur, TAOS will remain inactive. 0 = Disabled 1 = Enabled	R/W	0
D5	RCLKE	**Receive Clock Data** 0 = RPOS/RNEG data is updated on the rising edge of RCLK 1 = RPOS/RNEG data is updated on the falling edge of RCLK	R/W	0
D4	TCLKE	**Transmit Clock Data** 0 = TPOS/TNEG data is sampled on the falling edge of TCLK 1 = TPOS/TNEG data is sampled on the rising edge of TCLK	R/W	0
D3	DATAP	**Data Polarity** 0 = Transmit input and receive output data is active "High" 1 = Transmit input and receive output data is active "Low"	R/W	0
D2	Reserved	This Register Bit is Not Used	R/W	0
D1	GIE	**Global Interrupt Enable** The global interrupt enable is used to enable/disable all interrupt activity for all 14 channels. This bit must be set "High" for the interrupt pin to operate. 0 = Disable all interrupt generation 1 = Enable interrupt generation to the individual channel registers	R/W	0
D0	SRESET	**Software Reset** Writing a "1" to this bit for more than 10µS initiates a device reset for all internal circuits except the microprocessor register bits. To reset the registers to their default setting, use the Hardware Reset pin (See the pin description for more details).	R/W	0

TABLE 42: MICROPROCESSOR REGISTER 0XE1H BIT DESCRIPTION

GLOBAL REGISTER (0XE1H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	R/W	0
D6	Reserved	This Register Bit is Not Used	R/W	0
D5 D4	GAUGE1 GAUGE0	**Wire Gauge Select** 00 = 22 and 24 gauge 01 = 22 gauge 10 = 24 gauge 11 = 26 gauge	R/W	0 0
D3	Reserved	This Register Bit is Not Used	R/W	0
D2	RxMUTE	**Receiver Output Mute Enable** If RxMUTE is selected, RPOS/RNEG will be pulled "Low" for any channel that experiences an RLOS condition. If an RLOS condition does not occur, RxMUTE will remain inactive. 0 = Disabled 1 = Enabled	R/W	0
D1	EXLOS	**Extended Loss of Zeros** The number of zeros required to declare a Digital Loss of Signal is extended to 4,096. 0 = Normal Operation 1 = Enables the EXLOS function	R/W	0
D0	ICT	**In Circuit Testing** 0 = Normal Operation 1 = Sets all output pins to "High" impedance for in circuit testing	R/W	0

TABLE 43: MICROPROCESSOR REGISTER 0XE2H BIT DESCRIPTION

GLOBAL REGISTER (0XE2H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	R/W	0

GLOBAL REGISTER (0XE2H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D6	RxTCNTL	**Receive Termination Select Control** This bit sets the LIU to control the RxTSEL function with either the individual channel register bit or the global hardware pin. 0 = Control of the receive termination is set to the register bits 1 = Control of the receive termination is set to the hardware pin	R/W	0
D5 D4 D3 D2 D1 D0	EQFLAG5 EQFLAG4 EQFLAG3 EQFLAG2 EQFLAG1 EQFLAG0	**Equalizer Attenuation Flag** EQFLAG[5:0] is used to generate an interrupt condition for an RLOS other than the default setting described in the datasheet. A desired value can be programmed into this register. If EQFLAGE is enabled in register 0x04h and if this 6-Bit binary word is equal to the 6-Bit cable loss indicator, an interrupt will be generated.	R/W	0 0 0 0 0 0

TABLE 44: MICROPROCESSOR REGISTER 0XE3H BIT DESCRIPTION

GLOBAL REGISTER (0XE3H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	R/W	0
D6	Reserved	This Register Bit is Not Used	R/W	0
D5	Reserved	This Register Bit is Not Used	R/W	0
D4	Reserved	This Register Bit is Not Used	R/W	0
D3 D2	SL1 SL0	**Slicer Level Select** 00 = 50% 01 = 45% 10 = 55% 11 = 68%	R/W	0 0
D1 D0	EQG1 EQG0	**Equalizer Gain Control** 00 = Normal 01 = Reduce Gain by 1dB 10 = Reduce Gain by 3dB 11 = Normal	R/W	0

TABLE 45: MICROPROCESSOR REGISTER 0XE4H BIT DESCRIPTION

GLOBAL REGISTER (0XE4H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7 D6	MclkT1out1 MclkT1out0	**MCLKT1OUT Select** MclkT1out[1:0] is used to program the MCLKT1out pin. By default, the output clock is 1.544MHz. 00 = 1.544MHz 01 = 3.088MHz 10 = 6.176MHz 11 = 12.352MHz	R/W	0 0
D5 D4	MclkE1out1 MclkE1out0	**MCLKE1OUT Select** MclkE1out[1:0] is used to program the MCLKE1out pin. By default, the output clock is 2.048MHz. 00 = 2.048MHz 01 = 4.096MHz 10 = 8.192MHz 11 = 16.384MHz	R/W	0 0
D3	Reserved	This Register Bit is Not Used	R/W	0
D2	Reserved	This Register Bit is Not Used	R/W	0
D1	Reserved	This Register Bit is Not Used	R/W	0
D0	Reserved	This Register Bit is Not Used	R/W	0

TABLE 46: MICROPROCESSOR REGISTER 0XE5H BIT DESCRIPTION

GLOBAL REGISTER (0XE5H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	LCV/OFLW	**Line Code Violation / Counter Overflow Monitor Select** This bit is used to select the monitoring activity between the LCV and the counter overflow status. When the 16-bit LCV counter saturates, the counter overflow condition is activated. By default, the LCV activity is monitored by bit D4 in register 0x05h. 0 = Monitoring LCV 1 = Monitoring the counter overflow status	R/W	0
D6	CNTRDEN	**Line Code Violation Counter Read Enable** This bit enables the 16-bit LCV counter contents to be read from bits D[7:0] in register 0xE8h. If a counter reaches full scale, it saturates and remains at FFFFh until a reset is initiated in register 0xE6h. By default, the LCV counter readback function is disabled. 0 = Disabled 1 = Enables the 16-bit LCV Counters for Readback	R/W	0
D5	Reserved	This Register Bit is Not Used	R/W	0

GLOBAL REGISTER (0XE5H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D4	Reserved	This Register Bit is Not Used	R/W	0
D3 D2 D1 D0	LCVCH3 LCVCH2 LCVCH1 LCVCH0	**Line Code Violation Counter Select** These bits are used to select which channel is to be addressed for reading the contents in register 0xE8h. It is also used to address the counter for a given channel when performing an update or reset on a per channel basis. By default, Channel 0 is selected. 0000 = None 0001 = Channel 0 0010 = Channel 1 0011 = Channel 2 0100 = Channel 3 0101 = Channel 4 0110 = Channel 5 0111 = Channel 6 1000 = Channel 7 1001 = Channel 8 1010 = Channel 9 1011 = Channel 10 1100 = Channel 11 1101 = Channel 12 1110 = Channel 13	R/W	0 0 0 0

TABLE 47: MICROPROCESSOR REGISTER 0XE6H BIT DESCRIPTION

GLOBAL REGISTER (0XE6H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	R/W	0
D6	Reserved	This Register Bit is Not Used	R/W	0
D5	Reserved	This Register Bit is Not Used	R/W	0
D4	allRST	**LCV Counter Reset for All Channels** This bit is used to reset all internal LCV counters to their default state 0000h. This bit must be set to "1" for 1μS. 0 = Normal Operation 1 = Resets all Counters	R/W	0
D3	allUPDATE	**LCV Counter Update for All Channels** This bit is used to latch the contents of all 14 counters into holding registers so that the value of each counter can be read. The channel is addressed by using bits D[3:0] in register 0xE5h. 0 = Normal Operation 1 = Updates all Counters	R/W	0

GLOBAL REGISTER (0XE6H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D2	BYTEsel	**LCV Counter Byte Select** This bit is used to select the MSB or LSB for Reading the contents of the LCV counter for a given channel. The channel is addressed by using bits D[3:0] in register 0xE5h. By default, the LSB byte is selected. 0 = Low Byte 1 = High Byte	R/W	0
D1	chUPDATE	**LCV Counter Update Per Channel** This bit is used to latch the contents of the counter for a given channel into a holding register so that the value of the counter can be read. The channel is addressed by using bits D[3:0] in register 0xE5h. 0 = Normal Operation 1 = Updates the Selected Channel	R/W	0
D0	Reserved	**LCV Counter Reset Per Channel** This bit is used to reset the LCV counter of a given channel to its default state 0000h. The channel is addressed by using bits D[3:0] in register 0xE5h. This bit must be set to "1" for 1μS. 0 = Normal Operation 1 = Resets the Selected Channel	R/W	0

TABLE 48: MICROPROCESSOR REGISTER 0XE7H BIT DESCRIPTION

GLOBAL REGISTER (0XE7H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	R/W	0
D6	Reserved	This Register Bit is Not Used	R/W	0
D5	Reserved	This Register Bit is Not Used	R/W	0
D4	Reserved	This Register Bit is Not Used	R/W	0
D3	Reserved	This Register Bit is Not Used	R/W	0
D2	Reserved	This Register Bit is Not Used	R/W	0
D1	Reserved	This Register Bit is Not Used	R/W	0
D0	Reserved	This Register Bit is Not Used	R/W	0

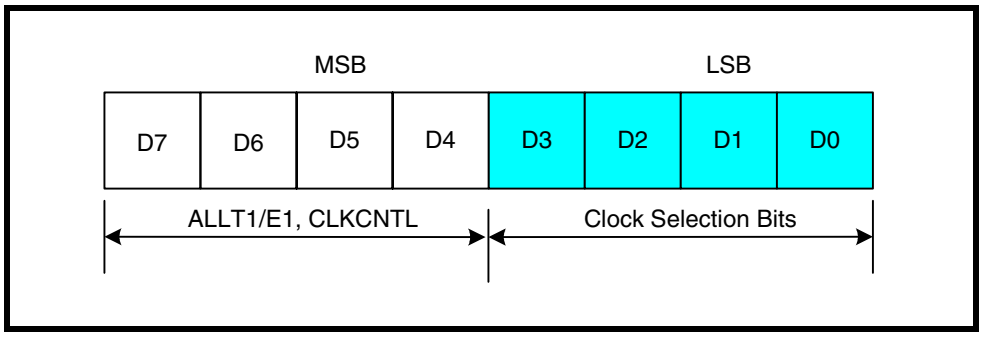
TABLE 49: MICROPROCESSOR REGISTER 0XE8H BIT DESCRIPTION

GLOBAL REGISTER (0XE8H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	LCVCNT7	**Line Code Violation Byte Contents**	R/W	0
D6	LCVCNT6	These bits contain the LCV counter contents of the Byte selected by bit D2 in register 0xE6h for a given channel. The channel is addressed by using bits D[3:0] in register 0xE5h. By default, the contents contain the LSB, however no channel is selected..		0
D5	LCVCNT5			0
D4	LCVCNT4			0
D3	LCVCNT3			0
D2	LCVCNT2			0
D1	LCVCNT1			0
D0	LCVCNT0			0

CLOCK SELECT REGISTER

The input clock source is used to generate all the necessary clock references internally to the LIU. The microprocessor timing is derived from a PLL output which is chosen by programming the Clock Select Bits in register 0xE9h. Therefore, if the clock selection bits are being programmed, the frequency of the PLL output will be adjusted accordingly. During this adjustment, it is important to "Not" write to any other bit location within the same register while selecting the input/output clock frequency. For best results, register 0xE9h can be broken down into two sub-registers with the MSB being bits D[7:4] and the LSB being bits D[3:0] as shown in Figure 42. Note: Bits D[7:6] are reserved.

FIGURE 42. REGISTER 0XE9H SUB REGISTERS



Programming Examples:

Example 1: Changing bits D[7:4]

If bits D[7:4] are the only values within the register that will change in a WRITE process, the microprocessor only needs to initiate ONE write operation.

Example 2: Changing bits D[3:0]

If bits D[3:0] are the only values within the register that will change in a WRITE process, the microprocessor only needs to initiate ONE write operation.

Example 3: Changing bits within the MSB and LSB

In this scenario, one must initiate TWO write operations such that the MSB and LSB do not change within ONE write cycle. It is recommended that the MSB and LSB be treated as two independent sub-registers. One can either change the clock selection (LSB) and then change bits D[5:4] (MSB) on the SECOND write, or vice-versa. No order or sequence is necessary.

TABLE 50: MICROPROCESSOR REGISTER 0XE9H BIT DESCRIPTION

GLOBAL REGISTER (0XE9H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	R/W	0
D6	Reserved	This Register Bit is Not Used	R/W	0

GLOBAL REGISTER (0XE9H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D5	ALLT1/E1	**T1/E1 Control** This bit is used to reduce system noise and power consumption. If the ALL T1/E1 mode is enabled, all output clock references (excluding the 8kHzout in E1 mode only) are internally shut off. By default, the ALL T1/E1 mode is enabled. 0 = Enabled (reduce clock switching and power consumption) 1 = Disabled (all clock references are available)	R/W	0
D4	TCLKCNL	**Transmit Clock Control** This bit is used to select the transmit output activity at TTIP/TRING when TCLK is either pulled "Low", pulled "High", or missing. 0 = Transmit All Zeros 1 = TAOS (Transmit All Ones)	R/W	0
D3 D2 D1 D0	CLKSEL3 CLKSEL2 CLKSEL1 CLKSEL0	**Clock Input Select** CLKSEL[3:0] is used to select the input clock source used as the internal timing reference. 0000 = 2.048 MHz 0001 = 1.544 MHz 0010 = 8 kHz 0011 = 16 kHz 0100 = 56 kHz 0101 = 64 kHz 0110 = 128 kHz 0111 = 256 kHz 1000 = 4.096 Mhz 1001 = 3.088 Mhz 1010 = 8.192 Mhz 1011 = 6.176 Mhz 1100 = 16.384 Mhz 1101 = 12.352 Mhz 1110 = 2.048 Mhz 1111 = 1.544 Mhz	R/W	0 0 0 0

TABLE 51: MICROPROCESSOR REGISTER 0XEAH BIT DESCRIPTION

GLOBAL REGISTER (0XEAH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	GCHIS7	**Global Channel Interrupt Status for Channel 7** 0 = No interrupt activity from channel 7 1 = Interrupt was generated from channel 7	RUR	0
D6	GCHIS6	**Global Channel Interrupt Status for Channel 6** 0 = No interrupt activity from channel 6 1 = Interrupt was generated from channel 6	RUR	0
D5	GCHIS5	**Global Channel Interrupt Status for Channel 5** 0 = No interrupt activity from channel 5 1 = Interrupt was generated from channel 5	RUR	0
D4	GCHIS4	**Global Channel Interrupt Status for Channel 4** 0 = No interrupt activity from channel 4 1 = Interrupt was generated from channel 4	RUR	0
D3	GCHIS3	**Global Channel Interrupt Status for Channel 3** 0 = No interrupt activity from channel 3 1 = Interrupt was generated from channel 3	RUR	0
D2	GCHIS2	**Global Channel Interrupt Status for Channel 2** 0 = No interrupt activity from channel 2 1 = Interrupt was generated from channel 2	RUR	0
D1	GCHIS1	**Global Channel Interrupt Status for Channel 1** 0 = No interrupt activity from channel 1 1 = Interrupt was generated from channel 1	RUR	0
D0	GCHIS0	**Global Channel Interrupt Status for Channel 0** 0 = No interrupt activity from channel 0 1 = Interrupt was generated from channel 0	RUR	0

TABLE 52: MICROPROCESSOR REGISTER 0XEBH BIT DESCRIPTION

GLOBAL REGISTER (0XEBH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	RUR	0
D6	Reserved	This Register Bit is Not Used	RUR	0
D5	GCHIS13	**Global Channel Interrupt Status for Channel 13** 0 = No interrupt activity from channel 13 1 = Interrupt was generated from channel 13	RUR	0

GLOBAL REGISTER (0XEBH)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D4	GCHIS12	**Global Channel Interrupt Status for Channel 12** 0 = No interrupt activity from channel 12 1 = Interrupt was generated from channel 12	RUR	0
D3	GCHIS11	**Global Channel Interrupt Status for Channel 11** 0 = No interrupt activity from channel 11 1 = Interrupt was generated from channel 11	RUR	0
D2	GCHIS10	**Global Channel Interrupt Status for Channel 10** 0 = No interrupt activity from channel 10 1 = Interrupt was generated from channel 10	RUR	0
D1	GCHIS9	**Global Channel Interrupt Status for Channel 9** 0 = No interrupt activity from channel 9 1 = Interrupt was generated from channel 9	RUR	0
D0	GCHIS8	**Global Channel Interrupt Status for Channel 8** 0 = No interrupt activity from channel 8 1 = Interrupt was generated from channel 8	RUR	0

TABLE 53: E1 ARBITRARY SELECT

E1 ARBITRARY SELECT REGISTER (0XF4H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D[7:1]	Reserved			
D0	E1arben	**E1 Arbitrary Pulse Enable** This bit is used to enable the Arbitrary Pulse Generators for shaping the transmit pulse shape when E1 mode is selected. If this bit is set to "1", all 14 channels will be configured for the Arbitrary Mode. However, each channel is individually controlled by programming the channel registers 0xn8 through 0xnF, where n is the number of the channel. "0" = Disabled (Normal E1 Pulse Shape ITU G.703) "1" = Arbitrary Pulse Enabled	R/W	0

DEVICE "ID" REGISTER (0XFEH)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Device "ID"	The device "ID" of the XRT83SL314 short haul LIU is 0xFEh. Along with the revision "ID", the device "ID" is used to enable software to identify the silicon adding flexibility for system control and debug.	RO	1
D6				1
D5				1
D4				1
D3				1
D2				1
D1				1
D0				0

Microprocessor Register 0xFEh Bit Description

TABLE 54: MICROPROCESSOR REGISTER 0XFFH BIT DESCRIPTION

REVISION "ID" REGISTER (0XFFH)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Revision "ID"	The revision "ID" of the XRT83SL314 LIU is used to enable software to identify which revision of silicon is currently being tested. The revision "ID" for the first revision of silicon will be 0x01h.	RO	0
D6				0
D5				0
D4				0
D3				0
D2				0
D1				0
D0				1

ELECTRICAL CHARACTERISTICS

TABLE 55: ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Supply Voltage	-0.5V to +3.8V
Vin	-0.5V to +5.5V

TABLE 56: DC DIGITAL INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply Voltage	VDD	3.13	3.3	3.46	V
Input High Voltage	V_{IH}	2.0	-	5.0	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Output High Voltage IOH=2.0mA	V_{OH}	2.4	-		V
Output Low Voltage IOL=2.0mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_L	-	-	±10	µA
Input Capacitance	C_I	-	5.0		pF
Output Lead Capacitance	C_L	-	-	25	pF

NOTE: *Input leakage current excludes pins that are internally pulled "Low" or "High"*

TABLE 57: AC ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**
MCLKin Clock Duty Cycle		40	-	60	%
MCLKin Clock Tolerance		-	±50	-	ppm

TABLE 58: POWER CONSUMPTION

VDD=3.3V ±5%, T_A=25°C, INTERNAL IMPEDANCE, UNLESS OTHERWISE SPECIFIED								
MODE	SUPPLY VOLTAGE	IMPEDANCE	RECEIVER	TRANSMITTER	TYP	MAX	UNIT	TEST CONDITION
E1	3.3V	75Ω	1:1	1:2	2.80	3.29	W	100% ones
E1	3.3V	120Ω	1:1	1:2	2.52	2.96	W	100% ones
T1	3.3V	100Ω	1:1	1:2	2.81	3.31	W	100% ones
-	3.3V	-	1:1	1:2	620	730	mW	All Transmitters Turned Off

TABLE 59: E1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITION
Receiver Loss of Signal					
Number of consecutive zeros before RLOS is declared	10	175	255		
Input signal level at RLOS	15	20	-	dB	Cable attenuation @ 1024kHz
RLOS clear	12.5	-	-	dB	ITU-G.775, ETSI 300 233
Receiver Sensitivity (short haul with cable loss)	11	-	-	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω with -18dB interference signal added.
Input Impedance	-	13	-	kΩ	
Input Jitter Tolerance					
1Hz	37	-	-	UI_{p-p}	ITU-G.823
10kHz - 100kHz	0.2	-	-	UI_{p-p}	
Recovered Clock Jitter					
Transfer Corner Frequency	-	36	-	kHz	ITU-G.736
Peaking Amplitude	-	-	-0.5	dB	

TABLE 59: E1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**	**TEST CONDITION**
Jitter Attenuator Corner Frequency	-	10	-	Hz	ITU-G.736
JABW = 0	-	1.5	-	Hz	
JABW = 1					
Return Loss					
51kHz - 102kHz	14	-	-	dB	ITU-G.703
102kHz - 2048kHz	20	-	-	dB	
2048kHz - 3072kHz	16	-	-	dB	

TABLE 60: T1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**	**TEST CONDITION**
Receiver Loss of Signal					
Number of consecutive zeros before RLOS is declared	100	175	250		
Input signal level at RLOS	15	20	-	dB	Cable attenuation @ 772kHz
RLOS clear	12.5	-	-	% ones	ITU-G.775, ETSI 300 233
Receiver Sensitivity (short haul with cable loss)	12	-	-	dB	With nominal pulse amplitude of 3.0V for 100Ω termination.
Input Impedance	-	13	-	kΩ	
Input Jitter Tolerance					
1Hz	138	-	-	UI_{p-p}	AT&T Pub 62411
10kHz - 100kHz	0.4	-	-	UI_{p-p}	
Recovered Clock Jitter					
Transfer Corner Frequency	-	9.8	-	kHz	TR-TSY-000499
Peaking Amplitude	-	-	0.1	dB	
Jitter Attenuator Corner Frequency	-	6	-	Hz	AT&T Pub 62411
Return Loss					
51kHz - 102kHz	-	20	-	dB	
102kHz - 2048kHz	-	25	-	dB	
2048kHz - 3072kHz	-	25	-	dB	

TABLE 61: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**	**TEST CONDITION**
AMI Output Pulse Amplitude					
75Ω	2.185	2.37	2.555	V	1:2 Transformer
120Ω	2.76	3.00	3.24	V	
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05		ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05		ITU-G.703
Jitter Added by the Transmitter Output	-	0.025	0.05	UI_{p-p}	Broad Band with jitter free TCLK applied to the input.
Output Return Loss					
51kHz - 102kHz	8	-	-	dB	ETSI 300 166, CHPTT
102kHz - 2048kHz	14	-	-	dB	
2048kHz - 3072kHz	10	-	-	dB	

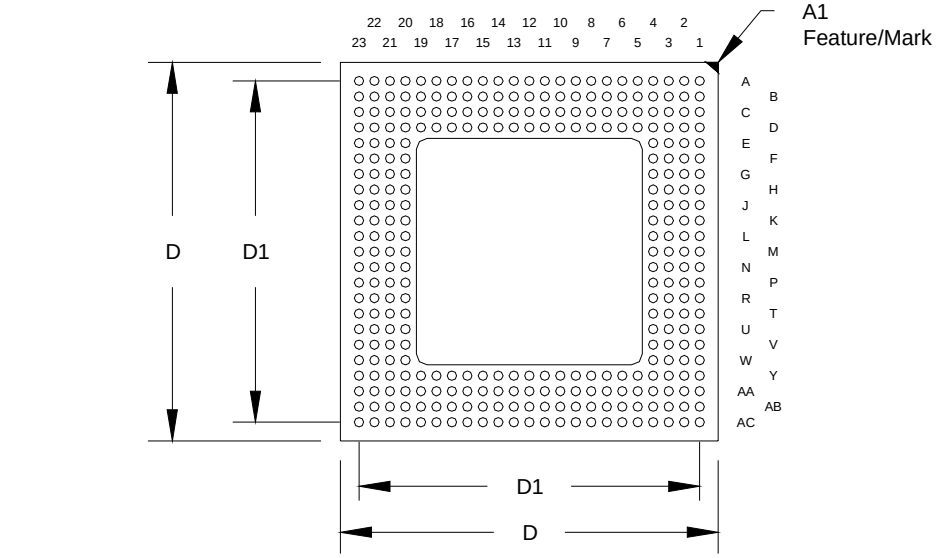
TABLE 62: T1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**	**TEST CONDITION**
AMI Output Pulse Amplitude	2.5	3.0	3.5	V	1:2 Transformer measured at DSX-1
Output Pulse Width	338	350	362	ns	ANSI T1.102
Output Pulse Width Imbalance	-	-	20		ANSI T1.102
Output Pulse Amplitude Imbalance	-	-	±200	mV	ANSI T1.102
Jitter Added by the Transmitter Output	-	0.025	0.05	UI_{p-p}	Broad Band with jitter free TCLK applied to the input.
Output Return Loss					
51kHz - 102kHz	-	15	-	dB	
102kHz - 2048kHz	-	15	-	dB	
2048kHz - 3072kHz	-	15	-	dB	

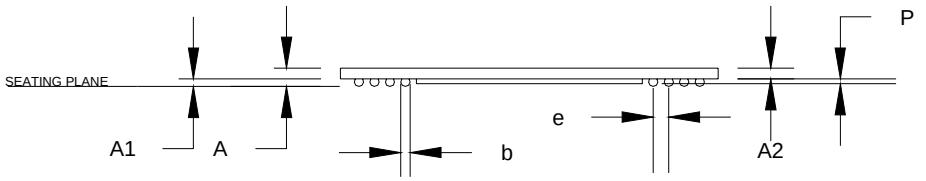
ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83SL314IB	304 LEAD TBGA	-40^{0}C to +85^{0}C

PACKAGE DIMENSIONS (DIE DOWN)



(A1 corner feature is mfger option)



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.051	0.067	1.30	1.70
A1	0.018	0.028	0.45	0.70
A2	0.031	0.071	0.80	1.80
P	0.004	0.012	0.10	0.30
D	1.213	1.228	30.80	31.20
D1	1.100 BSC		27.94 BSC	
b	0.024	0.035	0.60	0.90
e	0.050 BSC		1.27 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	01/22/03	First release of the 14-Channel LIU Preliminary Datasheet
P1.0.1	01/28/03	Added the Motorola 68K asynchronous Mode Timing
P1.0.2	02/14/03	Edited the Microprocessor Timing Specifications
P1.0.3	03/27/03	Added the 16-bit LCV Counter Details for Revision B Silicon
P1.0.4	09/19/03	Changed the Microprocessor Access Timing Parameters
P1.0.5	11/12/03	Added new E1 arbitrary pulse feature. Added descriptions to the global registers.
1.0.0	05/04/04	Final Release.
1.0.1	03/17/05	Modified INT pad description from open-drain to internal pulled-up.

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Copyright 2005 EXAR Corporation

Datasheet March 2005.

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View XRT83SL314IB on WIN SOURCE
- Exar Corporation Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management