




**THE DATASHEET OF  
840271BGILF**



**General Description**

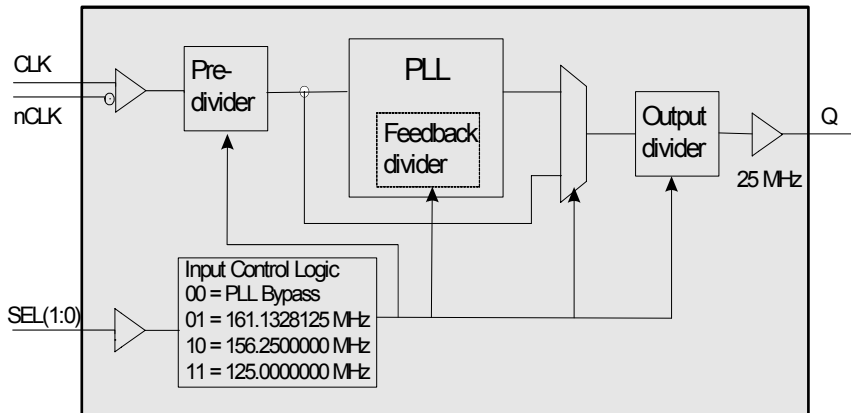


The ICS840271I is a PLL-based Frequency Translator intended for use in telecommunication applications such as Synchronous Ethernet. The internal PLL translates Ethernet clock frequencies such as 125MHz (1Gb Ethernet), 156.25MHz (10GbE XAU) and 161.1328MHz (10Gb Ethernet) to an output frequency of 25MHz. The PLL does not require any external components. The input frequency is selectable by a 2-pin interface. The ICS840271I is optimized for low cycle-to-cycle jitter on the 25MHz output signal. The input of the device accepts differential (LVPECL, LVDS, LVHSTL, SSTL, HCSL) or single-ended (LVCMOS) signals. The extended temperature range supports telecommunication and networking equipment requirements. The ICS840271I uses a small RoHS 6, 8-pin TSSOP package and is an effective solution for space-constrained applications.

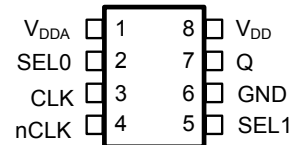
**Features**

- Clock frequency translator for Synchronous Ethernet applications
- One single-ended output (LVCMOS or LVTTTL levels), 16Ω output impedance
- Differential input pair (CLK, nCLK) accepts LVPECL, LVDS, LVHSTL, SSTL, HCSL input levels
- Supports input clock frequencies of: 125MHz, 156.25MHz or 161.1328MHz
- Generates a 25MHz output clock signal
- Internal resistor bias on nCLK pin allows the user to drive CLK input with external single-ended (LVCMOS/LVTTTL) input levels
- Internal PLL is optimized for low cycle-to-cycle jitter at the output
- Full 3.3V or 2.5V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

**Block Diagram**



**Pin Assignment**



**ICS840271I**  
**8 Lead TSSOP**  
**4.40mm x 3.0mm x 0.925mm**  
**package body**  
**G Package**  
**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	V <sub>DDA</sub>	Power		Analog supply pin.
2	SEL0	Input	Pulldown	Selects the input reference frequency and the PLL bypass mode. LVCMOS/LVTTL interface levels. See Table 3.
3	CLK	Input	Pulldown	Non-inverting differential clock input.
4	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to V <sub>DD</sub> /2.
5	SEL1	Input	Pullup	Selects the input reference frequency and the PLL bypass mode. LVCMOS/LVTTL interface levels. See Table 3.
6	GND	Power		Power supply ground.
7	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
8	V <sub>DD</sub>	Power		Core supply pin.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
R <sub>OUT</sub>	Output Impedance	V <sub>DD</sub> = 3.465V		16		Ω
		V <sub>DD</sub> = 2.625V		19		Ω

**Function Tables****Table 3. SEL[1:0] Function Table**

Inputs			Mode	Output (MHz)
SEL1	SEL0	CLK, nCLK (MHz)		
0	0	REF	PLL Bypass	REF/ 5
0	1	161.1328125	PLL Enabled	25
1 (default)	0 (default)	156.25	PLL Enabled	25
1	1	125	PLL Enabled	25

NOTE: REF = Input clock signal frequency

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$ (LVCMOS)	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	129.5°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.08$	3.3	$V_{DD}$	V
$I_{DD}$	Power Supply Current				75	mA
$I_{DDA}$	Analog Supply Current				8	mA

**Table 4B. Power Supply DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.08$	2.5	$V_{DD}$	V
$I_{DD}$	Power Supply Current				72	mA
$I_{DDA}$	Analog Supply Current				8	mA

**Table 4C. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.3V$	-0.3		0.8	V
		$V_{DD} = 2.5V$	-0.3		0.7	V
$I_{IH}$	Input High Current	SEL1 $V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu\text{A}$
		SEL0 $V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu\text{A}$
$I_{IL}$	Input Low Current	SEL1 $V_{DD} = 3.465V$ , $V_{IN} = 0V$	-150			$\mu\text{A}$
		SEL0 $V_{DD} = 3.465V$ , $V_{IN} = 0V$	-5			$\mu\text{A}$
$V_{OH}$	Output High Voltage	$V_{DD} = 3.465V$ , $I_{OH} = 12\text{mA}$	2.6			V
		$V_{DD} = 2.625V$ , $I_{OH} = 12\text{mA}$	1.8			V
$V_{OL}$	Output Low Voltage	$V_{DD} = 3.465V$ or $2.625V$ , $I_{OL} = -12\text{mA}$			0.5	V

**Table 4D. Differential DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK/nCLK $V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK $V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5			$\mu\text{A}$
		nCLK $V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu\text{A}$
$V_{PP}$	Peak-to-Peak Voltage; NOTE 1		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3V.NOTE 2: Common mode input voltage is defined as  $V_{IH}$ .

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency			25		MHz
$f_{jit(cc)}$	Cycle-to-Cycle Jitter	$SEL0 \neq SEL1$			40	ps
		$SEL0 = SEL1 = 1$			15	ps
$t_{LOCK}$	PLL Lock Time	$SEL1 = 0, SEL0 = 1$			1	s
		$SEL1 = 1, SEL0 = X$			50	ms
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		47		53	%

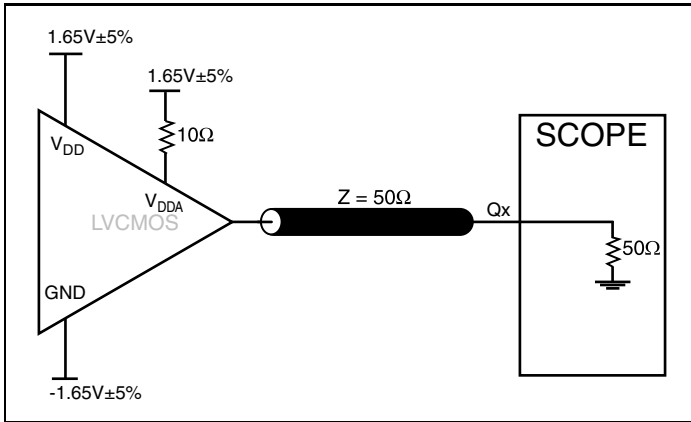
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

**Table 5B. AC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

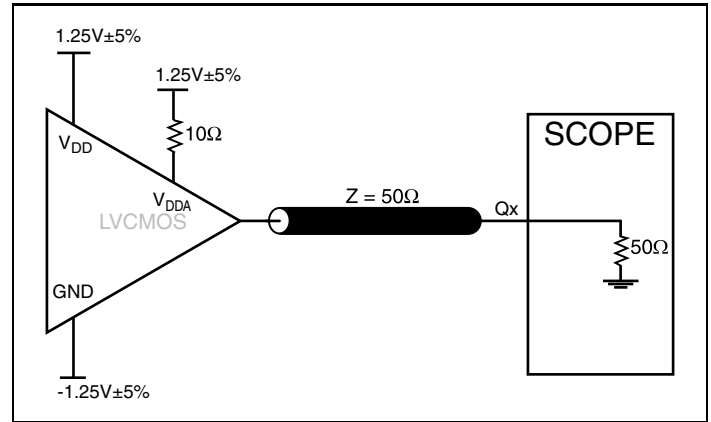
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency			25		MHz
$f_{jit(cc)}$	Cycle-to-Cycle Jitter	$SEL0 \neq SEL1$			50	ps
		$SEL0 = SEL1 = 1$			15	ps
$t_{LOCK}$	PLL Lock Time	$SEL1 = 0, SEL0 = 1$			1	s
		$SEL1 = 1, SEL0 = X$			50	ms
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		47		53	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

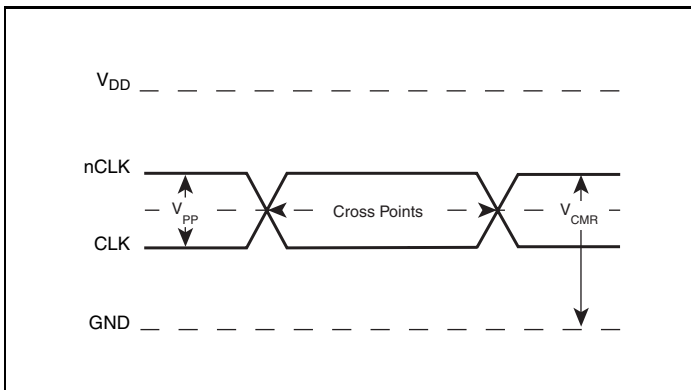
### Parameter Measurement Information



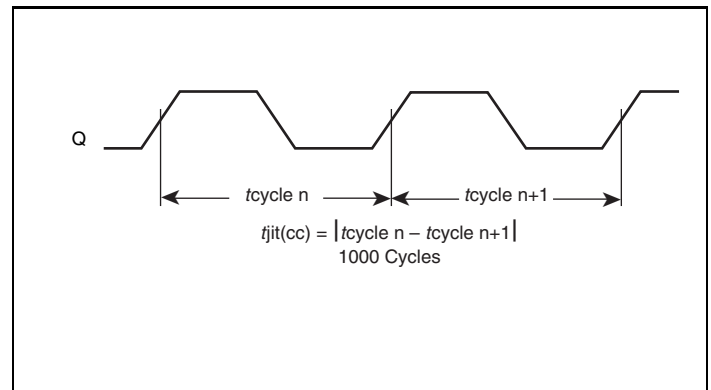
3.3V Output Load AC Test Circuit



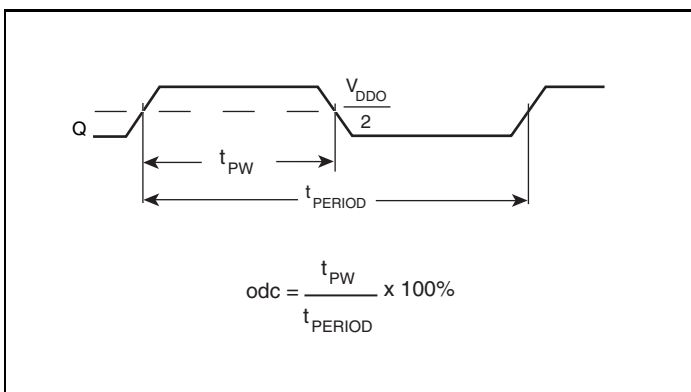
2.5V Output Load AC Test Circuit



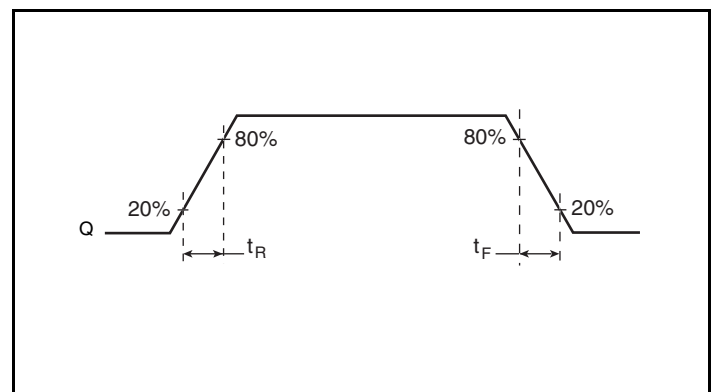
Differential Input Level



Cycle-to-Cycle Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

## Application Information

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS840271I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$  and  $V_{DDA}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{DDA}$  pin.

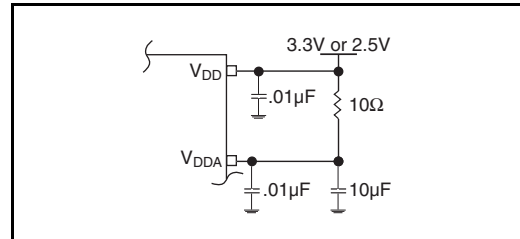


Figure 1. Power Supply Filtering

### Wiring the Differential Input to Accept Single Ended Levels

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors  $R1$ ,  $R2$  and  $C1$ . This bias circuit should be located as close as possible to the input pin. The ratio of  $R1$  and  $R2$  might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only  $2.5\text{V}$  and  $V_{DD} = 3.3\text{V}$ ,  $V_{REF}$  should be  $1.25\text{V}$  and  $R2/R1 = 0.609$ .

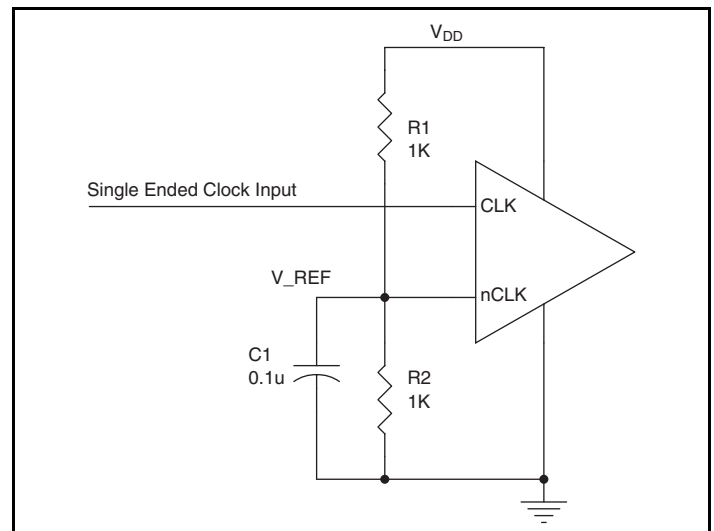


Figure 2. Single-Ended Signal Driving Differential Input

### Recommendations for Unused Input Pins

#### Inputs:

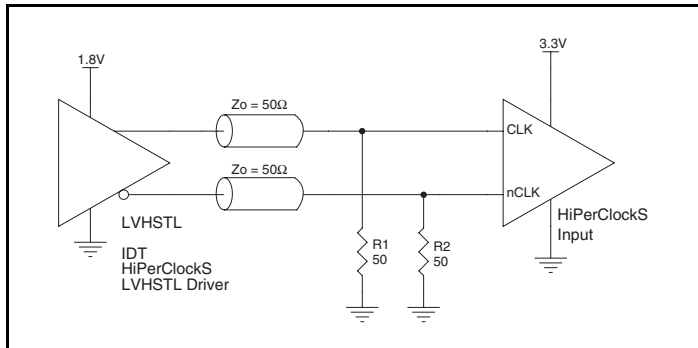
##### LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

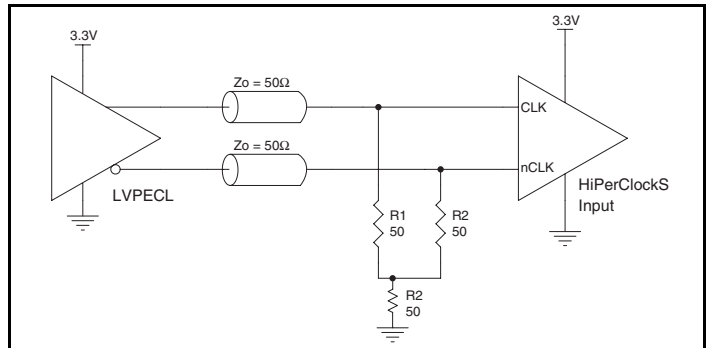
### Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3F show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver

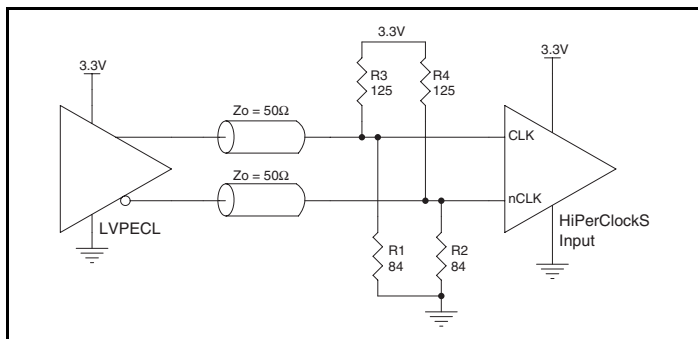
component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



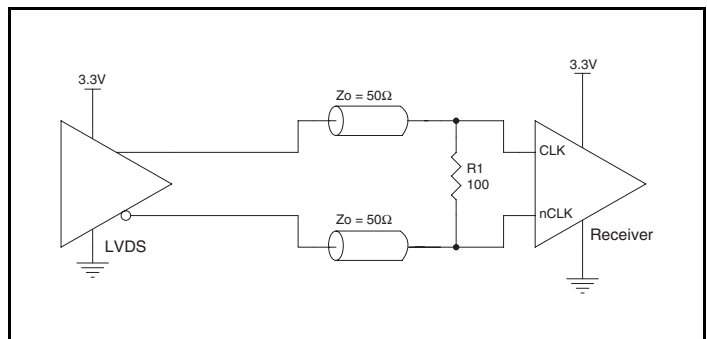
**Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver**



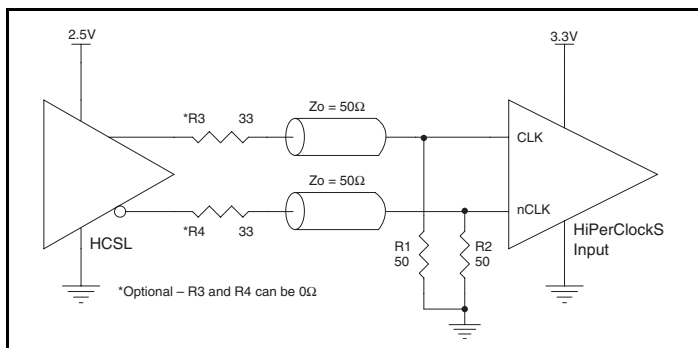
**Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



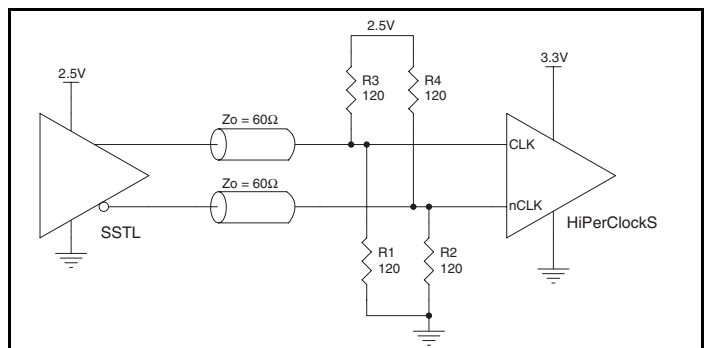
**Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver**



**Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver**



**Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver**

## Schematic Example

Figure 4 shows an example of ICS840271I applications schematic. In this example, the device is operated at  $V_{DD} = 3.3V$ . The input is driven by either a 3.3V LVPECL or LVDS driver. One example of

LVC MOS termination is shown in this schematic. The decoupling capacitors should be located as close as possible to the power pin.

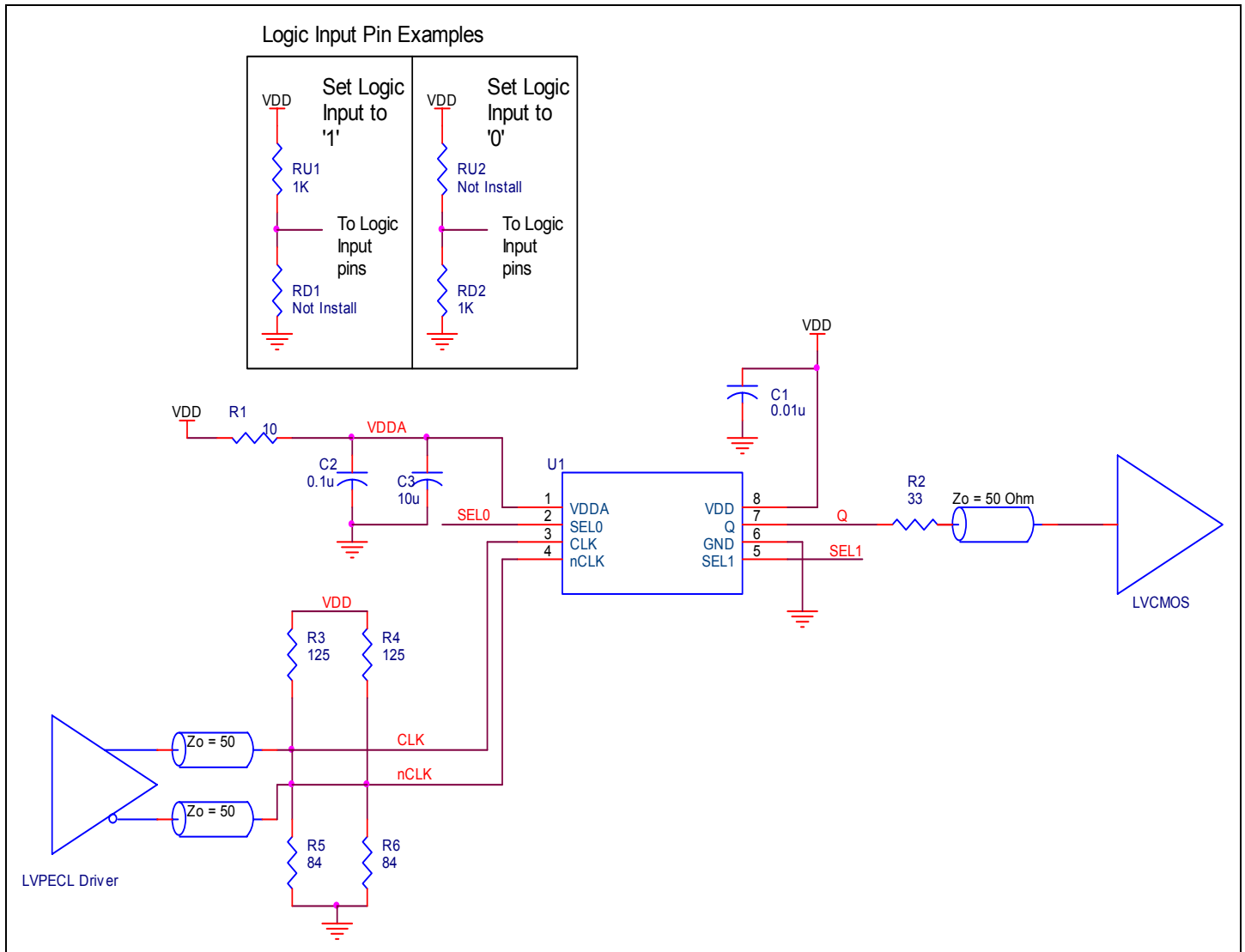


Figure 4. ICS840271I Schematic layout

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS840271I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS840271I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD} + I_{DDA}) = 3.465V * (75mA + 8mA) = \mathbf{287.6mW}$
- Output Impedance  $R_{OUT}$  Power Dissipation due to Loading  $50\Omega$  to  $V_{DD}/2$   
Output Current  $I_{OUT} = V_{DD\_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 16\Omega)] = \mathbf{26.25mA}$
- Power Dissipation on the  $R_{OUT}$  per LVCMOS output  
Power ( $R_{OUT}$ ) =  $R_{OUT} * (I_{OUT})^2 = 16\Omega * (26.25mA)^2 = \mathbf{11mW}$  per output

### Total Power Dissipation

- Total Power**  
= Power (core)<sub>MAX</sub> + Total Power ( $R_{OUT}$ )  
= 287.6mW + 11mW  
= **298.6mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.299\text{W} * 129.5^\circ\text{C/W} = 123.7^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 8 Lead TSSOP, Forced Convection**

Meters per Second	$\theta_{JA}$ by Velocity		
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 8 Lead TSSOP

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

## Transistor Count

The transistor count for ICS840271I is: 2732

## Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

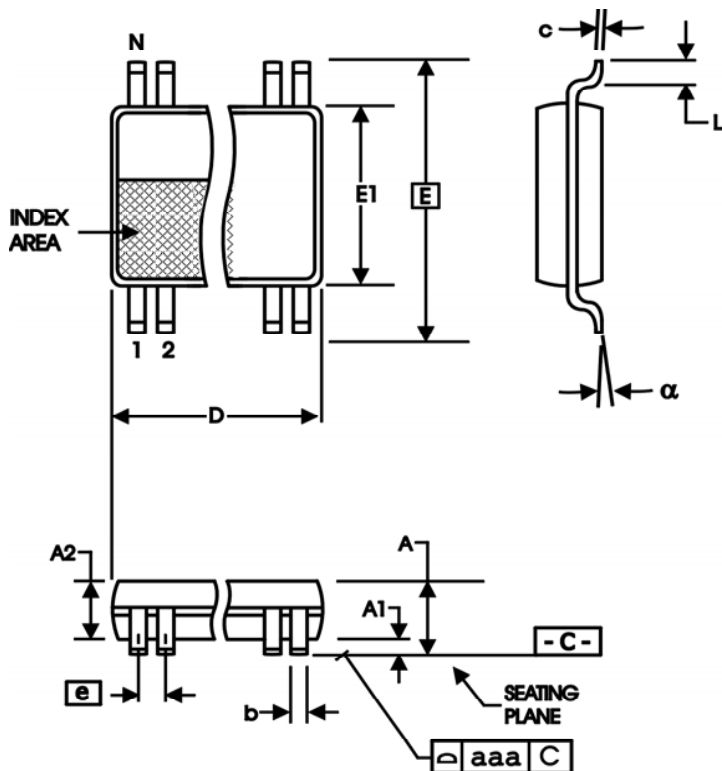


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840271BGILF	71BIL	"Lead-Free" 8 Lead TSSOP	Tube	-40°C to 85°C
840271BGILFT	71BIL	"Lead-Free" 8 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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