



**THE DATASHEET OF
CD54HC164F3A**



CDx4HC164, CDx4HCT164 High-Speed CMOS Logic 8-Bit Serial-In, Parallel-Out Shift Register

1 Features

- Buffered inputs
- Asynchronous reset
- Typical $f_{MAX} = 60\text{MHz}$ at $V_{CC} = 5\text{V}$, $C_L = 15\text{pF}$, $T_A = 25^\circ\text{C}$
- Fanout (overtemperature range)
 - Standard Outputs: 10 LSTTL loads
 - Bus driver outputs: 15 LSTTL loads
- Wide operating temp range: -55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- HC types
 - 2V to 6V operation
 - High noise immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5\text{V}$
- HCT types
 - 4.5V to 5.5V operation
 - Direct LSTTL input logic compatibility, $V_{IL} = 0.8\text{V}$ (Max), $V_{IH} = 2\text{V}$ (Min)
 - CMOS input compatibility, $I_I \leq 1\mu\text{A}$ at V_{OL} , V_{OH}

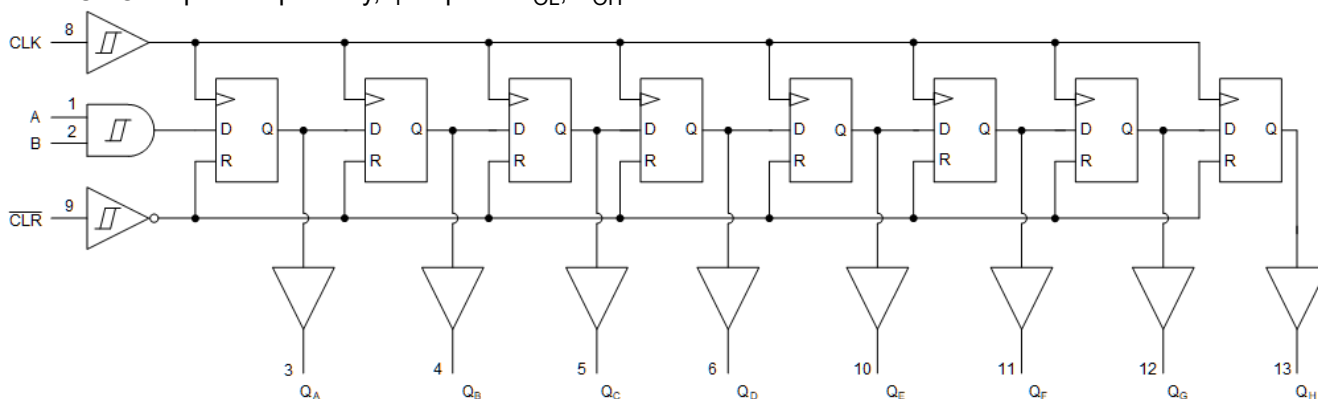
2 Description

The 'HC164 and 'HCT164 are 8-bit, serial-in, parallel-out, shift registers with asynchronous reset. Data is shifted on the positive edge of Clock (CLK). A LOW on the RESET (CLR) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (A and B) are provided, either one can be used as a data enable control.

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) |
|-------------|------------------------|------------------|
| CD74HC164M | SOIC (14) | 8.65mm × 3.90mm |
| CD74HCT164M | SOIC (14) | 8.65mm × 3.90mm |
| CD74HC164E | PDIP (14) | 19.31mm × 6.35mm |
| CD74HCT164E | PDIP (14) | 19.31mm × 6.35mm |
| CD54HC164F | CDIP (14) | 19.55mm × 6.71mm |

(1) For all available packages, see [Section 11](#).



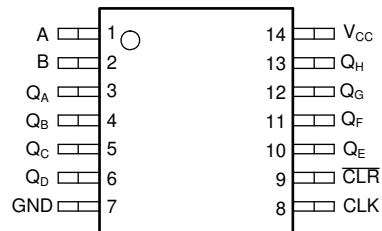
Functional Block Diagram



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3 Pin Configuration and Functions



**J, D, and N Package
14-Pin CDIP, SOIC, and PDIP
Top View**

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|---|-----|--------|
| V _{CC} | Supply voltage range | -0.5 | 7 | V |
| I _{IK} | Input clamp current ⁽²⁾ | (V _I < 0 or V _I > V _{CC}) | | ±20 mA |
| I _{OK} | Output clamp current ⁽²⁾ | (V _O < 0 or V _O > V _{CC}) | | ±20 mA |
| I _O | Continuous output current | (V _O = 0 to V _{CC}) | | ±25 mA |
| | Continuous current through V _{CC} or GND | | | ±50 mA |
| T _J | Junction temperature | | | 150 °C |
| T _{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Recommended Operating Conditions

| | | MIN | MAX | UNIT | |
|---------------------------------|--------------------------|-----------|-----------------|------|---|
| V _{CC} | Supply voltage range | HC types | 2 | 6 | V |
| | | HCT types | 4.5 | 5.5 | |
| V _I , V _O | Input or output voltage | 0 | V _{CC} | V | |
| | Input rise and fall time | 2 V | 1000 | ns | |
| | | 4.5 V | 500 | | |
| | | 6 V | 400 | | |
| T _A | Temperature range | -55 | 125 | °C | |

4.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | D (SOIC) | N (PDIP) | UNIT |
|-------------------------------|--|----------|----------|------|
| | | 14 PINS | 14 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 86 | 80 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

4.4 Electrical Characteristics

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | V _{CC} (V) | 25°C | | | –40°C to 85°C | | –55°C to 125°C | | UNIT |
|-----------------------------|---|---|---------------------|---------|-----|------|---------------|------|----------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | |
| V _{IH} | High level input voltage | | 2 | 1.5 | | 1.5 | | 1.5 | | V | |
| | | | 4.5 | 3.15 | | 3.15 | | 3.15 | | | |
| | | | 6 | 4.2 | | 4.2 | | 4.2 | | | |
| V _{IL} | Low level input voltage | | 2 | 0.5 | | 0.5 | | 0.5 | | V | |
| | | | 4.5 | 1.35 | | 1.35 | | 1.35 | | | |
| | | | 6 | 1.8 | | 1.8 | | 1.8 | | | |
| V _{OH} | High level output voltage | I _{OH} = – 20 μA | 2 | 1.9 | | 1.9 | | 1.9 | | V | |
| | | I _{OH} = – 20 μA | 4.5 | 4.4 | | 4.4 | | 4.4 | | | |
| | | I _{OH} = – 20 μA | 6 | 5.9 | | 5.9 | | 5.9 | | | |
| | High level output voltage | I _{OH} = – 4 mA | 4.5 | 3.98 | | 3.84 | | 3.7 | | | |
| | | I _{OH} = – 5.2 mA | 6 | 5.48 | | 5.34 | | 5.2 | | | |
| V _{OL} | Low level output voltage | I _{OL} = 20 μA | 2 | 0.1 | | 0.1 | | 0.1 | | V | |
| | | I _{OL} = 20 μA | 4.5 | 0.1 | | 0.1 | | 0.1 | | | |
| | | I _{OL} = 20 μA | 6 | 0.1 | | 0.1 | | 0.1 | | | |
| | Low level output voltage | I _{OL} = 4 mA | 4.5 | 0.26 | | 0.33 | | 0.4 | | | |
| | | I _{OL} = 5.2 mA | 6 | 0.26 | | 0.33 | | 0.4 | | | |
| I _I | Input leakage current | | 6 | ±0.1 | | ±1 | | ±1 | | μA | |
| I _{CC} | Supply current | V _I = V _{CC} or GND | 6 | 8 | | 80 | | 160 | | μA | |
| HCT TYPES | | | | | | | | | | | |
| V _{IH} | High level input voltage | | 4.5 to 5.5 | 2 | | 2 | | 2 | | V | |
| V _{IL} | Low level input voltage | | 4.5 to 5.5 | 0.8 | | 0.8 | | 0.8 | | V | |
| V _{OH} | High level output voltage | I _{OH} = – 20 μA | 4.5 | 4.4 | | 4.4 | | 4.4 | | V | |
| | High level output voltage | I _{OH} = – 4 μA | 4.5 | 3.98 | | 3.84 | | 3.7 | | | |
| V _{OL} | Low level output voltage | I _{OL} = 20 μA | 4.5 | 0.1 | | 0.1 | | 0.1 | | V | |
| | Low level output voltage | I _{OL} = 4 μA | 4.5 | 0.26 | | 0.33 | | 0.4 | | | |
| I _I | Input leakage current | V _I = V _{CC} or GND | 5.5 | ±0.1 | | ±1 | | ±1 | | μA | |
| I _{CC} | Supply current | V _I = V _{CC} or GND | 5.5 | 8 | | 80 | | 160 | | μA | |
| ΔI _{CC} (2) (3) | Additional supply current per input pin | Date Shift-In (1,2) | 4.5 to 5.5 | 100 108 | | 135 | | 147 | | μA | |
| | | CLR | 4.5 to 5.5 | 100 324 | | 405 | | 441 | | μA | |
| | | CLK | 4.5 to 5.5 | 100 252 | | 315 | | 343 | | μA | |

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

(3) Inputs held at V_{CC} – 2.1.

4.5 Prerequisite for Switching Characteristics

| PARAMETER | | V _{CC} (V) | 25°C | | – 40°C to 85°C | | – 55°C to 125°C | | UNIT |
|------------------|-------------------------------|---------------------|------|-----|----------------|-----|-----------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | |
| f _{MAX} | Maximum clock frequency | 2 | 6 | 5 | 4 | MHz | | | |
| | | 4.5 | 30 | 24 | 20 | MHz | | | |
| | | 6 | 35 | 28 | 24 | MHz | | | |
| t _W | CLR pulse width | 2 | 60 | 75 | 90 | ns | | | |
| | | 4.5 | 12 | 15 | 18 | ns | | | |
| | | 6 | 10 | 13 | 15 | ns | | | |
| t _W | CLK pulse width | 2 | 80 | 100 | 120 | ns | | | |
| | | 4.5 | 16 | 20 | 24 | ns | | | |
| | | 6 | 14 | 17 | 20 | ns | | | |
| t _{SU} | Set-up time | 2 | 60 | 75 | 90 | ns | | | |
| | | 4.5 | 12 | 15 | 18 | ns | | | |
| | | 6 | 10 | 13 | 15 | ns | | | |
| t _H | Hold time | 2 | 4 | 4 | 4 | ns | | | |
| | | 4.5 | 4 | 4 | 4 | ns | | | |
| | | 6 | 4 | 4 | 4 | ns | | | |
| t _{REM} | CLR to clock, Removal time | 2 | 80 | 100 | 120 | ns | | | |
| | | 4.5 | 16 | 20 | 24 | ns | | | |
| | | 6 | 14 | 17 | 20 | ns | | | |
| HCT TYPES | | | | | | | | | |
| f _{MAX} | Maximum clock frequency | 4.5 | 27 | 22 | 18 | MHz | | | |
| t _W | CLR pulse width | 6 | 18 | 23 | 27 | ns | | | |
| t _W | CLK pulse width | 4.5 | 18 | 23 | 27 | ns | | | |
| t _{SU} | Set-up time | 6 | 12 | 15 | 18 | ns | | | |
| t _H | Hold time | 4.5 | 4 | 4 | 4 | ns | | | |
| t _{REM} | CLR to clock, Removal time | 6 | 16 | 20 | 24 | ns | | | |

4.6 Switching Characteristics

Input t_r , $t_f = 6\text{ns}$. $C_L = 50\text{pF}$ unless otherwise noted

| PARAMETER | | V_{CC} (V) | 25°C | | - 40°C to 85°C | - 55°C to 125°C | UNIT |
|-----------------------|--|--------------|-------------------|-----|-------------------|--------------------|------|
| | | | TYP | MAX | MAX | MAX | |
| HC TYPES | | | | | | | |
| t_{PLH} , t_{PHL} | CLK to Q | 2 | | 170 | 212 | 255 | ns |
| | | 4.5 | 14 ⁽³⁾ | 34 | 43 | 51 | ns |
| | | 6 | | 29 | 36 | 43 | ns |
| t_{PLH} , t_{PHL} | $\overline{\text{CLR}}$ to Q | 2 | | 140 | 175 | 210 | ns |
| | | 4.5 | 11 ⁽³⁾ | 28 | 35 | 42 | ns |
| | | 6 | | 24 | 30 | 36 | ns |
| t_{TLH} , t_{THL} | Output transition times | 2 | | 75 | | 110 | ns |
| | | 4.5 | | 15 | | 22 | ns |
| | | 6 | | 13 | | 19 | ns |
| f_{MAX} | Maximum clock frequency | 5 | 60 ⁽³⁾ | | | | ns |
| C_{IN} | Input capacitance | | | 10 | 10 | 10 | pF |
| C_{PD} | Power dissipation capacitance ^{(1) (2)} | 5 | 47 | | | | pF |
| HCT TYPES | | | | | | | |
| t_{PLH} , t_{PHL} | CLK to Q | 4.5 | | 36 | 45 | 54 | ns |
| | | 5 | 15 ⁽³⁾ | | | | |
| t_{PLH} , t_{PHL} | $\overline{\text{CLR}}$ to Q | 4.5 | | 38 | 46 | 57 | ns |
| | | 5 | 16 ⁽³⁾ | | | | |
| t_{TLH} , t_{THL} | Output Transition time | 4.5 | | 15 | 19 | 22 | ns |
| C_{IN} | Input Capacitance | | | | | | pF |
| f_{MAX} | Maximum clock frequency | | 54 ⁽⁴⁾ | | | | MHz |
| C_{PD} | Power dissipation capacitance ^{(1) (2)} | 5 | 49 | 10 | 10 | 10 | pF |

(1) C_{PD} is used to determine the dynamic power consumption, per device.

(2) $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_o)$ where f_i = Input Frequency, f_o = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

(3) $C_L = 15\text{pF}$. $V_{CC} = 5$.

(4) $C_L = 15\text{pF}$.

5 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_t < 6\text{ns}$.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.

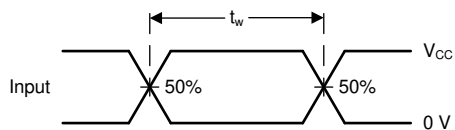


Figure 5-1. Voltage Waveforms, Standard CMOS Inputs Pulse Duration

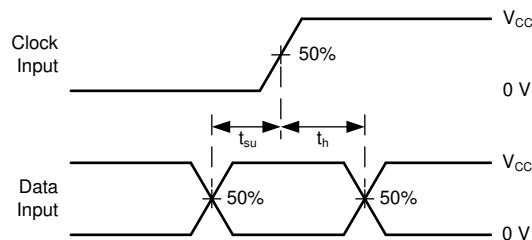


Figure 5-2. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times

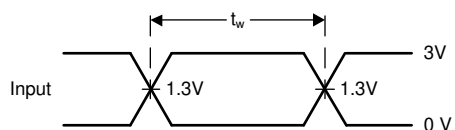


Figure 5-3. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

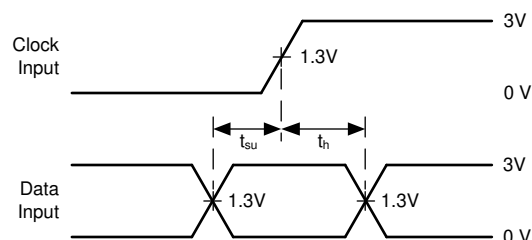


Figure 5-4. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times

6 Detailed Description

6.1 Overview

The 'HC164 and 'HCT164 are 8-bit, serial-in, parallel-out, shift registers with asynchronous reset. Data is shifted on the positive edge of Clock (CLK). A LOW on the RESET ($\overline{\text{CLR}}$) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (A and B) are provided, either one can be used as a data enable control.

6.2 Functional Block Diagram

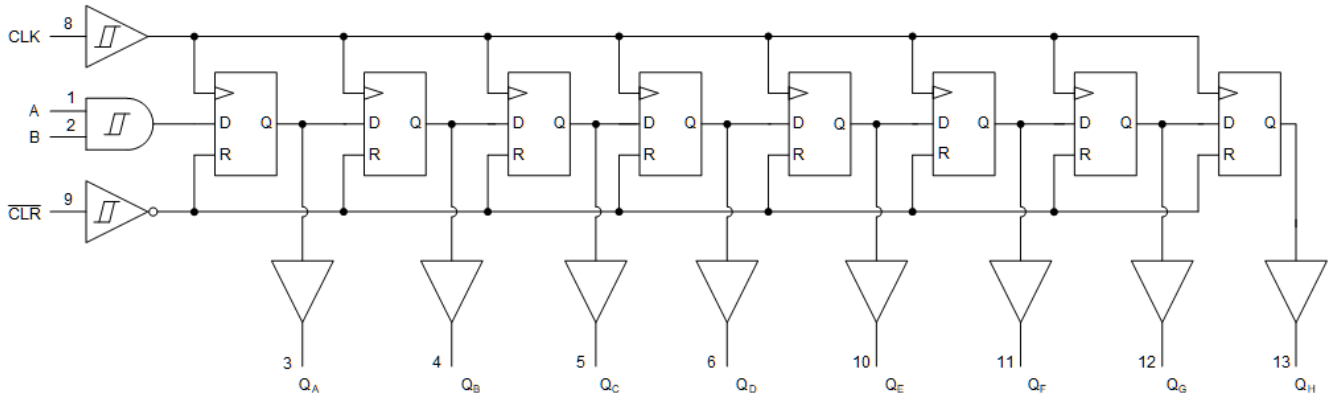


Figure 6-1. Functional Block Diagram

6.3 Device Functional Modes

Truth Table⁽¹⁾

| OPERATING MODE | INPUTS | | | | OUTPUTS | |
|----------------|-------------------------|-----|---|---|---------|-------------|
| | $\overline{\text{CLR}}$ | CLK | A | B | Q_A | $Q_B - Q_H$ |
| RESET (CLEAR) | L | X | X | X | L | L - L |
| Shift | H | ↑ | l | l | L | $q_A - q_F$ |
| | H | ↑ | l | h | L | $q_A - q_F$ |
| | H | ↑ | h | l | L | $q_A - q_F$ |
| | H | ↑ | h | h | H | $q_A - q_F$ |

- (1) H = High voltage level.
h = High voltage level one set-up time prior to the low-to-high clock transition.
l = Low voltage level one set-up time prior to the low-to-high clock transition.
L = Low voltage level.
X = Don't care.
↑ = Transition from low to high level.
 q_n = Lower case letters indicate the state of the reference input clock transition.

7 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating, located in the [Recommended Operating Conditions](#). Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. TI recommends a $0.1\mu\text{F}$ capacitor for this device. Paralleling multiple bypass caps is acceptable to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for better results.

8 Layout

8.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not be left floating. In many cases, functions of digital logic devices, or parts of functions, are unused. For example, when a triple-input AND gate only uses two inputs or the buffer gates only use three of the four buffers. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2022) to Revision E (March 2024) Page

- Updated the functional block diagram image..... 1

Changes from Revision C (August 2003) to Revision D (March 2022) Page

- Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect current data sheet standards..... 1
- Updated naming conventions to reflect modern TI function. DS1 is now A; DS2 is now B; Q₀ is now Q_A; Q₁ is now Q_B; Q₂ is now Q_C; Q₃ is now Q_D; CP is now CLK; \overline{MR} is now \overline{CLR} ; Q₄ is now Q_E; Q₅ is now Q_F; Q₆ is now Q_G; Q₇ is now Q_H 3

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|---------------------------------|-------------------------|
| 5962-8970401CA | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8970401CA CD54HCT164F3A | Samples |
| CD54HC164F | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54HC164F | Samples |
| CD54HC164F3A | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8416201CA CD54HC164F3A | Samples |
| CD54HCT164F3A | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8970401CA CD54HCT164F3A | Samples |
| CD74HC164E | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC164E | Samples |
| CD74HC164M96 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC164M | Samples |
| CD74HC164M96G4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC164M | Samples |
| CD74HCT164E | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT164E | Samples |
| CD74HCT164M96 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -55 to 125 | (HCT164, HCT164M) | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC164, CD54HCT164, CD74HC164, CD74HCT164 :

- Catalog : [CD74HC164](#), [CD74HCT164](#)
- Military : [CD54HC164](#), [CD54HCT164](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC164M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT164M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.6 | 9.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT164M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT164M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC164M96 | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| CD74HCT164M96 | SOIC | D | 14 | 2500 | 366.0 | 364.0 | 50.0 |
| CD74HCT164M96 | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| CD74HCT164M96 | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC164E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC164E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT164E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT164E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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