THE DATASHEET OF

CDCM1802RGTR

CDCM1802 Clock Buffer With Programmable Divider, LVPECL I/O + Additional LVCMOS Output

1 Features

- Distributes One Differential Clock Input to One LVPECL Differential Clock Output and One LVCMOS Single-Ended Output
- Programmable Output Divider for Both LVPECL and LVCMOS Outputs
- 1.6-ns Output Skew Between LVCMOS and LVPECL Transitions Minimizing Noise
- 3.3-V Power Supply (2.5-V Functional)
- Signaling Rate Up to 800-MHz LVPECL and 200-MHz LVCMOS
- Differential Input Stage for Wide Common-Mode Range Also Provides VBB Bias Voltage Output for Single-Ended Input Signals
- Receiver Input Threshold ±75 mV
- 16-Pin VQFN Package (3.00 mm × 3.00 mm)

2 Applications

- Networking and Data Communications
- Medical Imaging
- Portable Test and Measurement
- High-end A/V

3 Description

The CDCM1802 clock driver distributes one pair of differential clock input to one LVPECL differential clock output pair, Y0 and $\overline{Y0}$, and one single-ended LVCMOS output, Y1. It is specifically designed for driving 50-Ω transmission lines. The LVCMOS output is delayed by 1.6 ns over the PECL output stage to minimize noise impact during signal transitions.

The CDCM1802 has two control pins, S0 and S1, to select different output mode settings. The S[1:0] pins are 3-level inputs. Additionally, an enable pin EN is provided to disable or enable all outputs simultaneously. The CDCM1802 is characterized for operation from −40°C to 85°C.

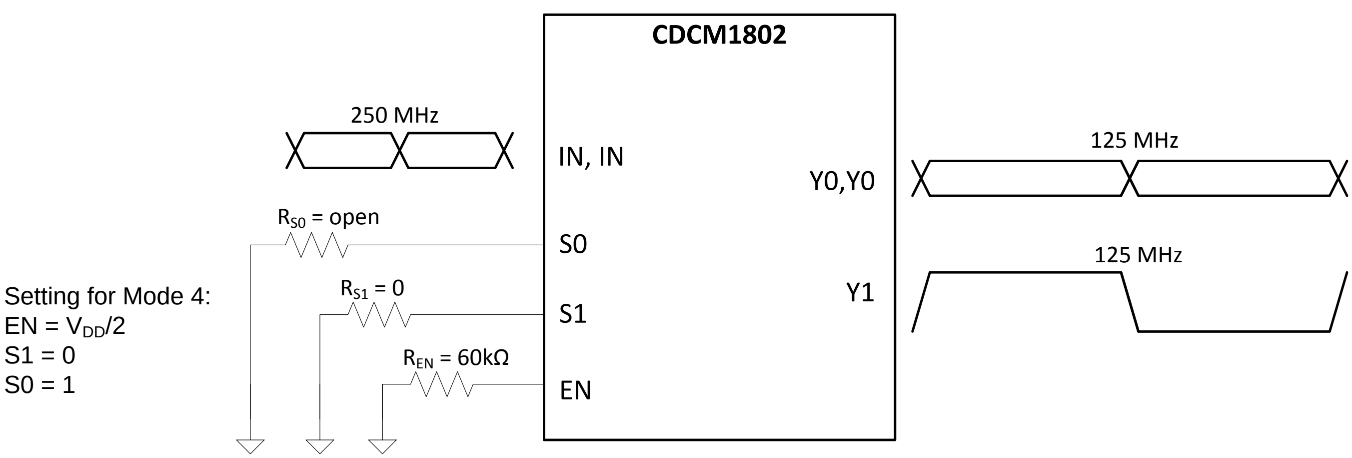
For single-ended driver applications, the CDCM1802 provides a VBB output pin that can be directly connected to the unused input as a common-mode voltage reference.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCM1802	VQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Example



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2015) to Revision C — **Page**

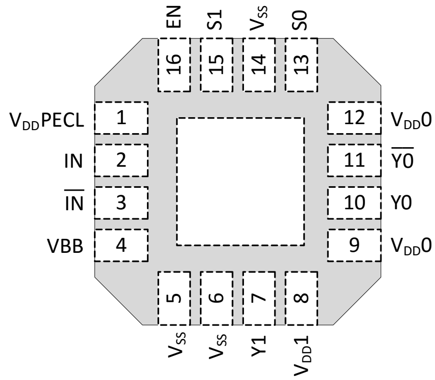
- Changed pin names for pins 3 and 11 from: IN and Y0 to: $\overline{\text{IN}}$ and $\overline{\text{Y0}}$. 3
- Removed duplicate thermal information line from *Layout Guidelines*. 19

Changes from Revision A (July 2008) to Revision B — **Page**

- Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

5 Pin Configuration and Functions

RGT Package
16-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	16	I (with 60-kΩ pullup)	ENABLE. Enables or disables all outputs simultaneously; The EN pin offers three different configurations: tie to GND (logic 0), external 60-kΩ pulldown resistor (pull to V_{DD}/2) or left floating (logic 1); EN = 1: outputs on according to S0 and S1 setting EN = V_{DD}/2: outputs on according to S0 and S1 setting EN = 0; outputs Y[1:0] off (high-impedance); see Table 1 for details.
IN	2	I Differential input	Differential input clock. Input stage is sensitive and has a wide common mode range. Therefore, almost any type of differential signal can drive this input (LVPECL, LVDS, CML, HSTL). Since the input is high-impedance, it is recommended to terminate the PCB transmission line before the input (for example, with 100-Ω across input). The input can also be driven by a single-ended signal, if the complementary input is tied to a dc reference voltage (for example, V_{CC}/2). The inputs deploy an ESD structure protecting the inputs in case of an input voltage exceeding the rails by more than ≈0.7 V. Reverse biasing of the IC through this inputs is possible and must be prevented by limiting the input voltage < VDD.
$\overline{IN}$	3		
S0	13	I	Select mode of operation. Defines the output configuration of Y0 and Y1. Each pin offers three different configurations: tied to GND (logic 0), external 60-kΩ pulldown resistor (pull to V_{DD}/2) or left floating (logic 1); see Table 1 for details.
S1	15	I (with 60-kΩ pullup)	
Y1	7	O	LVCMOS clock output. This output provides a copy of IN or a divided down copy of clock IN based on the selected mode of operation: S0, S1, and EN. Also, this output can be disabled by tying V_{DD}1 to GND.
Y0	10	O LVPECL	LVPECL clock output. This output provides a copy of IN or a divided down copy of clock IN based on the selected mode of operation: S1, S0, and EN. If Y0 output is unused, the output can simply be left open to save power and minimize noise impact to Y1.
$\overline{Y0}$	11		
VBB	4	O	Output bias voltage used to bias unused complementary input $\overline{IN}$ for single-ended input signals. The output voltage of VBB is V_{DD} −1.3 V. When driving a load, the output current drive is limited to about 1.5 mA.
V_{DD}PECL(1)	1	Supply	Supply voltage PECL input + internal logic
V_{DD}0(1)	9, 12	Supply	PECL output supply voltage for output Y0; Y0 can be disabled by pulling V_{DD}0 to GND. **Caution:** In this mode no voltage from outside may be forced because internal diodes could be forced in a forward direction. Thus, it is recommended to leave the output disconnected.
V_{DD}1	8	Supply	Supply voltage CMOS output; The CMOS output can be disabled by pulling V_{DD}1 to GND. Caution: In this mode no voltage from outside may be forced, because internal diodes could be forced in forward direction. Thus, it is recommended to leave Y1 unconnected, tied to GND, or terminated into GND.
V_{SS}	5, 6, 14	Supply	Device ground

(1) V_{DD}0, V_{DD}1, and V_{DD}PECL should have the same value.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.3	3.8	V
V_I	Input voltage	–0.2	(V_{DD} + 0.2)	V
V_O	Output voltage	–0.2	(V_{DD} + 0.2)	V
Yn, $\overline{Yn}$, I_{OSD}	Differential short circuit current	Continuous		
T_J	Maximum junction temperature	125	125	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{DD}	Supply voltage (only functionality)	2.375		3.6	V
T_A	Operating free-air temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC [1]		CDCM1802 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVPECL INPUT IN, $\overline{IN}$						
f_{clk}	Input frequency		0		800	MHz
V_{CM}	High-level input common mode		1		V_{DD} − 0.3	V
V_{IN}	Input voltage swing between IN and $\overline{IN}$	See (1)	500		1300	mV
		See (2)	150		1300	
I_{IN}	Input current	V_I = V_{DD} or 0 V			±10	µA
R_{IN}	Input impedance		300			kΩ
C_I	Input capacitance at IN, $\overline{IN}$			1		pF
LVPECL OUTPUT DRIVER Y0, $\overline{Y0}$						
f_{clk}	Output frequency (see Figure 3)		0		800	MHz
V_{OH}	High-level output voltage	Termination with 50 Ω to V_{DD} − 2 V	V_{DD} − 1.18		V_{DD} – 0.81	V
V_{OL}	Low-level output voltage	Termination with 50 Ω to V_{DD} − 2 V	V_{DD} − 1.98		V_{DD} – 1.55	V
V_O	Output voltage swing between Y and $\overline{Y}$ (see Figure 3)	Termination with 50 Ω to V_{DD} − 2 V	500			mV
I_{OZL}	Output 3-state	V_{DD} = 3.6 V, V_O = 0 V			5	µA
I_{OZH}		V_{DD} = 3.6 V, V_O = V_{DD} – 0.8 V			10	µA
C_O	Output capacitance	V_O = V_{DD} or GND		1		pF
LOAD	Expected output load			50		Ω
LVCMOS OUTPUT PARAMETER, Y1						
f_{clk}	Output frequency(3) (see Figure 4)		0		200	MHz
V_{OH}	High-level output voltage	V_{DD} = min to max, I_{OH} = −100 µA	V_{DD} – 0.1			V
		V_{DD} = 3 V, I_{OH} = −6 mA	2.4			
		V_{DD} = 3 V, I_{OH} = −12 mA	2			
V_{OL}	Low-level output voltage	V_{DD} = min to max, I_{OL} = 100 µA			0.1	V
		V_{DD} = 3 V, I_{OL} = 6 mA			0.5	
		V_{DD} = 3 V, I_{OL} = 12 mA			0.8	
I_{OH}	High-level output current	V_{DD} = 3.3 V, V_O = 1.65 V		−29		mA
I_{OL}	Low-level output current	V_{DD} = 3.3 V, V_O = 1.65 V		37		mA
I_{OZ}	High-impedance state output current	V_{DD} = 3.6 V, V_O = V_{DD} or 0 V			±5	µA
C_O	Output capacitance	V_{DD} = 3.3 V		2		pF
Load	Expected output loading (see Figure 9)			10		pF

(1) Required to maintain AC specifications
(2) Required to maintain device functionality
(3) Operating the CDCM1802 LVCMOS output above the maximum frequency will not cause a malfunction to the device, but the Y1 output signal swing will not achieve enough signal swing to meet the output specification. Therefore, the CDCM1802 can be operated at higher frequencies, while the LVCMOS output Y1 becomes unusable.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVPECL OUTPUT DRIVER Y0, $\overline{Y0}$						
t_{Duty}	Output duty cycle distortion (1)	Crossing point-to-crossing point distortion	−50		50	ps
$t_{sk(pp)}$	Part-to-part skew	Any Y0 (see Note A in Figure 7)		50		ps
t_r/t_f	Rise and fall time	20% to 80% of V_{OUTPP} (see Figure 8)	200		350	ps
LVPECL INPUT-TO-LVPECL OUTPUT PARAMETER						
$t_{pd(lh)}$	Propagation delay rising edge	VOX to VOX	320		600	ps
$t_{pd(hl)}$	Propagation delay falling edge	VOX to VOX	320		600	ps
$t_{sk(p)}$	LVPECL pulse skew (see Note B in Figure 7)	VOX to VOX			100	ps
LVCMOS OUTPUT PARAMETER, Y1						
$t_{skLVCMOS(o)}$	Output skew between the LVCMOS output Y1 and LVPECL output Y0	VOX to V_{DD} / 2 (see Figure 7)		1.6		ns
t_{Duty}	Output duty cycle distortion (2)	Measured at V_{DD} / 2	−150		150	ps
$t_{sk(pp)}$	Part-to-part skew	Y1 (see Note A in Figure 7)		300		ps
$t_{pd(lh)}$	Propagation delay rising edge from IN to Y1	VOX to V_{DD} / 2 load (see Figure 9)	1.6		2.6	ns
$t_{pd(hl)}$	Propagation delay falling edge from IN to Y1	VOX to V_{DD} / 2 load (see Figure 9)	1.6		2.6	ns
t_r	Output rise slew rate	20% to 80% of swing (see Figure 9)	1.4	2.3		V/ns
t_f	Output fall slew rate	80% to 20% of swing (see Figure 9)	1.4	2.3		V/ns

(1) For a 800-MHz signal, the 50-ps error would result into a duty cycle distortion of ±4% when driven by an ideal clock input signal.
(2) For a 200-MHz signal, the 150-ps error would result in a duty cycle distortion of ±3% when driven by an ideal clock input signal.

6.7 Jitter Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{jitterLVPECL}$	Additive phase jitter from input to LVPECL output Y0 (see Figure 1)	12 kHz to 20 MHz, f_{out} = 250 MHz to 800 MHz, divide by 1 mode			0.15	ps rms
		50 kHz to 40 MHz, f_{out} = 250 MHz to 800 MHz, divide by 1 mode			0.25	ps rms
$t_{jitterLVCMOS}$	Additive phase jitter from input to LVCMOS output Y1 (see Figure 2)	12 kHz to 20 MHz, f_{out} = 250 MHz, divide by 1 mode			0.25	ps rms
		50 kHz to 40 MHz, f_{out} = 250 MHz, divide by 1 mode			0.4	ps rms

6.8 Supply Current Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	Full load	All outputs enabled and terminated with 50 Ω to V_{DD} − 2 V on LVPECL outputs and 10 pF on LVCMOS output, f = 800 MHz for LVPECL outputs and 200 MHz for LVCMOS, V_{DD} = 3.3 V		100		mA
		No load	Outputs enabled, no output load, f = 800 MHz for LVPECL outputs and 200 MHz for LVCMOS, V_{DD} = 3.6 V			85	mA
I_{DDZ}	Supply current, 3-state		All outputs 3-state by control logic, f = 0 Hz, V_{DD} = 3.6 V			0.5	mA

6.9 Control Input Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rpullup	Internal pullup resistor on S0, S1, and EN input		42	60	78	kΩ
$V_{IH(H)}$	Three level input high, S0, S1, and EN pin (1)		$0.9 \times V_{DD}$			V
$V_{IM(M)}$	Three level input MID, S0, S1, and EN pin		$0.3 \times V_{DD}$		$0.7 \times V_{DD}$	V
$V_{IL(L)}$	Three level low, S0, S1, and EN pin				$0.1 \times V_{DD}$	V
I_{IH}	Input current, S0, S1, and EN pin	$V_I = V_{DD}$			–5	µA
I_{IL}	Input current, S0, S1, and EN pin	V_I = GND	38		85	µA

(1) Leaving this pin floating automatically pulse the logic level high to V_{DD} through an internal pullup resistor of 60 kΩ.

6.10 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{su}	Setup time, S0, S1, and EN pin before clock IN	25			ns
t_h	Hold time, S0, S1, and EN pin after clock IN	0			ns
$t_{(disable)}$	Time between latching the EN low transition and when all outputs are disabled (how much time is required until the outputs turn off)		10		ns
$t_{(enable)}$	Time between latching the EN low-to-high transition and when outputs are enabled based on control settings (how much time passes before the outputs carry valid signals)		1		µs

6.11 Bias Voltage VBB

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBB	Output reference voltage	V_{DD} = 3 V–3.6 V, I_{BB} = –0.2 mA	V_{DD} – 1.4		V_{DD} – 1.2	V

6.12 Typical Characteristics

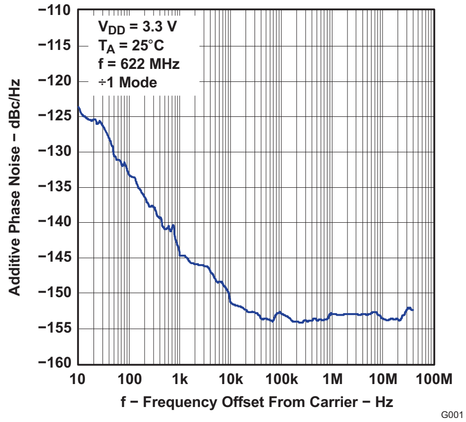


Figure 1. Additive Phase Noise vs Frequency Offset From Carrier − LVPECL

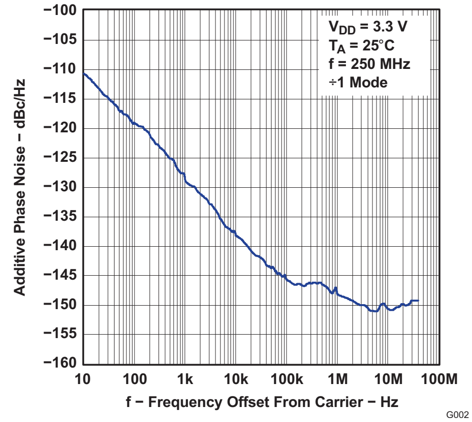


Figure 2. Additive Phase Noise vs Frequency Offset From Carrier − LVCMOS

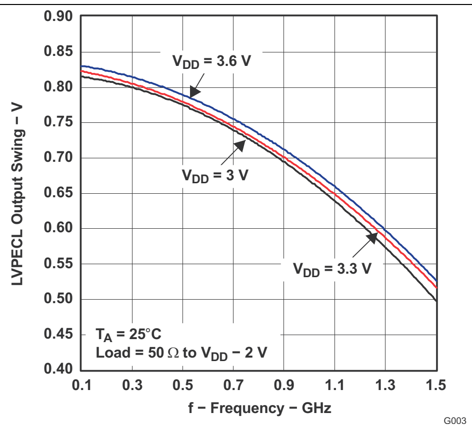


Figure 3. Amplitude PECL Peak-to-Peak vs Frequency

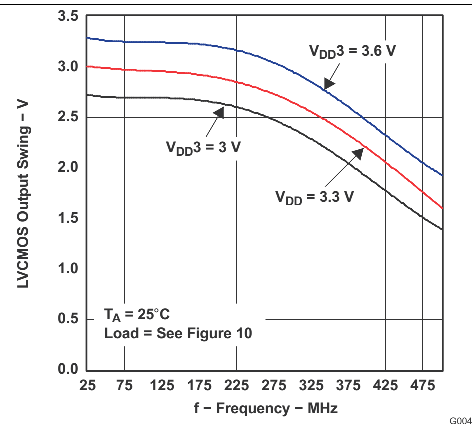


Figure 4. Amplitude CMOS Peak-to-Peak vs Frequency

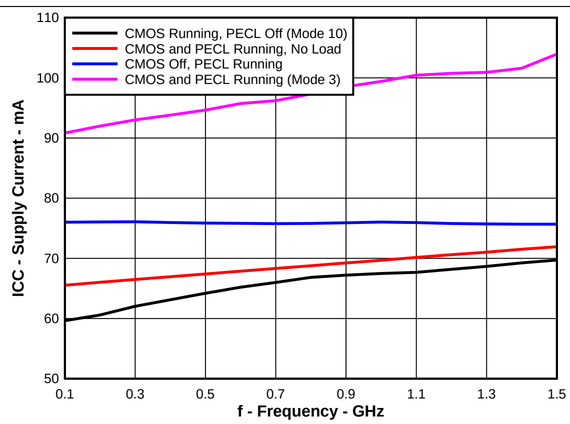


Figure 5. Supply current vs Frequency

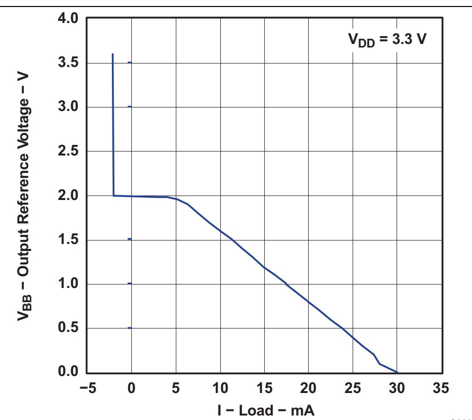
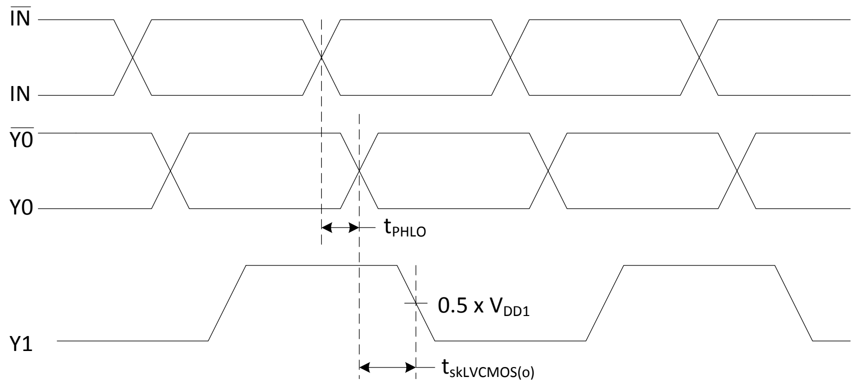


Figure 6. Output Reference Voltage (V_{BB}) vs Load

7 Parameter Measurement Information



A. Part-to-part skew, $t_{sk(pp)}$, is calculated as the greater of:
   − The difference between the fastest and the slowest $t_{pd(LH)n}$ across multiple devices
   − The difference between the fastest and the slowest $t_{pd(HL)n}$ across multiple devices

B. Pulse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low ($t_{pd(HL)}$ and the low-to-high ($t_{pd(LH)}$) propagation delays when a single switching input causes Y0 to switch, $t_{sk(p)}$ = | $t_{pd(HL)}$ − $t_{pd(LH)}$ |. Pulse skew is sometimes referred to as *pulse width distortion or duty cycle skew*.

Figure 7. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pp)}$

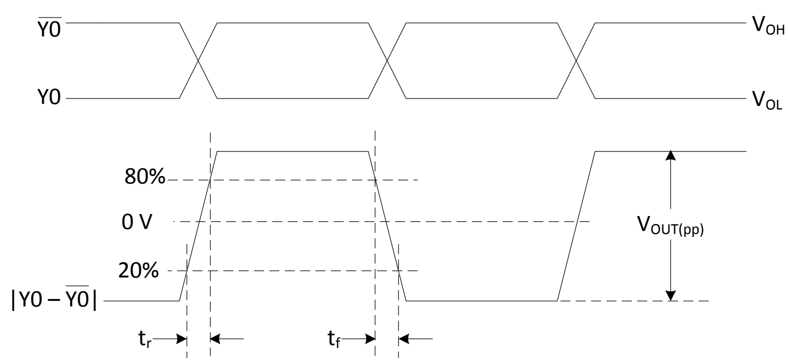


Figure 8. LVPECL Differential Output Voltage and Rise and Fall Time

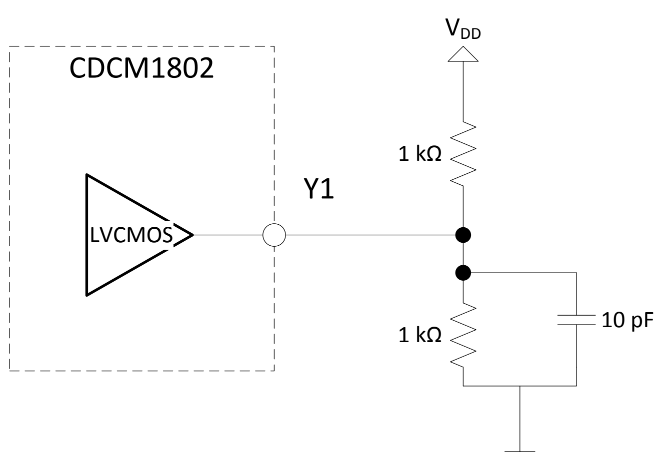


Figure 9. LVCMOS Output Loading During Device Test

Parameter Measurement Information (continued)

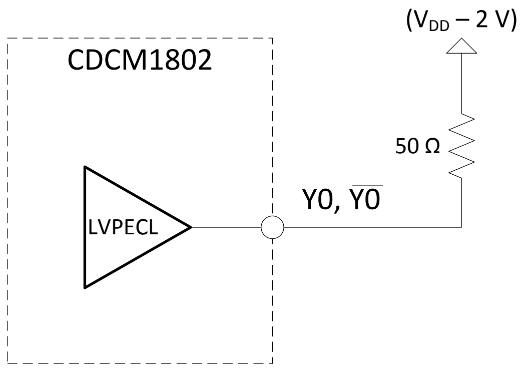


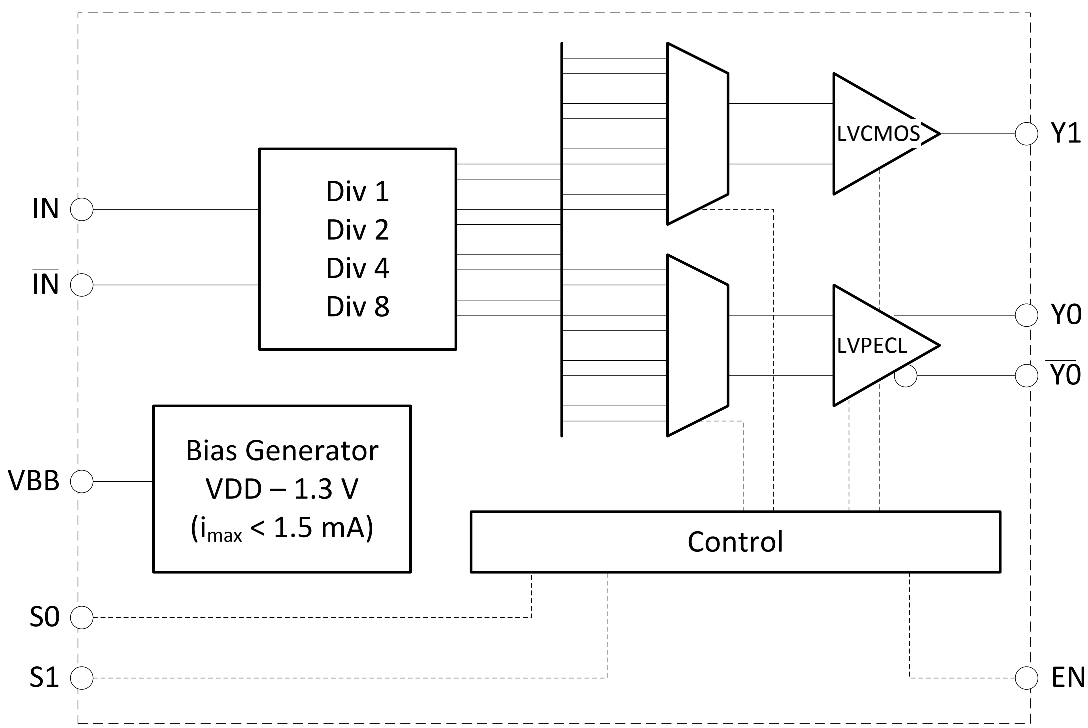
Figure 10. LVPECL Output Loading During Device Test

8 Detailed Description

8.1 Overview

The CDCM1802 is a clock buffer with a programmable divider. There is one LVCMOS and one LVPECL output. The LVCMOS output is specifically designed for driving 50-Ω transmission lines. It is delayed by 1.6 ns over the PECL output stage to minimize noise impact during signal transitions. Both outputs can be divided individually by 1, 2, 4, and 8. Divider settings can be selected with three 3-level control pins.

8.2 Functional Block Diagram



8.3 Feature Description

The CDCM1802 has two control pins, S0 and S1, to select different output mode settings. The S[1:0] pins are 3-level inputs. Additionally, an enable pin EN is provided to disable or enable all outputs simultaneously. For single-ended driver applications, the CDCM1802 provides a VBB output pin that can be directly connected to the unused input as a common-mode voltage reference.

8.4 Device Functional Modes

8.4.1 Control Pin Settings

The CDCM1802 has three control pins, S0, S1, and the enable pin (EN) to select different output mode settings. All three inputs (S0, S1, EN) are 3-level inputs. In addition, the EN input allows disabling all outputs and place them into a Hi-Z (or tristate) output state when pulled to GND.

Device Functional Modes (continued)

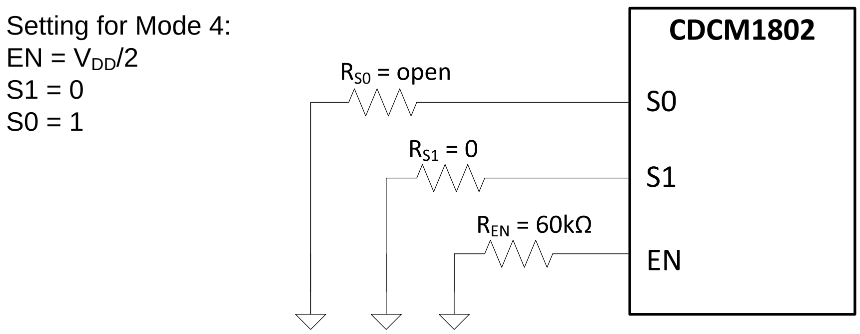


Figure 11. Control Pin Setting for Example

Each control input incorporates a 60-kΩ pullup resistor. Thus, it is easy to choose the input setting by designing a resistor pad between the control input and GND. To choose a logic zero, the resistor value must be zero. Setting the input high requires leaving the resistor pad empty (no resistor installed). For setting the input to $V_{DD}/2$, the installed resistor needs a value of 60 kΩ with a tolerance better or equal to 10%.

Table 1. Selection Mode Table

MODE	EN	S1	S0	LVPECL (1)	LVCMOS
				Y0	Y1
0	0	X	X	Off (high-z)	Off (high-z)
1	$V_{DD}/2$	0	$V_{DD}/2$	/1	/1
2	$V_{DD}/2$	$V_{DD}/2$	1	/1	/2
3	1	0	0	/1	/4
4	$V_{DD}/2$	0	1	/2	/2
5	1	0	1	/2	/4
6	$V_{DD}/2$	0	0	/4	/4
7	$V_{DD}/2$	1	0	/4	/8
8	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	/8	/1
9	1	1	0	/8	/4
10	1	1	1	Off (high-z)	/4

(1) The LVPECL outputs are open emitter stages. Thus, if you leave the unused LVPECL output Y0 unconnected, then the current consumption is minimized and noise impact to remaining outputs is neglectable. Also, each output can be individually disabled by connecting the corresponding VDD input to GND.

8.4.2 Device Behavior During RESET and Control Pin Switching

8.4.2.1 Output Behavior When Enabling the Device (EN = 0 → 1)

In disable mode (EN = 0), all output drivers are switched in high-Z mode. The bandgap, current references, the amplifier, and the S0 and S1 control inputs are also switched off. In the same mode, all flip-flops will be reset. The typical current consumption is likely below 500 µA (to be measured).

When the device will be enabled again it takes maximal 1 µs for the settling of the reference voltage and currents. During this time the output Y0 and $\overline{Y0}$ drive a high signal. Y1 is unknown (could be high or low). After the settle time, the outputs go into the low state. Due to the synchronization of each output driver signal with the input clock, the state of the waveforms after enabling the device look like those shown in Figure 12. The inverting input and output signal is not included. The Y:/1 waveform is the undivided output driver state.

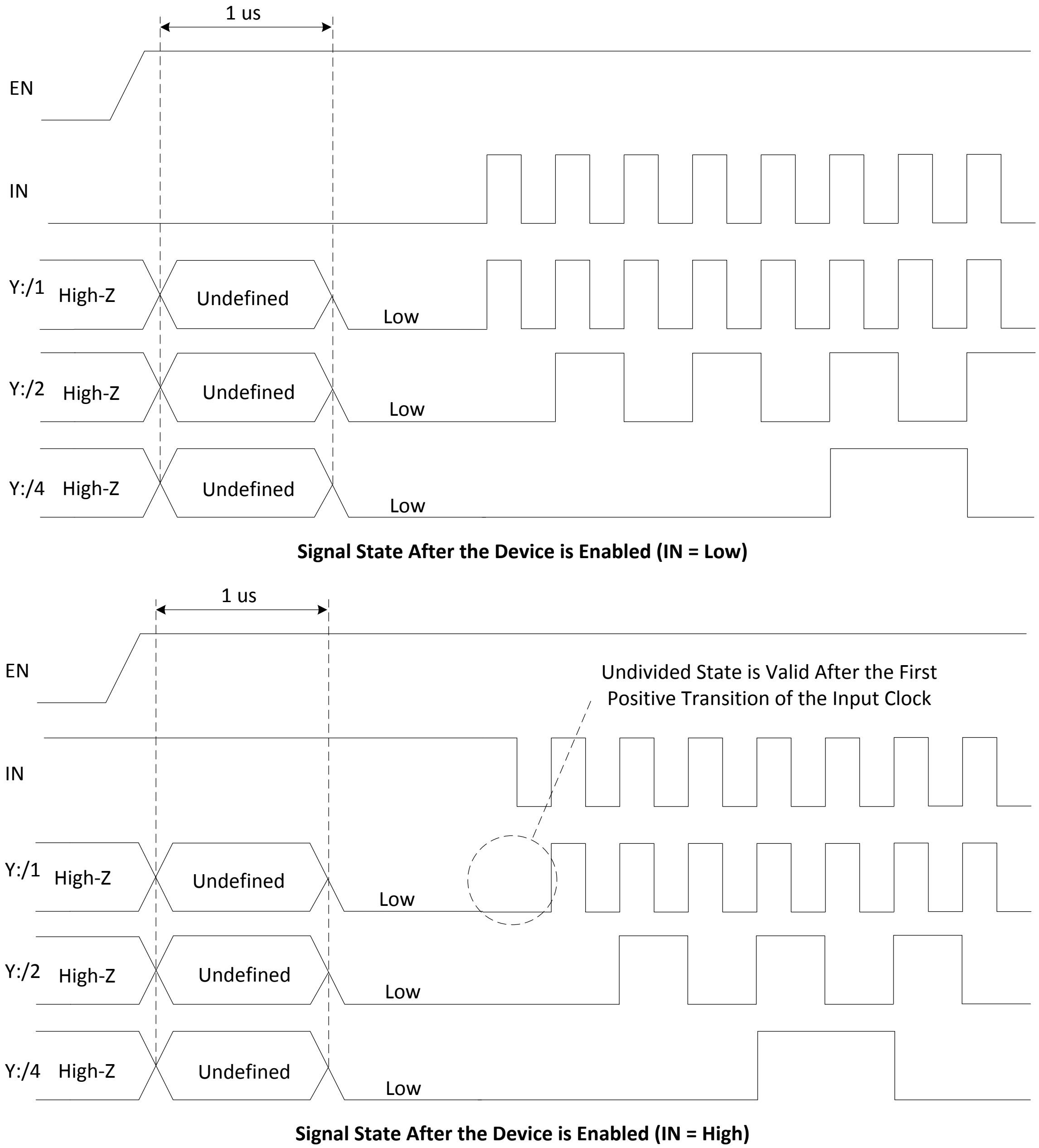


Figure 12. Waveforms

8.4.2.2 Enabling a Single Output Stage

If a single output stage becomes enabled:

- Y0 will either be low or high (undefined).
- $\overline{\text{Y0}}$ will be the inverted signal of Y0.

With the first positive clock transition, the undivided output becomes the input clock state. If a divide mode is used, the divided output states are equal to the actual internal divider. The internal divider does not get a reset while enabling single output drivers.

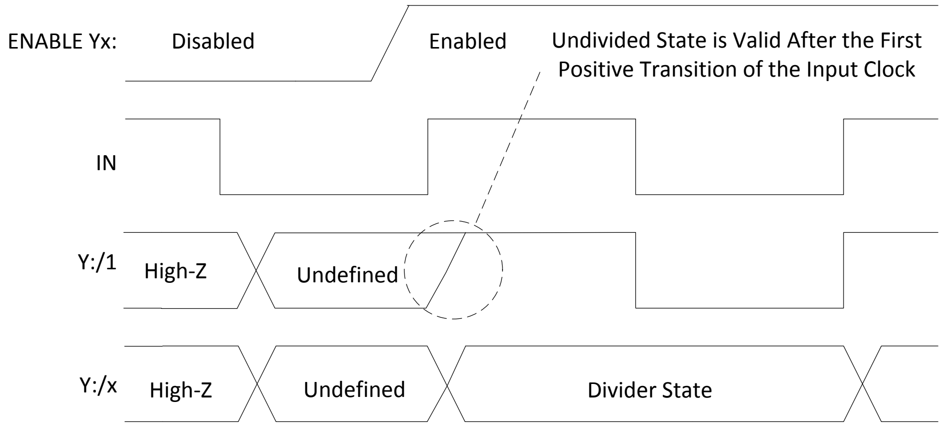


Figure 13. Signal State After an Output Driver Becomes Enabled While IN = 0

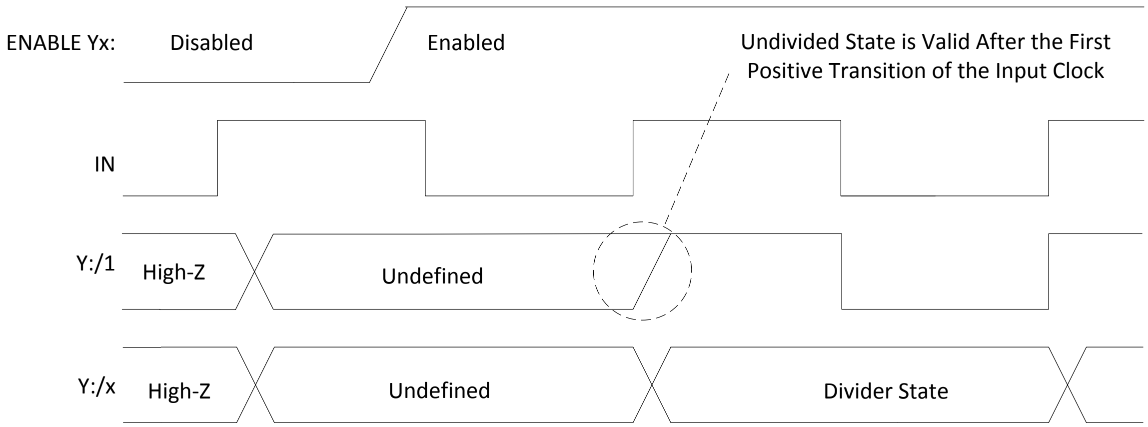


Figure 14. Signal State After an Output Driver Becomes Enabled While IN = 1

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 LVPECL Receiver Input Termination

The input of the CDCM1802 has high impedance and comes with a very large common mode voltage range. For optimized noise performance it is recommended to properly terminate the PCB trace (transmission line).

Additional termination techniques can be found in the following application notes: SCAA062 and SCAA059.

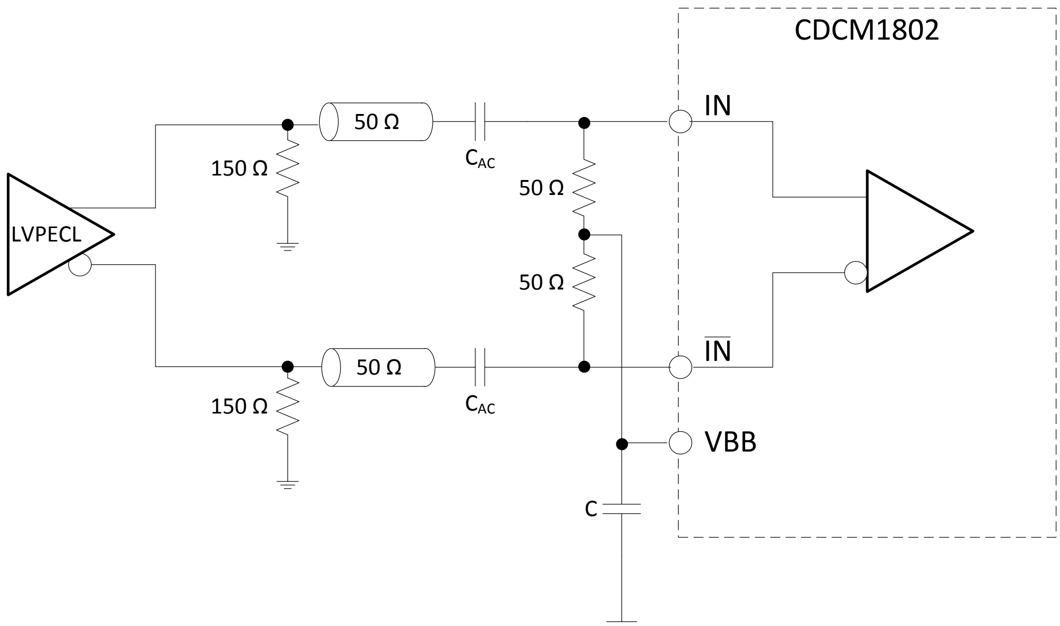


Figure 15. Recommended AC-Coupling LVPECL Receiver Input Termination

Application Information (continued)

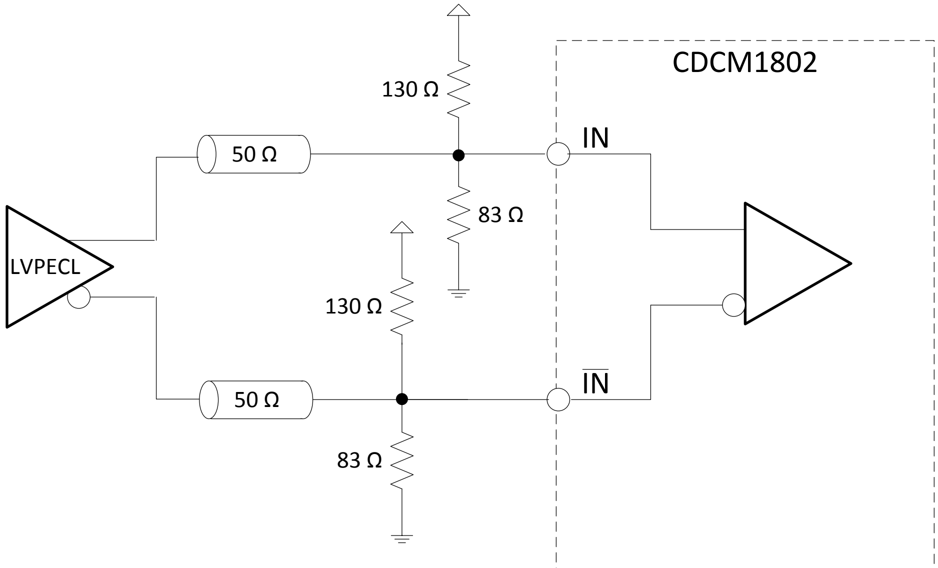
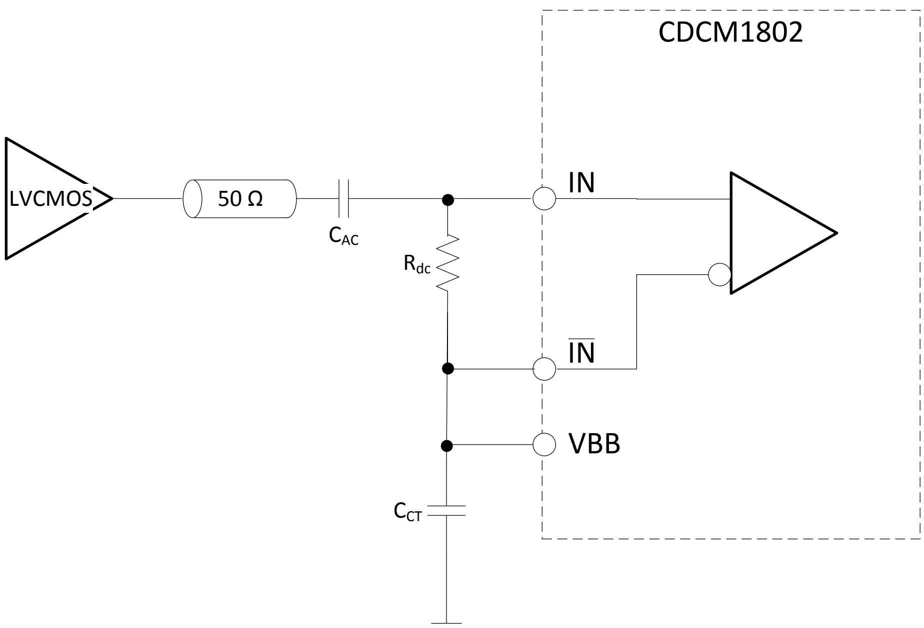


Figure 16. Recommended DC-Coupling LVPECL Receiver Input Termination

9.1.2 LVCMOS Receiver Input Termination



NOTE: C_{AC} − AC-coupling capacitor (for example, 10 nF)
C_{CT} − Capacitor keeps voltage at $\overline{\text{IN}}$ constant (for example, 10 nF)
R_{dc} − Load and correct duty cycle (for example, 50 Ω)
V_{BB} − Bias voltage output

Figure 17. Typical Application Setting for Single-Ended Input Signals Driving the CDCM1802

9.2 Typical Application

Figure 18 shows a fanout buffer application.

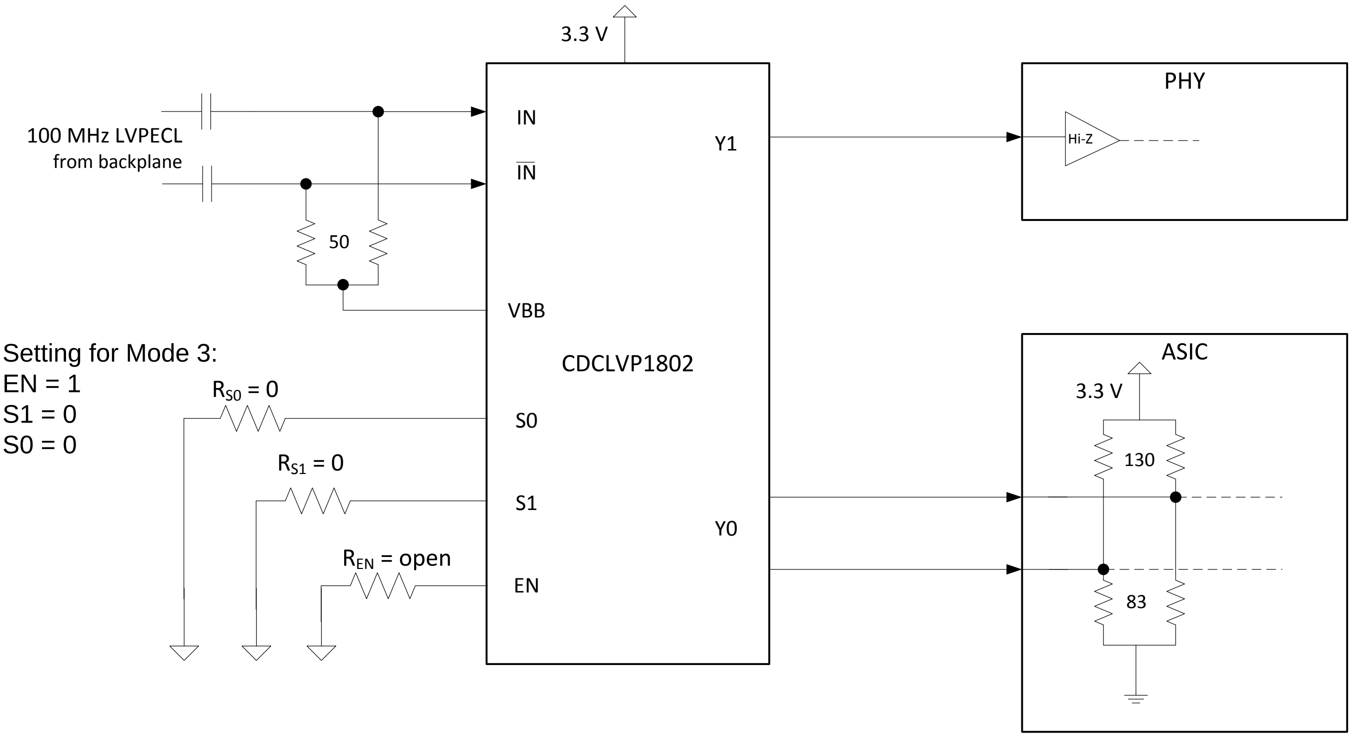


Figure 18. Typical Application Schematic, CDCM1802

9.2.1 Design Requirements

The CDCM1802 shown in Figure 18 is configured to be able to select an 100-MHz LVPECL clock from the backplane. The signal can be fanned out to desired devices, as shown. The CDCM1802 offers internal dividers for both the LVCMOS and LVPECL output. In the example the LVCMOS output is divided by 4 and the LVPECL output is divided by 1.

- The PHY device receive a single ended 25-MHz signal. Optionally a series resistance can be placed close to the output to match transmission line impedance and reduce reflections.
- The ASIC is capable of DC coupling with a 3.3-V LVPECL driver such as the CDCM1802. This ASIC features internal termination so no additional components are needed.
- S0, S1, EN needs to be set accordingly to ensure the required divider setting.

9.2.2 Detailed Design Procedure

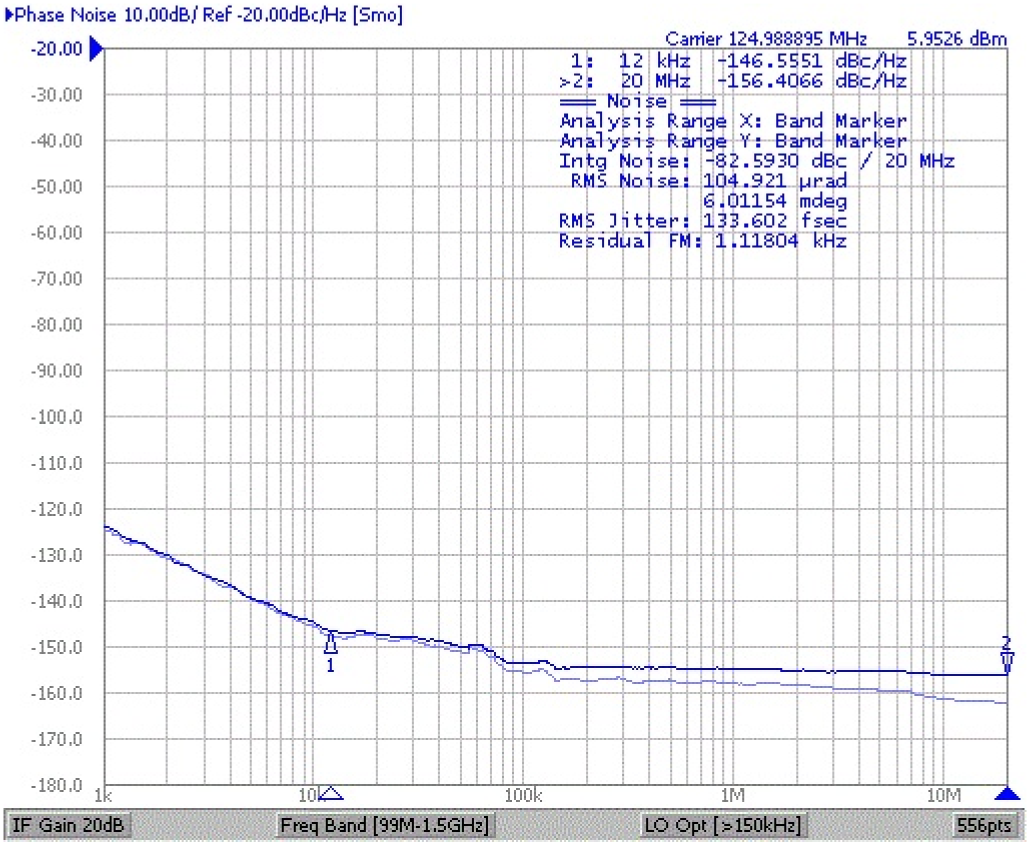
Refer to *LVPECL Receiver Input Termination* for proper input terminations, dependent on single-ended or differential inputs.

Refer to Figure 9 and Figure 10 for output termination schemes depending on the receiver application.

Refer to Table 1 for setting the desired divider modes.

Typical Application (continued)

9.2.3 Application Curve



Input (Vectron C5310A1) = 83 fs, rms   Output (LVPECL, divide 1) = 134 fs, rms
additive jitter = 105 fs, rms (typ)

Figure 19. Additive Jitter Performance

10 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is very critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and must have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply terminals and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1-µF) bypass capacitors as there are supply terminals in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 20 illustrates this recommended power-supply decoupling method.

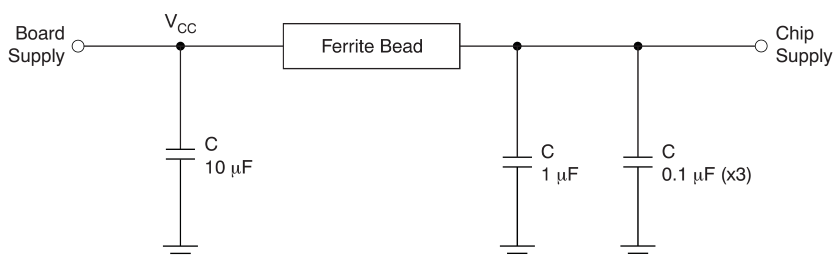


Figure 20. Power-Supply Decoupling

11 Layout

11.1 Layout Guidelines

TI recommends taking special care of the PCB design for good thermal flow from the VQFN 16-pin package to the PCB. The current consumption of the CDCM1802 is fixed. JEDEC JESD51−7 specifies thermal conductivity for standard PCB boards.

To ensure sufficient thermal flow, it is recommended to design with four thermal vias in applications.

See the SCBA017 and the SLUA271 application notes for further package-related information.

11.2 Layout Example

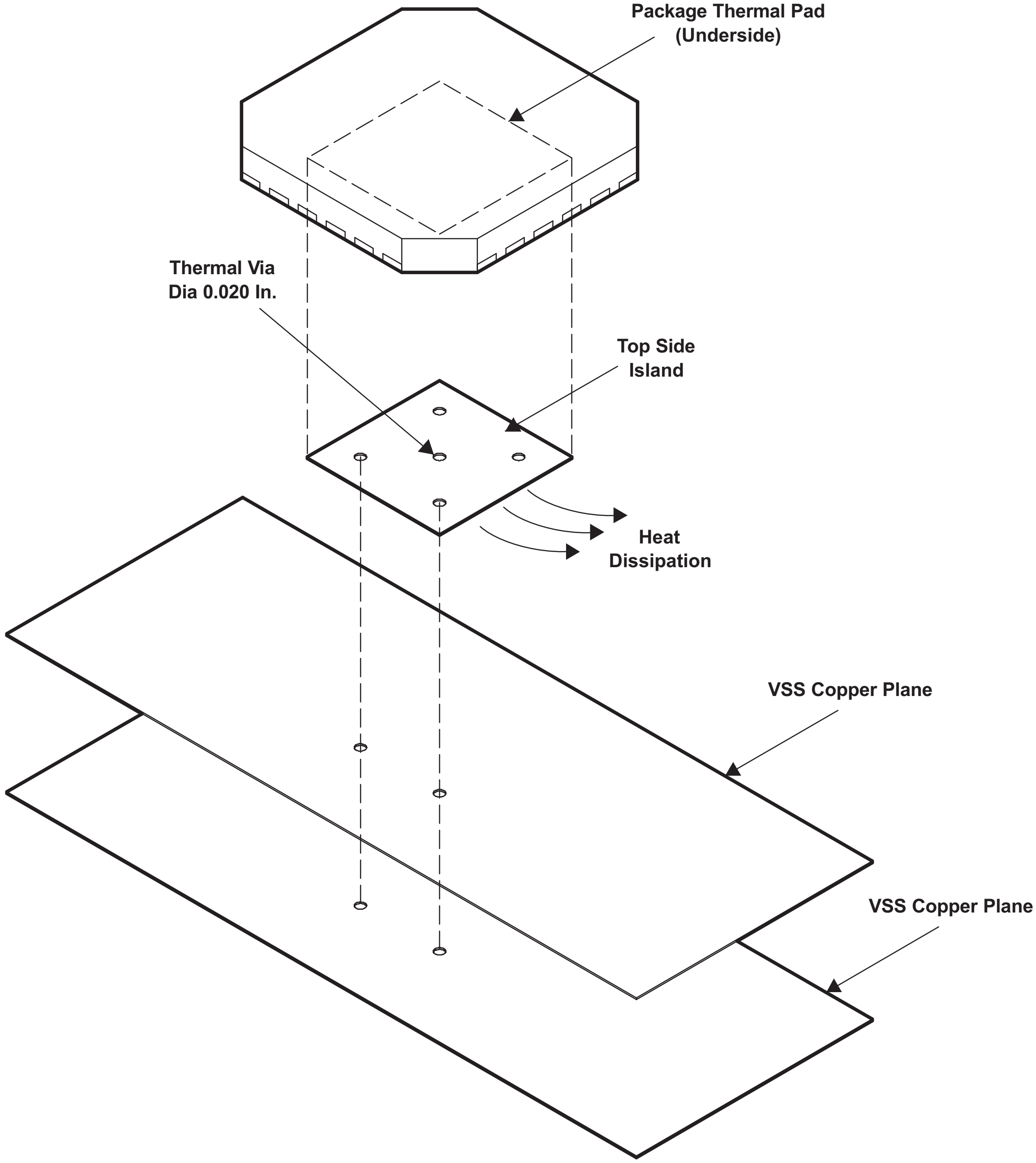


Figure 21. Recommended Thermal Via Placement

11.3 Thermal Considerations

Table 2. Package Thermal Resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	VQFN−16 package thermal resistance with thermal vias in PCB[(1)]	4-layer JEDEC test board (JESD51−7) with four thermal vias of 22-mil diameter each, airflow = 0 ft/min		48.4		°C/W

(1) It is recommended to provide four thermal vias to connect the thermal pad of the package effectively with the PCB and ensure a good heat sink.

Example:

Calculation of the junction-lead temperature with a 4-layer JEDEC test board using four thermal vias:

$T_{Chassis}$ = 85°C (temperature of the chassis)

$P_{effective} = I_{max} \times V_{max}$ = 85 mA × 3.6 V = 306 mW (max power consumption inside the package)

$\Delta T_{Junction} = R_{\theta JA} \times P_{effective}$ = 40.8°C/W × 306 mW = 12.48°C

$T_{Junction} = \Delta T_{Junction} + T_{Chassis}$ = 12.48°C + 85°C = 97.48°C (the maximum junction temperature of $T_{die-max}$ = 125°C is not violated)

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

SCAA062: *DC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML*

SCAA059: *AC-Coupling Between Differential LVPECL, LVDC, HSTL, and CML*

SCBA017: *Quad Flatpack No-Lead Logic Packages*

SLUA271: *QFN/SON PCB Attachment*

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCM1802RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AJW	Samples
CDCM1802RGTRG4	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AJW	Samples
CDCM1802RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AJW	Samples
CDCM1802RGTTG4	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AJW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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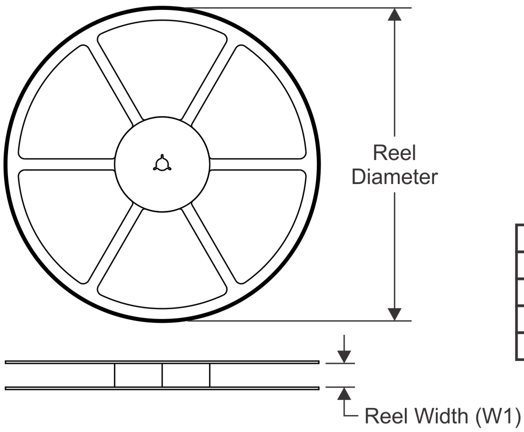
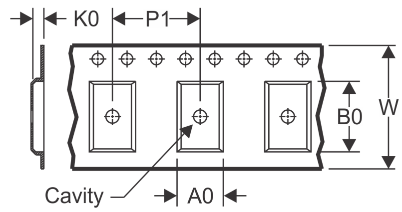
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

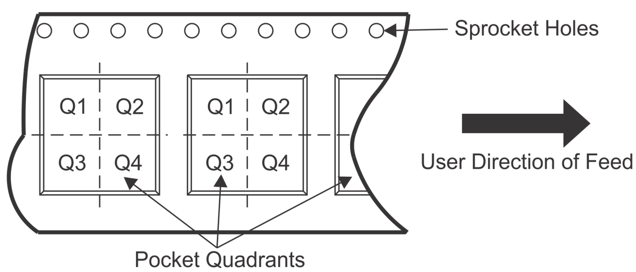


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

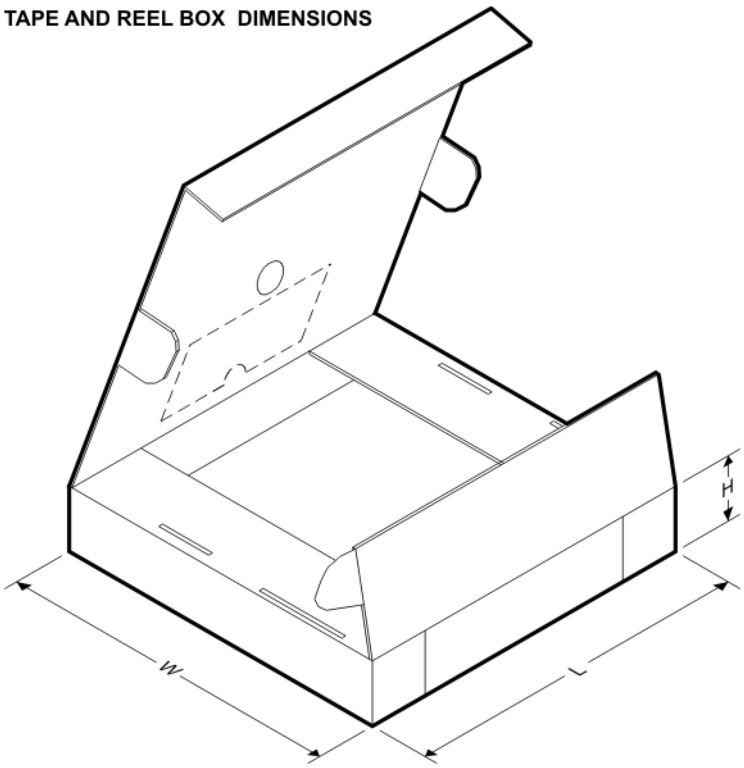
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

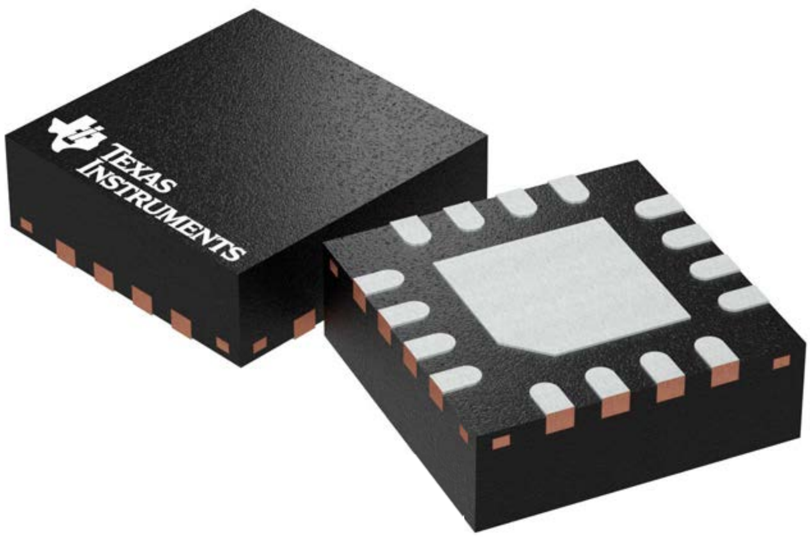
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCM1802RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
CDCM1802RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

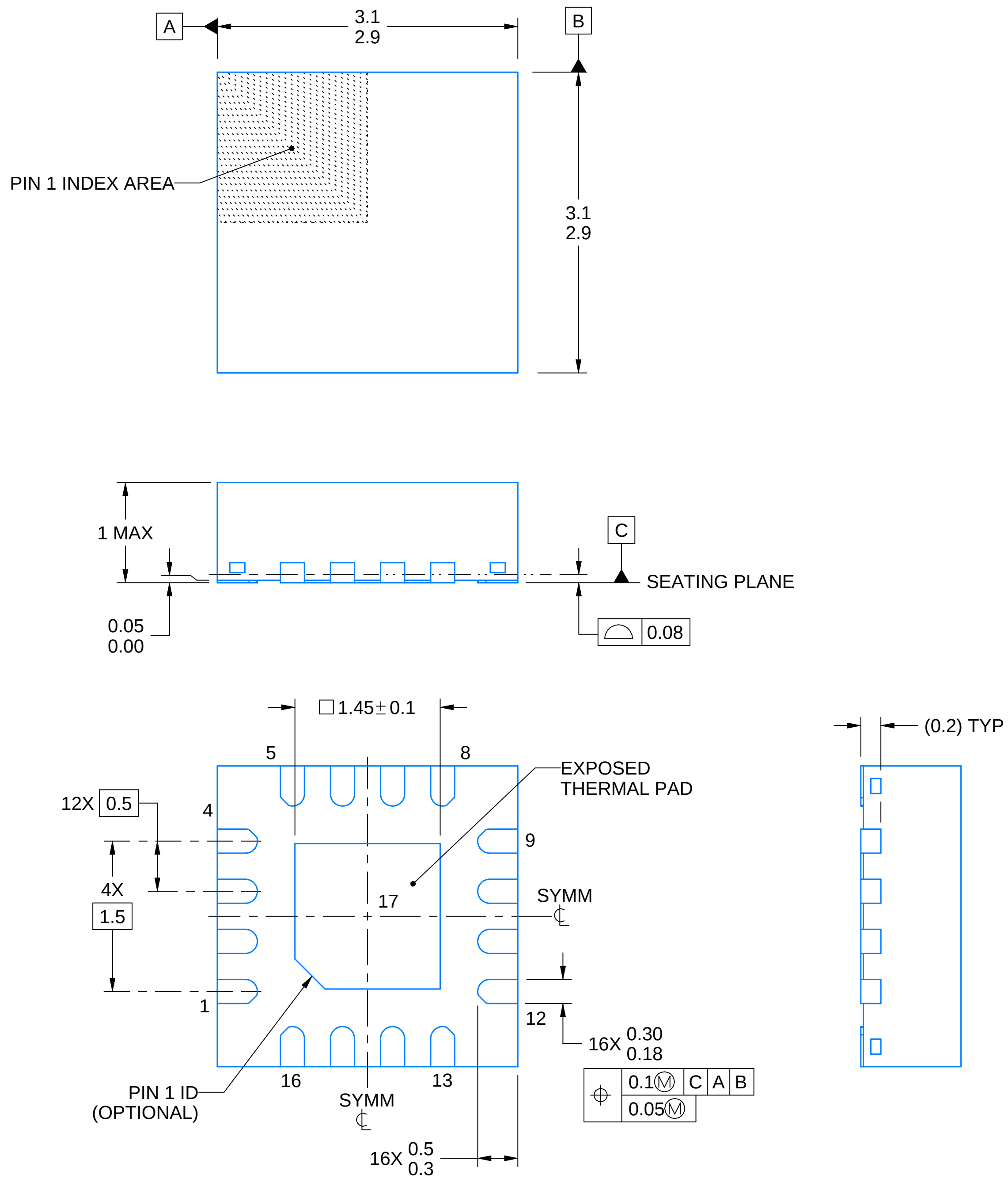


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCM1802RGTR	VQFN	RGT	16	3000	350.0	350.0	43.0
CDCM1802RGTT	VQFN	RGT	16	250	210.0	185.0	35.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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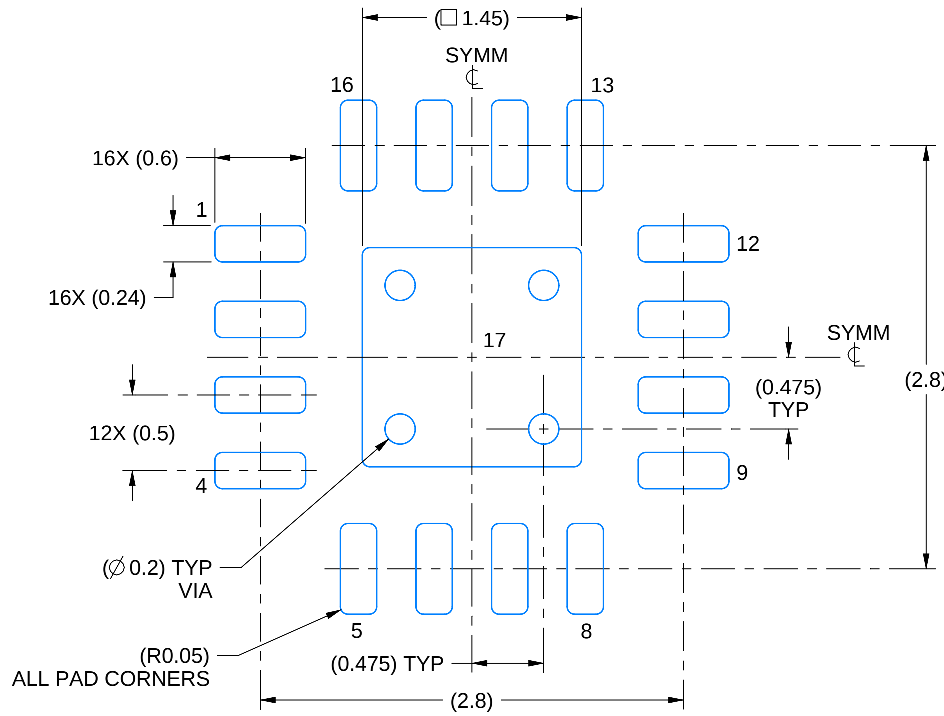
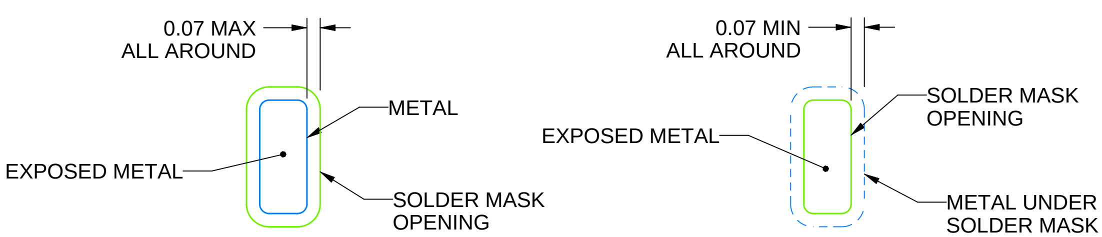
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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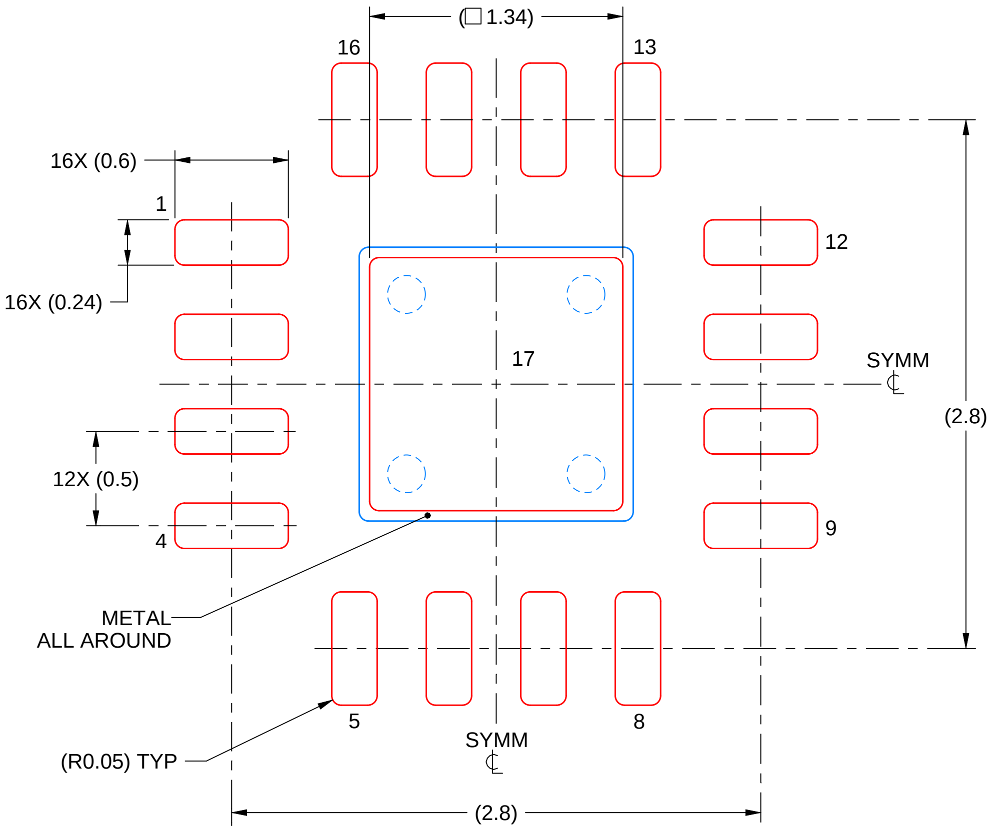
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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