THE DATASHEET OF

AMC7812SPAPR

12-Bit Analog Monitoring and Control Solution with Multichannel ADC, DACs, and Temperature Sensors

Check for Samples: AMC7812

FEATURES

- **12, 12-Bit DACs with Programmable Outputs:**
  - **0V to 5V**
  - **0V to 12.5V**
- **DAC Shutdown to User-Defined Level**
- **12-Bit, 500kSPS ADC with 16 Inputs:**
  - **16 Single-Ended or**
  - **Two Differential + 12 Single-Ended**
- **Two Remote Temperature Sensors:**
  - **–40°C to +150°C, ±2°C Accuracy**
- **One Internal Temperature Sensor:**
  - **–40°C to +125°C, ±2.5°C Accuracy**
- **Input Out-of-Range Alarms**
- **2.5V Internal Reference**
- **Eight General-Purpose Input/Outputs**
- **Configurable I²C-Compatible/ SPI™ Interface with 5V/3V Logic**
- **Power-Down Mode**
- **Wide Temperature Range:**
  - **–40°C to +105°C**
- **Small Packages: 9mm x 9mm QFN-64, and 10mm x 10mm HTQFP-64**

APPLICATIONS

- **RF Power Amplifier Control in Base Stations**
- **Test and Measurement**
- **Industrial Control**
- **General Analog Monitoring and Control**

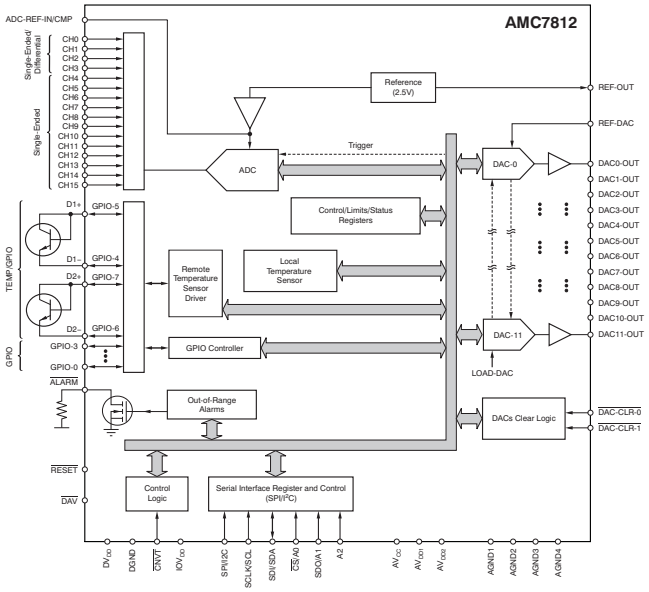
DESCRIPTION

The AMC7812 is a complete analog monitoring and control solution that includes a 16-channel, 12-bit analog-to-digital converter (ADC), twelve 12-bit digital-to-analog converters (DACs), eight GPIOs, and two remote/one local temperature sensor channels.

The AMC7812 has an internal reference of +2.5V that can configure the DAC output voltage to a range of either 0V to +5V or 0V to +12.5V. An external reference can be used as well. Typical power dissipation is 95mW. The AMC7812 is ideal for multichannel applications where board space, size, and low power are critical.

The AMC7812 is available in either a 64-lead QFN or HTQFP-64 PowerPAD™ package and is fully specified over the –40°C to +105°C temperature range.

For applications that require a different channel count, additional features, or converter resolutions, Texas Instruments offers a complete family of analog monitor and control (AMC) products. Visit http://www.ti.com/amc for more information.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
AMC7812	±1	±1	QFN-64	RGC	–40°C to +105°C	AMC7812
			HTQFP-64	PAP	–40°C to +105°C	AMC7812

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		AMC7812	UNIT
AV_{DD} to GND		–0.3 to +6	V
DV_{DD} to GND		–0.3 to +6	V
IOV_{DD} to GND		–0.3 to +6	V
AV_{CC} to GND		–0.3 to +18	V
DV_{DD} to DGND		–0.3 to +6	V
Analog input voltage to GND		–0.3 to AV_{DD} + 0.3	V
ALARM, GPIO-0, GPIO-1, GPIO-2, GPIO-3, SCLK/SCL, and SDI/SDA to GND		–0.3 to +6	V
D1+/GPIO-4, D1–/GPIO-5, D2+/GPIO-6, D2–/GPIO-7 to GND		–0.3 to AV_{DD} + 0.3	V
Digital input voltage to DGND		–0.3 to IOV_{DD} + 0.3	V
SDO and DAV to GND		–0.3 to IOV_{DD} + 0.3	V
Operating temperature range		–40 to +105	°C
Storage temperature range		–40 to +150	°C
Junction temperature range (T_J max)		+150	°C
ESD ratings	Human body model (HBM)	2.5	kV
	Charged device model (CDM)	1.0	kV

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		AMC7812		UNITS
		RGC (QFN)	PAP (HTQFP)	
		64 PINS	64 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	24.1	33.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	8.1	9.5	
θ_{JB}	Junction-to-board thermal resistance	3.2	9.0	
ψ_{JT}	Junction-to-top characterization parameter	0.1	0.3	
ψ_{JB}	Junction-to-board characterization parameter	3.3	8.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.6	0.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +105°C, AV_{DD} = DV_{DD} = 4.5V to 5.5V, AV_{CC} = +15V, AGND = DGND = 0V, IOV_{DD} = 2.7V to 5.5V, internal 2.5V reference, and the DAC output span = 0V to 5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AMC7812 MIN	AMC7812 TYP	AMC7812 MAX	UNIT
DAC PERFORMANCE						
DAC DC ACCURACY						
Resolution			12			Bits
INL	Relative accuracy	Measured by line passing through codes 020h and FFFh			±1	LSB
DNL	Differential nonlinearity	12-bit monotonic, Measured by line passing through codes 020h and FFFh		±0.3	±1	LSB
TUE	Total unadjusted error	T_A = +25°C, DAC output = 5.0V			±10	mV
		T_A = +25°C, DAC output = 12.5V			±30	mV
Offset error		T_A = +25°C, DAC output = 0V to +5V, code 020h			±2	mV
		T_A = +25°C, DAC output = 0V to +12.5V, code 020h			±5	mV
Offset error temperature coefficient				±1		ppm/°C
Gain error		External reference, output = 0V to +5V		±0.025	±0.15	%FSR
		External reference, output = 0V to +12.5V		-0.15	±0.3	%FSR
Gain temperature coefficient				±2		ppm/°C
DAC OUTPUT CHARACTERISTICS						
Output voltage range(1)		V_{REF} = 2.5V, gain = 2	0		5	V
		V_{REF} = 2.5V, gain = 5	0		12.5	V
Output voltage settling time(2)		DAC output = 0V to +5V, code 400h to C00h, to ½ LSB, from $\overline{CS}$ rising edge, R_L = 2kΩ, C_L = 200pF		3		µs
Slew rate(2)				1.5		V/µs
Short-circuit current(2)		Full-scale current shorted to ground		30		mA
Load current		Source within 200mV of supply, T_A = +25°C		+10		mA
		Sink within 300mV of supply, T_A = +25°C		-10		mA
		DAC output = 0V to +5V, code B33h. Source and/or sink with voltage drop < 25mV, T_A: -40°C to 95°C(3)	±8			mA
Capacitive load stability(2)		R_L = ∞	10			nF
DC output impedance(2)		Code 800h		0.3		Ω
Power-on overshoot		AV_{CC} 0 to 5V, 2ms ramp		5		mV
Digital-to-analog glitch energy		Code changes from 7FFh to 800h, 800h to 7FFh		0.15		nV-s
Digital feedthrough		Device is not accessed		0.15		nV-s
Output noise		T_A = +25°C, at 1kHz, code 800h, gain = 2, excludes reference		81		nV/√Hz
		f = 0.1Hz to 10Hz, excludes reference		8		μV_{PP}
DAC REFERENCE INPUT						
Reference voltage input range		REF-DAC pin	1		2.6	V
Input current(2)		V_{REF} = 2.5V		170		µA

(1) The output voltage must not be greater than AV_{CC}. See the *DAC Output* section for more details.
(2) Sampled during initial release to ensure compliance; not subject to production testing.
(3) Valid only for material manufactured on or after October 2012.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +105°C, AV_{DD} = DV_{DD} = 4.5V to 5.5V, AV_{CC} = +15V, AGND = DGND = 0V, IOV_{DD} = 2.7V to 5.5V, internal 2.5V reference, and the DAC output span = 0V to 5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AMC7812 MIN	AMC7812 TYP	AMC7812 MAX	UNIT
INTERNAL REFERENCE						
Output voltage		T_A = +25°C, REF-OUT pin	2.495	2.5	2.505	V
Output impedance				0.4		Ω
Reference temperature coefficient				10	25	ppm/°C
Output current (sourcing/sinking)				±5		mA
Output voltage noise		T_A = +25°C, f = 1kHz		260		nV/√Hz
		f = 0.1Hz to 10Hz		13		μV_{PP}
ADC PERFORMANCE						
ADC DC ACCURACY (for AV_{DD} = 5V)						
Resolution				12		Bits
INL	Integral nonlinearity			±0.5	±1	LSB
DNL	Differential nonlinearity			±0.5	±1	LSB
Single-Ended Mode						
Offset error				±1	±3	LSB
Offset error match				±0.4		LSB
Gain error		External reference		±1	±5	LSB
Gain error match				±0.4		LSB
Differential Mode						
Gain error		External reference, 0V to (2 · V_{REF}) mode, V_{CM} = 2.5V		±2	±5	LSB
		External reference, 0V to V_{REF} mode, V_{CM} = 1.25V		±1	±5	LSB
Gain error match				±0.5		LSB
Zero code error		0V to (2 · V_{REF}) mode, V_{CM} = 2.5V		±1	±3	LSB
		External reference, 0V to V_{REF} mode, V_{CM} = 1.25V		±1	±3	LSB
Zero code error match				±0.5		LSB
Common mode rejection		DC, 0V to (2 · V_{REF}) mode		67		dB
SAMPLING DYNAMICS						
Conversion rate		External single analog channel, auto mode		500		kSPS
		External single analog channel, direct mode		167		kSPS
Conversion time(4)		External single analog channel		2		µs
Autocycle update rate(4)		All 16 single-ended inputs enabled		32		µs
Throughput rate		SPI clock 12MHz or greater, single channel			500	kSPS
ANALOG INPUT(5)						
Full-scale input voltage		Single-ended, 0V to V_{REF}	0		V_{REF}	V
		Single-ended, 0V to (2 · V_{REF})	0		2 · V_{REF}	V
		V_{IN+} – V_{IN-}, fully-differential, 0V to V_{REF}	–V_{REF}		+V_{REF}	V
		V_{IN+} – V_{IN-}, fully-differential, 0V to (2 · V_{REF})	–2 · V_{REF}		2 · V_{REF}	V
Absolute input voltage			GND - 0.2		AV_{DD} + 0.2	V
Input capacitance(4)		0V to VREF mode		118		pF
		0V to (2 · VREF) mode		73		
DC input leakage current		Unselected ADC input			±10	µA

(4) Sampled during initial release to ensure compliance; not subject to production testing.
(5) V_{IN+} or V_{IN-} must remain within GND - 0.2V and AV_{DD} + 0.2V. See *Analog Inputs* section.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +105°C, AV_{DD} = DV_{DD} = 4.5V to 5.5V, AV_{CC} = +15V, AGND = DGND = 0V, IOV_{DD} = 2.7V to 5.5V, internal 2.5V reference, and the DAC output span = 0V to 5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AMC7812 MIN	AMC7812 TYP	AMC7812 MAX	UNIT
ADC REFERENCE INPUT						
Reference input voltage range			1.2		AV_{DD}	V
Input current		V_{REF} = 2.5V		145		µA
INTERNAL ADC REFERENCE BUFFER						
Offset		T_A = +25°C			±5	mV
INTERNAL TEMPERATURE SENSOR						
Operating range			–40		+125	°C
Accuracy		AV_{DD} = 5V, T_A = –40°C to +125°C		±1.25	±2.5	°C
		AV_{DD} = 5V, T_A = 0°C to +100°C			±1.5	°C
Resolution		Per LSB		0.125		°C
Conversion rate		External temperature sensors are disabled		15		ms
EXTERNAL TEMPERATURE SENSOR (Using 2N3906 external transistor)						
Operating range		Limited by external diode	–40		+150	°C
Accuracy[6][7]		AV_{DD} = 5V, T_A = 0°C to +100°C, T_D = –40°C to +150°C			±1.5	°C
		AV_{DD} = 5V, T_A = –40°C to +100°C, T_D = –40°C to +150°C			±2	°C
Resolution		Per LSB		0.125		°C
Conversion rate per sensor		With resistance cancellation (RC bit = '1')	72	93	100	ms
		Without resistance cancellation (RC bit = '0')	33	44	47	ms
DIGITAL LOGIC: GPIO[8][9] and $\overline{ALARM}$						
V_{IH}	Input high voltage	IOV_{DD} = +5V	2.1		0.3 + IOV_{DD}	V
		IOV_{DD} = +3.3V	2.1		0.3 + IOV_{DD}	V
V_{IL}	Input low voltage	IOV_{DD} = +5V	–0.3		0.8	V
		IOV_{DD} = +3.3V	–0.3		0.8	V
V_{OL}	Output low voltage	IOV_{DD} = +5V, sinking 5mA			0.4	V
		IOV_{DD} = +3.3V, sinking 2mA			0.4	V
High-impedance leakage					5	µA
High-impedance output capacitance					10	pF

(6) T_D is the external diode temperature.
(7) Auto conversion mode disabled
(8) For pins GPIO0-3, the external pull up resistor must be connected to a voltage less than or equal to 5.5V.
(9) For pins GPIO4-7, the external pull up resistor must be connected to a voltage less than or equal to AV_{DD}.

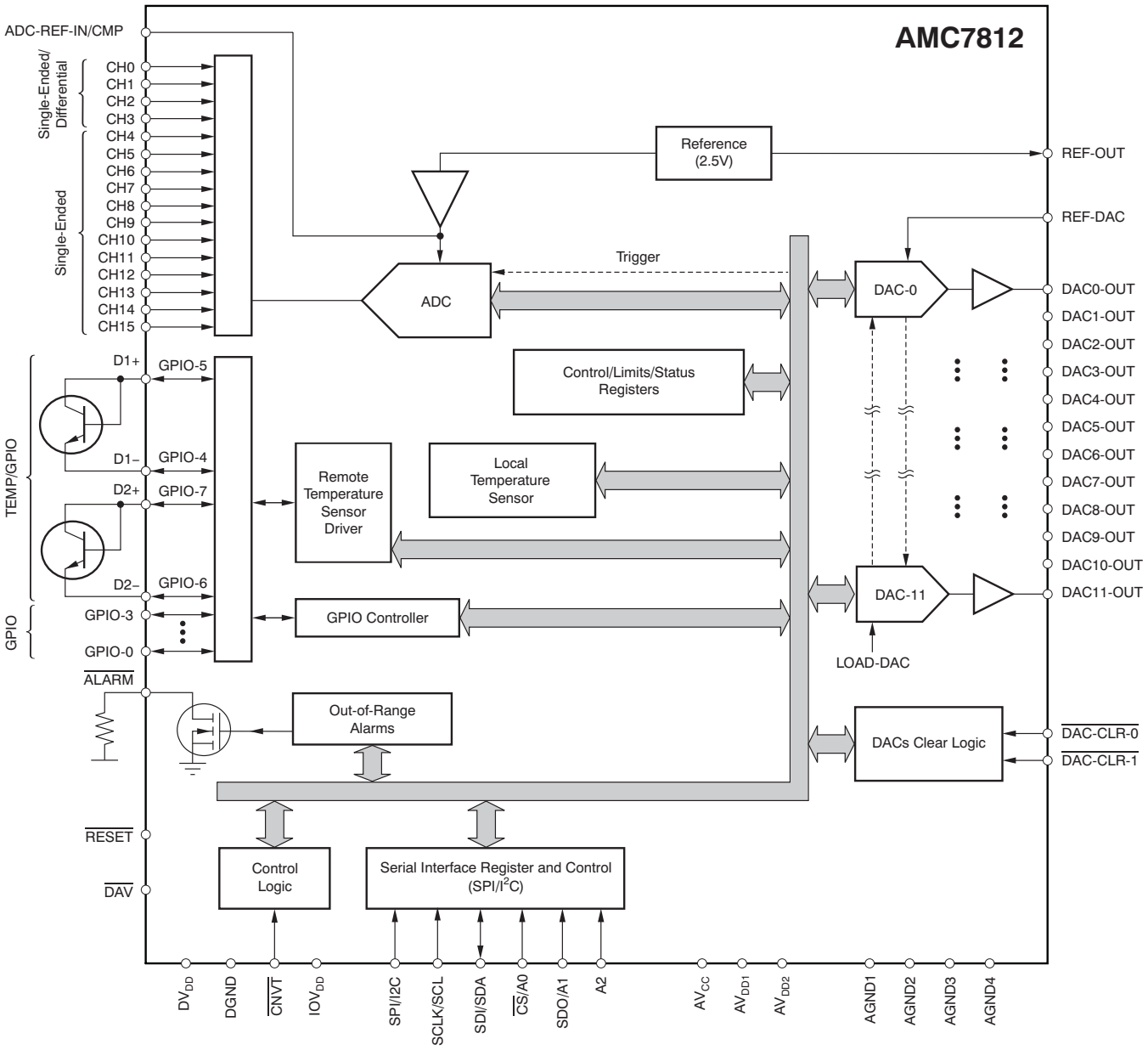
ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +105°C, AV_{DD} = DV_{DD} = 4.5V to 5.5V, AV_{CC} = +15V, AGND = DGND = 0V, IOV_{DD} = 2.7V to 5.5V, internal 2.5V reference, and the DAC output span = 0V to 5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AMC7812 MIN	AMC7812 TYP	AMC7812 MAX	UNIT
DIGITAL LOGIC: All Except SCL, SDA, $\overline{ALARM}$, and GPIO						
V_{IH}	Input high voltage	IOV_{DD} = +5V	2.1		0.3 + IOV_{DD}	V
		IOV_{DD} = +3.3V	2.1		0.3 + IOV_{DD}	V
V_{IL}	Input low voltage	IOV_{DD} = +5V	–0.3		0.8	V
		IOV_{DD} = +3.3V	–0.3		0.8	V
Input current					±1	µA
Input capacitance					5	pF
V_{OH}	Output high voltage	IOV_{DD} = +5V, sourcing 3mA	4.8			V
		IOV_{DD} = +3.3V, sourcing 3mA	2.9			V
V_{OL}	Output low voltage	IOV_{DD} = +5V, sinking 3mA			0.4	V
		IOV_{DD} = +3.3V, sinking 3mA			0.4	V
High-impedance leakage					±5	µA
High-impedance output capacitance					10	pF
DIGITAL LOGIC: SDA, SCL (I^2C-Compatible Interface)						
V_{IH}	Input high voltage	IOV_{DD} = +5V	2.1		0.3 + IOV_{DD}	V
		IOV_{DD} = +3.3V	2.1		0.3 + IOV_{DD}	V
V_{IL}	Input low voltage	IOV_{DD} = +5V	–0.3		0.8	V
		IOV_{DD} = +3.3V	–0.3		0.8	V
Input current					±5	µA
Input capacitance					5	pF
V_{OL}	Output low voltage	IOV_{DD} = +5V, sinking 3mA	0		0.4	V
		IOV_{DD} = +3.3V, sinking 3mA	0		0.4	V
High-impedance leakage					±5	µA
High-impedance output capacitance					10	pF
TIMING REQUIREMENTS						
Power-on delay		From AV_{DD} , DV_{DD} ≥ 2.7V and AV_{CC} ≥ 4.5V to normal operation		100	250	µs
Power-down recovery time		from $\overline{CS}$ rising edge			70	µs
Reset delay		Delay to normal operation from any reset		100	250	µs
Convert pulse width			20			ns
Reset pulse width			20			ns
POWER-SUPPLY REQUIREMENTS						
AV_{DD}		AV_{DD} must be ≥ (V_{REF} + 1.2V)	+2.7		+5.5	V
AI_{DD}		AV_{DD} and DV_{DD} combined, normal operation, no DAC load		7.9	12.5	mA
		AV_{DD} and DV_{DD} combined, all blocks in power down		1.6		mA
AV_{CC}			+4.5		+18	V
IV_{CC}		AV_{CC}, no load, DACs at code 800h			6.5	mA
Power dissipation		Normal operation(10), AV_{DD} = DV_{DD} = 5V, AV_{CC} = 15V		95	120	mW
DV_{DD}			+2.7		+5.5	V
IOV_{DD}			+2.7		+5.5	V
TEMPERATURE RANGE						
Specified performance			–40		+105	°C

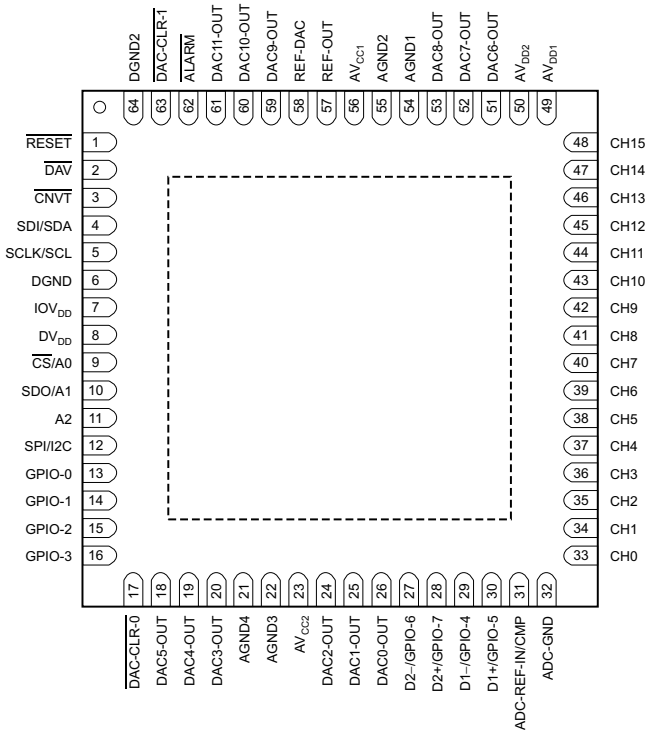
(10) No DAC load, all DACs at 800h and both ADCs at the fastest auto conversion rate

FUNCTIONAL BLOCK DIAGRAM

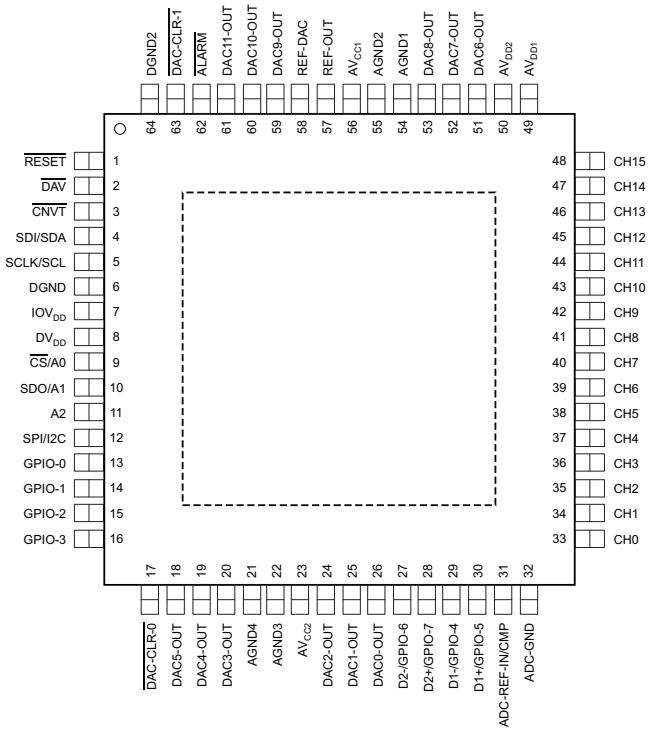


PIN CONFIGURATION

RGC PACKAGE
QFN-64
(TOP VIEW)



PAP PACKAGE
HTQFP-64
(TOP VIEW)



PIN DESCRIPTIONS

PIN (QFN / HTQFP)		DESCRIPTION
NO.	NAME	
1	$\overline{\text{RESET}}$	Reset input, active low. Logic low on this pin causes the device to perform a hardware reset.
2	$\overline{\text{DAV}}$	Data available indicator, active low output. In direct mode, the $\overline{\text{DAV}}$ pin goes low (active) when the conversion ends. In auto mode, a 1µs pulse (active low) appears on this pin when a conversion cycle finishes (see the *Primary ADC Operation* and *Registers* sections for details). $\overline{\text{DAV}}$ stays high when deactivated.
3	$\overline{\text{CNVT}}$	External conversion trigger, active low. The falling edge starts the sampling and conversion of the ADC.
4	SDI/SDA	Serial interface data. SDI for the serial peripheral interface (SPI) when the SPI/I2C pin is high. SDA for I^2C when the SPI/I2C pin is low.
5	SCLK/SCL	Serial clock input of the main serial interface. SPI clock when the SPI/I2C pin is high; I^2C clock when the SPI/I2C pin is low.
6	DGND	Digital ground
7	IOV_{DD}	Interface power supply
8	DV_{DD}	Digital power supply (+3V to +5V). Must be the same value as AV_{DD}.
9	$\overline{\text{CS}}$/A0	Chip select signal for SPI when the SPI/I2C pin is high. Slave address selection A0 for I^2C when the SPI/I2C pin is low.
10	SDO/A1	SDO for SPI when the SPI/I2C pin is high. Slave address selection A1 for I^2C when the SPI/I2C pin is low.
11	A2	Slave address selection A2 for I^2C when the SPI/I2C pin is low.
12	SPI/I2C	Interface selection pin. Digital input. When this pin is tied to IOV_{DD}, the SPI is enabled and the I^2C interface is disabled. When this pin is tied to ground, the SPI is disabled and the I^2C interface is enabled.
13	GPIO-0	General-purpose digital input/output. This pin is a bidirectional open-drain, digital input/output, and requires an external pull-up resistor. See the *General Purpose Input/Output Pins* section for more details.
14	GPIO-1	
15	GPIO-2	
16	GPIO-3	

PIN DESCRIPTIONS (continued)

PIN (QFN / HTQFP)		DESCRIPTION
NO.	NAME	
17	$\overline{\text{DAC-CLR-0}}$	DAC clear control signal, digital input, active low. When low, all DACs associated with the DAC-CLR-0 pin enter a clear state, the DAC Latch is loaded with predefined code, and the output is set to the corresponding level. However, the DAC-Data Register does not change. When the DAC goes back to normal operation, the DAC Latch is loaded with the previous data from the DAC-Data Register and the output returns to the previous level, regardless of the status of the SLDAC-n bit. When this pin is high, the DACs are in normal operation.
18	DAC5-OUT	Output of DAC channels 3, 4, and 5
19	DAC4-OUT	
20	DAC3-OUT	
21	AGND4	Analog ground
22	AGND3	
23	AV_{CC2}	Positive analog power for DAC0-OUT, DAC1-OUT, DAC2-OUT, DAC3-OUT, DAC4-OUT, DAC5-OUT, must be tied to AV_{CC1}
24	DAC2-OUT	Output of DAC channels 0, 1, and 2
25	DAC1-OUT	
26	DAC0-OUT	
27	D2–/GPIO-6	Remote sensor D2 negative input when D2 enabled; GPIO-6 when D2 disabled. Pull-up required for output.
28	D2+/GPIO-7	Remote sensor D2 positive input when D2 enabled; GPIO-7 when D2 disabled. Pull-up required for output.
29	D1–/GPIO4	Remote sensor D1 negative input when D1 enabled; GPIO-6 when D1 disabled. Pull-up required for output.
30	D1+/GPIO-5	Remote sensor D1 positive input when D1 enabled; GPIO-7 when D1 disabled. Pull-up required for output.
31	ADC-REF-IN/CMP	External ADC reference input when external V_{REF} is used to drive ADC. Compensation capacitor connection (connect 4.7µF capacitor between this pin and AGND) when Internal V_{REF} is used to drive ADC.
32	ADC-GND	ADC ground. Must be connected to AGND.
33-48	CH0 to CH15	Analog inputs of channel 0 to 15. CH4 to CH15 are single-ended. CH0, CH1, CH2, and CH3 can be programmed as differential or single-ended.
49	AV_{DD1}	Positive analog power supply
50	AV_{DD2}	
51	DAC6-OUT	Output of DAC channels 6, 7, and 8
52	DAC7-OUT	
53	DAC8-OUT	
54	AGND1	Analog ground
55	AGND2	
56	AV_{CC1}	Positive analog power for DAC6-OUT, DAC7-OUT, DAC8-OUT, DAC9-OUT, DAC10-OUT, DAC11-OUT, must be tied to AV_{CC2}
57	REF-OUT	Internal reference output
58	REF-DAC	DAC reference Input
59	DAC9-OUT	Output of DAC channels 9, 10, and 11
60	DAC10-OUT	
61	DAC11-OUT	
62	$\overline{\text{ALARM}}$	Global alarm. Open drain output. External 10kΩ pull-up resistor required. This pin goes low (active) when one (or more) of the analog channels are out of range.
63	$\overline{\text{DAC-CLR-1}}$	DAC clear control signal, digital input, active low. When low, all DACs associated with the DAC-CLR-1 pin enter a clear state, the DAC Latch is loaded with predefined code, and the output is set to the corresponding level. However, the DAC-Data Register does not change. When the DAC goes back to normal operation, the DAC Latch is loaded with the previous data from the DAC-Data Register and the output returns to the previous level, regardless of the status of the SLDAC-n bit. When this pin is high, the DACs are in normal operation.
64	DGND2	Digital ground

I²C-COMPATIBLE TIMING DIAGRAMS

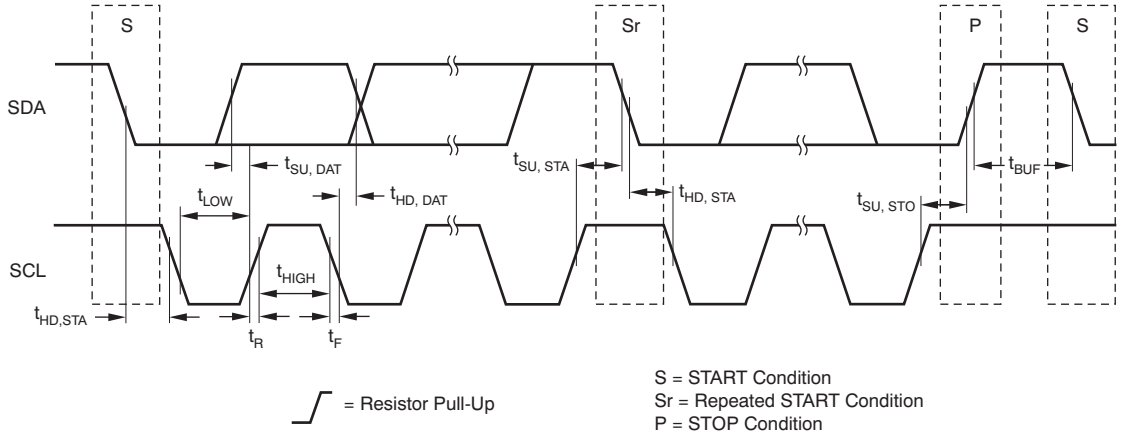


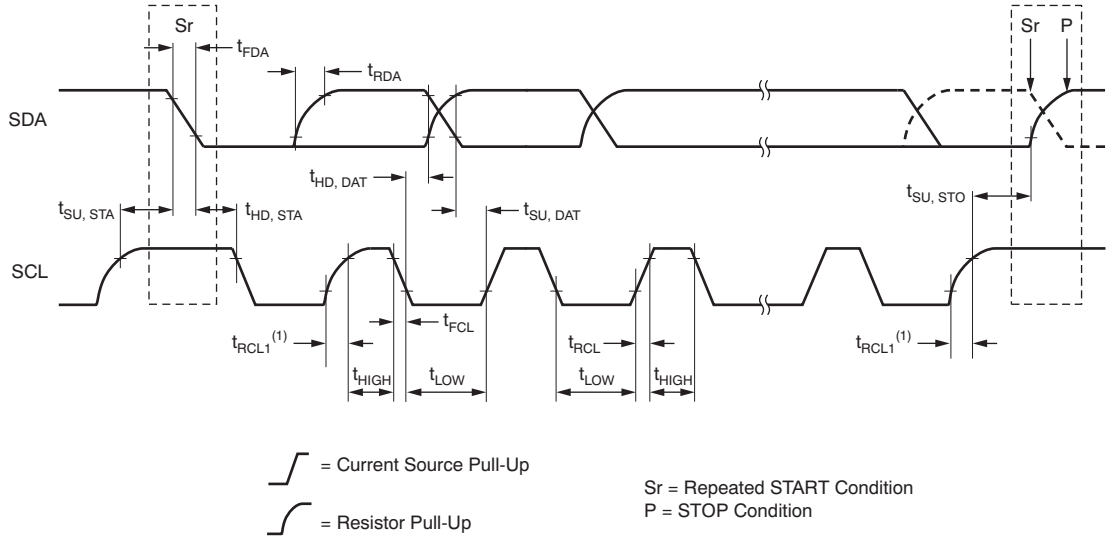
Figure 1. Timing for Standard and Fast Mode Devices on the I²C Bus

TIMING CHARACTERISTICS: SDA and SCL for Standard and Fast Modes(1)

At –40°C to +105°C, AV_{DD} = DV_{DD} = 4.5V to 5.5V, AGND = DGND = 0V, and IOV_{DD} = 2.7V to 5.5V, unless otherwise noted.

PARAMETER		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL} (2)	SCL clock frequency	0	100	0	400	kHz
t_{LOW}	Low period of the SCL clock	4.7	—	1.3	—	µs
t_{HIGH}	High period of the SCL clock	4.0	—	0.6	—	µs
$t_{SU, STA}$	Set-up time for a repeated start condition	4.7	—	0.6	—	µs
$t_{HD, STA}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated	4.0	—	0.6	—	µs
$t_{SU, DAT}$	Data set-up time	250	—	100	—	ns
$t_{HD, DAT}$	Data hold time: for I²C-bus devices	0	3.45	0	0.9	µs
$t_{SU, STO}$	Set-up time for stop condition	4.0	—	0.6	—	µs
t_R	Rise time of both SDA and SCL signals	—	1000	$20 + 0.1C_B$ (3)	300	ns
t_F	Fall time of both SDA and SCL signals	—	300	$20 + 0.1C_B$ (3)	300	ns
t_{BUF}	Bus free time between a stop and start condition	4.7	—	1.3	—	µs
C_B	Capacitive load for each bus line	—	400	—	400	pF
t_{SP}	Pulse width of spike suppressed	NA	NA	0	50	ns

(1) All values refer to V_{IHmin} and V_{ILmax} levels.
(2) An SCL operating frequency of at least 1kHz is recommended to avoid activating the I²C timeout function. See the Timeout Function section for details.
(3) C_B = total capacitance of one bus line in pF.



(1) First rising edge of the SCL signal after Sr and after each acknowledge bit.

Figure 2. Timing for High-Speed (Hs) Mode Devices on the I²C Bus

TIMING CHARACTERISTICS: SDA and SCL for Hs Mode(1)

At –40°C to +105°C, AV_{DD} = 4.5V to 5.5V, DV_{DD} = 2.7V to 5.5V, AGND = DGND = 0V, and IOV_{DD} = 2.7V to 5.5V, unless otherwise noted.

PARAMETER		C_B = 10pF to 100pF		C_B = 400pF		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL} (2)	SCL clock frequency	0	3.4	0	1.7	MHz
$t_{SU, STA}$	Setup time for (repeated) start condition	160	—	160	—	ns
$t_{HD, STA}$	Hold time (repeated) start condition	160	—	160	—	ns
t_{LOW}	Low period of the SCL clock	160	—	320	—	ns
t_{HIGH}	High period of the SCL clock	60	—	120	—	ns
$t_{SU, DAT}$	Data setup time	10	—	10	—	ns
$t_{HD, DAT}$	Data hold time	0	70	0	150	ns
t_{RCL}	Rise time of SCL signal	10	40	20	80	ns
t_{RCL1}	Rise time of SCL signal after a repeated start condition and after an acknowledge bit	10	80	20	160	ns
t_{FCL}	Fall time of SCL signal	10	40	20	80	ns
t_{RDA}	Rise time of SDA signal	10	80	20	160	ns
t_{FDA}	Fall time of SDA signal	10	80	20	160	ns
$t_{SU, STO}$	Set-up time for stop condition	160	—	160	—	ns
C_B (3)	Capacitive load for SDA and SCL lines	10	100	—	400	pF
t_{SP}	Pulse width of spike suppressed	0	10	0	10	ns

(1) All values refer to V_{IHmin} and V_{ILmax} levels.
(2) An SCL operating frequency of at least 1kHz is recommended to avoid activating the I²C timeout function. See the Timeout Function section for details.
(3) For bus line loads where C_B is between 100pF and 400pF, the timing parameters must be linearly interpolated.

SPI TIMING DIAGRAMS

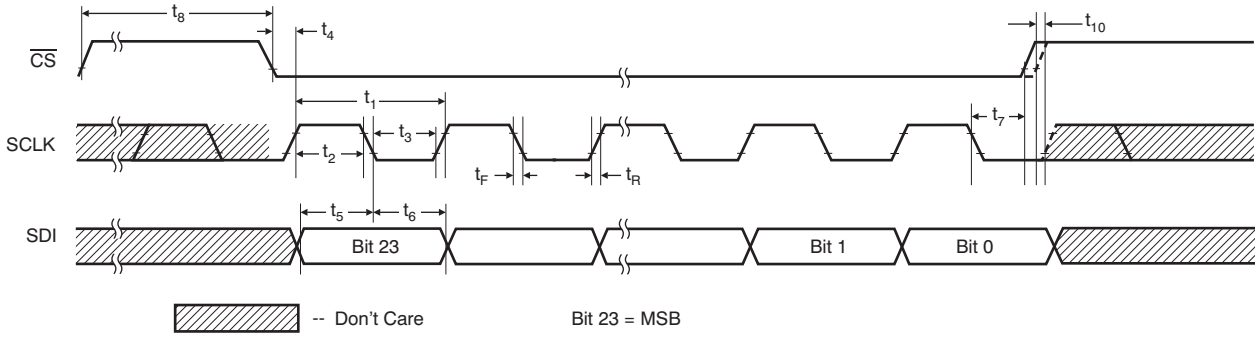


Figure 3. SPI Single-Chip Write Operation

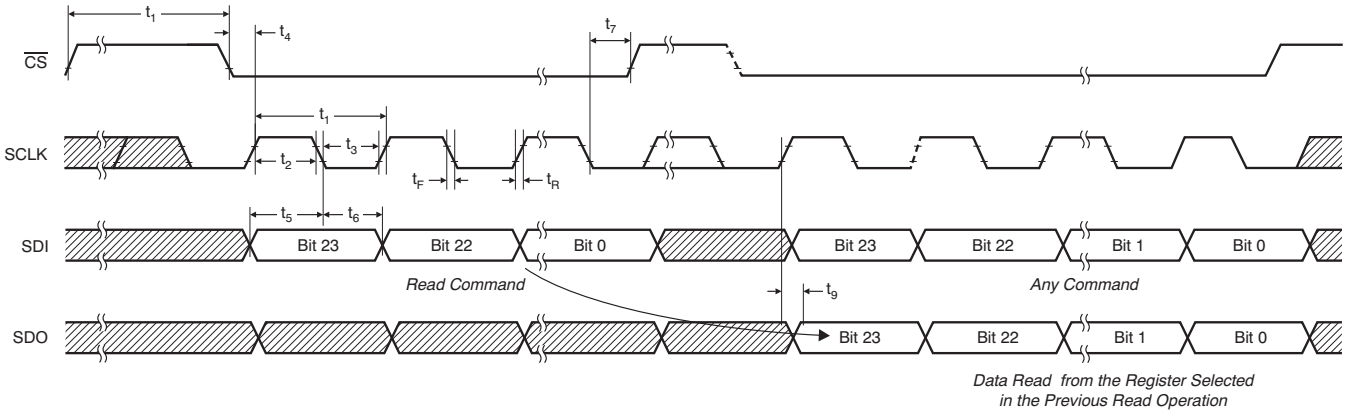


Figure 4. SPI Single-Chip Read Operation

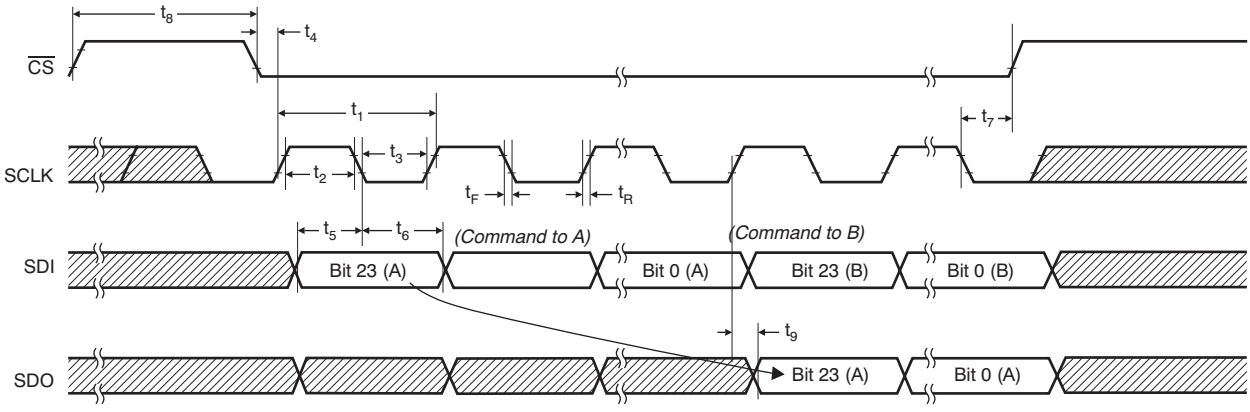


Figure 5. Daisy-Chain Operation: Two Devices

TIMING CHARACTERISTICS: SPI Bus(1)(2)

At –40°C to +105°C, AV_{DD} = DV_{DD} = 4.5V to 5.5V, AGND = DGND = 0V, and IOV_{DD} = 3.0V to 5.5V, unless otherwise noted.

PARAMETER		LIMIT AT T_{MIN}, T_{MAX} MIN	LIMIT AT T_{MIN}, T_{MAX} MAX	UNIT
f_{SCLK}	Clock frequency		50	MHz
t_1	SCLK cycle time	20		ns
t_2	SCLK high time	8		ns
t_3	SCLK low time	8		ns
t_4	$\overline{CS}$ falling edge to SCLK rising edge setup time	5		ns
t_5	Input data setup time	5		ns
t_6	Input data hold time	4		ns
t_7	SCLK falling edge to $\overline{CS}$ rising edge	10		ns
t_8	Minimum $\overline{CS}$ high time	30		ns
t_9	Output data valid time	3	20	ns
t_{10}	$\overline{CS}$ rising to next SCLK rising edge	3		ns

(1) Specified by design; not production tested.
(2) SDO loaded with 10pF load capacitance for SDO timing specifications, t_R = t_F ≤ 5 ns.

TYPICAL CHARACTERISTICS: DAC

At +25°C, unless otherwise noted.

DIFFERENTIAL LINEARITY ERROR vs CODE

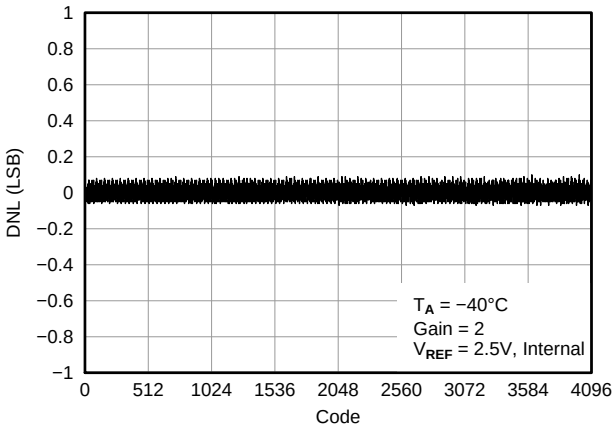


Figure 6.

LINEARITY ERROR vs CODE

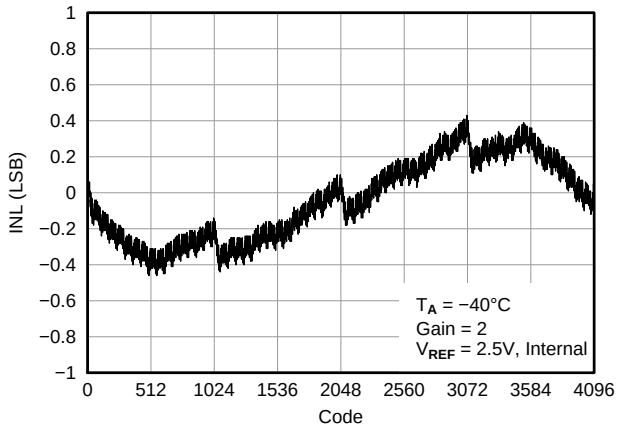


Figure 7.

DIFFERENTIAL LINEARITY ERROR vs CODE

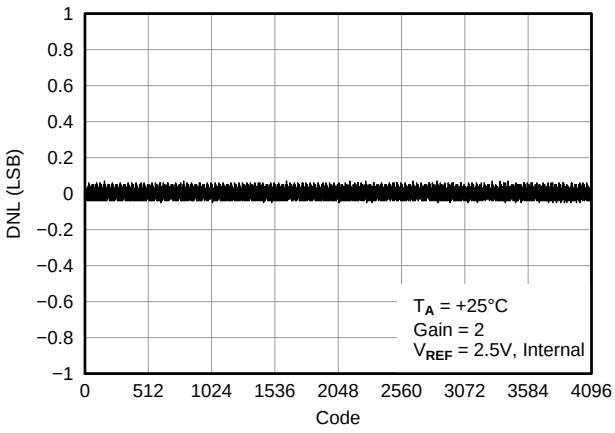


Figure 8.

LINEARITY ERROR vs CODE

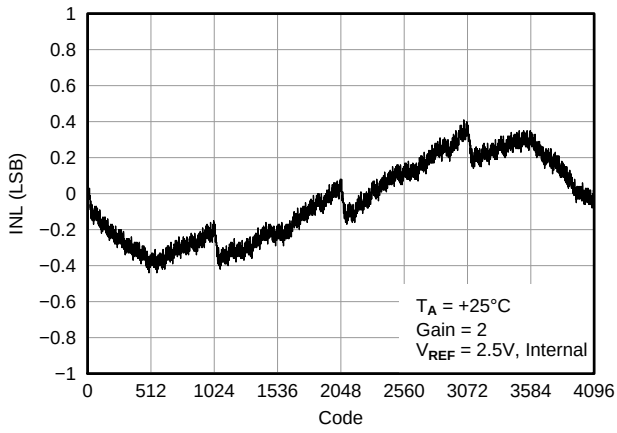


Figure 9.

DIFFERENTIAL LINEARITY ERROR vs CODE

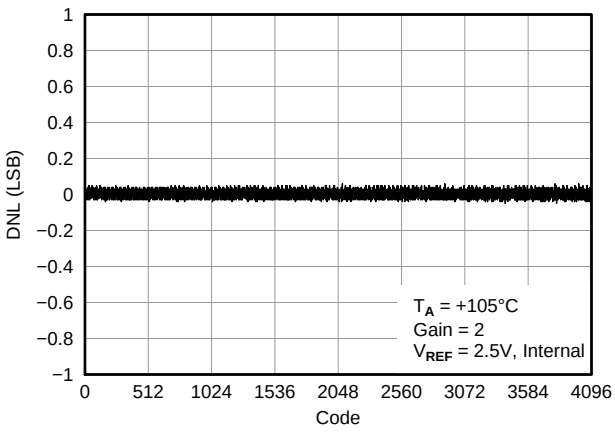


Figure 10.

LINEARITY ERROR vs CODE

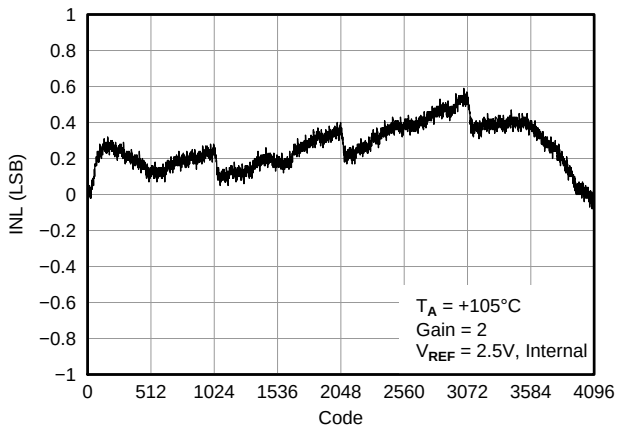


Figure 11.

TYPICAL CHARACTERISTICS: DAC (continued)

At +25°C, unless otherwise noted.

DIFFERENTIAL LINEARITY ERROR vs CODE

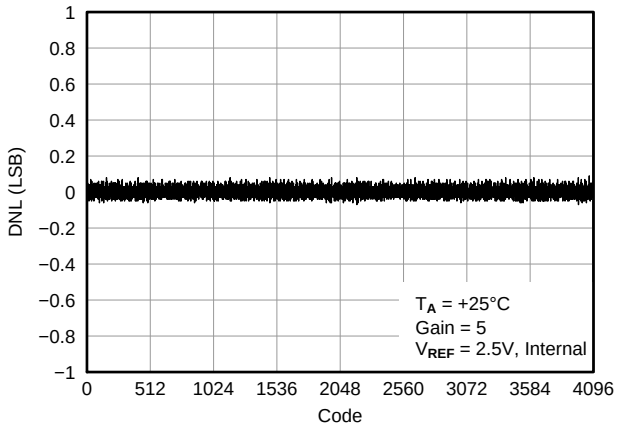


Figure 12.

LINEARITY ERROR vs CODE

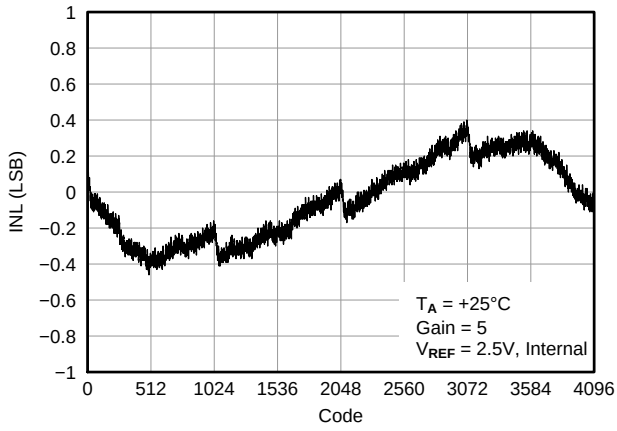


Figure 13.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

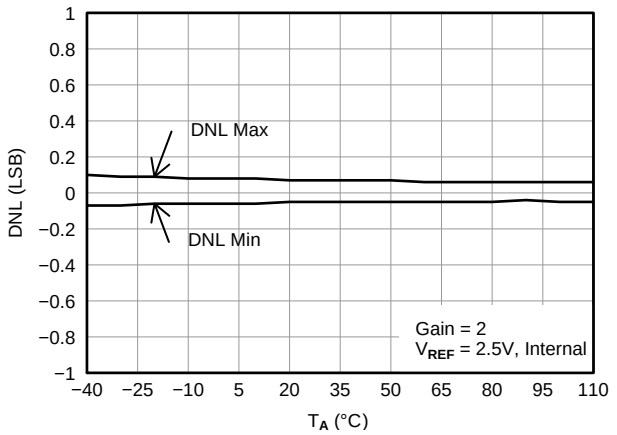


Figure 14.

LINEARITY ERROR vs TEMPERATURE

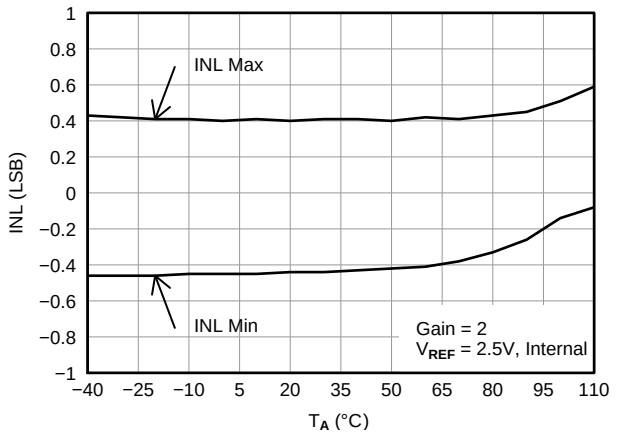


Figure 15.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

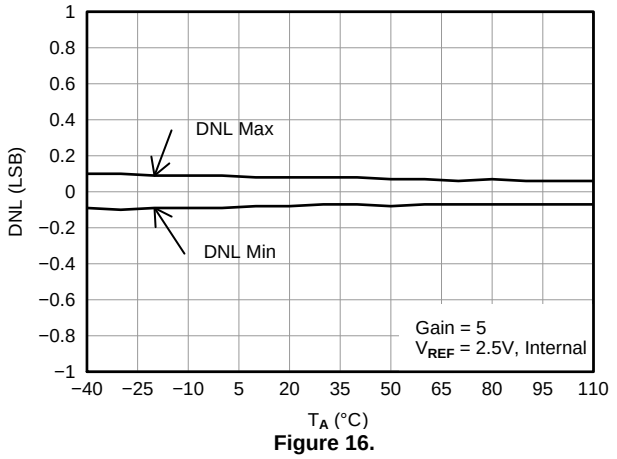


Figure 16.

LINEARITY ERROR vs TEMPERATURE

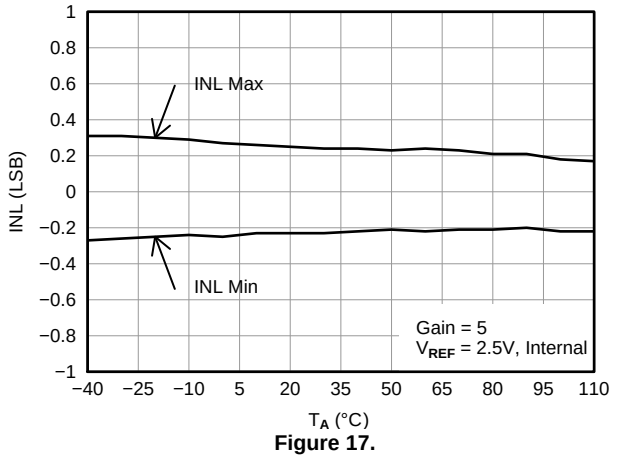


Figure 17.

TYPICAL CHARACTERISTICS: DAC (continued)

At +25°C, unless otherwise noted.

DIFFERENTIAL LINEARITY ERROR vs CODE

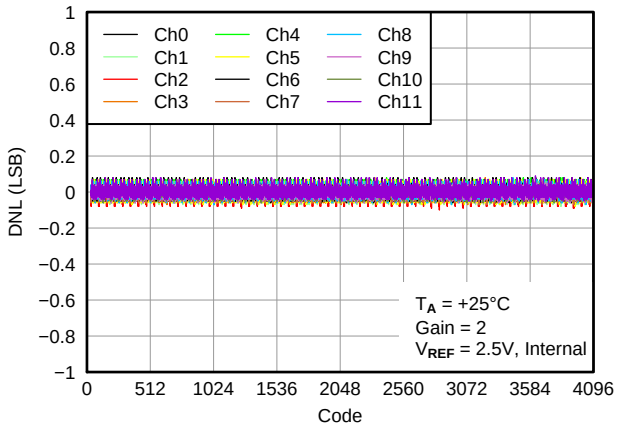


Figure 18.

LINEARITY ERROR vs CODE

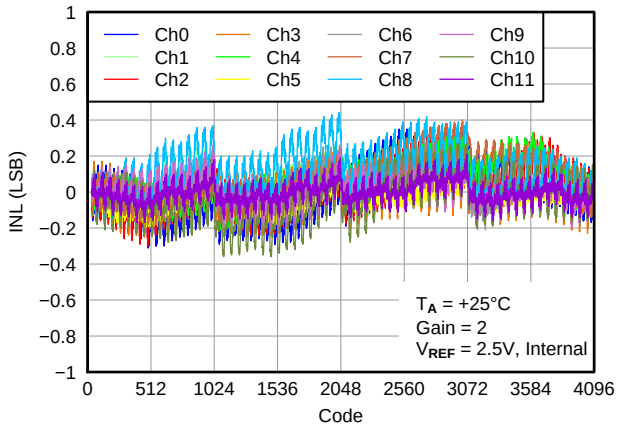


Figure 19.

GAIN ERROR

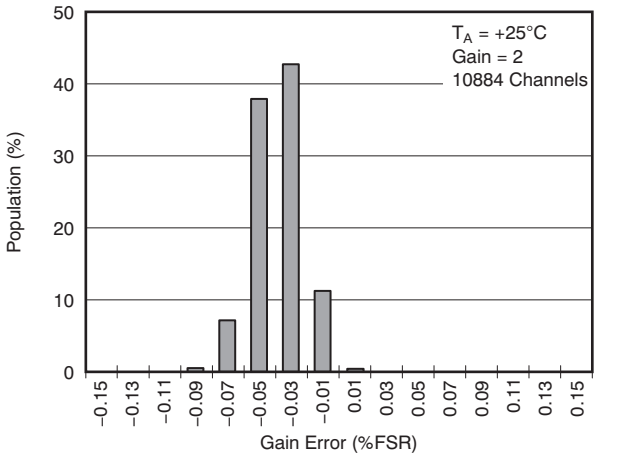


Figure 20.

GAIN ERROR

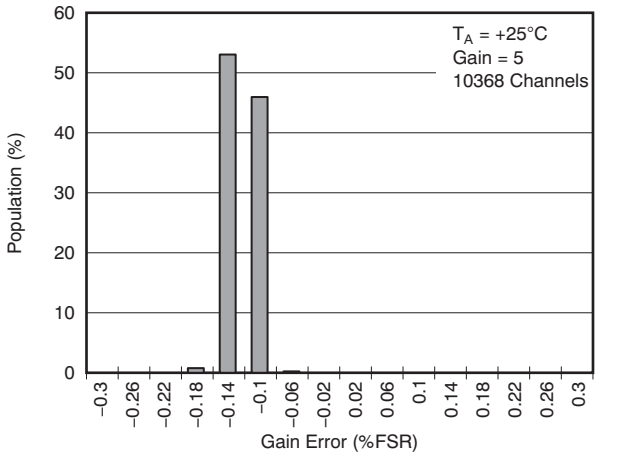


Figure 21.

GAIN ERROR vs TEMPERATURE

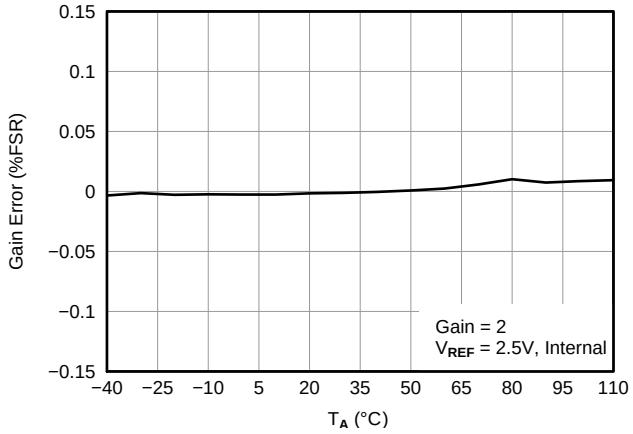


Figure 22.

GAIN ERROR vs TEMPERATURE

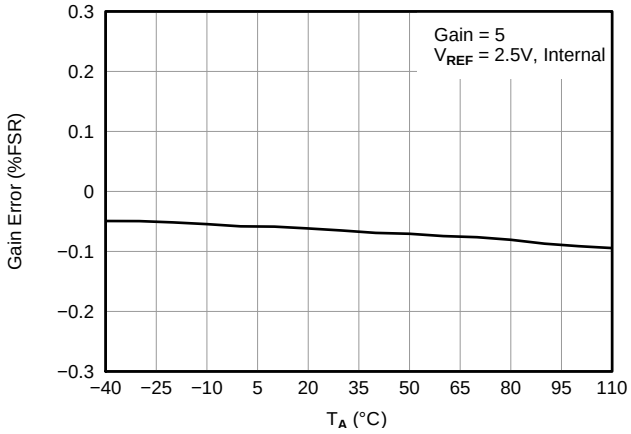


Figure 23.

TYPICAL CHARACTERISTICS: DAC (continued)

At +25°C, unless otherwise noted.

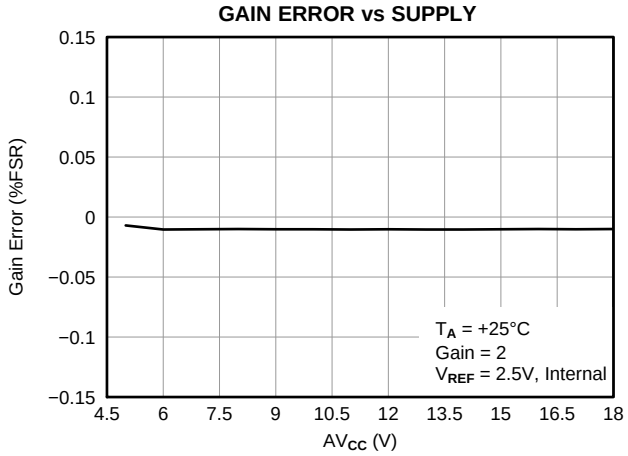


Figure 24.

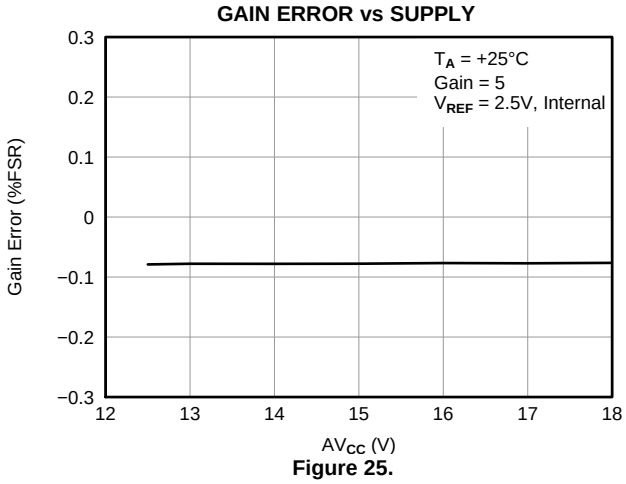


Figure 25.

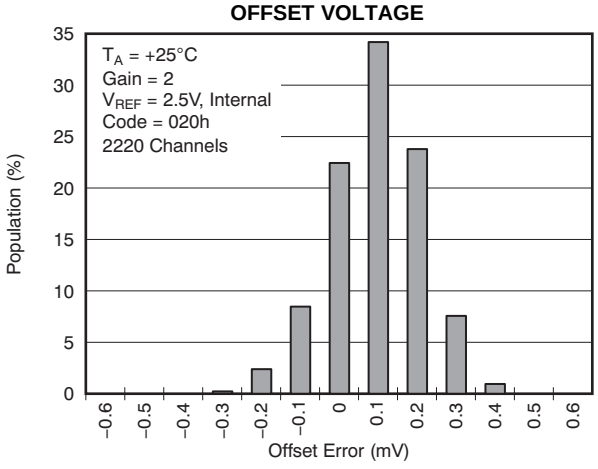


Figure 26.

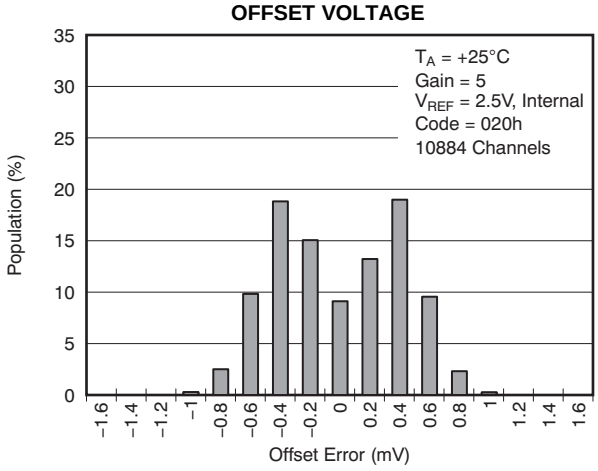


Figure 27.

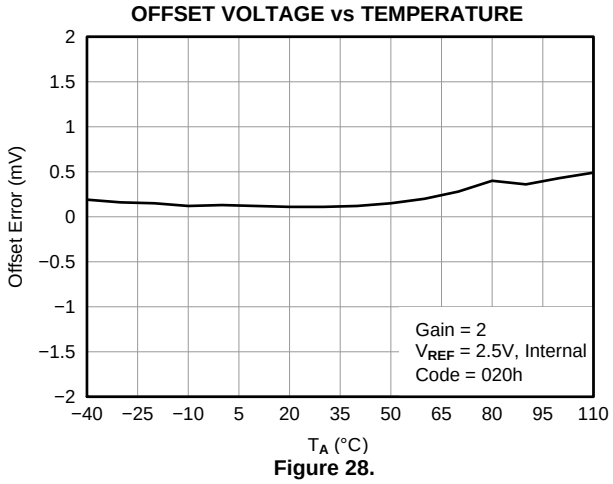


Figure 28.

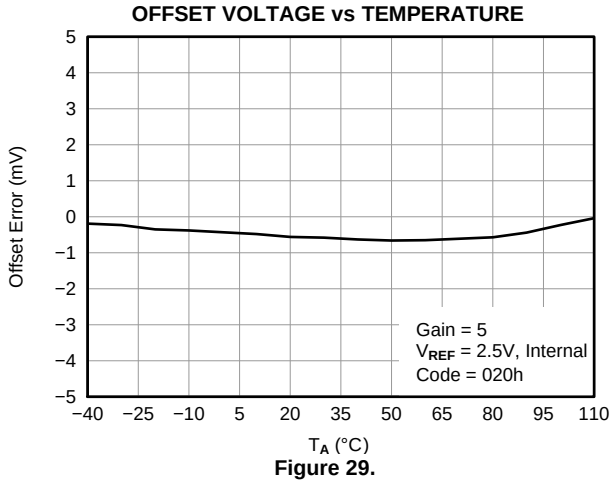


Figure 29.

TYPICAL CHARACTERISTICS: DAC (continued)

At +25°C, unless otherwise noted.

OFFSET VOLTAGE vs SUPPLY VOLTAGE

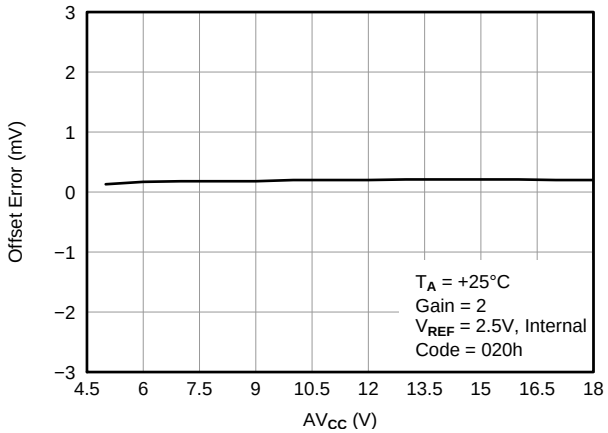


Figure 30.

OFFSET VOLTAGE vs SUPPLY VOLTAGE

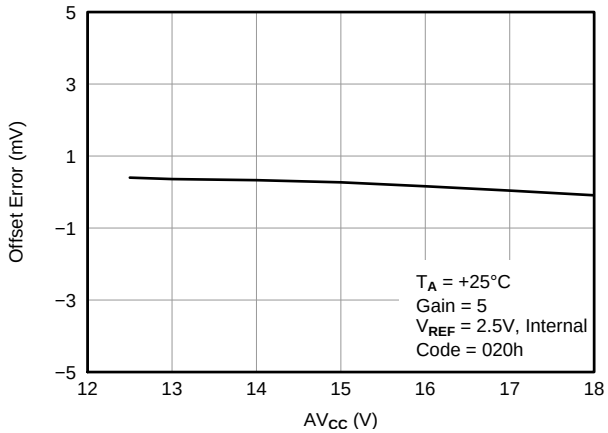


Figure 31.

OUTPUT VOLTAGE vs OUTPUT CURRENT

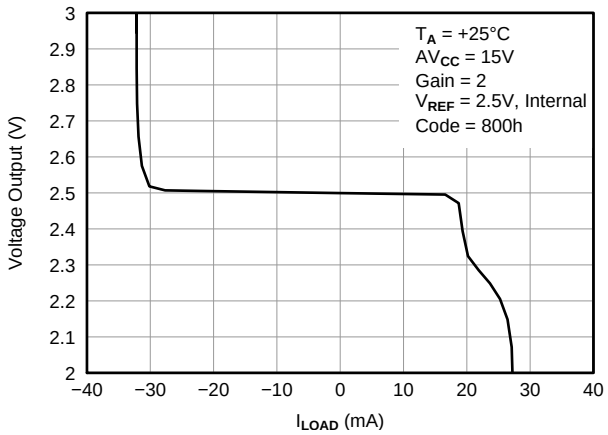


Figure 32.

OUTPUT VOLTAGE vs SOURCE CURRENT CAPABILITY

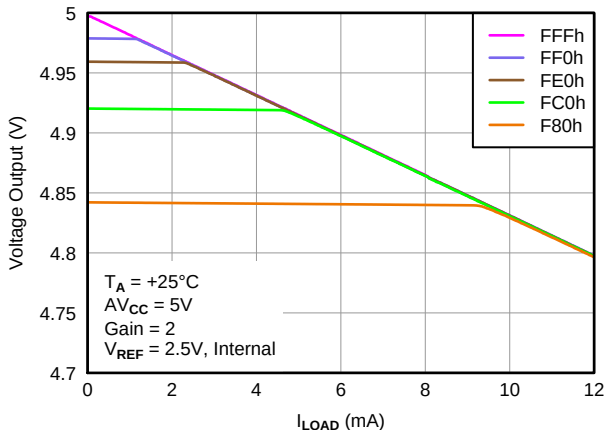


Figure 33.

OUTPUT VOLTAGE vs SINK CURRENT CAPABILITY

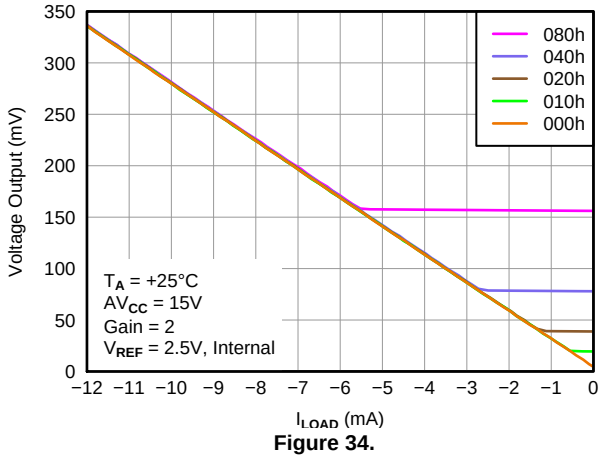


Figure 34.

DAC SUPPLY CURRENT vs DAC SUPPLY VOLTAGE

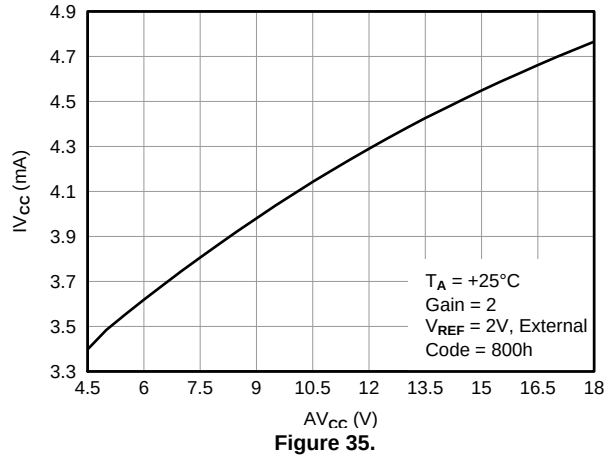


Figure 35.

TYPICAL CHARACTERISTICS: DAC (continued)

At +25°C, unless otherwise noted.

SUPPLY CURRENT vs DAC CODE

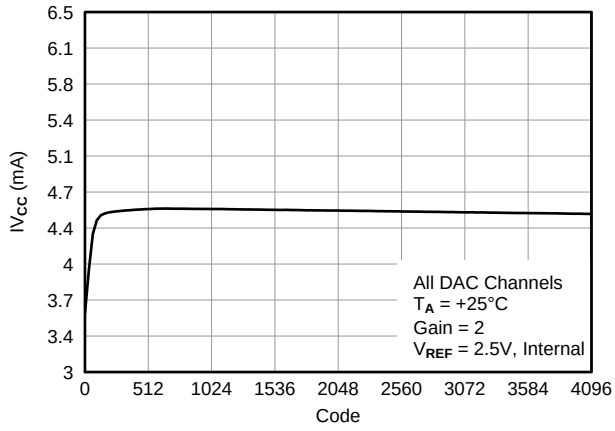


Figure 36.

SUPPLY CURRENT vs TEMPERATURE

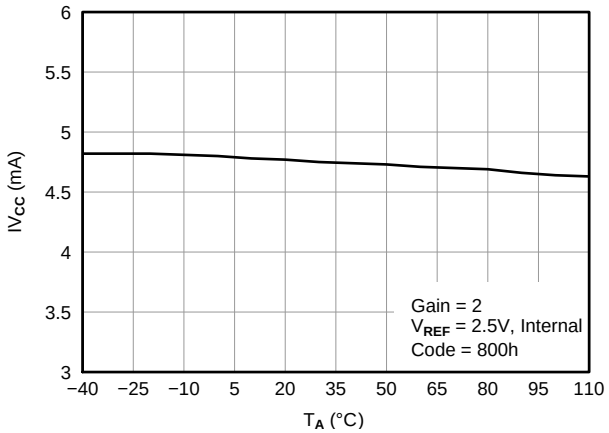


Figure 37.

DAC SUPPLY CURRENT

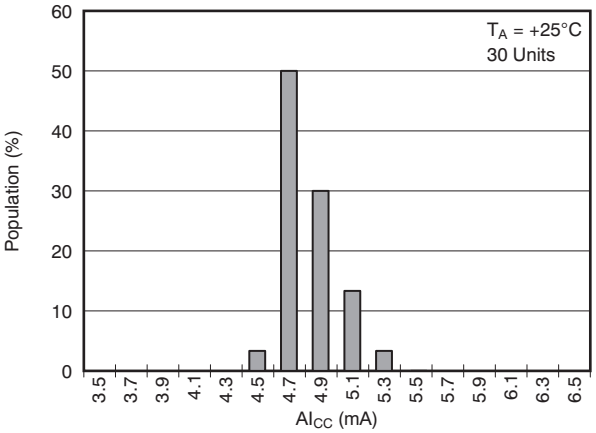


Figure 38.

DAC NOISE VOLTAGE vs FREQUENCY

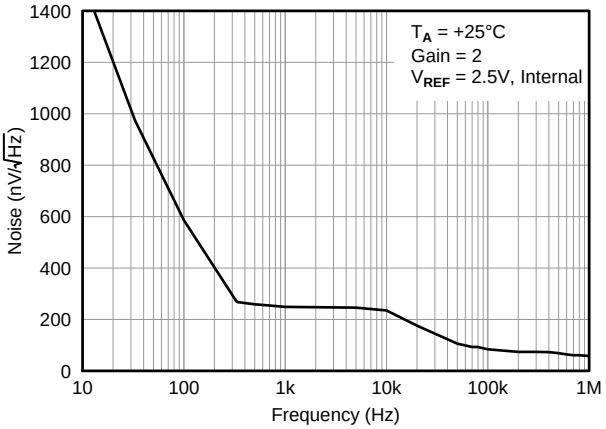


Figure 39.

DAC NOISE 0.1Hz to 10Hz

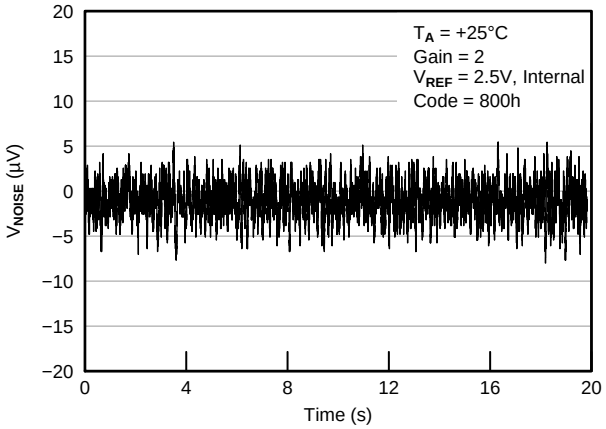


Figure 40.

SETTLING TIME RISING EDGE

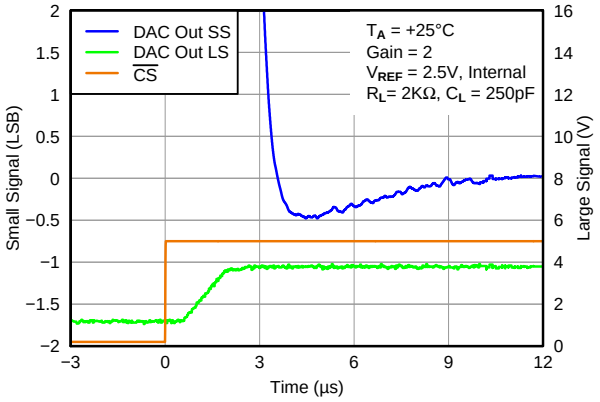


Figure 41.

TYPICAL CHARACTERISTICS: DAC (continued)

At +25°C, unless otherwise noted.

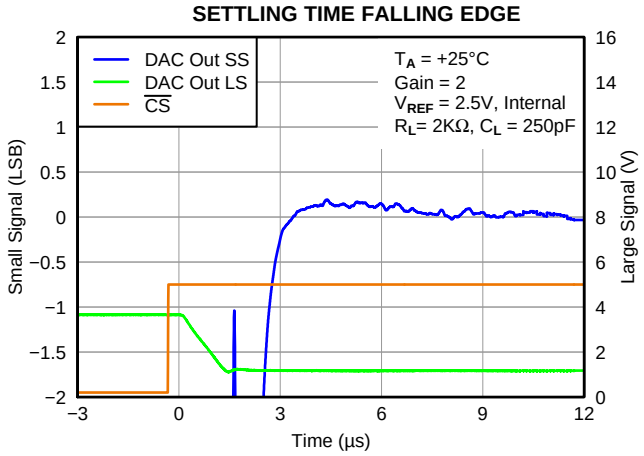


Figure 42.

TYPICAL CHARACTERISTICS: ADC

At +25°C, unless otherwise noted.

DIFFERENTIAL LINEARITY ERROR vs CODE

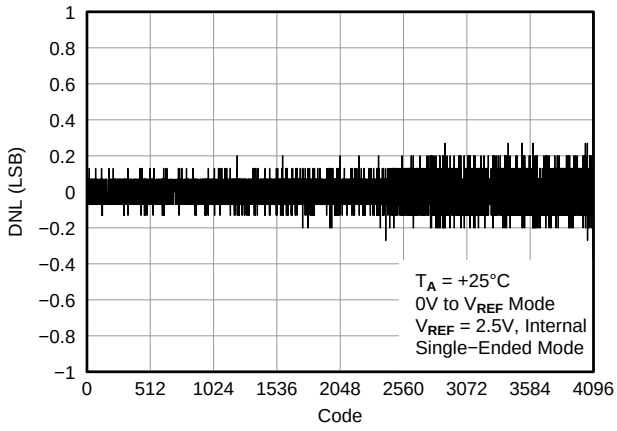


Figure 43.

LINEARITY ERROR vs CODE

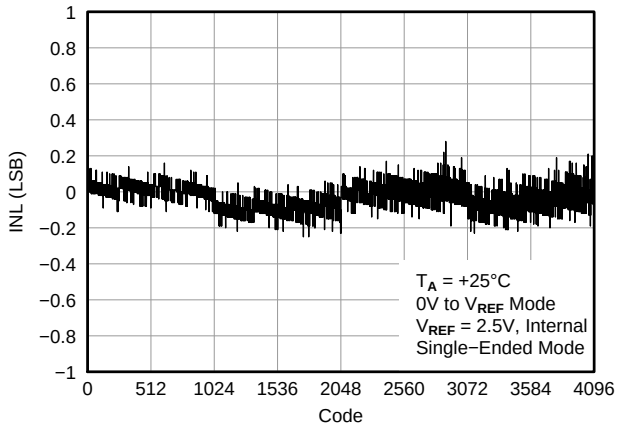


Figure 44.

DIFFERENTIAL LINEARITY ERROR vs CODE

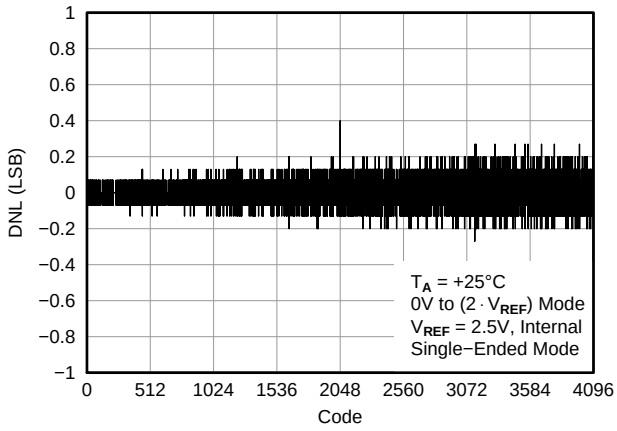


Figure 45.

LINEARITY ERROR vs CODE

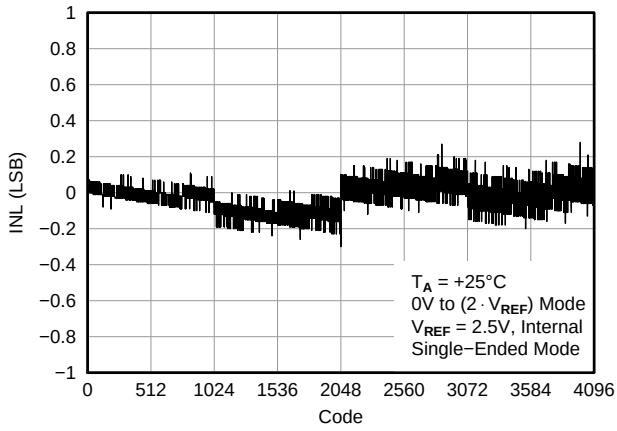


Figure 46.

DIFFERENTIAL LINEARITY ERROR vs CODE

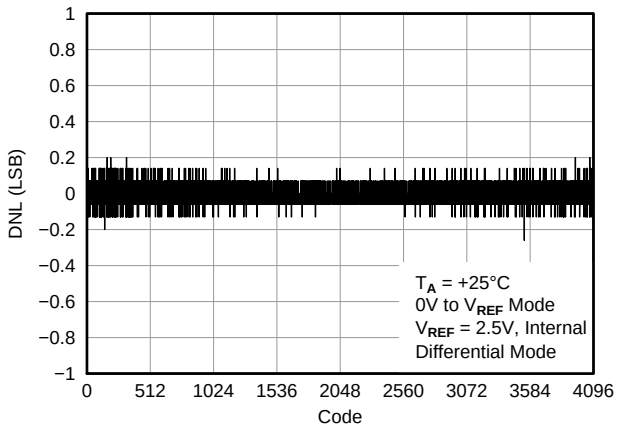


Figure 47.

LINEARITY ERROR vs CODE

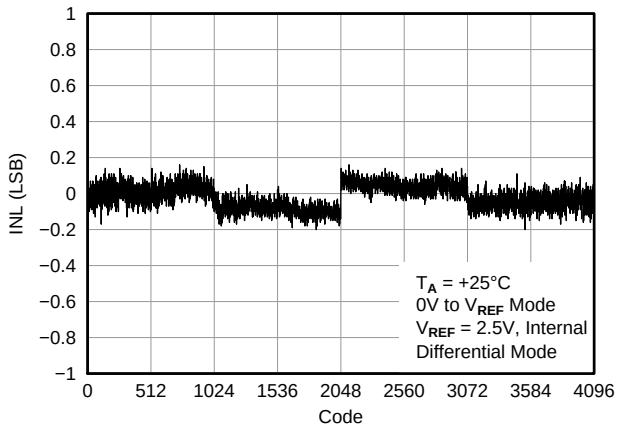


Figure 48.

TYPICAL CHARACTERISTICS: ADC (continued)

At +25°C, unless otherwise noted.

DIFFERENTIAL LINEARITY ERROR vs CODE

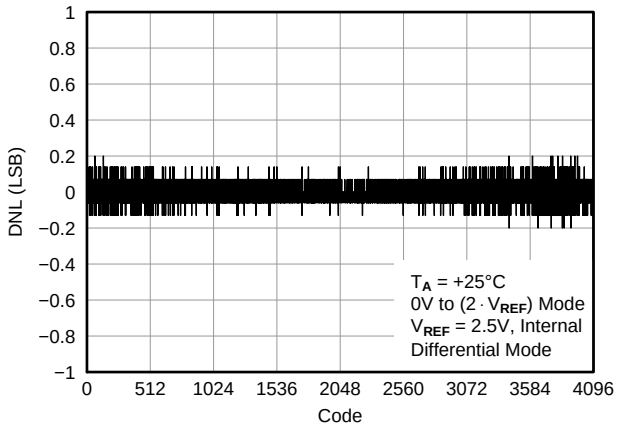


Figure 49.

LINEARITY ERROR vs CODE

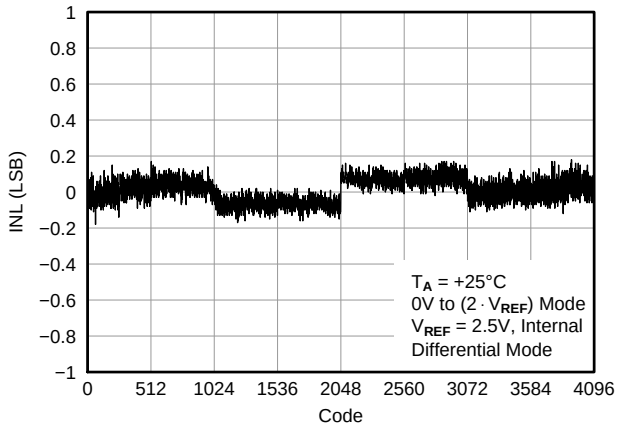


Figure 50.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

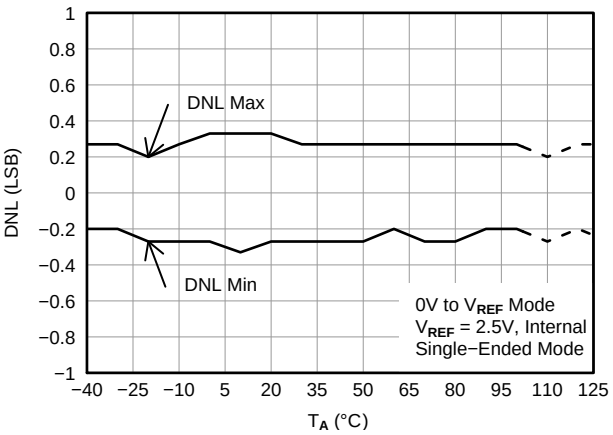


Figure 51.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

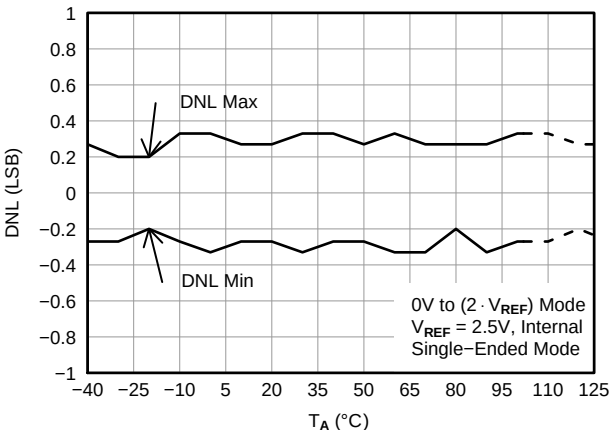


Figure 52.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

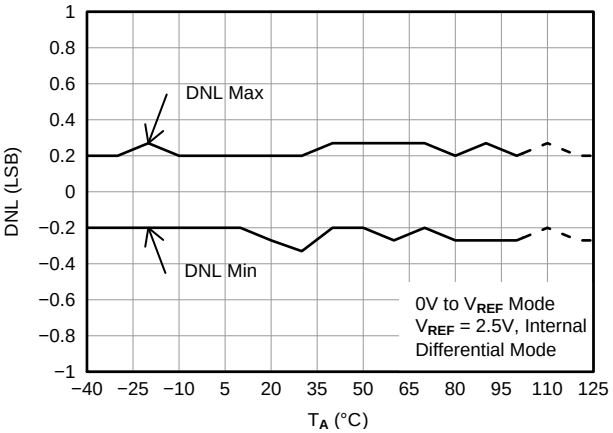


Figure 53.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

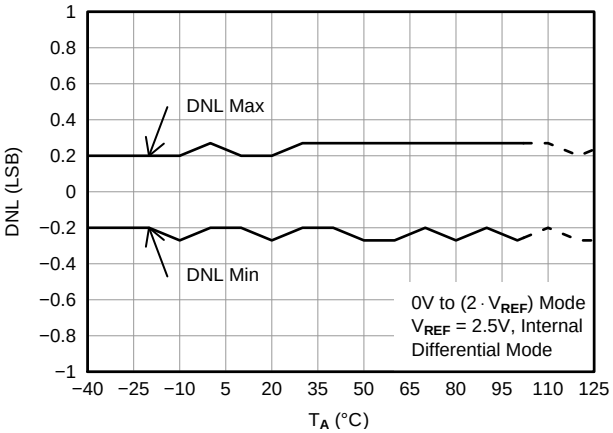


Figure 54.

TYPICAL CHARACTERISTICS: ADC (continued)

At +25°C, unless otherwise noted.

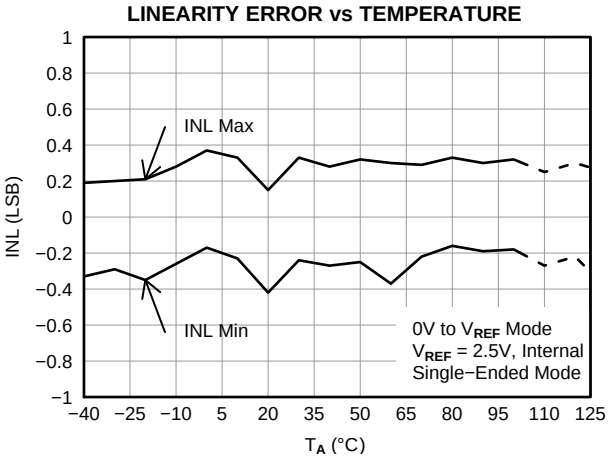


Figure 55.

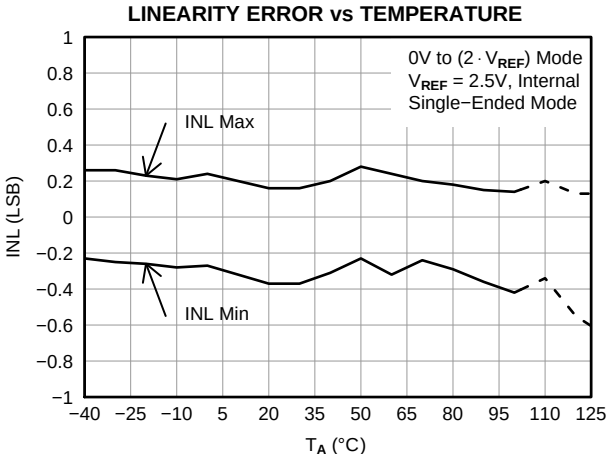


Figure 56.

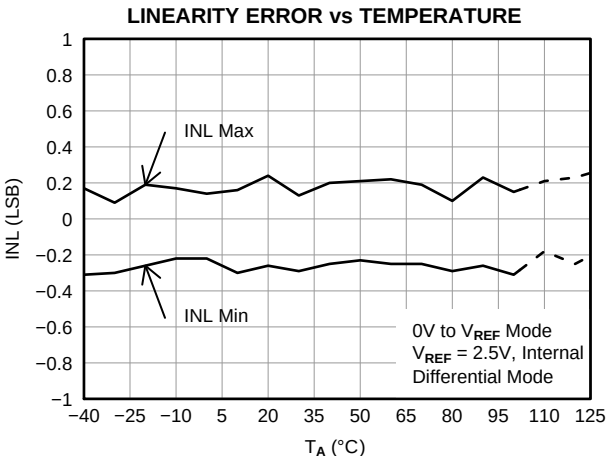


Figure 57.

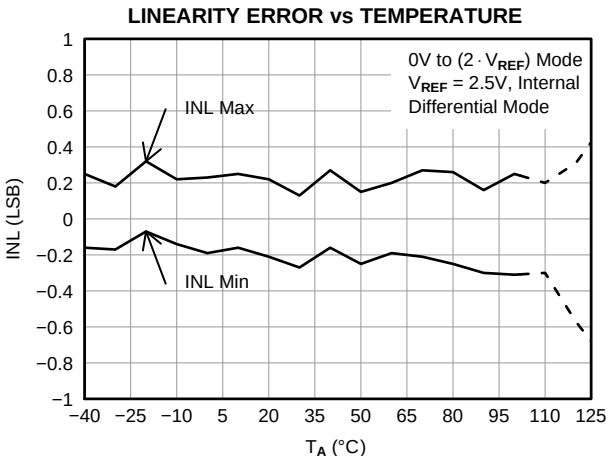


Figure 58.

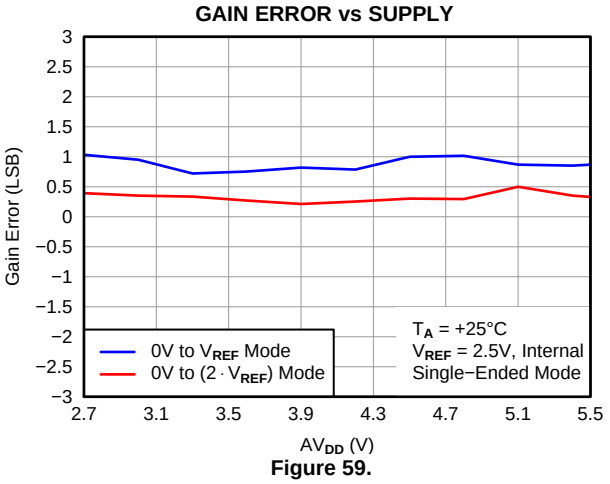


Figure 59.

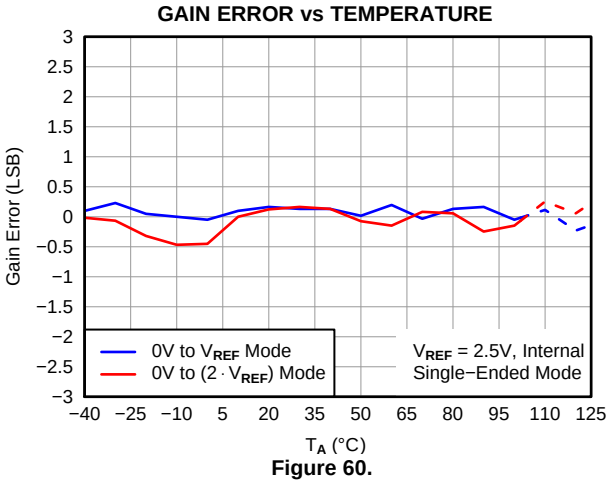


Figure 60.

TYPICAL CHARACTERISTICS: ADC (continued)

At +25°C, unless otherwise noted.

OFFSET vs TEMPERATURE

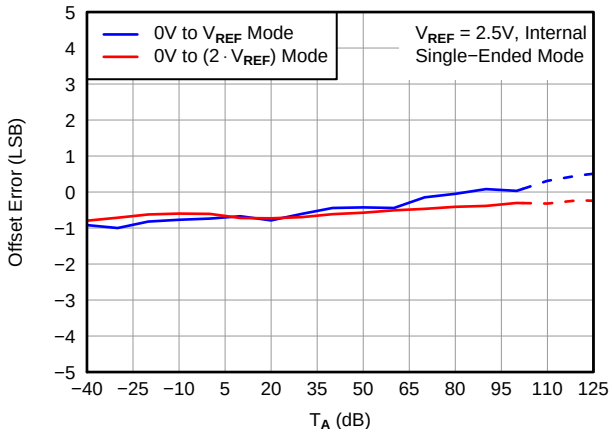


Figure 61.

CONVERSION FREQUENCY

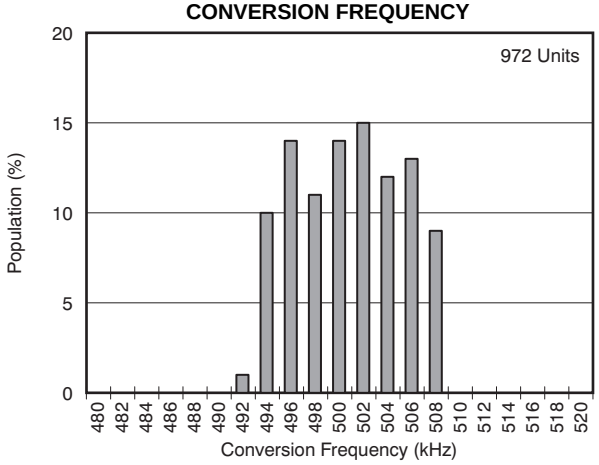


Figure 62.

CONVERSION FREQUENCY vs SUPPLY

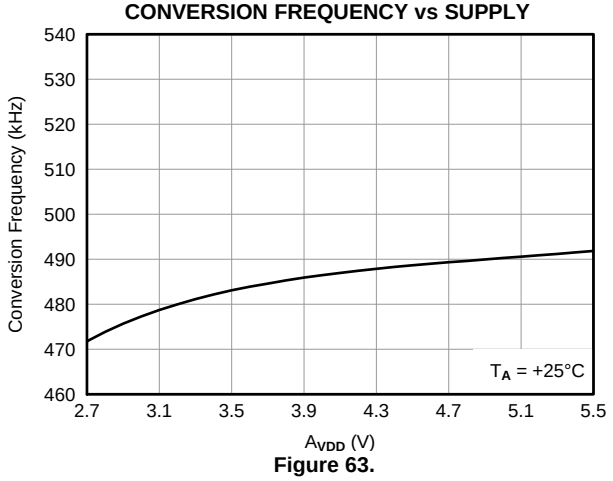


Figure 63.

CONVERSION FREQUENCY vs TEMPERATURE

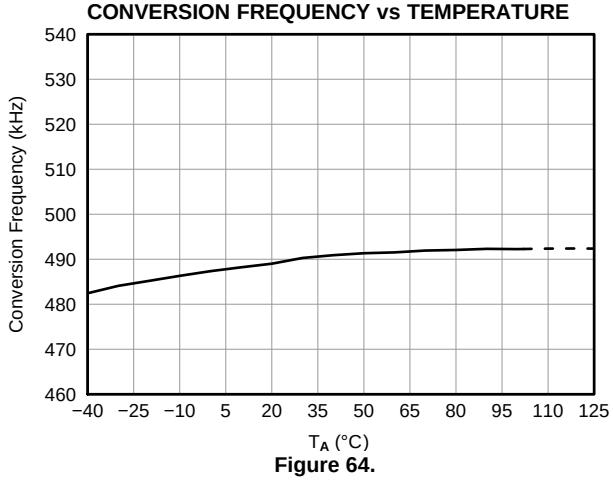


Figure 64.

SUPPLY CURRENT vs SUPPLY VOLTAGE

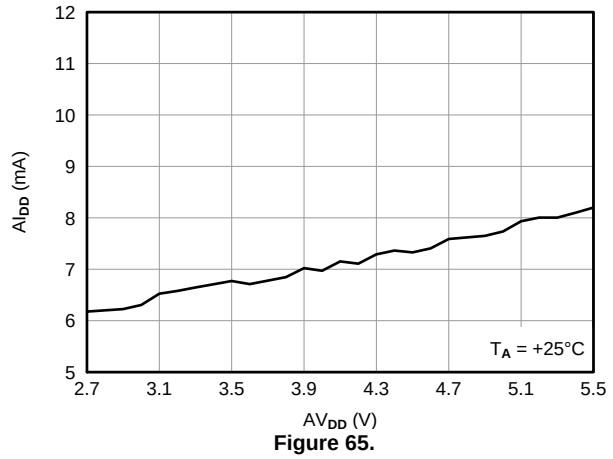


Figure 65.

SUPPLY CURRENT vs TEMPERATURE

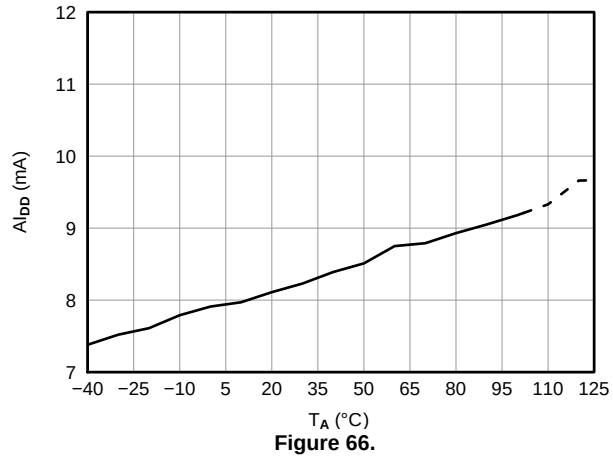


Figure 66.

TYPICAL CHARACTERISTICS: ADC (continued)

At +25°C, unless otherwise noted.

SUPPLY CURRENT vs CONVERSION RATE

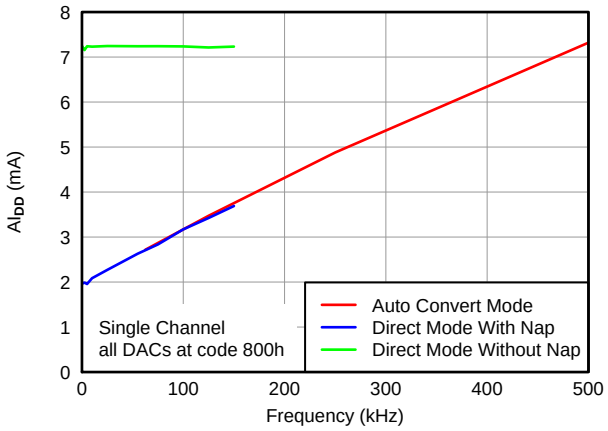


Figure 67.

COMBINED AV_{DD} AND DV_{DD} SUPPLY CURRENT

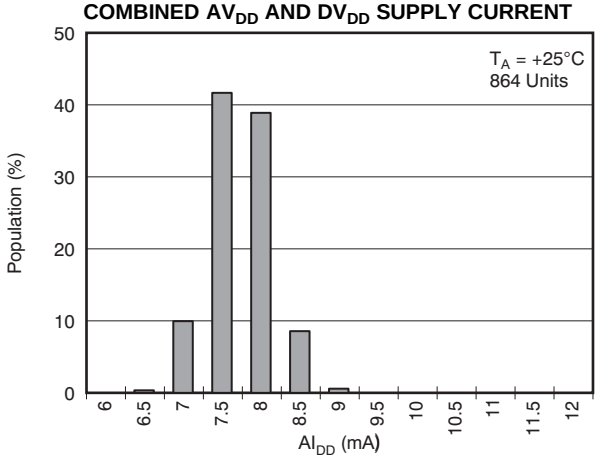


Figure 68.

TYPICAL CHARACTERISTICS: INTERNAL REFERENCE

At +25°C, unless otherwise noted.

OUTPUT VOLTAGE vs TEMPERATURE

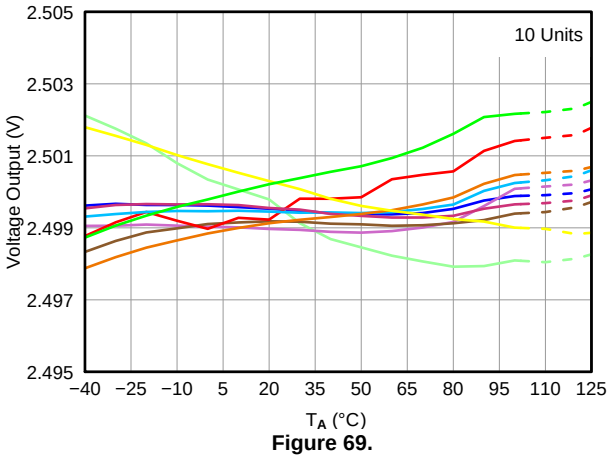


Figure 69.

OUTPUT VOLTAGE vs SUPPLY

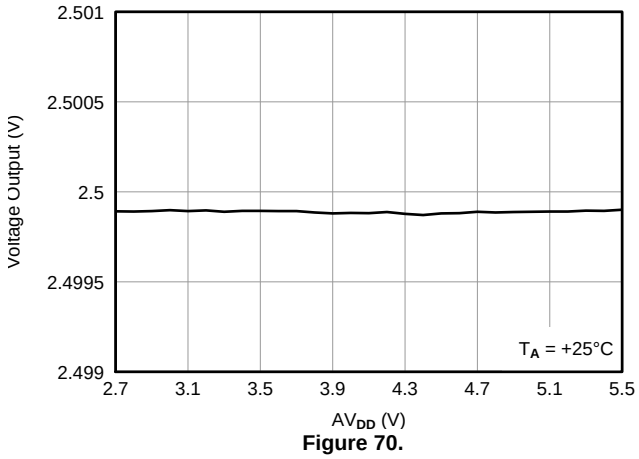


Figure 70.

OUTPUT VOLTAGE vs OUTPUT CURRENT

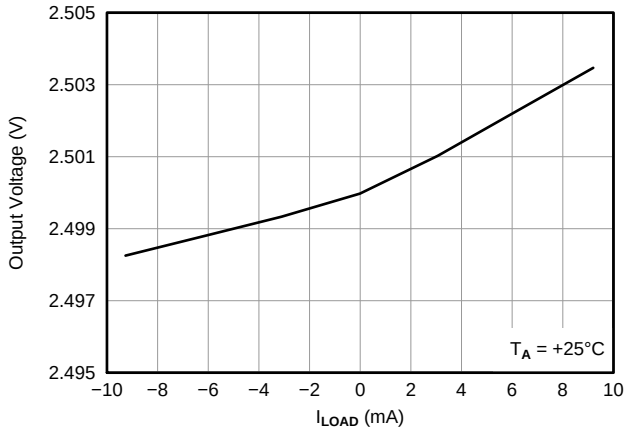


Figure 71.

OUTPUT VOLTAGE DRIFT

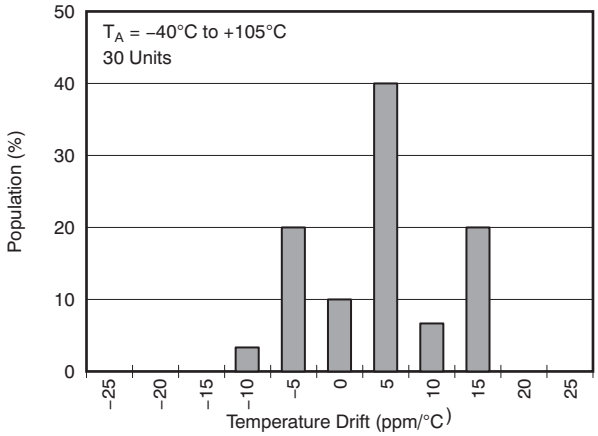


Figure 72.

INTERNAL REFERENCE NOISE vs FREQUENCY

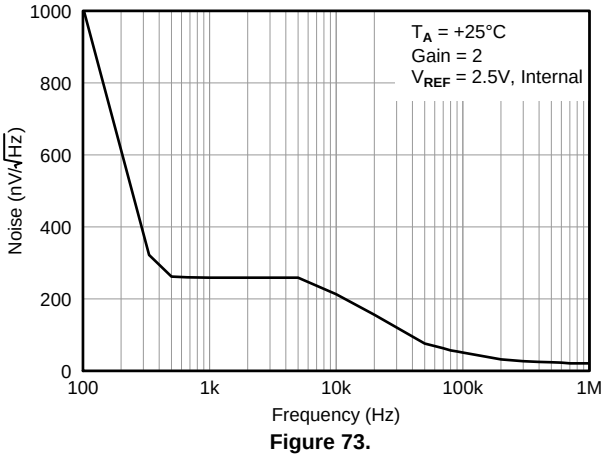


Figure 73.

INTERNAL REFERENCE NOISE 0.1Hz to 10Hz

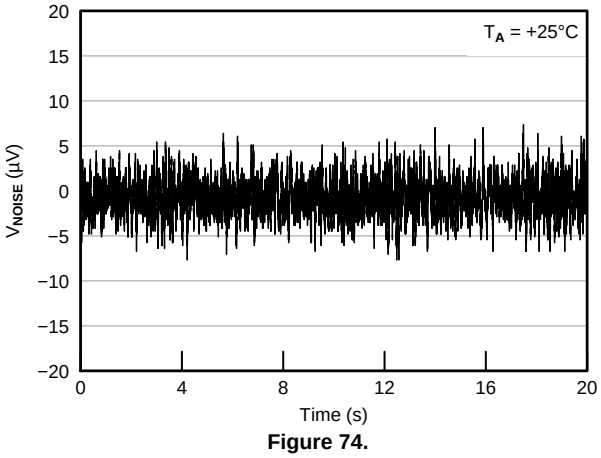


Figure 74.

TYPICAL CHARACTERISTICS: TEMPERATURE SENSOR

At +25°C, unless otherwise noted.

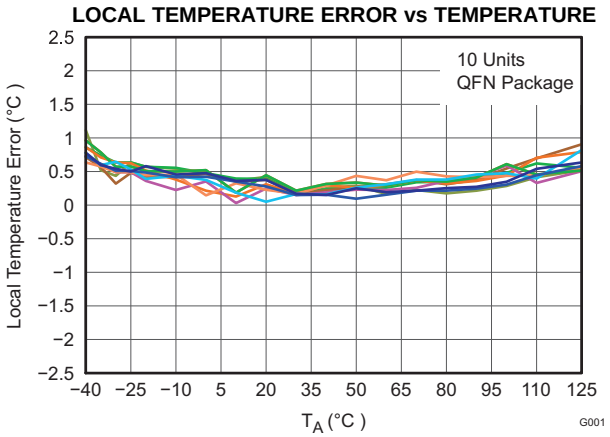


Figure 75.

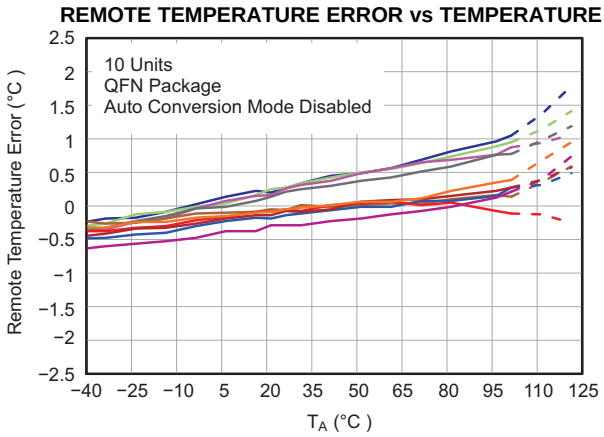


Figure 76.

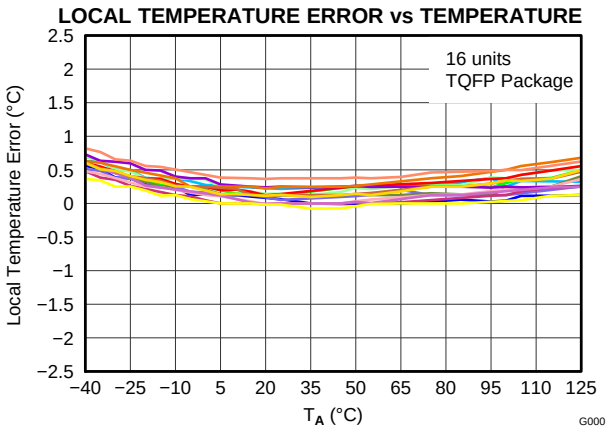


Figure 77.

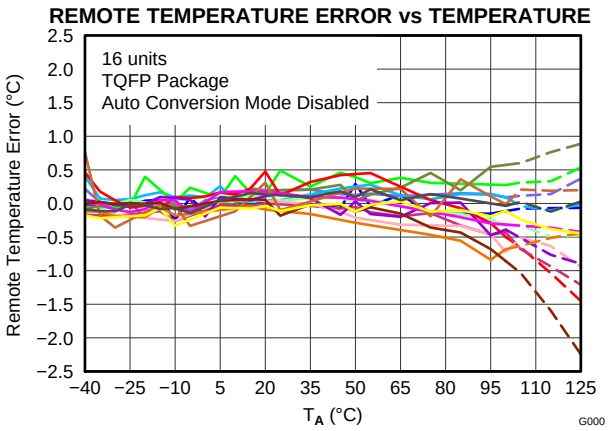


Figure 78.

TYPICAL CHARACTERISTICS: DIGITAL INPUTS

At +25°C, unless otherwise noted.

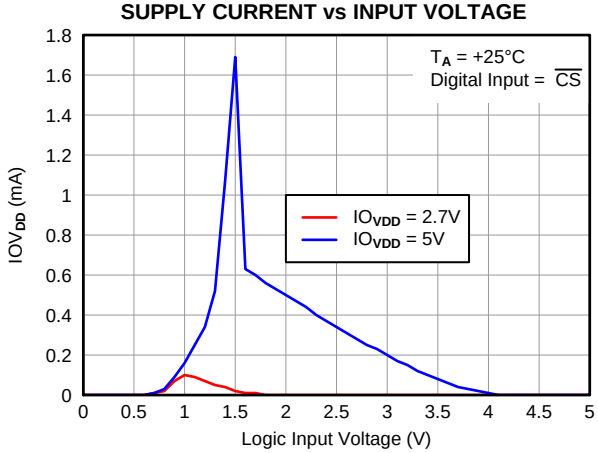


Figure 79.

THEORY OF OPERATION

ADC OVERVIEW

The AMC7812 has two analog-to-digital converters (ADCs): a primary ADC and a secondary ADC. The primary ADC features a 16-channel multiplexer, an on-chip track-and-hold, and a successive approximation register (SAR) ADC based on a capacitive digital-to-analog converter (DAC). This ADC runs at 500kSPS and converts the analog channel inputs, CH0 to CH15. The analog input range for the device can be selected as 0V to V_{REF} or 0V to ($2 \cdot V_{REF}$). The analog input can be configured for either single-ended or differential signals. The AMC7812 has an on-chip 2.5V reference that can be disabled when an external reference is preferred. If the internal ADC reference is to be used elsewhere in the system, the output must first be buffered. The various monitored and uncommitted input signals are multiplexed into the ADC. The secondary ADC is a part of the temperature sensing function that converts the analog temperature signals.

ANALOG INPUTS

The AMC7812 has 16 uncommitted analog inputs; 12 of these inputs (CH4 to CH15) are single-ended. The inputs for CH0 to CH3 can be configured as four single-ended inputs or two fully-differential channels, depending on the setup of the ADC Channel Registers, ADC Channel Register 0 and ADC Channel Register 1. See the *Registers* section for details. Figure 80 shows the equivalent input circuit of the AMC7812. The (peak) input current through the analog inputs depends on the sample rate, input voltage, and source impedance. The current into the AMC7812 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance to a 12-bit settling level within the acquisition time. When the converter goes into hold mode, the input impedance is greater than 1GΩ.

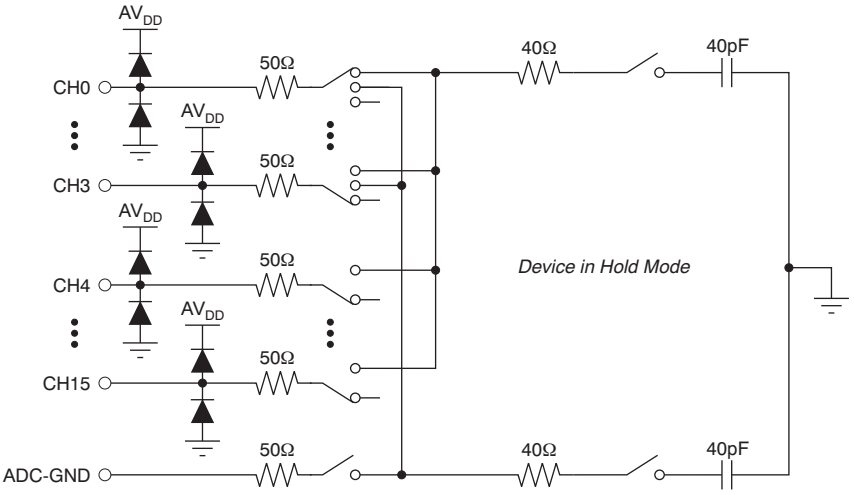


Figure 80. Equivalent Input Circuit

Single-Ended Analog Input

In applications where the signal source has high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range can be programmed to be either 0V to V_{REF} or 0V to $(2 \cdot V_{REF})$. In $2 \cdot V_{REF}$ mode, the input is effectively divided by two before the conversion takes place. Note that the voltage with respect to GND on the ADC analog input pins cannot exceed AV_{DD}.

Fully-Differential Input

When the AMC7812 is configured as a differential input, the differential signal is defined as V_{DM}, as shown in Figure 81(a). It is the equivalent of the difference between the signals of V1 and V2, as shown in Figure 81(b). The common-mode input V_{COMMON} is equal to (V1 + V2)/2.

When the conversion occurs, only the differential mode voltage (V_{DM}) is converted; the common mode voltage (V_{COMMON}) is rejected. This process results in a virtually noise-free signal with a maximum amplitude of $-V_{REF}$ to $+V_{REF}$ for V_{REF} range, or $(-2 \cdot V_{REF})$ to $(+2 \cdot V_{REF})$ for $(2 \cdot V_{REF})$ range. The results are stored in straight binary or twos complement format.

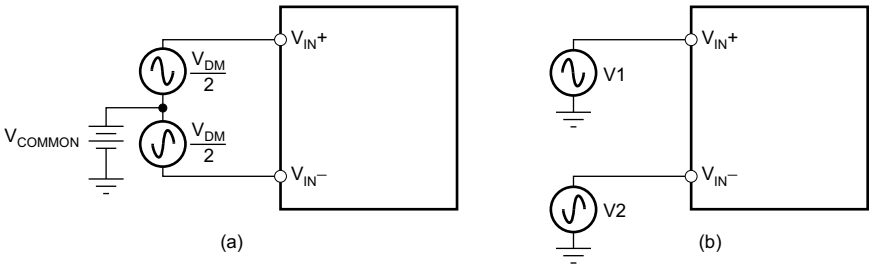


Figure 81. Fully-Differential Analog Input

PRIMARY ADC OPERATION

The following sections describe the operation of the primary ADC.

ADC Trigger Signals (see AMC Configuration Register 0)

The ADC can be triggered externally by the falling edge of the external trigger $\overline{CNVT}$, or internally by writing to the ICONV bit in AMC Configuration Register 0. The ADC Channel Registers specify which external analog channel is converted.

When a new trigger activates, the ADC stops any existing conversion immediately and starts a new cycle. For example, the ADC is programmed to sample channel 0 to channel 3 repeatedly (auto-mode). During the conversion of channel 1, an external trigger is activated. The ADC stops the conversion of channel 1 immediately and starts the conversion of channel 0 again, instead of proceeding to convert channel 2.

Conversion Mode

Two types of ADC conversions are available: direct mode and auto mode. The CMODE (conversion mode) bit of the AMC Configuration 0 Register specifies the conversion mode.

In direct mode, each analog channel within the specified group is converted a single time. After the last channel is converted, the ADC goes into an idle state and waits for a new trigger.

Auto mode is a continuous operation. In auto mode, each analog channel within the specified group is converted sequentially and repeatedly.

The flow chart of the ADC conversion sequence in Figure 82 shows the conversion process.

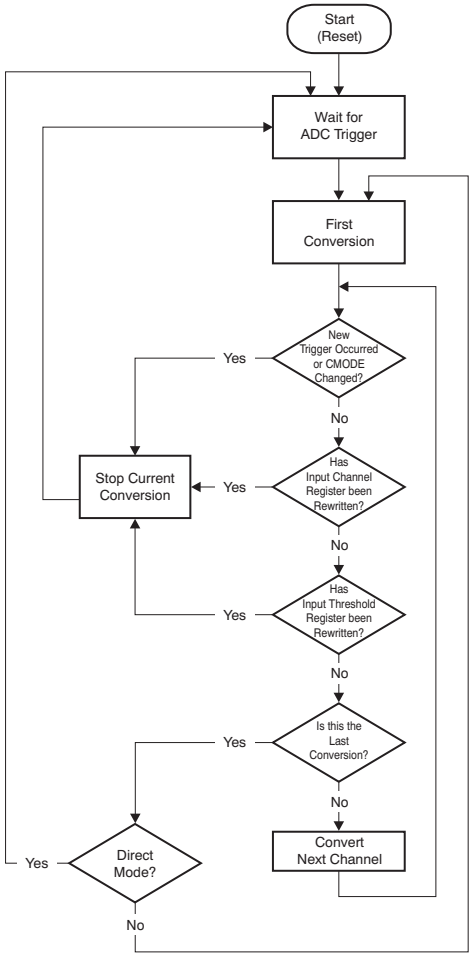


Figure 82. ADC Conversion Sequence

When any of following events occur, the current conversion cycle stops immediately:

- A new trigger is issued.
- The conversion mode changes.
- Either ADC channel register is rewritten.
- Any of the analog input threshold registers is rewritten.

When a new external or internal trigger activates, the ADC starts a new conversion cycle.

The internal trigger should not be issued at the same time the conversion mode is changed. If a '1' is simultaneously written to the ICONV bit when changing the CMODE bit to '0' or '1', the current conversion stops and immediately returns to the *wait for ADC trigger* state.

Double-Buffered ADC Data Registers

The host can access all sixteen, double-buffered ADC Data Registers, as shown in Figure 83. The conversion result from the analog input with channel address *n* (where n = 0 to 15) is stored in the ADC-*n*-Data Register. When the conversion of an individual channel is completed, the data are immediately transferred into the corresponding ADC-*n* temporary (TMPRY) register, the first stage of the data buffer. When the conversion of the last channel completes, all data in the ADC-*n* TMPRY Registers are simultaneously transferred into the corresponding ADC-*n*-Data Registers, the second stage of the data buffer. However, if a data transfer is in progress between any ADC-*n*-Data Register and the AMC Shift Register, all ADC-*n*-Data Registers are not updated until the data transfer is complete. The conversion result from channel address *n* is stored in the ADC-*n*-Data Register. For example, the result from channel 0 is stored in the ADC-0-Data Register, and the result from channel 3 is stored in the ADC-3-Data Register.

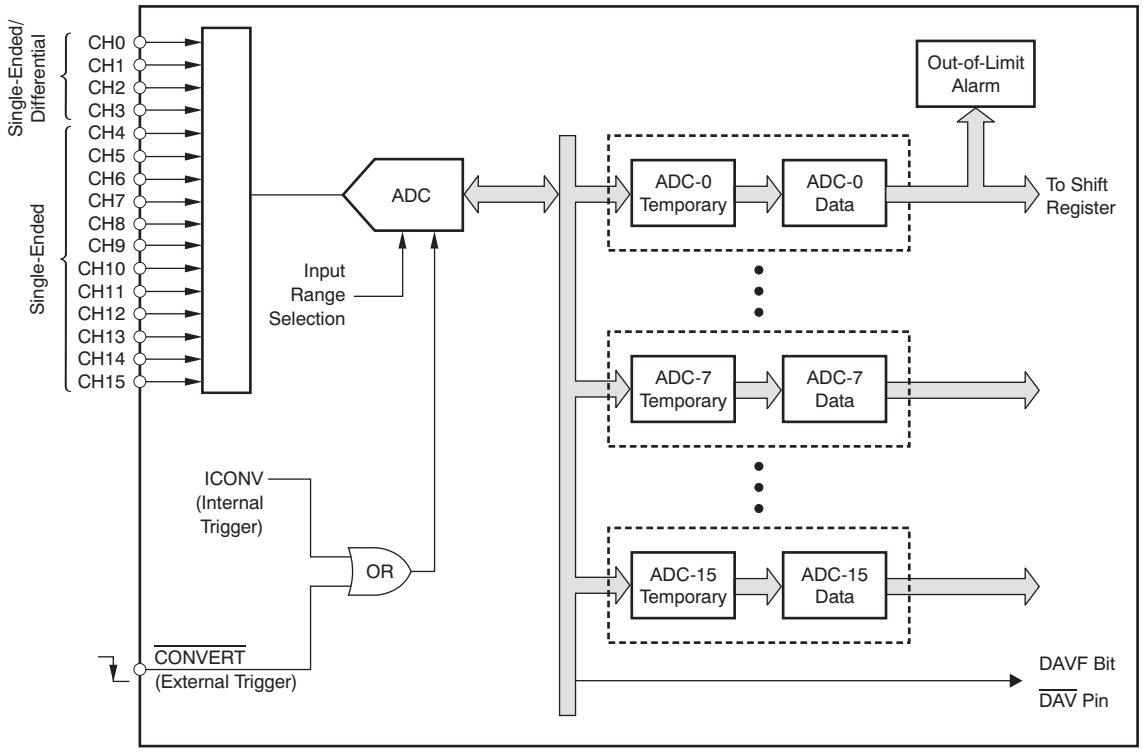


Figure 83. Double-Buffered ADC Structure

ADC Data Format

For a single ended input, the conversion result is stored in straight binary format. For a differential input, the results are stored in twos complement format.

SCLK Clock Noise Reduction

To avoid noise caused by the bus clock, it is recommended that no bus clock activity occurs for at least the conversion process time immediately after the ADC conversion starts.

Programmable Conversion Rate

The maximum conversion rate is 500kSPS for a single channel in auto mode, as shown in Table 1. The conversion rate is programmable through the CONV-RATE-[1:0] bits of AMC Configuration Register 1. When more than one channel is selected, the conversion rate is divided by the number of channels selected in ADC Channel Register 0 and ADC Channel Register 1. In auto mode, the CONV-RATE-[1:0] bits determine the actual conversion rate. In direct mode, the CONV-RATE-[1:0] bits limit the maximum possible conversion rate. The actual conversion rate in direct mode is determined by the rate of the conversion trigger. Note that when a trigger is issued, there may be a delay of up to 4µs to internally synchronize and initiate the start of the sequential channel conversion process. In both direct and auto modes, when the CONV-RATE-[1:0] bits are set to a value other than the maximum rate ('00'), nap mode is activated between conversions. By activating nap mode, the AI_{DD} supply current is reduced; see Figure 67.

Table 1. ADC Conversion Rate

CONV-RATE-1	CONV-RATE-0	t_{ACQ} (µs)	t_{CONV} (µs)	NAP ENABLED	THROUGHPUT (Single-Channel Auto Mode)
0	0	0.375	1.625	No	500kSPS (default)
0	1	2.375	1.625	Yes	250kSPS
1	0	6.375	1.625	Yes	125kSPS
1	1	14.375	1.625	Yes	62.5kSPS

Handshaking with the Host (see AMC Configuration Register 0)

The DAV pin and the DAVF (data available flag) bit in AMC Configuration Register 0 provide handshaking with the host. Pin and bit status depend on the conversion mode (direct or auto), as shown in Figure 84 and Figure 85. In direct mode, after ADC-*n*-Data Registers of all of the selected channels are updated, the DAVF bit in AMC Configuration Register 0 is set immediately to '1', and the DAV pin is active (low) to signify that new data are available. Reading the ADC-*n*-Data Register or restarting via the external $\overline{\text{CNVT}}$ pin, the ADC clears the DAVF bit to '0' and deactivates the DAV pin (high). If an internal convert start (ICONV bit) is used to start the new ADC conversion, in order to reset the DAV status, an ADC-*n*-Data Register must be read after the current conversion finishes before a new conversion can be started.

In auto-mode, after the ADC-*n*-Data Registers of the selected channels are updated, a pulse of 1µs (low) appears on the DAV pin to signify that new data are available. However, the DAVF bit is always cleared to '0' in auto-mode.

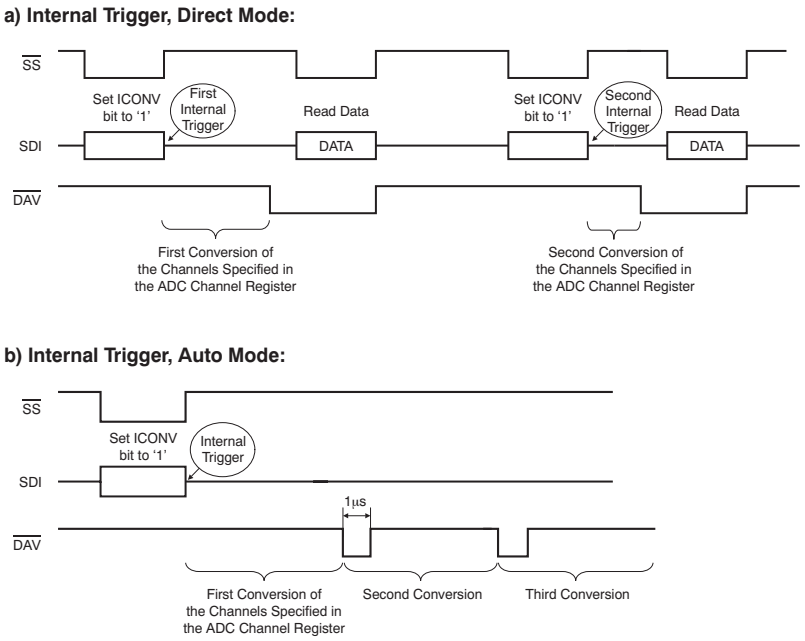


Figure 84. ADC Internal Trigger

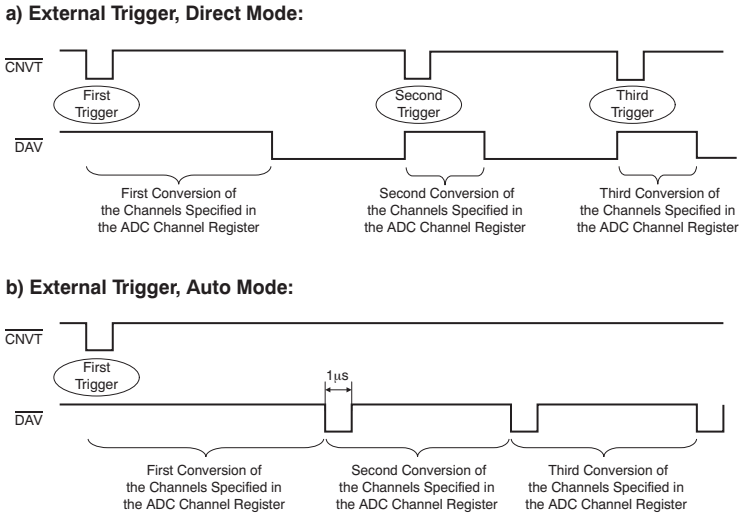


Figure 85. ADC External Trigger

Data Available Pin ($\overline{DAV}$)

$\overline{DAV}$ is an output pin that indicates the completion of ADC conversions. The DAVF bit in AMC Configuration Register 0 determines the status of the $\overline{DAV}$ pin. In direct mode, after the selected group of input channels have been converted and the ADC has been stopped, the DAVF bit is set to '1' and the $\overline{DAV}$ pin is driven to logic low (active). In ADC auto mode, each time the group of input channels have been sequentially converted, a 1µs pulse (low) appears on the $\overline{DAV}$ pin.

Convert Pin ($\overline{CNVT}$)

$\overline{CNVT}$ is the input pin for the external ADC trigger signal. ADC channel conversions begin on the falling edge of the $\overline{CNVT}$ pulse. If a $\overline{CNVT}$ pulse occurs when the ADC is already converting, then the ADC continues conversion of the current channel. After the completion of the current channel, the existing conversion cycle finishes and a new conversion cycle starts. The selected channels specified in the ADC Channel Registers are converted sequentially in order of enabled channels.

Analog Input Out-of-Range Detection (see the *Analog Input Out-of-Range Alarm* Section)

The analog inputs of CH0 to CH3 and the temperature inputs are implemented with out-of-range detection. When any one of them is out of the preset range, the corresponding alarm flag in the Status Register is set. If any inputs are out of range, the global out-of-range pin ($\overline{ALARM}$) goes low. To avoid a false alarm, the device is implemented with false-alarm protection. See the *Alarm Operation* section for more details.

Full-Scale Range of the Analog Input

The Gain bit of the ADC Gain Register determines the full-scale range of the analog input. Full-scale range is V_{REF} when ADG*n* = 0, or $(2 \cdot V_{REF})$ when ADG*n* = 1. If a channel pair is configured for differential operation, the input ranges are either $\pm V_{REF}$ or $\pm(2 \cdot V_{REF})$. In $(2 \cdot V_{REF})$ mode, the input is effectively divided by two before the conversion takes place. Each input must not exceed the supply value of AV_{DD} + 0.2V or AGND - 0.2V. When the REF-OUT pin is connected to the REF-ADC pin, the internal reference is used as the ADC reference. When an external reference voltage is applied to the REF-ADC pin, the external reference is used as the ADC reference.

SECONDARY ADC/TEMPERATURE SENSOR OPERATION

The AMC7812 contains one local and two remote temperature sensors. The temperature sensors continuously monitor the three temperature inputs, and new readings are automatically available every cycle. The on-chip integrated temperature sensor (shown in Figure 86) is used to measure the device temperature, and two remote diode sensor inputs are used to measure the two external temperatures. All analog signals are converted by the secondary ADC that runs in the background at a lower speed. The measurement relies on the characteristics of a semiconductor junction operation at a fixed current level. The forward voltage of the diode (V_{BE}) depends on the current passing through it and the ambient temperature. The change in V_{BE} when the diode operates at two different currents (a low current of I_{LOW} and a high current of I_{HIGH}, is shown in Equation 1:

$$V_{BE\_HIGH} - V_{BE\_LOW} = \frac{\eta kT}{q} \ln\left(\frac{I_{HIGH}}{I_{LOW}}\right) \quad (1)$$

Where:

k is Boltzmann's constant.
q is the charge of the carrier.
T is the absolute temperature in Kelvins (K).
η is the ideality of the transistor as sensor.

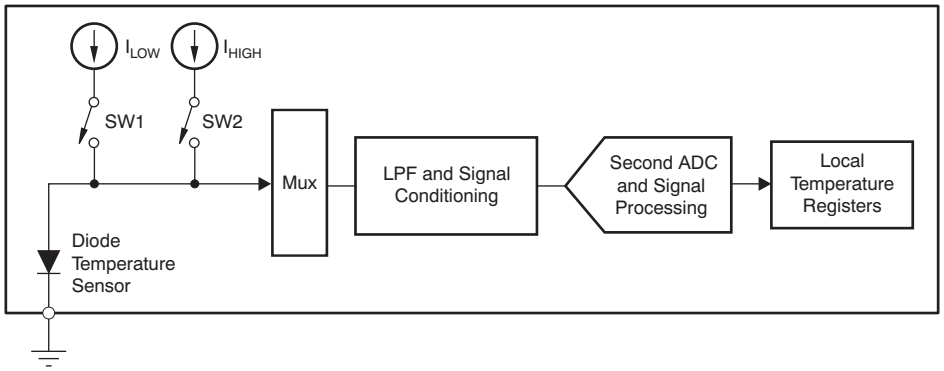


Figure 86. Integrated Local Temperature Sensor

The remote sensing transistor can be a discrete small-signal type transistor or substrate transistor built within the microprocessor. This architecture is shown in Figure 87. An internal voltage source biases the D– terminal above ground to prevent the ground noise from interfering with the measurement. An external capacitor (up to 330pF) may be placed between D+ and D– to further reduce noise interference.

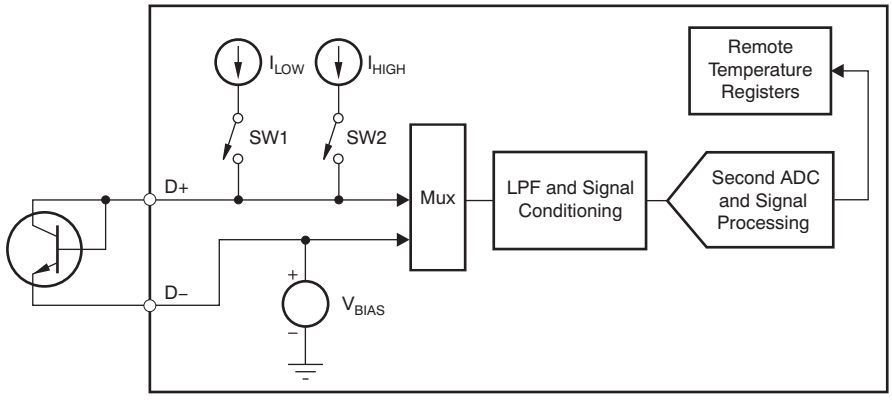


Figure 87. Remote Temperature Sensor

The AMC7812 has three temperature sensors: two remote (D1 and D2) and one on-chip (LT). If any sensor is not used, it can be disabled by clearing the corresponding enable bit (bits D2EN, D1EN, and LTEN of the Temp Configuration Register). When disabled, the sensors are not converted. The AMC7812 continuously monitors the selected temperature sensors in the background, leaving the user free to perform conversions on the other channels. When one monitor cycle finishes, a signal passes to the control logic to automatically initiate a new conversion.

The analog sensing signal is preprocessed by a low-pass filter and signal conditioning circuitry, and then digitized by the ADC. The resulting digital signal is further processed by the digital filter and processing unit. The final result is stored in the LT-Temperature-Data Register, the D1-Temperature-Data Register, and the D2-Temperature-Data Register, respectively. The format of the final result is in twos complement, as shown in Table 2. Note that the device measures the temperature from –40°C to +150°C.

Table 2. Temperature Data Format

TEMPERATURE (°C)	DIGITAL CODE
+255.875	011111111111
+150	010010110000
+100	001100100000
+50	000110010000
+25	000011001000
+1	000000001000
0	000000000000
–1	111111111000
–25	111100111000
–50	111001110000
–100	110011100000
–150	101101010000
–256	100000000000

Remote Sensing Diode

Errors in remote temperature sensor readings are typically the consequence of the ideality factor and current excitation used by the AMC7812 versus the manufacturer-specified operating current for a given transistor. Some manufacturers specify a low-level (I_{LOW}) and high-level (I_{HIGH}) current for the temperature-sensing substrate transistors. The AMC7812 uses 6µA for I_{LOW} and 120µA for I_{HIGH}. The AMC7812 is designed to work with discrete transistors, such as the 2N3904 and 2N3906. If an alternative transistor is used, the AMC7812 operates as specified, as long as the following conditions are met:

1. Base-emitter voltage > 0.25V at 6µA, at the highest sensed temperature.
2. Base-emitter voltage < 0.95V at 120µA, at the lowest sensed temperature.
3. Base resistance < 100Ω.
4. Tight control of V_{BE} characteristics indicated by small variations in h_{FE} (that is, 50 to 150).

Ideality Factor

The ideality factor (η) is a measured characteristic of a remote temperature sensor diode as compared to an ideal diode. The AMC7812 allows for different η-factor values, according to Table 3. The AMC7812 is trimmed for a power-on reset (POR) value of η = 1.008. If η is different, the η-Factor Correction Register can be used. The value (N_{ADJUST}) written in this register must be in twos complement format, as shown in Table 3. This value is used to adjust the effective η-factor according to Equation 2 and Equation 3.

Table 3. η-Factor Range (Single Byte)

N_{ADJUST}			η_{EFF}
BINARY	HEX	DECIMAL	
0111 1111	7F	127	1.747977
0000 1010	0A	10	1.042759
0000 1000	08	8	1.035616
0000 0110	06	6	1.028571
0000 0100	04	4	1.021622
0000 0010	02	2	1.014765
0000 0001	01	1	1.011371
0000 0000	00	0	1.008
1111 1111	FF	–1	1.004651
1111 1110	FE	–2	1.001325
1111 1100	FC	–4	0.994737
1111 1010	FA	–6	0.988235
1111 1000	F8	–8	0.981818
1111 0110	F6	–10	0.975484
1000 0000	80	–128	0.706542

$$\eta_{eff} = \frac{1.008 \times 300}{300 - N_{ADJUST}} \quad (2)$$

$$N_{ADJUST} = 300 - \left(\frac{300 \times 1.008}{\eta_{eff}} \right)$$

Where:

η_{EFF} is the actual ideality of the transistor being used
N_{ADJUST} is the corrected ideality being used in the calculation (3)

Filtering

Figure 88 shows the connection of recommended (a) NPN or (b) PNP transistors. Remote junction temperature sensors are usually implemented in a noisy environment. Noise is most often created by fast digital signals, and it can corrupt measurements. The AMC7812 has a built-in 65kHz filter on the inputs of D+ and D-, to minimize the effects of noise. However, a bypass capacitor placed differentially across the inputs of the remote temperature sensor can make the application more robust against unwanted coupled signals. If filtering is required, the capacitance between D+ and D– should be limited to 330pF or less for optimum measurement performance. This capacitance includes any cable capacitance between the remote temperature sensor and the AMC7812.

(a) NPN (b) PNP

Figure 88. Remote Temperature Sensor Using Transistor

Series Resistance Cancellation

Parasitic resistance (seen in series with the remote diode) to the D+ and D– inputs to the AMC7812 is caused by a variety of factors, including printed circuit board (PCB) trace resistance and trace length. This series resistance appears as a temperature offset in the remote sensor temperature measurement, and causes more than 0.45°C error per ohm. The AMC7812 implements a technology to automatically cancel out the effect of this series resistance, giving a more accurate result without the need for user characterization of this resistance. With this technology, the AMC7812 is able to reduce the effects of series resistance to typically less than 0.0075°C per ohm. The resistance cancellation is disabled when the RC bit in Temperature Configuration Register is cleared ('0').

Reading Temperature Data

The temperature is always read as 12-bit data. When the conversion finishes, the temperature is sent to the corresponding Temp-Data Register. However, if a data transfer is in progress between the Temp-Data Register and the AMC Shift Register, the Temp-Data Register is frozen until the data transfer is complete.

Conversion Time

The conversion time depends on the type of sensor and configuration, as shown in Table 4.

Table 4. Conversion Times

TEMPERATURE SENSOR	MONITORING CYCLE TIME (ms)	PROGRAMMABLE DELAY RANGE (s)
Local sensor is active, remote sensors are disabled or in power-down	15	0.48 to 3.84
One remote sensor is active and RC = '0', local sensor and one remote sensor are disabled or in power-down	44	1.40 to 11.2
One remote sensor is active and RC = '1', local sensor and one remote sensor are disabled or in power-down	93	2.97 to 23.8
One remote sensor and local sensor are active and RC = '0', one remote sensor is disabled or in power-down	59	1.89 to 15.1
One remote sensor and local sensor are active and RC = '1', one remote sensor is disabled or in power-down	108	3.45 to 27.65
Two remote sensors are active and RC = '0', local sensor is disabled or in power-down	88	2.81 to 22.5
Two remote sensors are active and RC = '1', local sensor is disabled or in power-down	186	5.95 to 47.6
All sensors are active and RC = '0'	103	3.92 to 26.38
All sensors are active and RC = '1'	201	6.43 to 51.45

REFERENCE OPERATION

The following sections describe the operation of the internal and external references.

Internal Reference

The AMC7812 includes a 2.5V internal reference. The internal reference is externally available at the REF-OUT pin. A 100pF to 10nF capacitor is recommended between the reference output and GND for noise filtering. The internal reference is a bipolar transistor-based, precision bandgap voltage reference. The output current is limited by design to approximately 100mA.

The internal reference drives all temperature sensors. When connecting the REF-OUT pin to the REF-DAC pin, the internal reference works as the DAC reference.

The ADC-REF-IN/CMP pin has a dual function. When an external reference is connected to this pin, the external reference is used as the ADC reference. When a compensation capacitor (4.7µF, typical) is connected between this pin and AGND, the internal reference is used as the ADC reference. When using an external reference to drive the ADC, the ADC-REF-INT bit in AMC Configuration Register 0 must be cleared ('0') to turn off the ADC reference buffer. When using the internal reference to drive the ADC, the ADC-REF-INT bit in AMC Configuration Register 0 must be set to '1' to turn on the ADC reference buffer.

External Reference

Figure 89 shows how the external reference is used as the DAC reference when applied on the DAC-REF pin, and as the ADC reference when applied on the ADC-REF pin. Figure 90 shows the use of the internal reference.

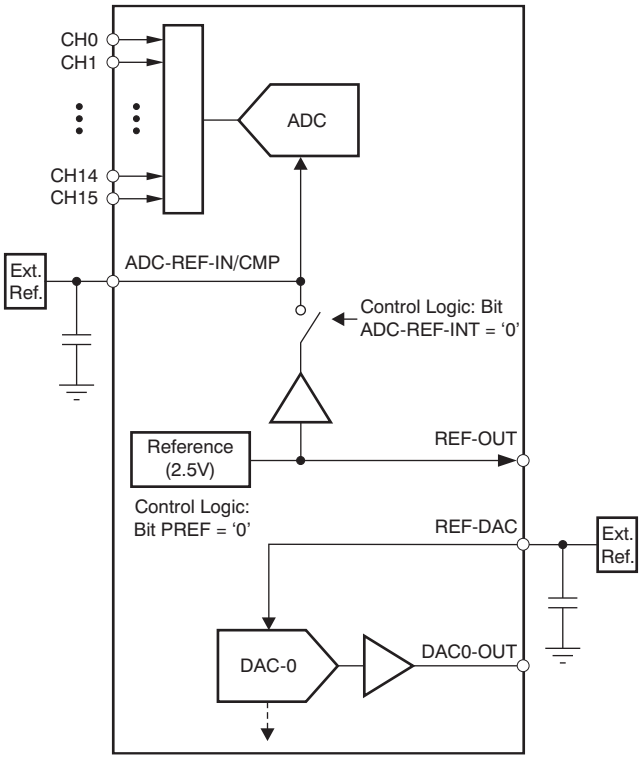


Figure 89. Use of the External Reference

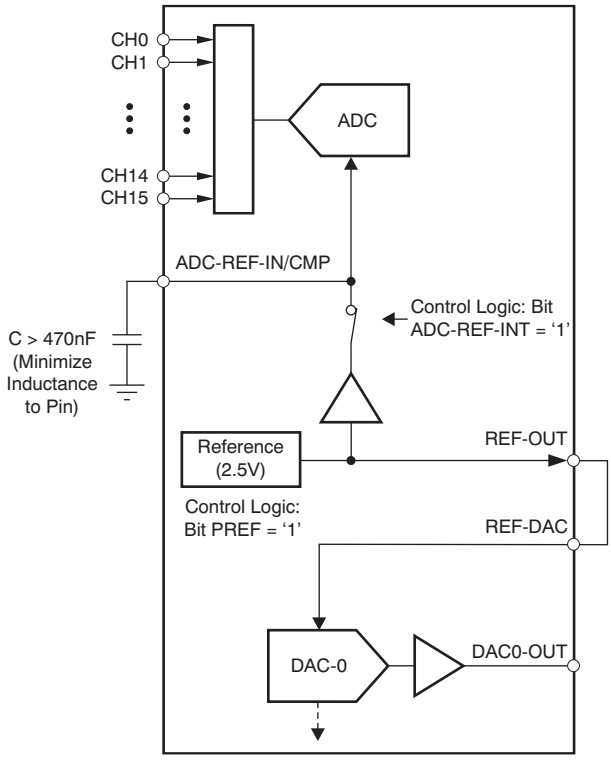
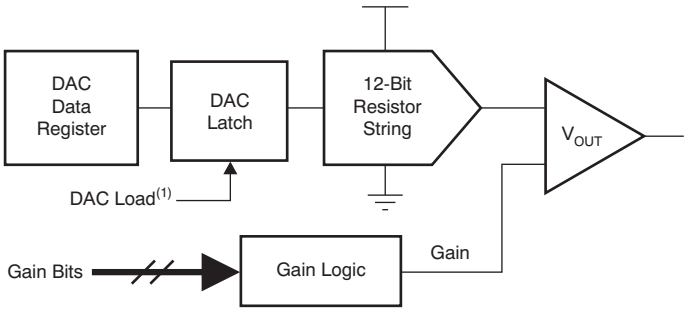


Figure 90. Use of the Internal Reference

DAC OPERATION

The AMC7812 contains 12 DACs that provide digital control with 12 bits of resolution using an internal or external reference. The DAC core is a 12-bit string DAC and output buffer. The DAC drives the output buffer to provide an output voltage. Refer to the DAC Configuration Register for details. Figure 91 shows a function block diagram of the DAC architecture. The DAC Latch stores the code that determines the output voltage from the DAC string. The code is transferred from the DAC-*n*-Data Register to the DAC Latch when the internal DAC-Load signal is generated.



(1) Internal DAC load is generated by writing '1' to ILDAC bit in synchronous mode. In asynchronous mode, the DAC latch is transparent.

Figure 91. DAC Block Diagram

Resistor String

The resistor string structure is shown in Figure 92. It consists of a string of resistors, each of value *R*. The code loaded to the DAC Latch determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. This architecture is inherently monotonic, voltage out, and low glitch. It is also linear because all the resistors are of equal value.

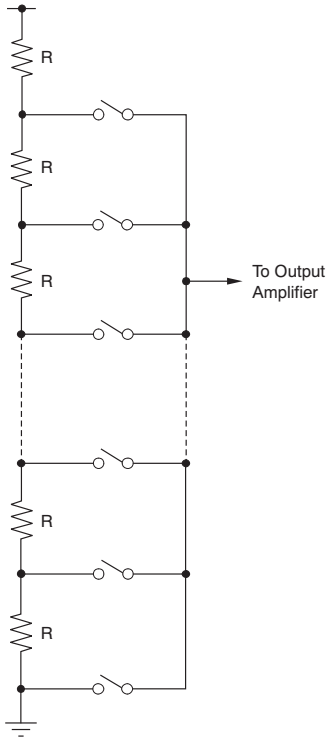


Figure 92. Resistor String

DAC Output

The output range is programmable from 0 to ($2 \cdot V_{REF}$) or from 0 to ($5 \cdot V_{REF}$), depending on the gain bits in the DAC Gain Register. The maximum output is AV_{CC}. The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0V to AV_{CC}. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics. The slew rate is 1.5V/µs with a typical ¼ to ¾ scale settling time of 3µs with the output unloaded.

Double-Buffered DAC Data Registers

There are 12 double-buffered DAC data registers. Each DAC has an internal latch preceded by a DAC Data Register. Data are initially written to an individual DAC-*n*-Data Register and then transferred to the corresponding DAC-*n* Latch. When the DAC-*n* Latch is updated, the output of DAC-*n* changes to the newly set value. When the host reads the register memory map location labeled DAC-*n* Data, the value held in the DAC-*n* Latch is returned (not the value held in the input DAC-*n*-Data Register).

Full-Scale Output Range

The full-scale output range of each DAC is set by the product of the value of the reference voltage times the gain of the DAC output buffer ($V_{REF} \cdot$ Gain). The gain bits of the DAC Gain Register set the output range of the individual DAC-*n*. The full-scale output range of each DAC is limited by the analog power supply. The maximum output from the DAC must not be greater than AV_{CC}, and the minimum output must not be less than AGND.

DAC Output After Power-On Reset

After power on, the DAC output buffer is in power-down mode. The output buffer is in a Hi-Z state and the DAC-Out output pin connects to the analog ground through an internal 10kΩ resistor. After power on or hardware reset, all DAC-*n*-Data Registers, all DAC-*n* Latches, and the DAC output are set to default values (000h).

Load DAC Latch

See Figure 91 for the structure of the DAC register and DAC latch. The contents of the DAC-*n* Latch determine the output level of the DAC-*n* pin. After writing to the DAC-*n*-Data Register, the DAC Latch can be loaded in the following ways:

- In asynchronous mode (SLDAC-*n* bit = '0'), the data are loaded into the DAC-*n* Latch immediately after the write operation.
- In synchronous mode (SLDAC-*n* bit = '1'), the DAC latch updates when the synchronous DAC loading signal occurs. Setting the ILDAC bit in AMC Configuration Register 0 generates the loading signal.

Synchronous Load, Asynchronous Load, and Output Updating

The SLDA-*n* (synchronous load) bit of the DAC Configuration Register determines the DAC updating mode, as shown in Table 5. When SLDA-*n* is cleared to '0', asynchronous mode is active, the DAC Latch updates immediately after writing to the DAC-*n*-Data Register, and the output of DAC-*n* changes accordingly.

Table 5. DAC-*n* Output Update Summary for Manual Mode Update

SLDA-*n* BIT	WRITING TO ILDAC BIT	OPERATION
0	Don't care	Update DAC-*n* individually. The DAC-*n* Latch and DAC-*n* output are immediately updated after writing to the DAC-*n*-Data Register.
1	1	Simultaneously update all DACs by internal trigger. Writing '1' to the ILDAC bit generates an internal load DAC trigger signal that updates the DAC-*n* Latches and DAC-*n* outputs with the contents of the corresponding DAC-*n*-Data Register.

When the SLDA-*n* bit is set to '1', synchronous mode is selected. The value of the DAC-*n*-Data Register is transferred to the DAC-*n* Latch only after an active DAC synchronous loading signal (ILDAC) occurs, which immediately updates the DAC-*n* output. Under synchronous loading operation, writing data into a DAC-*n*-Data Register changes only the value in that register, but not the content of DAC-*n* Latch nor the output of DAC-*n*, until the synchronous load signal occurs.

The DAC synchronous load is triggered by writing '1' to the ILDAC bit in AMC Configuration Register 0. When this DAC synchronous load signal occurs, all DACs with the SLDA-*n* bit set to '1' are simultaneously updated with the value of the corresponding DAC-*n*-Data Register. By setting the SLDA-n bit properly, several DACs can be updated at the same time. For example, to update DAC0 and DAC1 synchronously, set bits SLDA-0 and SLDA-1 to '1' first, and then write the proper values into the DAC-0 and DAC-1-Data Registers, respectively. After this presetting, set the ILDAC bit = '1' to simultaneously load DAC0 and DAC1. The outputs of DAC0 and DAC1 change at the same time.

The AMC7812 updates the DAC Latch only if it has been accessed since the last time ILDAC was issued, thereby eliminating any unnecessary glitch. Any DAC channels that have not been accessed are not reloaded again. When the DAC Latch is updated, the corresponding output changes to the new level immediately.

NOTE

When DACs are *cleared* by an external DAC-CLR-n or by the internal CLR bit, the DAC Latch is loaded with the predefined value of the DAC-*n*-CLR-Setting Register and the output is set to the corresponding level immediately, regardless of the SLDA-*n* bit value. However, the DAC Data Register does not change.

Clear DACs

DAC-*n* can be cleared using hardware or software as shown in Figure 93. When DAC-*n* goes to a *clear* state, it is immediately loaded with predefined code in the DAC-*n*-CLR-Setting Register, and the output is set to the corresponding level to shut down the external LDMOS device. However, the DAC-DATA-*n* Register does not change. When the DAC goes back to normal operation, DAC-*n* is immediately loaded with the previous data from the DAC-DATA-*n* Register and the output of DAC-*n*-Out is set back to the previous level to restore LDMOS to the status before shutdown, regardless of the SLDAC-*n* bit status.

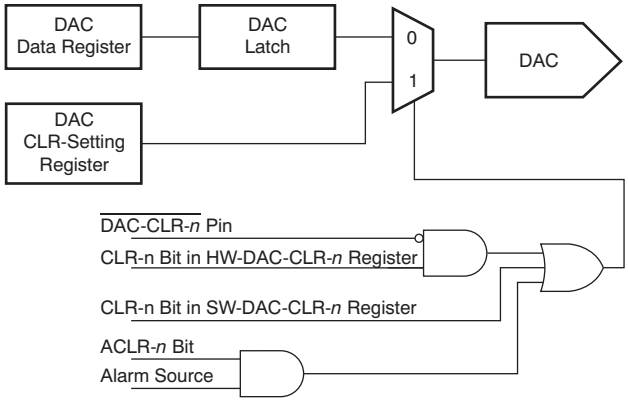


Figure 93. Clearing DAC-*n*

The AMC7812 is implemented with two external control lines, the $\overline{\text{DAC-CLR-0}}$ and $\overline{\text{DAC-CLR-1}}$ pins, to clear the DACs. When either pin goes low, the corresponding user-selected DACs are in a *cleared* state. The HW_DAC-CLR-0 Register determines which DAC is cleared when the $\overline{\text{DAC-CLR-0}}$ pin is low. The register contains 12 clear bits (CLR-*n*), one per DAC. If the CLR-*n* bit = '1', DAC-*n* is in a cleared state when the $\overline{\text{DAC-CLR-0}}$ pin is low. However, if the CLR-*n* bit = '0', DAC-*n* does not change when the pin is low. Likewise, the HW-DAC-CLR-1 Register determines which DAC is cleared when the $\overline{\text{DAC-CLR-1}}$ pin is low.

Writing directly to the SW_DAC_CLR Register puts the selected DACs in a cleared state. DACs can also be forced into a clear state by alarm events. The AUTO-DAC-CLR-SOURCE Register specifies which alarm events force the DACs into a clear state, and the AUTO-DAC-CLR-EN Register defines which DACs are forced into a clear state. Refer to the AUTO-DAC-CLR-SOURCE and AUTO-DAC-CLR-EN Registers for further details.

DAC Output Thermal Protection

A significant amount of power can be dissipated in the DAC outputs. The AMC7812 is implemented with a thermal protection circuit that sets the THERM-ALR bit in the Status Register if the die temperature exceeds +150°C. The THERM-ALR bit can be used in combination with THERM-ALR-CLR (bit 2 in the AUTO-DAC-CLR-SOURCE Register) and ACLR-*n* (bits[14:3] in the AUTO-DAC-CLR-EN Register) to set the DAC output to a predefined code when this condition occurs. Note that this feature is disabled when the local temperature sensor powers down.

Alarm Operation

The AMC7812 continuously monitors all analog inputs and temperatures in normal operation. When any input is out of the specified range, an alarm triggers. When an alarm state occurs, the corresponding individual alarm bit in the Status Register is set ('1'). Global alarm bit GALR in AMC Configuration Register 0 is the OR of individual alarms, see Figure 94. When the ALARM-LATCH-DIS bit in the Alarm Control Register is cleared ('0'), the alarm is latched. The global alarm bit (GALR) maintains '1' until the corresponding error condition[s] subside and the alarm status is read. The alarm bits are referred to as being *latched* because they remain set until read by software. This design ensures that out-of-limit events cannot be missed if the software is polling the device periodically. All bits are cleared when reading the Status Register, and all bits are reasserted if the out-of limit condition still exists on the next monitoring cycle, unless otherwise noted.

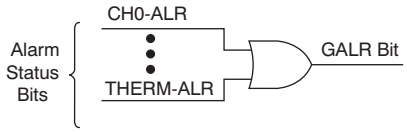


Figure 94. Global Alarm Bit

When the ALARM-LATCH-DIS bit in the Alarm Control Register is set ('1'), the alarm bit is not latched. The alarm bit in the Status Register goes to '0' when the error condition subsides, regardless of whether the bit is read or not. When GALR = '1', the ALARM pin goes low. When the GALR bit = '0', the ALARM is high (inactive).

Analog Input Out-of-Range Alarm

The AMC7812 provides out-of-range detection for four individual analog inputs (CH0, CH1, CH2, and CH3) as shown in Figure 95. When the measurement is out-of-range, the corresponding alarm bit in the Status Register is set to '1' to flag the out-of-range condition. The value in the High-Threshold Register defines the upper bound threshold of the nth analog input, while the value in Low-Threshold defines the lower bound. These two bounds specify a window for the out-of-range detection.

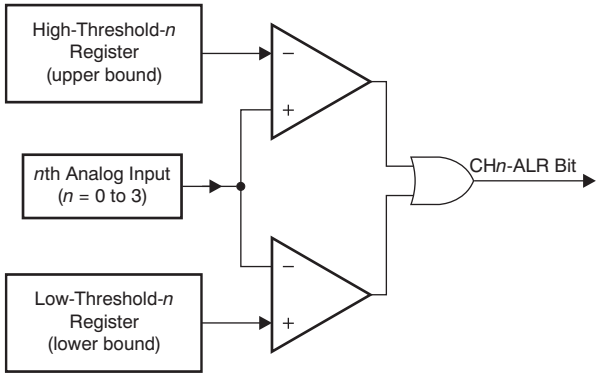


Figure 95. CH*n* Out-of-Range Alarm

The AMC7812 also has high-limit or low-limit detection for the temperature sensors (D1, D2, and LT), as shown in Figure 96. To implement single, upper-bound threshold detection for analog input CH*n*, the host processor can set the upper-bound threshold to the desired value and the lower-bound threshold to the default value. For lower-bound threshold detection, the host processor can set the lower-bound threshold to the desired value and the upper-bound threshold to the default value. Note that the value of the High-Threshold Register must not be less than the value of the Low-Threshold Register; otherwise, ALR-*n* is always set to '1' and the alarm indicator is always active. Each temperature sensor has two alarm bits: High-ALR (high-limit alarm) and Low-ALR (low-limit alarm).

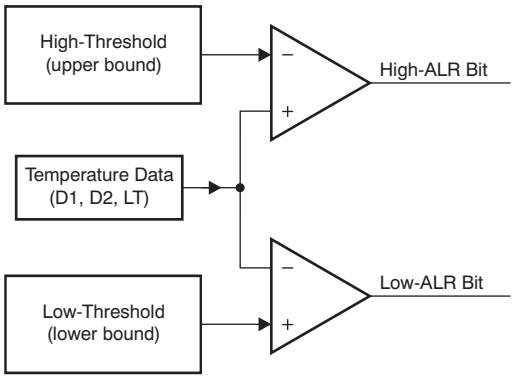


Figure 96. Temperature Out-of-Range Alarm

$\overline{\text{ALARM}}$ pin

The $\overline{\text{ALARM}}$ pin is a global alarm indicator. $\overline{\text{ALARM}}$ is an open-drain pin, as Figure 97 illustrates; an external pull-up resistor is required. When the pin is activated, it goes low. When the pin is inactive, it is in Hi-Z status. The $\overline{\text{ALARM}}$ pin works as an interrupt to the host so that it may query the Status Register to determine the alarm source. Any alarm event (including analog inputs, temperatures, diode status, and device thermal condition) activates the pin if the alarm is not masked (the corresponding EALR bit in the Alarm Control Register = '1'). When the alarm pin is masked (EN-ALARM bit = '0'), the occurrence of the event sets the corresponding status bit in Status Register to '1', but does not activate the $\overline{\text{ALARM}}$ pin.

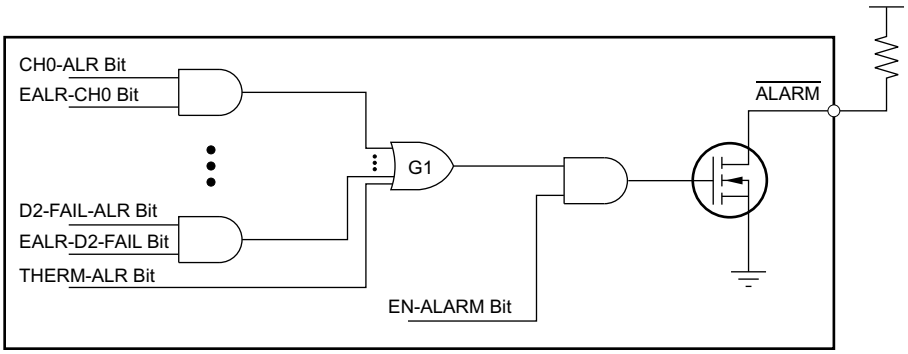


Figure 97. $\overline{\text{ALARM}}$ Pin

When the ALARM-LATCH-DIS bit in the Alarm Control Register is cleared ('0'), the alarm is latched. Reading the Status Register clears the alarm status bit. Whenever an alarm status bit is set, indicating an alarm condition, it remains set until the event that caused it is resolved and the Status Register is read. The alarm bit can only be cleared by reading the Status Register after the event is resolved, or by hardware reset, software reset, or power-on reset (POR). All bits are cleared when reading the Status Register, and all bits are reasserted if the out-of limit condition still exists after the next conversion cycle, unless otherwise noted. When the ALARM-LATCH-DIS bit in the Alarm Control Register is set ('1'), the $\overline{\text{ALARM}}$ pin is not latched. The alarm bit clears to '0' when the error condition subsides, regardless of whether the bit is read or not.

Hysteresis

The AMC7812 continuously monitors the analog input channels and temperatures. If any of the alarms are out of range and the alarm is enabled, its alarm bit is set ('1'). However, the alarm condition is cleared only when the conversion result returns to a value of at least *hys* below the value of High Threshold Register, or *hys* above the value of Low Threshold Register. The Hysteresis Registers store the value for each analog input (CH0, CH1, CH2, and CH3) and temperature (D1, D2, and LT). *hys* is the value of hysteresis that is programmable: 0 LSB to 127 LSB for analog input, and 0°C to +31°C for temperatures. For the THERM-ALR bit, the hysteresis is fixed at 8°C. The hysteresis behavior is shown in Figure 98.

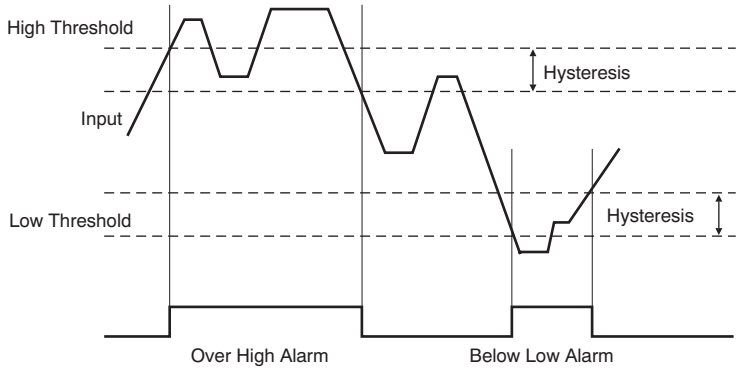


Figure 98. Hysteresis

False Alarm Protection

As noted previously, the AMC7812 continuously monitors all analog inputs and temperatures in normal operation. When any input is out of the specified range in *N* consecutive conversions, the corresponding alarm bit is set ('1'). If the input returns to the normal range before *N* consecutive times, the alarm bit remains clear ('0'). This design avoids false alarms.

The number *N* is programmable by the CH-FALR-CT-[2:0] bits in AMC Configuration Register 1 for analog input CH-n as shown in Table 6, or by the TEMP-FALR-CT-[1:0] bits for temperature monitors as shown in Table 7.

Table 6. Consecutive Sample Number for False Alarm Protection for CH-*n*

CH-FALR-CT-2	CH-FALR-CT-1	CH-FALR-CT-0	*N* CONSECUTIVE SAMPLES BEFORE ALARM IS SET
0	0	0	1
0	0	1	4
0	1	0	8
0	1	1	16 (default)
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

Table 7. Consecutive Sample Number for False Alarm Protection for Temperature Channels

TEMP-FALR-CT-1	TEMP-FALR-CT-0	*N* CONSECUTIVE SAMPLES BEFORE ALARM IS SET
0	0	1
0	1	2
1	0	4 (default)
1	1	8

GENERAL-PURPOSE INPUT/OUTPUT PINS (GPIO-0 to GPIO-7)

The AMC7812 has eight GPIO pins. The GPIO-0, -1, -2 and -3 pins are dedicated to general, bidirectional, digital I/O signals. GPIO-4, GPIO-5, GPIO-6 and GPIO-7 are dual-function pins and can be programmed as either bidirectional digital I/O pins or remote temperature sensors D1 and D2. When D1 or D2 is disabled, the pins work as a GPIO. These pins can receive an input or produce an output. When the GPIO-*n* pin acts as an output, it has an open-drain, and the status is determined by the corresponding GPIO-*n* bit of the GPIO Register. The output state is high impedance when the GPIO-*n* bit is set to '1', and is logic low when the GPIO-*n* bit is cleared ('0'). Note that a 10kΩ pullup resistor is required when using the GPIO-*n* pin as an output, see Figure 99. The dual function GPIO-4, -5, -6 and -7 pins should not be tied to a pullup voltage that exceeds the AV_{DD} supply. The dedicated GPIO-0, -1, -2 and -3 pins are only restricted by the absolute maximum voltage. To use the GPIO-*n* pin as an input, the corresponding GPIO-*n* bits in the GPIO Register must be set to '1'. When the GPIO-*n* pin acts as input, the digital value on the pin is acquired by reading the corresponding GPIO-*n* bit. After a power-on reset or any forced hardware or software reset, all GPIO-*n* bits are set to '1', and the GPIO-*n* pin goes to a high-impedance state.

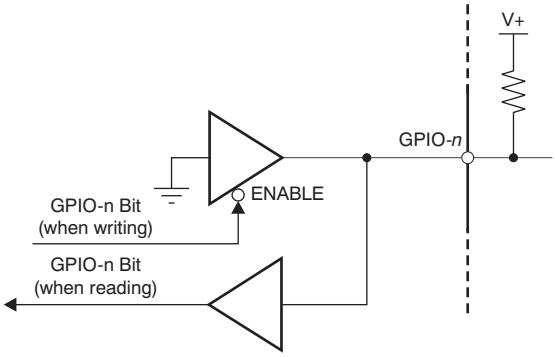


Figure 99. GPIO Pins

HARDWARE RESET

Pulling the $\overline{\text{RESET}}$ pin low performs a hardware reset. When the $\overline{\text{RESET}}$ pin is low, the device enters a reset state, all registers are set to the default values (including the Power-Down Register); therefore, all function blocks (except the internal temperature sensor) are in power-down mode. On the rising edge of $\overline{\text{RESET}}$, the device returns to the normal operating mode. After returning, all registers remain set to the default value until a new value is written. Note that after reset, it is important to properly write to the power-down register in order to activate the device. Hardware reset should only be issued when DVDD has reached the minimum specification of 2.7V or above.

SOFTWARE RESET

Software reset returns all register settings to their default and can be performed by writing to the Software Reset Register. In the case of I^2C communication, any value written to this register results in a reset condition. In the case of SPI communications, only writing the specific value of 6600h to this register resets the device. See the *Registers* section for details. During reset, all communication is blocked. After issuing the reset, the user should wait at least 30µs before attempting to resume communication.

POWER-ON RESET (POR)

When powered on, the internal POR circuit invokes a power-on reset, which performs the equivalent function of the $\overline{\text{RESET}}$ pin. To ensure a POR, DVDD must start from a level below 750mV.

POWER SUPPLY SEQUENCE

The preferred (not required) order for applying power is IOVDD, DVDD/AVDD and then AVCC. All registers initialize to the default values after these supplies have been established. Communication with the AMC7812 will be valid after a 250µS maximum power-on reset delay. The default state of all analog blocks is off as determined by the power-down register (6Bh). Before writing to this register, a hardware reset should be issued to ensure specified operation of the AMC7812. Communication to the AMC7812 will be valid after a maximum 250µS reset delay from the rising edge of $\overline{\text{RESET}}$.

If DVDD falls below 2.7V, the minimum supply value of DVDD, either a hardware or power-on reset should be issued before proper operation can be resumed.

To avoid activating the ESD protection diodes of the AMC7812, GPIO-4, GPIO-5, GPIO-6 and GPIO-7 inputs should not be applied before the AVDD is established. Also, if using the external reference configuration of the ADC, ADC-REF-IN/CMP should not be applied before AVDD.

PRIMARY COMMUNICATION INTERFACE

The AMC7812 communicates with the system controller through the primary communication interface, which can be configured as either an I^2C-compatible two-wire bus or an SPI bus. When the SPI/I2C pin is tied to ground, the I^2C interface is enabled, and the SPI is disabled. When the SPI/I2C pin is tied to IOVDD, the I^2C interface is disabled, and SPI is enabled.

I^2C-Compatible Interface

This device uses a two-wire serial interface compatible with the I^2C-bus specification, version 2.1. The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C-compatible devices connect to the I^2C bus through open-drain I/O pins SDA and SCL. A master device, usually a micro controller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the start and stop of data transfers. A slave device receives and/or transmits data on the bus under control of the master device. The AMC7812 works as a slave and supports the following data transfer modes, as defined in the I^2C-bus specification: standard mode (100kbps), fast mode (400kbps), and high-speed mode (3.4Mbps). The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as F/S mode in this document. The protocol for high-speed mode is different from the F/S mode, and is referred to as Hs mode. The AMC7812 supports 7-bit addressing. However 10-bit addressing and general call addressing are not supported. The slave address of the AMC7812 is determined by the status of pins A0, A1, and A2, as shown in Table 8.

Table 8. Slave Addresses

A0	A1	A2	SLAVE ADDRESS
GND	GND	GND	1100001
GND	GND	IOV_{DD}	0101100
GND	IOV_{DD}	GND	1100100
GND	IOV_{DD}	IOV_{DD}	0101110
IOV_{DD}	GND	GND	1100010
IOV_{DD}	GND	IOV_{DD}	0101101
IOV_{DD}	IOV_{DD}	GND	1100101
IOV_{DD}	IOV_{DD}	IOV_{DD}	0101111

F/S-Mode Protocol

- The master initiates the data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 2. All I^2C-compatible devices must recognize a start condition.
- The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data are valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 2). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 2) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master recognizes that communication link with a slave has been established.
- The master generates further SCL cycles to either transmit data to the slave (R/W bit = '1') or receive data from the slave (R/W bit = '0'). In either case, the receiver must acknowledge the data sent by the transmitter. Therefore, an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.
- To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high (see Figure 2). This action releases the bus and stops the communication link with the addressed slave. All I^2C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices recognize that the bus is released and wait for a start condition followed by a matching address.

Hs-Mode Protocol

- When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.
- The master generates a start condition followed by a valid serial byte containing Hs master code 00001xxx. This transmission is made in F/S mode at no more than 400 kbps. No device is allowed to acknowledge the Hs master code, but all devices must recognize it and switch their internal setting to support 3.4 Mbps operation.
- The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as for F/S mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends Hs mode and switches all the internal settings of the slave devices to support F/S mode. Note that instead of using a stop condition, repeated start conditions should be used to secure the bus in Hs mode.

Address Pointer

The Address Pointer Register of AMC7812 is an 8-bit register. Each register has an address and when it is accessed, the address pointer points to it. All registers in the AMC7812 are 16-bit, consisting of a high byte (D15:D8) and a low byte (D7:D0). The high byte is always accessed first, and the low byte accessed second. When the register is accessed, the entire register is frozen until the operation on the low byte is complete. During write operation, the new content does not take effect until the low byte is written. In read operation, the whole register value is frozen until the low byte is read.

The address pointer does not change after the current register is accessed. To change the pointer, the master issues a slave address byte with the R/W bit low, followed by the Pointer Register byte; no additional data are required.

Timeout Function

The AMC7812 resets the serial interface if either SCL or SDA are held low for 32.8ms (typical) between a START and STOP condition. If the AMC7812 is holding the bus low, it will release the bus and wait for a START condition. To avoid activating the timeout function, it is necessary to maintain a communication speed of at least 1kHz for the SCL operating frequency.

AMC7812 Communication Protocol for I²C

The AMC7812 uses the following I²C protocols.

Writing a Single Word of Data to a 16-Bit Register (Figure 100)

1. The master device asserts a start condition.
2. The master then sends the 7-bit AMC7812 slave address followed by a zero for the direction bit, indicating a write operation.
3. The AMC7812 asserts an acknowledge signal on SDA.
4. The master sends a register address.
5. The AMC7812 asserts an acknowledge signal on SDA.
6. The master sends a data byte of the high byte of the register (D15:D8).
7. The AMC7812 asserts an acknowledge signal on SDA.
8. The master sends a data byte of the low byte of the register (D7:D0).
9. The AMC7812 asserts an acknowledge signal on SDA.
10. The master asserts a stop condition to end the transaction.

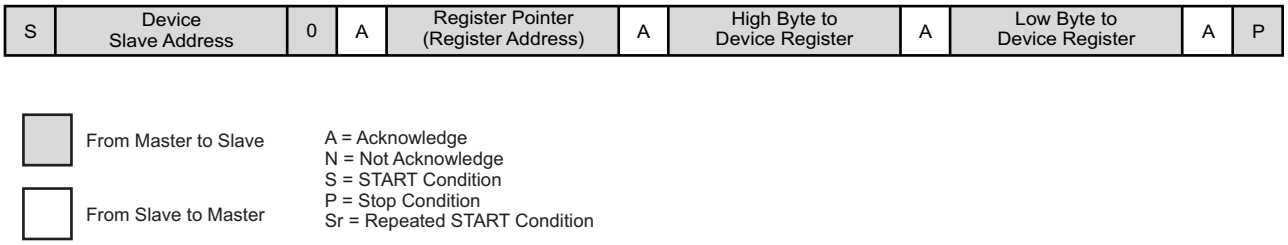


Figure 100. Write Single Byte

Writing Multiple Words to Different Registers (Figure 101)

A complete word must be written to a register (high byte and low byte) for proper operation.

1. The master device asserts a start condition.
2. The master then sends the 7-bit AMC7812 slave address followed by a zero for the direction bit, indicating a write operation.
3. The AMC7812 asserts an acknowledge signal on SDA.
4. The master sends the first register address.
5. The AMC7812 asserts an acknowledge signal on SDA.
6. The master sends the high byte of the data word to the first register.
7. The AMC7812 asserts an acknowledge signal on SDA.
8. The master sends the low byte of the data word to the first register.
9. The AMC7812 asserts an acknowledge signal on SDA.
10. The master sends a second register address.
11. The AMC7812 asserts an acknowledge signal on SDA.
12. The master then sends the high byte of the data word to the second register.
13. The AMC7812 asserts an acknowledge on SDA.
14. The master sends the low byte of the data word to the second register.
15. The AMC7812 asserts an acknowledge signal on SDA.
16. The master and the AMC7812 repeat steps 4 to 15 until the last data are transferred.
17. The master then asserts a stop condition to end the transaction.

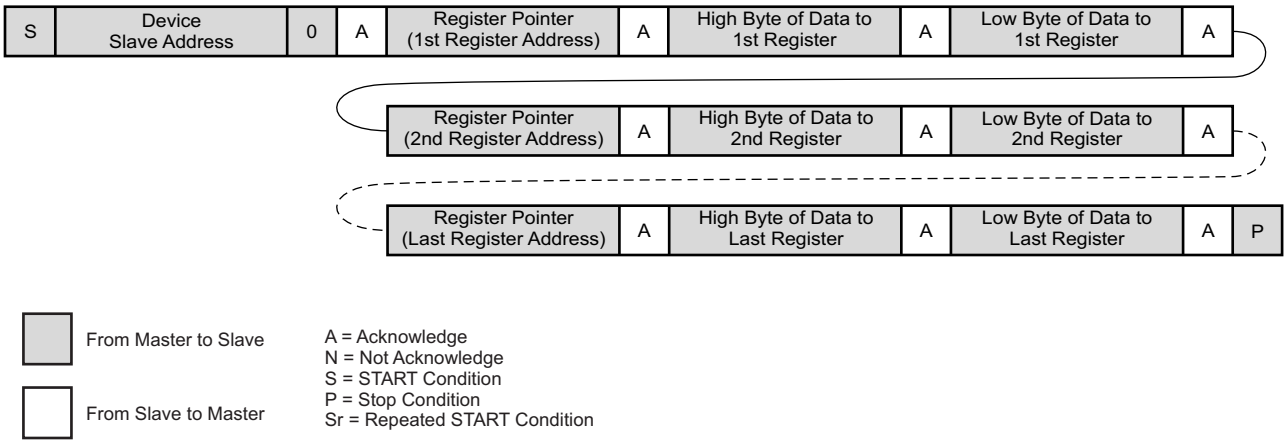


Figure 101. Write to Multiple 16-Bit Registers

Reading a Single Word from Any Register (Figure 102)

1. The master device asserts a start condition.
2. The master then sends the 7-bit AMC7812 slave address followed by a zero for the direction bit, indicating a write operation.
3. The AMC7812 asserts an acknowledge signal on SDA.
4. The master sends a register address.
5. The AMC7812 asserts an acknowledge signal on SDA.
6. The master device asserts a restart condition.
7. The master then sends the 7-bit AMC7812 slave address followed by a '1' for the direction bit, indicating a read operation.
8. The AMC7812 asserts an acknowledge signal on SDA.
9. The AMC7812 then sends the high byte of the register (D15:D8).
10. The master asserts an acknowledge signal on SDA.
11. The AMC7812 sends the low byte of the register (D7:D0).
12. The master asserts a not acknowledge signal on SDA.
13. The master then asserts a stop condition to end the transaction.

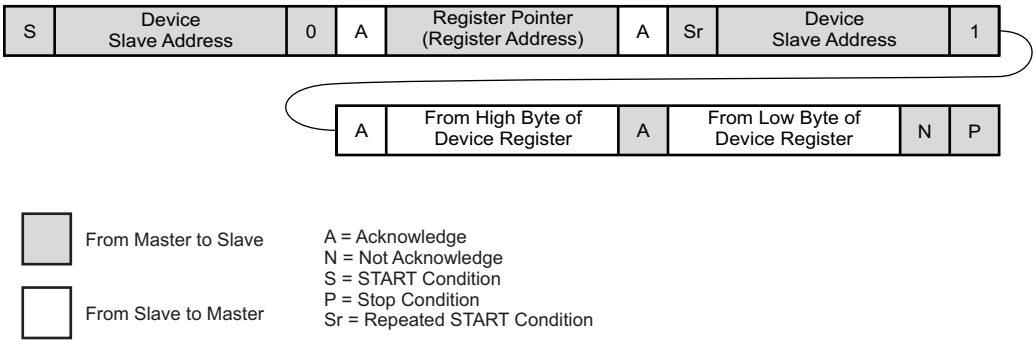


Figure 102. Read a Single Word

Reading the Same Register Multiple Times (Figure 103 and Figure 104)

1. The master device asserts a start condition.
2. The master then sends the 7-bit AMC7812 slave address followed by a zero for the direction bit, indicating a write operation.
3. The AMC7812 asserts an acknowledge signal on SDA.
4. The master sends a register address.
5. The AMC7812 asserts an acknowledge signal on SDA.
6. The master device asserts a restart condition.
7. The master then sends the 7-bit AMC7812 slave address followed by a '1' for the direction bit, indicating a read operation.
8. The AMC7812 asserts an acknowledge signal on SDA.
9. The AMC7812 then sends the high byte of the register (D15:D8).
10. The master asserts an acknowledge signal on SDA.
11. The AMC7812 sends the low byte of the register (D7:D0).
12. The master asserts an acknowledge signal on SDA.
13. The AMC7812 and the master repeat steps 9 to 12 until the low byte of last reading is transferred.
14. After receiving the low byte of the last register, the master asserts a not acknowledge signal on SDA.
15. The master then asserts a stop condition to end the transaction.

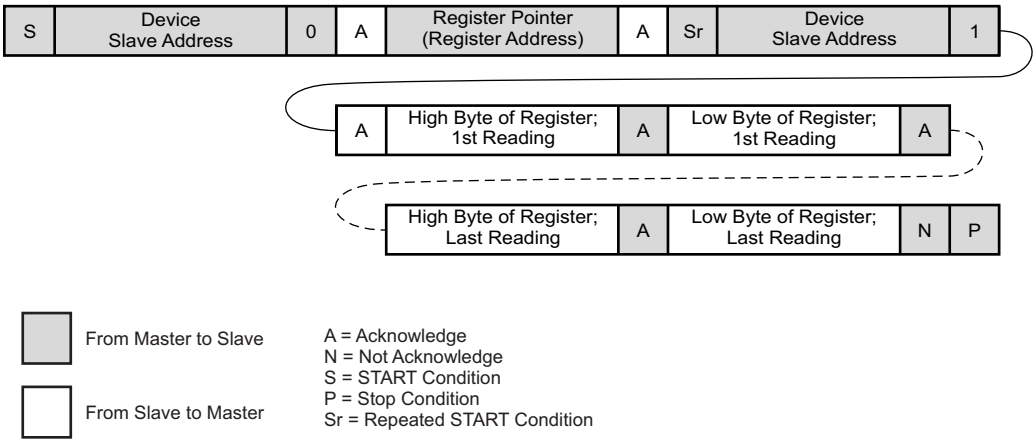


Figure 103. Read Multiple Words

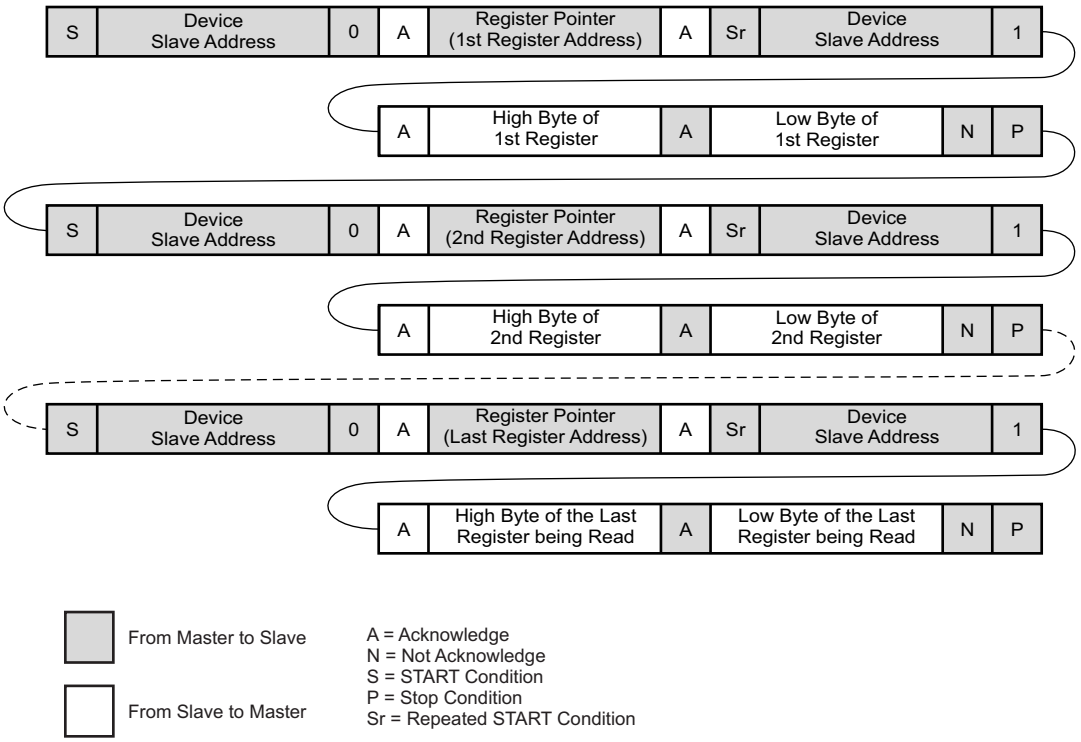


Figure 104. Read Multiple Registers Using the *Reading Single Word from Any Register* Method

Serial Peripheral Interface (SPI)

The AMC7812 can be controlled over a versatile 3-wire serial interface that operates at clock rates of up to 50MHz and is compatible with SPI, QSPI™, MICROWIRE™, and DSP standards. The SPI communication command consists of a read/write bit, seven register address bits, and 16 data bits (as shown in Table 9), for a total of 24 bits. The timing for this operation is shown in the SPI timing diagrams (Figure 3, Figure 4, and Figure 5).

SPI Shift Register

The SPI shift register is 24 bits wide. Data are loaded into the device MSB first as a 24-bit word under the control of the serial clock input, SCLK. The falling edge of $\overline{CS}$ starts the communication cycle. The data are latched into the SPI shift register on the falling edge of SCLK, while $\overline{CS}$ is low. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked out and the SDO line is in a high-impedance state. The contents of the SPI shift register are loaded into the device internal register on the rising edge of $\overline{CS}$ (with delay). During the transfer, the command is decoded and the new data are transferred into the proper registers.

The serial interface works with both a continuous and non-continuous serial clock. A continuous SCLK source can only be used if $\overline{CS}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{CS}$ must be taken high after the final clock to latch the data.

AMC7812 Communications Command for SPI

The AMC7812 is entirely controlled by registers. Reading from and writing to these registers is accomplished by issuing a 24-bit operation word shown in Table 9.

Table 9. 24-Bit Word Structure for Read/Write Operation

OPERATION	I/O	BIT 23 (MSB)	BIT22:BIT16	BIT15:BIT0
Write	SDI	0 (R/W)	Addr6:Addr0	Data to be written
	SDO	Data is undefined	Data is undefined	Undefined or data depending on the previous frame
Read frame 1	SDI	1 (R/W)	Addr6:Addr0	don't care
	SDO	Data is undefined	Data is undefined	Undefined or data depending on the previous frame
Read frame 2	SDI	1 (R/W)	Addr6:Addr0	don't care
	SDO	Data is undefined	Data is undefined	Data for address specified in frame 1

Bit 23 **R/W**. Indicates a read from or a write to the addressed register.

Bit = '0' sets the write operation and the data are written to the specified register.
Bit = '1' sets the read operation where bits [addr6:addr0] select the register to be read. The remaining bits are *don't care*. The data read from the selected register appear on SDO pin in the next SPI cycle.

Bits[22:16] **Addr6:Addr0.** Register address; specifies which register is accessed.

Bits[15:0] **DATA.** 16-bit data bits.

In write operation, these bits are written to bits[15:0] of the register with the address of [Addr6:Addr0].
In read operation, these bits are determined by previous operation. If previous operation is a read, these bits are from bits[15:0] of the internal register specified in previous read operation. If previous operation is a write, these data bits are *don't care* (undefined). The data read from current read operation appears on SDO in the next operation cycle.

Standalone Operation

In standalone mode, as shown in Figure 105, each AMC7812 has its own SPI bus. The serial clock can be continuous or gated. The first falling edge of $\overline{CS}$ starts the operation cycle. Exactly 24 falling clock edges must be applied before $\overline{CS}$ is brought high again. If $\overline{CS}$ is brought high before the 24th falling SCLK edge, or if more than 24 falling SCLK edges are applied before $\overline{CS}$ is brought high, then the input data are incorrect. The device input register is updated from the Shift Register on the rising edge of $\overline{CS}$, and data are automatically transferred to the addressed registers as well. In order for another serial transfer to occur, $\overline{CS}$ must be brought low again. Figure 106 and Figure 107 show write, and read operations in standalone mode.

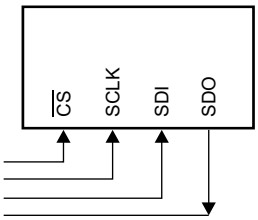
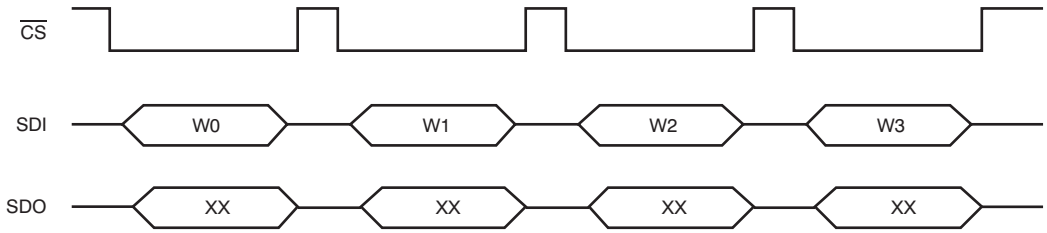
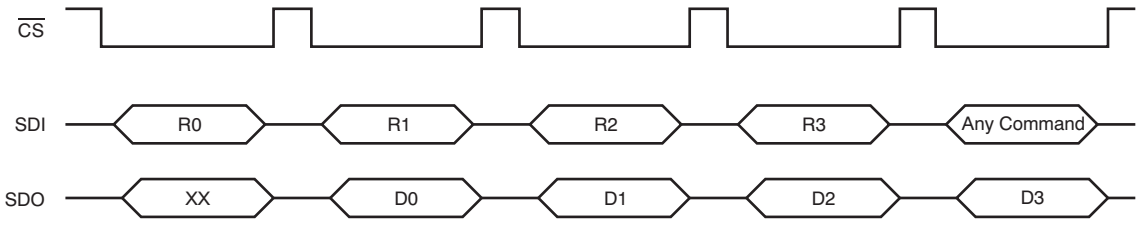


Figure 105. Standalone Operation



W*n* = Write Command for Register *N*
XX = Don't care, undefined

Figure 106. Write Operation in Standalone Mode



R*n* = Read Command for Register *N*
D*n* = Data from Register *N*
XX = Don't care, undefined

Figure 107. Read Operation in Standalone Mode

Daisy-Chain Operation

For systems that contain several AMC7812s, the SDO pin can be used to daisy-chain multiple devices together. This daisy-chain feature is useful in reducing the number of serial interface lines. The first falling edge of $\overline{CS}$ starts the operation cycle. SCLK is continuously applied to the Input Shift Register when $\overline{CS}$ is low.

If more than 24 clock pulses are applied, the data ripple out of the Shift Register and appear on the SDO line. These data are clocked out on the rising edge of SCLK and are valid on the falling edge. By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24*N*, where *N* is the total number of AMC7812s in the daisy chain. When the serial transfer to all devices is complete, $\overline{CS}$ is taken high. This action transfers the data from the SPI Shifter Registers to the internal register of each AMC7812 in the daisy chain and prevents any further data from being clocked in. The serial clock can be continuous or gated. A continuous SCLK source can only be used if $\overline{CS}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{CS}$ must be taken high after the final clock in order to latch the data.

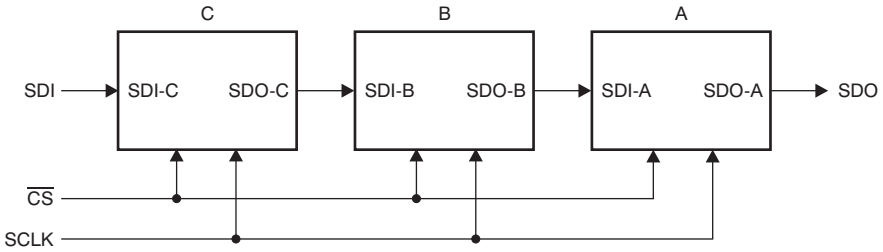
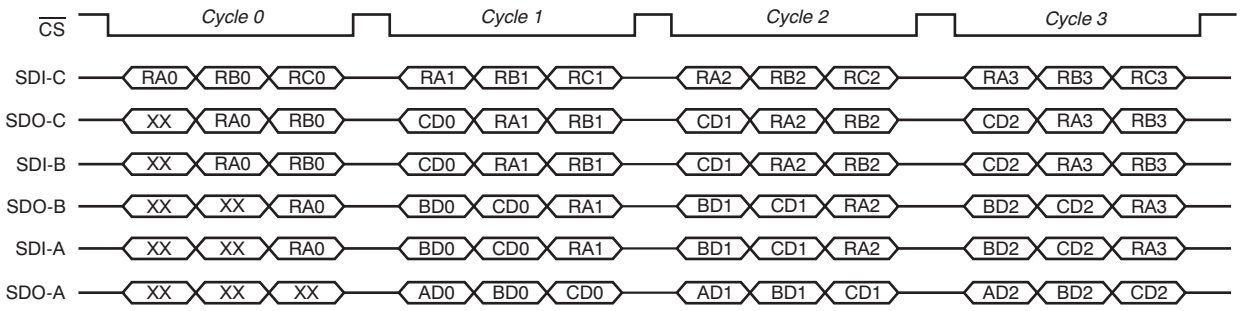
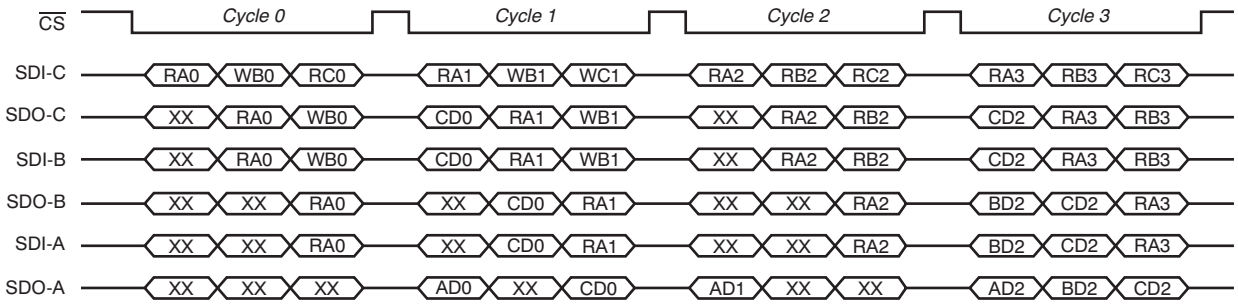


Figure 108. Three AMC7812s in a Daisy-Chain Configuration



RA*n* (RB*n*, RC*n*) = Read Command for Register *N* of device A (B,C)
AD*n* (BD*n*, CD*n*) = Data from Register *N* of device A (B, C)
XX = Don't care, undefined

Figure 109. Reading Multiple Registers



WB*n* (WC*n*) = Write Command for Register *N* of device A (B,C)
RA*n* (RB*n*, RC*n*) = Read Command for Register *N* of device A (B, C)
AD*n* (BD*n*, CD*n*) = Data from Register *N* of device A (B, C)
XX = Don't care, undefined

Figure 110. Mixed Operation: Reading Devices A and C, and Writing to Device B; then Reading A, and Writing to B and C; then Reading A, B, and C Twice

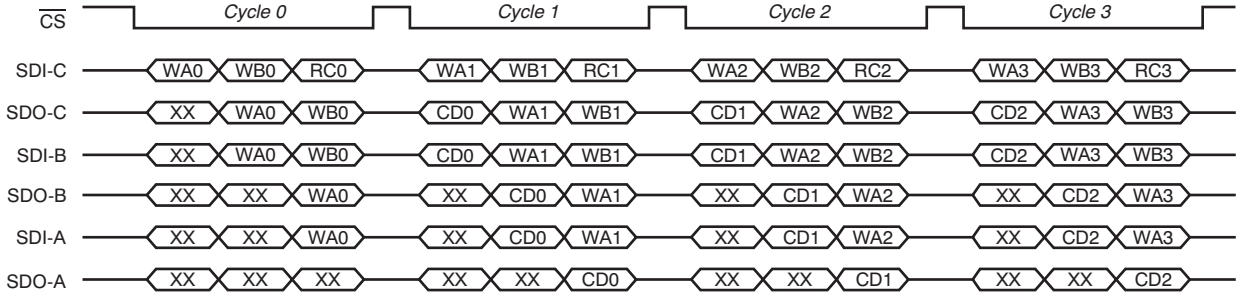


Figure 111. Writing to Devices A and B, and Reading Device C

REGISTERS

REGISTER MAP

The AMC7812 has several 16-bit registers that consist of a high byte (8 MSBs) and a low byte (8 LSBs). An 8-bit register pointer points to the proper register. The pointer does not change after the operation. Table 10 lists the registers for the AMC7812. Note that the default values are for SPI operation; see the register descriptions for I^2C default values.

Table 10. Register Map

ADDRESS (HEX)	R/W	DEFAULT (HEX)	REGISTER	ADDRESS (HEX)	R/W	DEFAULT (HEX)	REGISTER
00	R	0000	LT-Temperature-Data	45	R/W	0000	DAC-6-CLR-Setting
01	R	0000	D1-Temperature-Data	46	R/W	0000	DAC-7-CLR-Setting
02	R	0000	D2-Temperature-Data	47	R/W	0000	DAC-8-CLR-Setting
0A	R/W	003C(1)	Temperature Configuration	48	R/W	0000	DAC-9-CLR-Setting
0B	R/W	0007(1)	Temperature Conversion Rate	49	R/W	0000	DAC-10-CLR-Setting
21	R/W	0000(1)	η-Factor Correction (for D1)	4A	R/W	0000	DAC-11-CLR-Setting
22	R/W	0000(1)	η-Factor Correction (for D2)	4B	R/W	00FF	GPIO
23	R	0000	ADC-0-Data	4C	R/W	2000	AMC Configuration 0
24	R	0000	ADC-1-Data	4D	R/W	0070	AMC Configuration 1
25	R	0000	ADC-2-Data	4E	R/W	0000	Alarm Control
26	R	0000	ADC-3-Data	4F	R	0000	Status
27	R	0000	ADC-4-Data	50	R/W	0000	ADC Channel 0
28	R	0000	ADC-5-Data	51	R/W	0000	ADC Channel 1
29	R	0000	ADC-6-Data	52	R/W	FFFF	ADC Gain
2A	R	0000	ADC-7-Data	53	R/W	0004	AUTO-DAC-CLR-SOURCE
2B	R	0000	ADC-8-Data	54	R/W	0000	AUTO-DAC-CLR-EN
2C	R	0000	ADC-9-Data	55	R/W	0000	SW-DAC-CLR
2D	R	0000	ADC-10-Data	56	R/W	0000	HW-DAC-CLR-EN-0
2E	R	0000	ADC-11-Data	57	R/W	0000	HW-DAC-CLR-EN-1
2F	R	0000	ADC-12-Data	58	R/W	0000	DAC Configuration
30	R	0000	ADC-13-Data	59	R/W	0000	DAC Gain
31	R	0000	ADC-14-Data	5A	R/W	0FFF	Input-0-High-Threshold
32	R	0000	ADC-15-Data	5B	R/W	0000	Input-0-Low-Threshold
33	R/W	0000	DAC-0-Data	5C	R/W	0FFF	Input-1-High-Threshold
34	R/W	0000	DAC-1-Data	5D	R/W	0000	Input-1-Low-Threshold
35	R/W	0000	DAC-2-Data	5E	R/W	0FFF	Input-2-High-Threshold
36	R/W	0000	DAC-3-Data	5F	R/W	0000	Input-2-Low-Threshold
37	R/W	0000	DAC-4-Data	60	R/W	0FFF	Input-3-High-Threshold
38	R/W	0000	DAC-5-Data	61	R/W	0000	Input-3-Low-Threshold
39	R/W	0000	DAC-6-Data	62	R/W	07FF	LT-High-Threshold
3A	R/W	0000	DAC-7-Data	63	R/W	0800	LT-Low-Threshold
3B	R/W	0000	DAC-8-Data	64	R/W	07FF	D1-High-Threshold
3C	R/W	0000	DAC-9-Data	65	R/W	0800	D1-Low-Threshold
3D	R/W	0000	DAC-10-Data	66	R/W	07FF	D2-High-Threshold
3E	R/W	0000	DAC-11-Data	67	R/W	0800	D2-Low-Threshold
3F	R/W	0000	DAC-0-CLR-Setting	68	R/W	0810	Hysteresis-0
40	R/W	0000	DAC-1-CLR-Setting	69	R/W	0810	Hysteresis-1
41	R/W	0000	DAC-2-CLR-Setting	6A	R/W	2108	Hysteresis-2
42	R/W	0000	DAC-3-CLR-Setting	6B	R/W	0000	Power-Down
43	R/W	0000	DAC-4-CLR-Setting	6C	R	1220	Device ID
44	R/W	0000	DAC-5-CLR-Setting	7C	R/W	N/A	Software Reset

(1) See register descriptions for I^2C default values.

TEMPERATURE DATA REGISTERS (Read-Only)

In twos complement format, 0.125°C/LSB.

LT-Temperature-Data Register (Address = 00h, Default 0000h, 0°C)

Store the local temperature sensor reading in twos complement data format.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
LT-11	LT-10	LT-9	LT-8	LT-7	LT-6	LT-5	LT-4	LT-3	LT-2	LT-1	LT-0	0	0	0	0

D1-Temperature-Data Register (Address = 01h, Default 0000h, 0°C)

Store the remote temperature sensor D1 reading in twos complement data format.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
D1-11	D1-10	D1-9	D1-8	D1-7	D1-6	D1-5	D1-4	D1-3	D1-2	D1-1	D1-0	0	0	0	0

D2-Temperature-Data Register (Address = 02h, Default 0000h, 0°C)

Store the remote temperature sensor D2 reading in twos complement data format.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
D2-11	D2-10	D2-9	D2-8	D2-7	D2-6	D2-5	D2-4	D2-3	D2-2	D2-1	D2-0	0	0	0	0

TEMPERATURE CONFIGURATION REGISTER (Read/Write, Address = 0Ah)

When using the SPI, the following bit configuration must be used; default = 003Ch.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	0	0	0	0	0	0	D2EN	D1EN	LTEN	RC	0	0

When using the I^2C interface, the following bit configuration must be used; default = 3CFFh.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	D2EN	D1EN	LTEN	RC	0	0	1	1	1	1	1	1	1	1

The bit descriptions are shown in Table 11.

Table 11. Temperature Configuration Register Bit Descriptions

NAME	DEFAULT	R/W	DESCRIPTION
D2EN	1	R/W	Remote temperature sensor D2 enable. If this bit = '1', D2 is enabled. If this bit = '0', D2 is disabled.
D1EN	1	R/W	Remote temperature sensor D1 enable. If this bit = '1', D1 is enabled. If this bit = '0', D1 is disabled.
LTEN	1	R/W	Local temperature sensor enable. If this bit = '1', LT is enabled. If this bit = '0', LT is disabled.
RC	1	R/W	Resistance correction enable. If this bit = '1', correction is enabled. If this bit = '0', correction is disabled.

TEMPERATURE CONVERSION RATE REGISTER (Read/Write, Address = 0Bh)

When using the SPI, the following bit configuration must be used; default = 0007h.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	0	0	0	0	0	0	0	0	0	R2	R1	R0

When using the I^2C interface, the following bit configuration must be used; default = 07FFh.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	0	R2	R1	R0	1	1	1	1	1	1	1	1

The bit descriptions are shown in Table 12.

Table 12. Temperature Conversion Time

R2	R1	R0	CONVERSION TIME
0	0	0	128x minimum
0	0	1	64x minimum
0	1	0	32x minimum
0	1	1	16x minimum
1	0	0	8x minimum
1	0	1	4x minimum
1	1	0	2x minimum
1	1	1	Minimum cycle time

Table 13. Temperature Monitoring Cycle Time

TEMPERATURE SENSOR STATUS	MONITORING CYCLE TIME
Local sensor is active, remote sensors are disabled or in power-down.	15ms
One remote sensor is active and RC = '0', local sensor and one remote sensor are disabled or in power-down.	44ms
One remote sensor is active and RC = '1', local sensor and one remote sensor are disabled or in power-down.	93ms
One remote sensor and local sensor are active and RC = '0', one remote sensor is disabled or in power-down.	59ms
One remote sensor and local sensor are active and RC = '1', one remote sensor is disabled or in power-down.	108ms
Two remote sensors are active and RC = '0', local sensor is disabled or in power-down.	88ms
Two remote sensors are active and RC = '1', local sensor is disabled or in power-down.	186ms
All sensors are active and RC = '0'.	103ms
All sensors are active and RC = '1'.	201ms

η-FACTOR CORRECTION REGISTER (Read/Write, Addresses = 21h and 22h)

Only the low byte is used; the high byte is ignored.

When using the SPI interface, the following bit configuration must be used; (Default = 0000h).

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	0	0	0	0	N_{ADJUST}							

When using the I^2C, the following bit configuration must be used; (Default = 00FFh).

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
N_{ADJUST}								1	1	1	1	1	1	1	1

The N_{ADJUST} value for ideality correction is stored as shown in Table 14. η_{EFF} is the actual ideality of the transistor being used. Refer to the *Ideality Factor* section for more details.

Table 14. N_{ADJUST} and η_{EFF} Values

N_{ADJUST}			η_{EFF}
BINARY	**HEX**	**DECIMAL**	
0111 1111	7F	127	1.747977
0000 1010	0A	10	1.042759
0000 1000	08	8	1.035616
0000 0110	06	6	1.028571
0000 0100	04	4	1.021622
0000 0010	02	2	1.014765
0000 0001	01	1	1.011371
0000 0000	00	0	1.008 (Default)
1111 1111	FF	–1	1.004651
1111 1110	FE	–2	1.001325
1111 1100	FC	–4	0.994737
1111 1010	FA	–6	0.988235
1111 1000	F8	–8	0.981818
1111 0110	F6	–10	0.975484
1000 0000	80	–128	0.706542

ADC-*n*-DATA REGISTERS (Read-Only, Addresses = 23h to 32h)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Bits[11:0] ADC data.

Four ADC data registers are available. The ADC-*n*-Data Registers (where n = 0 to 15) store the conversion results of the corresponding analog channel-*n*, as shown in Table 15.

Table 15. ADC Data Register Definitions

INPUT CHANNEL	INPUT TYPE	CONVERSION RESULT STORED IN	FORMAT
Channel 0	Single-Ended	ADC-0-Data Register	Straight binary
Channel 1	Single-Ended	ADC-1-Data Register	Straight binary
Channel 2	Single-Ended	ADC-2-Data Register	Straight binary
Channel 3	Single-Ended	ADC-3-Data Register	Straight binary
CH0+/CH1–	Differential	ADC-0-Data Register	Twos complement
CH2+/CH3–	Differential	ADC-2-Data Register	Twos complement
Channel 4	Single-Ended	ADC-4-Data Register	Straight binary
Channel 5	Single-Ended	ADC-5-Data Register	Straight binary
Channel 6	Single-Ended	ADC-6-Data Register	Straight binary
Channel 7	Single-Ended	ADC-7-Data Register	Straight binary
Channel 8	Single-Ended	ADC-8-Data Register	Straight binary
Channel 9	Single-Ended	ADC-9-Data Register	Straight binary
Channel 10	Single-Ended	ADC-10-Data Register	Straight binary
Channel 11	Single-Ended	ADC-11-Data Register	Straight binary
Channel 12	Single-Ended	ADC-12-Data Register	Straight binary
Channel 13	Single-Ended	ADC-13-Data Register	Straight binary
Channel 14	Single-Ended	ADC-14-Data Register	Straight binary
Channel 15	Single-Ended	ADC-15-Data Register	Straight binary

DAC-*n*-DATA REGISTERS (Read/Write, Addresses = 33h to 3Eh, Default 0000h)

Each DAC has a DAC data register to store the data [DAC11:DAC0] that is loaded into the DAC Latches.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Bits[11:0] DAC data.

DAC-*n*-CLR-SETTING REGISTERS (Read/Write, Addresses = 3Fh to 4Ah, Default 0000h)

Each DAC has a DAC-CLR-Setting Register to store the data to be loaded into the DAC Latch when the DAC is cleared.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	DCLR 11	DCLR 10	DCLR 9	DCLR 8	DCLR 7	DCLR 6	DCLR 5	DCLR 4	DCLR 3	DCLR 2	DCLR 1	DCLR 0

GPIO REGISTER (Read/Write, Address = 4Bh, Default = 00FFh)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	0	0	0	0	GPIO-7	GPIO-6	GPIO-5	GPIO-4	GPIO-3	GPIO-2	GPIO-1	GPIO-0

For write operations, the GPIO pin operates as an output. Writing a '1' to the GPIO-*n* bit sets the GPIO-*n* pin to high impedance. Writing a '0' sets the GPIO-*n* pin to logic low. An external pull-up resistor is required when using the GPIO pin as an output.

For read operations, the GPIO pin operates as an input. Read the GPIO-*n* bit to receive the status of the GPIO-*n* pin. Reading a '0' indicates that the GPIO-*n* pin is low; reading a '1' indicates that the GPIO-*n* pin is high.

After power-on reset, or any forced hardware or software reset, the GPIO-*n* bit is set to '1' and is in a high-impedance state.

When D1 is enabled, GPIO-4 and GPIO-5 are ignored.

When D2 is enabled, GPIO-6 and GPIO-7 are ignored.

AMC CONFIGURATION REGISTER 0 (Read/Write, Address = 4Ch, Default = 2000h)

Table 16. AMC Configuration Register 0

BIT	NAME	DEFAULT	R/W	DESCRIPTION
15	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
14	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
13	CMODE	1	R/W	ADC Conversion Mode Bit. This bit selects between the two operating conversion modes (direct or auto). CMODE = '0': Direct mode. The analog inputs specified in the ADC Channel Registers are converted sequentially (see the ADC Channel Registers) one time. When one set of conversions is complete, the ADC is idle and waits for a new trigger. CMODE = '1': Auto mode. The analog inputs specified in the AMC Channel Registers are converted sequentially and repeatedly (see the ADC Channel Registers). When one set of conversions is complete, the ADC multiplexer returns to the first channel and repeats the process. Repetitive conversions continue until the CMODE bit is cleared ('0').
12	ICONV	0	R/W	Internal conversion bit. Set this bit to '1' to start the ADC conversion internally. The bit is automatically cleared ('0') after the ADC conversion starts.
11	ILDAC	0	R/W	Load DAC bit. Set this bit to '1' to synchronously load the DAC Data Registers, which are programmed for synchronous update mode (SLDAC-*n* = 1). The AMC7812 updates the DAC Latch only if the ILDAC bit is set ('1'), thereby eliminating any unnecessary glitch. Any DAC channels that have not been accessed are not reloaded. When the DAC Latch is updated, the corresponding output changes to the new level immediately. This bit is cleared ('0') after the DAC Data Register is updated.
10	ADC-REF-INT	0	R/W	ADC V_{REF} select bit. When this bit = '0', the internal reference buffer is off, and the external reference drives the ADC. When this bit = '1', the internal buffer is on and the internal reference drives the ADC. Note that a compensation capacitor is required.
9	EN-ALARM	0	R/W	Enable $\overline{\text{ALARM}}$ pin bit. When this bit = '0', the $\overline{\text{ALARM}}$ pin is disabled. When this bit = '1', the $\overline{\text{ALARM}}$ pin is enabled.
8	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
7	DAVF		R	ADC Data available flag bit. For Direct mode only. Always cleared (set to '0') in Auto mode. DAVF = '1': The ADC conversions are complete and new data are available. DAVF = '0': The ADC conversion is in progress (data are not ready) or the ADC is in Auto mode. In Direct mode, the DAVF bit sets the DAV pin. DAV goes low when DAVF = '1', and goes high when DAVF = '0'. In Auto mode, DAVF is always cleared to '0'. However, a 1µs pulse (active low) appears on the DAV pin when the last input specified in the ADC Channel Registers is converted. DAVF is cleared to '0' in one of three ways: (1) reading the ADC Data Register, (2) starting a new ADC conversion, or (3) writing '0' to this bit. Reading the Status Register does not clear this bit.
6	GALR	0	R	Global alarm bit. This bit is the OR function of all individual alarm bits of the Status Register. This bit is set ('1') when any alarm condition occurs, and remains '1' until the Status Register is read. This bit is cleared ('0') after reading the Status Register.
5	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
4	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
3	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
2	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
1	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
0	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.

AMC CONFIGURATION REGISTER 1 (Read/Write, Address = 4Dh, Default = 0070h)

Table 17. AMC Configuration Register 1

BIT	NAME	DEFAULT	R/W	DESCRIPTION
15	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
14	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
13	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
12	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
11	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
10	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
9	CONV-RATE-1	0	R/W	ADC conversion rate bit. See Table 18.
8	CONV-RATE-0	0	R/W	ADC conversion rate bit. See Table 18.
7	CH-FALR- CT-2	0	R/W	False alarm protection bit for CH0 to CH3. See Table 19.
6	CH-FALR- CT-1	1	R/W	False alarm protection bit for CH0 to CH3. See Table 19.
5	CH-FALR- CT-0	1	R/W	False alarm protection bit for CH0 to CH3. See Table 19.
4	TEMP-FALR- CT-1	1	R/W	False alarm protection bit for temperature monitor. See Table 20.
3	TEMP-FALR- CT-0	0	R/W	False alarm protection bit for temperature monitor. See Table 20.
2	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
1	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
0	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.

Table 18. CONV-RATE-[1:0] Bit Settings

CONV-RATE-1	CONV-RATE-0	ADC CONVERSION RATE
0	0	500 kSPS, the specified rate (default)
0	1	½ of the specified rate
1	0	1/4 of the specified rate
1	1	1/8 of the specified rate

Table 19. CH-FALR-CT-[2:0] Bit Settings

CH-FALR-CT-2	CH-FALR-CT-1	CH-FALR-CT-0	*N* CONSECUTIVE SAMPLES BEFORE ALARM IS SET
0	0	0	1
0	0	1	4
0	1	0	8
0	1	1	16 (default for CH-0 to CH-3)
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

Table 20. TEMP-FALR-CT-[1:0] Bit Settings

TEMP-FALR-CT-1	TEMP-FALR-CT-0	*N* CONSECUTIVE SAMPLES BEFORE ALARM IS SET
0	0	1
0	1	2
1	0	4 (default)
1	1	8

ALARM CONTROL REGISTER (Read/Write, Address = 4Eh, Default = 0000h)

The Alarm Control Register determines whether the $\overline{\text{ALARM}}$ pin is accessed when a corresponding alarm event occurs. However, this register does not affect the status bit in the Status Register. Note that the thermal alarm is always enabled. When the THERM_ALR bit = '1', the $\overline{\text{ALARM}}$ pin goes low, if the pin is enabled.

Table 21. Alarm Control Register

BIT	NAME	DEFAULT	R/W	DESCRIPTION
15	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
14	EALR-CH0	0	R/W	CH0 and (CH0+/CH1–) alarm enable bit. If EALR-CH0 = '1', the alarm is enabled, the CH0-ALR bit is set, and the $\overline{\text{ALARM}}$ pin goes low (if enabled) when the input of CH0 or (CH0+/CH1–) is out of range. If EALR-CH0 = '0', the alarm is masked. When the input of CH0 or (CH0+/CH1–) is out of range, the $\overline{\text{ALARM}}$ pin does not go low, but the CH0-ALR bit is set.
13	EALR-CH1	0	R/W	CH1 alarm enable bit. If EALR-CH1 = '1', the alarm is enabled, the CH1-ALR bit is set, and the $\overline{\text{ALARM}}$ pin goes low (if enabled) when the input of CH1 is out of range. If EALR-CH1 = '0', the alarm is masked. When the input of CH1 is out of range, the $\overline{\text{ALARM}}$ pin does not go low, but the CH1-ALR bit is set.
12	EALR-CH2	0	R/W	CH2 and (CH2+/CH3–) alarm enable bit. If EALR-CH2 = '1', the alarm is enabled, the CH2-ALR bit is set, and the $\overline{\text{ALARM}}$ pin goes low (if enabled) when the input of CH2 or (CH2+/CH3–) is out of range. If EALR-CH2 = '0', the alarm is masked. When the input of CH2 or (CH2+/CH3–) is out of range, the $\overline{\text{ALARM}}$ pin does not go low, but the CH2-ALR bit is set.
11	EALR-CH3	0	R/W	CH3 alarm enable bit. If EALR-CH3 = '1', the alarm is enabled, the CH3-ALR bit is set, and the $\overline{\text{ALARM}}$ pin goes low (if enabled) when the input of CH3 is out of range. If EALR-CH3 = '0', the alarm is masked. When the input of CH3 is out of range, the $\overline{\text{ALARM}}$ pin does not go low, but the CH3-ALR bit is set.
10	EALR-LT-Low	0	R/W	Local sensor low alarm enable bit. If EALR-LT-Low = '1', the LT-Low alarm is enabled. When LT is below the specified range, the LT-Low-ALR bit is set ('1') and the $\overline{\text{ALARM}}$ pin goes low (if enabled). If EALR-LT-Low = '0', the LT-Low alarm is masked. When LT is below the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the LT-Low-ALR bit is set.
9	EALR-LT-High	0	R/W	Local sensor high alarm enable bit. If EALR-LT-High = '1', the LT-High alarm is enabled. When LT is above the specified range, the LT-High-ALR bit is set ('1') and the $\overline{\text{ALARM}}$ pin goes low (if enabled). If EALR-LT-High = '0', the LT-High alarm is masked. When LT is above the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the LT-High-ALR bit is set.
8	EALR-D1-Low	0	R/W	D1 low alarm enable bit. If EALR-D1-Low = '1', the D1-Low alarm is enabled. When D1 is below the specified range, the D1-Low-ALR bit is set ('1'), and the $\overline{\text{ALARM}}$ pin goes low (if enabled). If EALR-D1-Low = '0', the D1-Low alarm is masked. When D1 is below the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the D1-Low-ALR bit is set.
7	EALR-D1-High	0	R/W	D1 high alarm enable bit. If EALR-D1-High = '1', the D1-High alarm is enabled. When D1 is above the specified range, the D1-High-ALR bit is set ('1'), and the $\overline{\text{ALARM}}$ pin goes low (if enabled). If EALR-D1-High = '0', the D1-High alarm is masked. When D1 is above the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the D1-High-ALR bit is set.
6	EALR-D2-Low	0	R/W	D2 low alarm enable bit. If EALR-D2-Low = '1', the D2-Low alarm is enabled. When D2 is below the specified range, the D2-Low-ALR bit is set ('1'), and the $\overline{\text{ALARM}}$ pin goes low (if enabled). If EALR-D2-Low = '0', the D2-Low alarm is masked. When D2 is below the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the D2-Low-ALR bit is set.
5	EALR-D2-High	0	R/W	D2 high alarm enable bit. If EALR-D2-High = '1', the D2-High alarm is enabled. When D2 is above the specified range, the D2-High-ALR bit is set ('1'), and the $\overline{\text{ALARM}}$ pin goes low (if enabled). If EALR-D2-High = '0', the D2-High alarm is masked. When D2 is above the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the D2-High-ALR bit is set.
4	EALR-D1-FAIL	0	R/W	D1 fail alarm enable bit. If EALR-D1-FAIL = '1', the D1-Fail alarm is enabled. When D1 fails, the D1-FAIL-ALR bit is set ('1'), the $\overline{\text{ALARM}}$ pin goes low (if enabled). If EALR-D1-FAIL = '0', the D1-FAIL alarm is masked. When D1 fails, the $\overline{\text{ALARM}}$ pin does not go low, but the D1-FAIL-ALR bit is set.

Table 21. Alarm Control Register (continued)

BIT	NAME	DEFAULT	R/W	DESCRIPTION
3	EALR-D2-FAIL	0	R/W	D2 fail alarm enable bit. If EALR-D2-FAIL = '1', the D2-Fail alarm is enabled. When D2 fails, the D2-FAIL-ALR bit is set ('1'), the $\overline{\text{ALARM}}$ pin goes low (if enabled). If EALR-D2-FAIL = '0', the D2-FAIL alarm is masked. When D2 fails, the $\overline{\text{ALARM}}$ pin does not go low, but the D2-FAIL-ALR bit is set.
2	ALARM-LATCH-DIS	0	R/W	Alarm latch disable bit. When ALARM-LATCH-DIS = '1', the Status Register bits are not latched. When the alarm condition subsides, the alarm bits are cleared regardless of whether the Status Register has been read or not. When ALARM-LATCH-DIS = '0', the Status Register bits are latched. When an alarm occurs, the corresponding alarm bit is set ('1'). The alarm bit remains '1' until the error condition subsides and the Status Register is read. Before reading, the alarm bit is not cleared ('0') even if the alarm condition disappears.
1	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
0	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.

STATUS REGISTER (Read Only, Address = 4Fh, Default = 0000h)

The AMC7812 continuously monitors all analog inputs and temperatures during normal operation. When any input is out of the specified range *N* consecutive times, the corresponding alarm bit is set ('1'). If the input returns to the normal range before *N* consecutive times, the corresponding alarm bit remains clear ('0'). This configurations avoids any false alarms.

When an alarm status occurs, the corresponding alarm bit is set ('1'). When the ALARM-LATCH-DIS bit in the Alarm Control Register is cleared ('0'), the $\overline{\text{ALARM}}$ pin is latched. Whenever an alarm status bit is set, it remains set until the event that caused it is resolved and the Status Register is read. Reading the Status Registers clears the alarm status bit. The alarm bit can only be cleared by reading the Status Register after the event is resolved, or by hardware reset, software reset, or power-on reset. All alarm status bits are cleared when reading the Status Register, and all these bits are reasserted if the out-of-limit condition still exists after the next conversion cycle, unless otherwise noted.

When the ALARM-LATCH-DIS bit in the Alarm Control Register is set ('1'), the $\overline{\text{ALARM}}$ pin is not latched. The alarm bit goes to '0' when the error condition subsides, regardless of whether the bit is read or not.

Table 22. Status Register

BIT	NAME	DEFAULT	R/W	DESCRIPTION
15	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
14	CH0-ALR	0	R	CH0-ALR = '1' when single-ended channel 0 or differential input pair (CH0+/CH1–) is out of the range defined by the corresponding threshold registers. CH0-ALR = '0' when the analog input is not out of the specified range.
13	CH1-ALR	0	R	CH1-ALR = '1' when single-ended channel 1 is out of the range defined by the corresponding threshold registers. CH1-ALR = '0' when the analog input is not out of the specified range.
12	CH2-ALR	0	R	CH2-ALR = '1' when single-ended channel 2 or differential input pair (CH2+/CH3–) is out of the range defined by the corresponding threshold registers. CH2-ALR = '0' when the analog input is not out of the specified range.
11	CH3-ALR	0	R	CH3-ALR = '1' when single-ended channel 3 is out of the range defined by the corresponding threshold registers. CH3-ALR = '0' when the analog input is not out of the specified range.
10	LT-Low-ALR	0	R	Local temperature under-range flag. LT-Low-ALR = '1' when the local temperature is less than the low-bound threshold. LT-Low-ALR = '0' when the local temperature is not less than the range. This bit is only checked when LT is enabled (EN-LT = '1'); it is ignored when EN-LT = '0'.
9	LT-High-ALR	0	R	Local temperature over-range flag. LT-High-ALR = '1' when the local temperature is greater than the high-bound threshold. LT-High-ALR = '0' when the local temperature is not greater than the range. This bit is only checked when LT is enabled (EN-LT = '1'); it is ignored when EN-LT = '0'.
8	D1-Low-ALR	0	R	Remote temperature reading of D1when less than the range flag. D1-Low-ALR = '1' when the local temperature is less than the low-bound threshold. D1-Low-ALR = '0' when the local temperature is not less than the range. This bit is only checked when D1 is enabled (EN-D1 = '1'); it is ignored when EN-D1 = '0'.
7	D1-High -ALR	0	R	Remote temperature reading of D1 when greater than the range flag. D1-High-ALR = '1' when the local temperature is greater than the high-bound threshold. D1-High-ALR = '0' when the local temperature is not greater than the range. This bit is only checked when D1 is enabled (EN-D1 = '1'); it is ignored when EN-D1 = '0'.
6	D2-Low-ALR	0	R	Remote temperature reading of D2 when less than the range flag. D2-Low-ALR = '1' when the local temperature is less than the low-bound threshold. D2-Low-ALR = '0' when the local temperature is not less than the range. This bit is only checked when D2 is enabled (EN-D2 = '1'); it is ignored when EN-D2 = '0'.
5	D2-High -ALR	0	R	Remote temperature reading of D2 when greater than the range flag. D2-High-ALR = '1' when the local temperature is greater than the high-bound threshold. D2-High-ALR = '0' when the local temperature is not greater than the range. This bit is only checked when D2 is enabled (EN-D2 = '1'); it is ignored when EN-D2 = '0'.
4	D1-FAIL-ALR	0	R	Remote sensor D1 failure flag. D1-FAIL-ALR = '1' when the sensor is an open-circuit or short-circuit. D1-FAIL-ALR = '0' when the sensor is in a normal condition. This bit is only checked when D1 is enabled (EN-D1 = '1'); it is ignored when EN-D1 = '0'.
3	D2-FAIL-ALR	0	R	Remote sensor D2 failure flag. D2-FAIL-ALR = '1' when the sensor is an open-circuit or short-circuit. D2-FAIL-ALR = '0' when the sensor is in a normal condition. This bit is only checked when D2 is enabled (EN-D2 = '1'); it is ignored when EN-D2 = '0'.
2	THERM-ALR	0	R	Thermal alarm flag. When the die temperature is equal to or greater than +150°C, the bit is set ('1') and the THERM-ALR flag activates. The on-chip temperature sensor (LT) monitors the die temperature. If LT is disabled, the THERM-ALR bit is always '0'. The hysteresis of this alarm is 8°C.
1	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
0	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.

ADC CHANNEL REGISTER 0 (Read/Write, Address = 50h, Default = 0000h)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	SE0	SE1	DF (CH0+/ CH1–)	SE2	SE3	DF (CH2+/ CH3–)	SE4	SE5	SE6	SE7	SE8	SE9	SE10	SE11	SE12

These bits specify the external analog auxiliary input channels (CH0 to CH12) to be converted. The specified channel(s) is accessed sequentially in order from bit 14 to bit 0. The input is converted when the corresponding bit is set ('1').

Bit 15 Reserved. Writing to this bit causes no change. Reading this bit returns '0'.

Bits 14, 13, 11, 10, 8:0 **SE0 to SE12.** External single-ended analog input for CH*n*. The result is stored in ADC-*n*-Data Register in straight binary format.

Bit 12 **DF (CH0+CH1–).** External analog differential input pair, CH0 and CH1, with CH0 as positive and CH1 as negative. The difference of (CH0 – CH1) is converted and the result is stored in the ADC-0-Data Register in twos complement format.

Bit 9 **DF(CH2+/CH3-).** External analog differential input pair, CH2 and CH3, with CH2 as positive and CH3 as negative. The difference of (CH2 – CH3) is converted and the result is stored in the ADC-2-Data Register in twos complement format.

Table 23. CH0 and CH1 Bit Settings

BIT 14	BIT 13	BIT 12	DESCRIPTION
1	1	0	CH0 and CH1 are both accessed as single-ended inputs. Bit 12 is ignored.
1	0	0	CH0 is accessed as a single-ended input. CH1 is not accessed. Bit 12 is ignored.
0	1	0	CH1 is accessed as a singled-ended. CH0 is not accessed. Bit 12 is ignored.
0	0	1	Differential input pair CH0 + and CH1– is accessed as a differential input.
0	0	0	CH0, CH1, and differential pair CH0+/CH1– are not accessed.

Table 24. CH2 and CH3 Bit Settings

BIT 11	BIT 10	BIT 9	DESCRIPTION
1	1	0	CH2 and CH3 are both accessed as single-ended inputs. Bit 9 is ignored.
1	0	0	CH2 is accessed as a single-ended input. CH3 is not accessed. Bit 9 is ignored.
0	1	0	CH3 is accessed as a singled-end input. CH2 is not accessed. Bit 9 is ignored.
0	0	1	Differential input pair CH2+ and CH3– is accessed as a differential input.
0	0	0	CH2, CH3, and differential pair CH2+/CH3– are not accessed.

Table 25. CH4 to CH12 Bit Settings

BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DESCRIPTION
1	—	—	—	—	—	—	—	—	CH4 is accessed as a single-ended input
—	1	—	—	—	—	—	—	—	CH5 is accessed as a single-ended input
—	—	1	—	—	—	—	—	—	CH6 is accessed as a single-ended input
—	—	—	1	—	—	—	—	—	CH7 is accessed as a single-ended input
—	—	—	—	1	—	—	—	—	CH8 is accessed as a single-ended input
—	—	—	—	—	1	—	—	—	CH9 is accessed as a single-ended input
—	—	—	—	—	—	1	—	—	CH10 is accessed as a single-ended input
—	—	—	—	—	—	—	1	—	CH11 is accessed as a single-ended input
—	—	—	—	—	—	—	—	1	CH12 is accessed as a single-ended input

ADC CHANNEL REGISTER 1 (Read/Write, Address = 51h, Default = 0000h)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	SE13	SE14	SE15	0	0	0	0	0	0	0	0	0	0	0	0

These bits specify the external analog auxiliary input channels (CH13, CH14,and CH 15) to be converted. The specified channel is accessed sequentially in the order from bit 14 to bit 0 of ADC Channel Register 0, and then bit 14 to bit 12 of ADC Channel Register 1. The input is converted when the corresponding bit is set ('1').

Bits[14:12] **SE*n***: External single-ended analog input CH*n*. The result is stored in the ADC-*n*-Data Register in straight binary format.

ADC GAIN REGISTER (Read/Write, Address = 52h, Default = FFFFh)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
ADG0	ADG1	ADG2	ADG3	ADG4	ADG5	ADG6	ADG7	ADG8	ADG9	ADG10	ADG11	ADG12	ADG13	ADG14	ADG15

Bit 15 **ADG0.**
When ADG0 = '1', the analog input range of single-ended input CH0 (SE0) is 0 to ($2 \cdot V_{REF}$) or differential input pair DF(CH0+/CH1–) is ($-2 \cdot V_{REF}$) to ($+2 \cdot V_{REF}$).
When ADG0 = '0', the analog input range of single-ended input CH0 (SE0) is 0 to V_{REF} or differential input pair DF(CH0+/CH1–) is $-V_{REF}$ to $+V_{REF}$.

Bit 14 **ADG1.**
When ADG1 = '1', the analog input range is 0 to ($2 \cdot V_{REF}$).
When ADG1 = '0', the analog input range of single-ended input CH1 (SE1) is 0 to V_{REF}.

Bit 13 **ADG2.**
When ADG2 = '1', the analog input range of single-ended input CH2 (SE2) is 0 to ($2 \cdot V_{REF}$) or differential input pair DF(CH2+/CH3–) is ($-2 \cdot V_{REF}$) to ($+2 \cdot V_{REF}$).
When ADG2 = '0', the analog input range of single-ended input CH2 (SE2) is 0 to V_{REF} or differential input pair DF(CH2+/CH3–) is $-V_{REF}$ to $+V_{REF}$.

Bit 12 **ADG3.**
When ADG3 = '1', the analog input range is 0 to ($2 \cdot V_{REF}$).
When ADG3 = '0', the analog input range of single-end input CH3 (SE3) is 0 to V_{REF}.

Bit[11:0] **ADG4 to ADG15.**
When these bits = '1', the analog input range is 0 to ($2 \cdot V_{REF}$).
When these bits = '0', the analog input range of CH*n* (where n = 4 to 15) is 0 to V_{REF}

AUTO-DAC-CLR-SOURCE REGISTER (Read/Write, Address = 53h, Default = 0004h)

This register selects which alarm forces the DAC into a *clear* state, regardless of which DAC operation mode is active, auto or manual.

Table 26. AUTO-DAC-CLR-SOURCE Register

BIT	NAME	DEFAULT	R/W	DESCRIPTION
15	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
14	CH0-ALR-CLR	0	R/W	CH0 alarm clear bit. If CH0-ALR_CLR = '1', and if both the ACLR*n* bit in the AUTO-DAC-CLR-EN Register and the CH0-ALR bit in the Status Register are set ('1'), then DAC-*n* is forced to a clear status. If CH0-ALR_CLR = '0', then CH1-ALR goes to '1' and does not force any DAC to a clear status.
13	CH1-ALR-CLR	0	R/W	CH1 alarm clear bit. If CH1-ALR_CLR = '1', and if both the ACLR*n* bit in the AUTO-DAC-CLR-EN Register and the CH1-ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If CH1-ALR_CLR = '0', then CH1-ALR goes to '1' and does not force any DAC to a clear status.
12	CH2-ALR-CLR	0	R/W	CH2 alarm clear bit. If CH2-ALR_CLR = '1', and if both the ACLR*n* bit in the AUTO-DAC-CLR-EN Register and the CH2-ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If CH2-ALR_CLR = '0', then CH2-ALR goes to '1' and does not force any DAC to a clear status.

Table 26. AUTO-DAC-CLR-SOURCE Register (continued)

BIT	NAME	DEFAULT	R/W	DESCRIPTION
11	CH3-ALR-CLR	0	R/W	CH3 alarm clear bit. If CH3-ALR_CLR = '1', and if both the ACLR*n* bit in the AUTO-DAC-CLR-EN Register and the CH3-ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If CH3-ALR_CLR = '0', then CH3-ALR goes to '1' and does not force any DAC to a clear status.
10	LT-Low-ALR-CLR	0	R/W	Local temperature sensor low alarm clear bit. If LT-Low-ALR-CLR = '1', and if both the ACLR*n* bit in the AUTO-DAC-CLR-EN Register and the LT-Low-ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If LT-Low-ALR-CLR = '0', then LT-Low-ALR goes to '1' and does not force any DAC to a clear status.
9	LT-High-ALR-CLR	0	R/W	Local temperature sensor high alarm clear bit. If LT-High-ALR-CLR = '1', and if both the ACLR*n* bit in the AUTO-DAC-CLR-EN Register and the LT-High-ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If LT-High-ALR-CLR = '0', then LT-High-ALR goes to '1' and does not force any DAC to a clear status.
8	D1-Low-ALR-CLR	0	R/W	Remote temperature sensor D1 low alarm clear bit. If D1-Low-ALR-CLR = '1', and if both the ACLR*n* bit in the AUTO-DAC-CLR-EN Register and the D1-Low-ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If D1-Low-ALR-CLR = '0', then D1-Low-ALR goes to '1' and does not force any DAC to a clear status.
7	D1-High-ALR-CLR	0	R/W	Remote temperature sensor D1 high alarm clear bit. If D1-High-ALR-CLR = '1', and if both the ACLR*n* bit in the AUTO-DAC-CLR-EN Register and the D1-High-ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If D1-High-ALR-CLR = '0', then D1-High-ALR goes to '1' and does not force any DAC to a clear status.
6	D2-Low-ALR-CLR	0	R/W	Remote temperature sensor D2 low alarm clear bit. If D2-Low-ALR-CLR = '1', and if both the ACLR*n* bit in the AUTO-DAC-CLR-EN Register and the D2-Low-ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If D2-Low-ALR-CLR = '0', then D2-Low-ALR goes to '1' and does not force any DAC to a clear status.
5	D2-High-ALR-CLR	0	R/W	Remote temperature sensor D2 high alarm clear bit. If D2-High-ALR-CLR = '1', and if both the ACLR*n* bit in the AUTO-DAC-CLR-EN Register and the D2-High-ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If D2-High-ALR-CLR = '0', then D2-High-ALR goes to '1' and does not force any DAC to a clear status.
4	D1-FAIL-CLR	0	R/W	D1 fail alarm clear bit. If D1-FAIL-CLR = '1', and if both the ACLR*n* bit in the AUTO-DAC-CLR-EN Register and the D2-FAIL-ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If D1-FAIL-ALR-CLR = '0', then D1-FAIL-ALR goes to '1' and does not force any DAC to a clear status.
3	D2-FAIL-CLR	0	R/W	D2 fail alarm clear bit. If D2-FAIL-CLR = '1', and if both the ACLR*n* bit in the AUTO-DAC-CLR-EN Register and the D2-FAIL-ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If D2-FAIL-ALR-CLR = '0', then D2-FAIL-ALR goes to '1' and does not force any DAC to a clear status.
2	THERM-ALR-CLR	1	R/W	Thermal alarm clear bit. If THERM-ALR-CLR = '1', and if both the ACLR*n* bit in the AUTO-DAC-CLR-EN Register and the THERM-ALR bit in the Status Register are set ('1'), then DAC*n* is forced to a clear status. If THERM-ALR-CLR = '0', then THERM-ALR goes to '1' and does not force any DAC to a clear status.
1	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.
0	—	0	R	Reserved. Writing to this bit causes no change. Reading this bit returns '0'.

AUTO-DAC-CLR-EN REGISTER (Read/Write, Address = 54h, Default = 0000h)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	ACLR 11	ACLR 10	ACLR 9	ACLR 8	ACLR 7	ACLR 6	ACLR 5	ACLR 4	ACLR 3	ACLR 2	ACLR 1	ACLR 0	0	0	0

Bits[14:3] **ACLR*n*:** Auto clear DAC-*n* enable bit.

If ACLR*n* = '1', DAC-*n* is forced into a clear state when the alarm occurs.

If ACLR*n* = '0', DAC-*n* is not forced into a clear state when the alarm occurs (default).

NOTE

ACLR*n* is always ignored when an alarm occurs for a temperature greater than +150°C (THERM-ALR = '1'). If an alarm activates for a temperature greater than +150°C, and if the THERM-ALR-CLR bit in the AUTO-DAC-CLR-SOURCE Register is set ('1'), all DACs are forced into a clear status. However, if THERM-ALR-CLR is cleared ('0'), the over +150°C alarm does not force any DAC to a clear status.

SW-DAC-CLR REGISTER (Read/Write, Address = 55h, Default = 0000h)

This register uses software to force the DAC into a clear state.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	ICLR 11	ICLR 10	ICLR 9	ICLR 8	ICLR 7	ICLR 6	ICLR 5	ICLR 4	ICLR 3	ICLR 2	ICLR 1	ICLR 0	0	0	0

Bits[14:3] **ICLR*n*:** Software clear DAC*n* bit.

If ICLR*n* = '1', DAC*n* is forced into a clear state.

If ICLR*n* = '0', DAC*n* is restored to normal operation.

HW-DAC-CLR-EN 0 REGISTER (Read/Write, Address = 56h, Default = 0000h)

This register determines which DAC is in a clear state when the $\overline{\text{DAC-CLR-0}}$ pin goes low.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	H0CLR 11	H0CLR 10	H0CLR 9	H0CLR 8	H0CLR 7	H0CLR 6	H0CLR 5	H0CLR 4	H0CLR 3	H0CLR 2	H0CLR 1	H0CLR 0	0	0	0

Bits[14:3] **H0CLR*n*:** Hardware clear DAC-*n* enable 1 bit.

If H0CLR*n* = '1', DAC-*n* is forced into a clear state when the $\overline{\text{DAC-CLR-0}}$ pin goes low.

If H0CLR*n* = '0', pulling the $\overline{\text{DAC-CLR-0}}$ pin low does not effect the state of DAC-*n*.

HW-DAC-CLR-EN 1 REGISTER (Read/Write, Address = 57h, Default = 0000h)

This register determines which DAC is in a clear state when the $\overline{\text{DAC-CLR-1}}$ pin goes low.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	H1CLR 11	H1CLR 10	H1CLR 9	H1CLR 8	H1CLR 7	H1CLR 6	H1CLR 5	H1CLR 4	H1CLR 3	H1CLR 2	H1CLR 1	H1CLR 0	0	0	0

Bits[14:3] **H1CLR*n*:** Hardware clear DAC-*n* enable 1 bit.

If H1CLR*n* = '1', DAC-*n* is forced into a clear state when the $\overline{\text{DAC-CLR-1}}$ pin goes low.

If H1CLR*n* = '0', pulling the $\overline{\text{DAC-CLR-1}}$ pin low does not effect the state of DAC-*n*.

DAC CONFIGURATION REGISTER (Read/Write, Address = 58h, Default = 0000h)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	SLDA 11	SLDA 10	SLDA 9	SLDA 8	SLDA 7	SLDA 6	SLDA 5	SLDA 4	SLDA 3	SLDA 2	SLDA 1	SLDA 0

Bits[11:0] **SLDA-*n*:** DAC synchronous load enable bit.

If SLDA-*n* = '1', synchronous load is enabled. When internal load DAC signal ILDAC occurs, the DAC-*n* Latch is loaded with the value of the corresponding DAC*n*-Data Register, and the output of DAC-*n* is updated immediately. The internal load DAC signal ILDAC is generated by writing a '1' to the ILDAC bit in the AMC Configuration Register. In synchronous Load, a write command to the DAC-*n*-Data Register updates that register only, and does not change the DAC-*n* output.

If SLDA-*n* = '0', asynchronous load is enabled. A write command to the DAC-*n*-Data Register immediately updates the DAC-*n* Latch and the output of DAC-*n*. The synchronous load DAC signal (ILDAC) does not affect DAC*n*. the default value of SLDA-*n* = '0'. The AMC7812 updates the DAC Latch only if the ILDAC bit was set ('1'), thereby eliminating unnecessary glitch. Any DAC channels that have not been accessed are not reloaded. When the DAC Latch is updated, the corresponding output changes to the new level immediately. Note that the SLDA-*n* bit is ignored in auto mode (DAC-*n* Mode bits do not equal '00'). In auto mode, the DAC Latch is always updated asynchronously.

NOTE

The DACs can be forced into a clear state immediately by the external $\overline{\text{DAC-CLR-n}}$ signal, by alarm events, and by writing to the SW-DAC-CLR Register. In these cases, the SLDA-*n* bit is ignored.

DAC GAIN REGISTER (Read/Write, Address = 59h, Default = 0000h)

The DAC*n* GAIN bits specify the output range of DAC*n*.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	DAC11 GAIN	DAC10 GAIN	DAC9 GAIN	DAC8 GAIN	DAC7 GAIN	DAC6 GAIN	DAC5 GAIN	DAC4 GAIN	DAC3 GAIN	DAC2 GAIN	DAC1 GAIN	DAC0 GAIN

Bits[11:0] **DAC*n*GAIN:** DAC*n* gain bit.

If DAC*n* GAIN = '1', the gain = 5 and the output is 0 to 5 · VREF

If DAC*n* GAIN = '0', the gain = 2 and the output is 0 to 2 · VREF

ANALOG INPUT CHANNEL THRESHOLD REGISTERS (Read/Write, Addresses = 5Ah to 61h)

Four analog auxiliary inputs (CH0, CH1, CH2, and CH3) and three temperature sensors (LT, D1, and D2) implement an out-of-range alarm function. Threshold-High-*n* and Threshold-Low-*n* (where n = 0, 1, 2, 3) define the upper bound and lower bound of the *n*th analog input range, as shown in Table 27. This window determines whether the nth input is out-of-range. When the input is outside the window, the corresponding CH-ALR-*n* bit in the Status Register is set to '1'.

For normal operation, the value of Threshold-High-*n* must be greater than the value of Threshold-Low-*n*; otherwise, CH-ALR-*n* is always set to '1' and an alarm is always indicated. Note that when the analog channel is accessed as single-ended input, its threshold is in a straight binary format. However, when the channel is accessed as a differential pair, its threshold is in twos complement format.

Table 27. Threshold Coding

INPUT CHANNEL	INPUT TYPE	THRESHOLD STORED IN	FORMAT
Channel 0	Single-Ended	Input-0-Threshold-High-Byte Input-0-Threshold-Low-Byte	Straight binary
Channel 1	Single-Ended	Input-1-Threshold- High-Byte Input-1-Threshold- Low-Byte	Straight binary
Channel 2	Single-Ended	Input-2-Threshold- High-Byte Input-2-Threshold- Low-Byte	Straight binary
Channel 3	Single-Ended	Input-3-Threshold- High-Byte Input-3-Threshold- Low-Byte	Straight binary
CH0+/CH1–	Differential	Input-0-Threshold- High-Byte Input-0-Threshold- Low-Byte	Twos complement
CH2+/CH3–	Differential	Input-2-Threshold- High-Byte Input-2-Threshold- Low-Byte	Twos complement

Input-*n*-High-Threshold Register (where n = 0, 1, 2, 3) (Read/Write, Default = 0FFFh)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	THRH 11	THRH 10	THRH 9	THRH 8	THRH 7	THRH 6	THRH 5	THRH 4	THRH 3	THRH 2	THRH 1	THRH 0

Bits[15:12] Reserved. These bits are '0' when read back. Writing to these bits has no effect.

Bits[11:0] **THRH*n*:** Data bits of the upper-bound threshold of the *n*th analog input.

Input-*n*-Low-Threshold Register (where n = 0, 1, 2, 3) (Read/Write, Default = 0000h)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	THRL 11	THRL 10	THRL 9	THRL 8	THRL 7	THRL 6	THRL 5	THRL 4	THRL 3	THRL 2	THRL 1	THRL 0

Bits[15:12] Reserved. These bits are '0' when read back. Writing to these bits has no effect.

Bits[11:0] **THRL*n*:** Data bits of the lower-bound threshold of the *n*th analog input.

TEMPERATURE THRESHOLD REGISTERS

LT-High-Threshold Register (Read/Write, Address = 62h, Default = 07FFh, +255.875°C)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	THRH 11	THRH 10	THRH 9	THRH 8	THRH 7	THRH 6	THRH 5	THRH 4	THRH 3	THRH 2	THRH 1	THRH 0

Bits [15:12] = ‘0' when read back. Writing these bits causes no change

LT-Low-Threshold Register (Read/Write, Address = 63h, Default = 0800h, –256°C)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	THRL 11	THRL 10	THRL 9	THRL 8	THRL 7	THRL 6	THRL 5	THRL 4	THRL 3	THRL 2	THRL 1	THRL 0

Bits [15:12] = Reserved. Writing to these bits causes no change. Reading these bits returns '0'.

D1-High-Threshold Register (Read/Write, Address = 64h, Default = 07FFh, +255.875°C)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	THRH 11	THRH 10	THRH 9	THRH 8	THRH 7	THRH 6	THRH 5	THRH 4	THRH 3	THRH 2	THRH 1	THRH 0

Bits [15:12] = ‘0' when read back. Writing these bits causes no change

D1-Low-Threshold Register (Read/Write, Address = 65h, Default = 0800h, –256°C)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	THRL 11	THRL 10	THRL 9	THRL 8	THRL 7	THRL 6	THRL 5	THRL 4	THRL 3	THRL 2	THRL 1	THRL 0

Bits [15:12] = ‘0' when read back. Writing these bits causes no change

D2-High-Threshold Register (Read/Write, Address = 66h, Default = 07FFh, +255.875°C)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	THRH 11	THRH 10	THRH 9	THRH 8	THRH 7	THRH 6	THRH 5	THRH 4	THRH 3	THRH 2	THRH 1	THRH 0

Bits [15:12] = ‘0' when read back. Writing these bits causes no change

D2-Low-Threshold Register (Read/Write, Address = 67h, Default = 0800h, –256°C)

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	THRL 11	THRL 10	THRL 9	THRL 8	THRL 7	THRL 6	THRL 5	THRL 4	THRL 3	THRL 2	THRL 1	THRL 0

Bits [15:12] = ‘0' when read back. Writing these bits causes no change

HYSTERESIS REGISTERS

The hysteresis registers define the hysteresis in the alarm detection of an individual alarm.

Hysteresis Register 0 (Read/Write, Address = 68h, Default = 0810h, 8 LSB)

This register contains the hysteresis values for CH0 and CH1.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	CH0-HYS-6	CH0-HYS-5	CH0-HYS-4	CH0-HYS-3	CH0-HYS-2	CH0-HYS-1	CH0-HYS-0	CH1-HYS-6	CH1-HYS-5	CH1-HYS-4	CH1-HYS-3	CH1-HYS-2	CH1-HYS-1	CH1-HYS-0	0

Bits[14:8] **CH0-HYS-*n*:** Hysteresis of CH0, 1 LSB per step.

Bits[7:1] **CH1-HYS-*n*:** Hysteresis of CH1, 1 LSB per step.

Hysteresis Register 1 (Read/Write, Address = 69h, Default = 0810h, 8 LSB)

This register contains the hysteresis values for CH2 and CH3.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	CH2-HYS-6	CH2-HYS-5	CH2-HYS-4	CH2-HYS-3	CH2-HYS-2	CH2-HYS-1	CH2-HYS-0	CH3-HYS-6	CH3-HYS-5	CH3-HYS-4	CH3-HYS-3	CH3-HYS-2	CH3-HYS-1	CH3-HYS-0	0

Bits[14:8] **CH2-HYS-*n*:** Hysteresis of CH2, 1 LSB per step.

Bits[7:1] **CH3-HYS-*n*:** Hysteresis of CH3, 1 LSB per step.

Hysteresis Register 2 (Read/Write, Address = 6Ah, Default = 2108h, 8°C)

This register contains the hysteresis values for D2, D1, and LT. The range is 0°C to +31°C.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	D2-HYS-7	D2-HYS-6	D2-HYS-5	D2-HYS-4	D2-HYS-3	D1-HYS-7	D1-HYS-6	D1-HYS-5	D1-HYS-4	D1-HYS-3	LT-HYS-7	LT-HYS-6	LT-HYS-5	LT-HYS-4	LT-HYS-3

Bits[14:10] **D2-HYS-*n*:** Hysteresis of D2, 1°C per step. Note that bits D2-HYS-[2:0] are always '0'.

Bits[9:5] **D1-HYS-*n*:** Hysteresis of D1, 1°C per step. Note that bits D1-HYS-[2:0] are always '0'.

Bits[4:0] **LT-HYS-*n*:** Hysteresis of LT, 1°C per step. Note that bits LT-HYS-[2:0] are always '0'.

POWER-DOWN REGISTER (Read/Write, Address = 6Bh, Default = 0000h)

After power-on or reset, all bits in the Power-Down Register are cleared to '0', and all the components controlled by this register are either powered-down or off. The Power-Down Register allows the host to manage the AMC7812 power dissipation. When not required, the ADC, the reference buffer amplifier, and any of the DACs can be put into an inactive low-power mode to reduce current drain from the supply. The bits in the Power-Down Register control this power-down function. Set the respective bit to '1' to activate the corresponding function.

MSB BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	PADC	PREF	PDAC 0	PDAC 1	PDAC 2	PDAC 3	PDAC 4	PDAC 5	PDAC 6	PDAC 7	PDAC 8	PDAC 9	PDAC 10	PDAC 11	0

Bit 14 **PADC:** Power-down mode control bit.
If PADC = '1', the ADC is in normal operating mode.
If PADC = '0', the ADC is inactive in low-power mode.

Bit 13 **PREF:** Internal reference in power-down mode control bit.
If PREF = '1', the reference buffer amplifier is powered on.
If PREF = '0', the reference buffer amplifier is inactive in low-power mode.

Bits[12:1] **PDAC*n*:** DAC*n* power-down control bit.
If PDAC*n* = '1', DAC*n* is in normal operating mode.
If PDAC*n* = '0', DAC*n* is inactive in low-power mode and its output buffer amplifier is in a Hi-Z state. The output pin of DAC*n* is internally switched from the buffer output to the analog ground through an internal resistor.

Device ID Register (Read-Only, Address = 6Ch, Default = 1220h)

Model and revision information.

Software Reset Register (Read/Write, Address = 7Ch, Default = NA)

The Software Reset Register resets all registers to default values, except for the DAC Data Register, DAC Latch, and DAC Clear Register. The software reset is similar to a hardware reset, which resets all registers including the DAC Data Register, DAC Latch, and DAC Clear Register. After a software reset, make sure that the DAC Data Register, DAC latch, and DAC Clear Register are set to the desired values before the DAC is powered on.

SPI Mode

In SPI Mode, writing 6600h to this register forces the device reset.

I^2C Mode

Writing to this register (with any data) forces the device to perform a software reset. Reading this register returns an undefined value that must be ignored. Note that this register is 8-bit, instead of 16-bit. Both reading from and writing to this register are single-byte operations. Writing data to the Software Reset Register in I^2C Mode is shown in the following steps:

1. The master device asserts a start condition.
2. The master then sends the 7-bit AMC7812 slave address followed by a zero for the direction bit, indicating a write operation.
3. The AMC7812 asserts an acknowledge signal on SDA.
4. The master sends register address 7Ch.
5. The AMC7812 asserts an acknowledge signal on SDA.
6. The master sends a data byte.
7. The AMC7812 asserts an acknowledge signal on SDA.
8. The master asserts a stop condition to end the transaction.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2012) to Revision E **Page**

- Changed 2nd, 4th, 5th, and 7th values in Slave Address column in Table 8 49

Changes from Revision C (March 2012) to Revision D **Page**

- Added T_A = +25°C to Load current Test Conditions for Source within 200mV 3
- Added T_A = +25°C to Load current Test Conditions for Sink within 300mV 3
- Added DAC output = 0V to +5V, code B33h. Source and/or sink, voltage drop < 25mV, T_A: -40°C to 95°C(1) to Load current Test Conditions 3
- Added 0V to VREF mode to Input capacitance 4
- Added 0V to (2 · VREF) mode to Input capacitance 4
- Changed UNIT from ms to µs in TIMING CHARACTERISTICS: SDA and SCL for Standard and Fast Modes 10
- Added I^2C Timeout Function Section. 10
- Added Note recommending an SCL frequency of at least 1kHz to avoid a timeout event. 10
- Added I^2C Timeout Function Section. 11
- Added Note recommending an SCL frequency of at least 1kHz to avoid a timeout event. 11
- Changed Output data valid time in TIMING CHARACTERISTICS: SPI Bus 13
- Added I^2C Timeout Function Section. 50
- Changed Register Map address 4B default to 00FF 60
- Changed GPIO Register Default address to 00FFh 65
- Changed - Hysteresis Register 2 text From: "The range is 0°C to +32°C" To: "The range is 0°C to +31°C" 78

(1) Valid only for material manufactured on or after October 2012.

Changes from Revision B (November 2011) to Revision C **Page**

- Changed Features Bullet From: Small Packages: 9mm x 9mm QFN-64 To: Small Packages: 9mm x 9mm QFN-64, and 10mm x 10mm HTQFP-64 1
- Added HTQFP-64 package option to the Description 1
- Added HTQFP-64 package to the PACKAGE/ORDERING INFORMATION table 2
- Added PAP (HTQFP) to the Thermal Information table 2
- Added the HTQFP-64 Pin Configuration 8
- Added text "QFN Package" to Figure 75 and Figure 76 27
- Added Figure 77 and Figure 78 27
- η-Factor Range Table, Changed From: 0000 0020 To: 0000 0010 37
- η-Factor Range Table, Changed From 1111 0000 To: 1000 0000 37

Changes from Revision A (March 2011) to Revision B **Page**

- Added text to *Desciption* section 1
- Added Reset Delay parameter to Electrical Characteristics 6
- Added Convert Pulse Width parameter to Electrical Characteristics 6
- Added Reset Pulse Width parameter to Electrical Characteristics 6
- Changed recommended compensation capacitor from 470nF to 4.7µF 9
- Changed recommended compensation capacitor value from 470nF to 4.7µF to reflect bench characterization conditions 39
- Changed text in first paragraph of *Clear DACs* section 43
- Clarified voltage condition for hardware reset 48
- Added description of software reset function 48
- Added voltage condition for initiation of POR 48
- Added *Power Supply Sequence* section. 49

Changes from Original (January 2011) to Revision A **Page**

- Changed Load Current to include separate source/sink test conditions; updated from one row with typical value of ±7mA at 200mV 3
- Added Direct Mode test condition to Conversion Rate parameter 4
- Deleted test condition from Absolute Input Voltage parameter 4
- Added note to clarify Power Dissipation conditions 6
- Added missing figure number for Figure 6 14
- Updated X axis range in Figure 34 to include –12mA 18
- Changed Y axis label to "Offset Error" in Figure 61 (typo) 23
- Added Figure 67 25
- Updated *Programmable Conversion Rate* section 32
- Added Nap Enabled column to Table 1 32
- Changed latch position in Figure 93 43
- Changed Table 9 to show SDI/SDO relationship 56
- Changed bit 12 entries of Table 23 from *don't care* to 0 71
- Changed bit 9 entries of Table 24 from *don't care* to 0 71

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC7812SPAP	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC7812	Samples
AMC7812SPAPR	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC7812	Samples
AMC7812SRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC7812	Samples
AMC7812SRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC7812	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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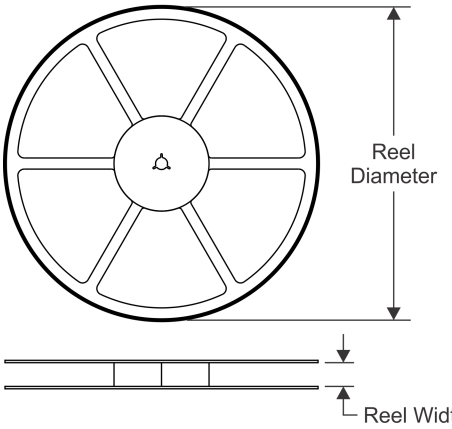
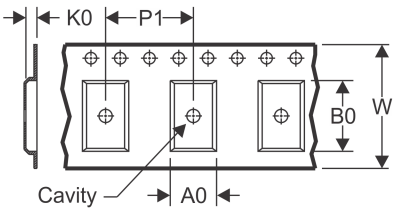
TAPE AND REEL INFORMATION

REEL DIMENSIONS

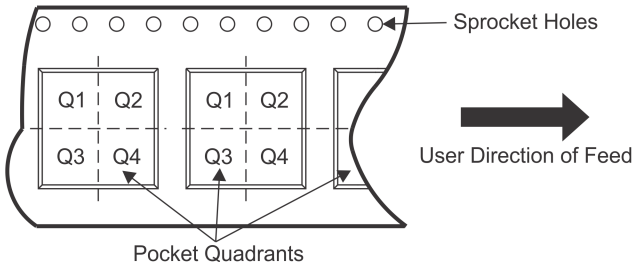


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

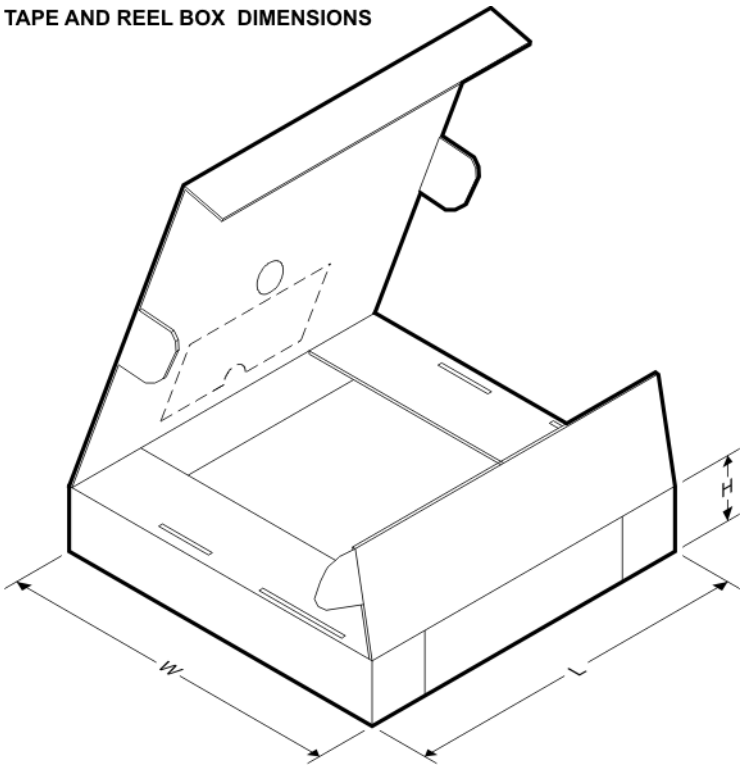
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC7812SPAPR	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
AMC7812SRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
AMC7812SRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

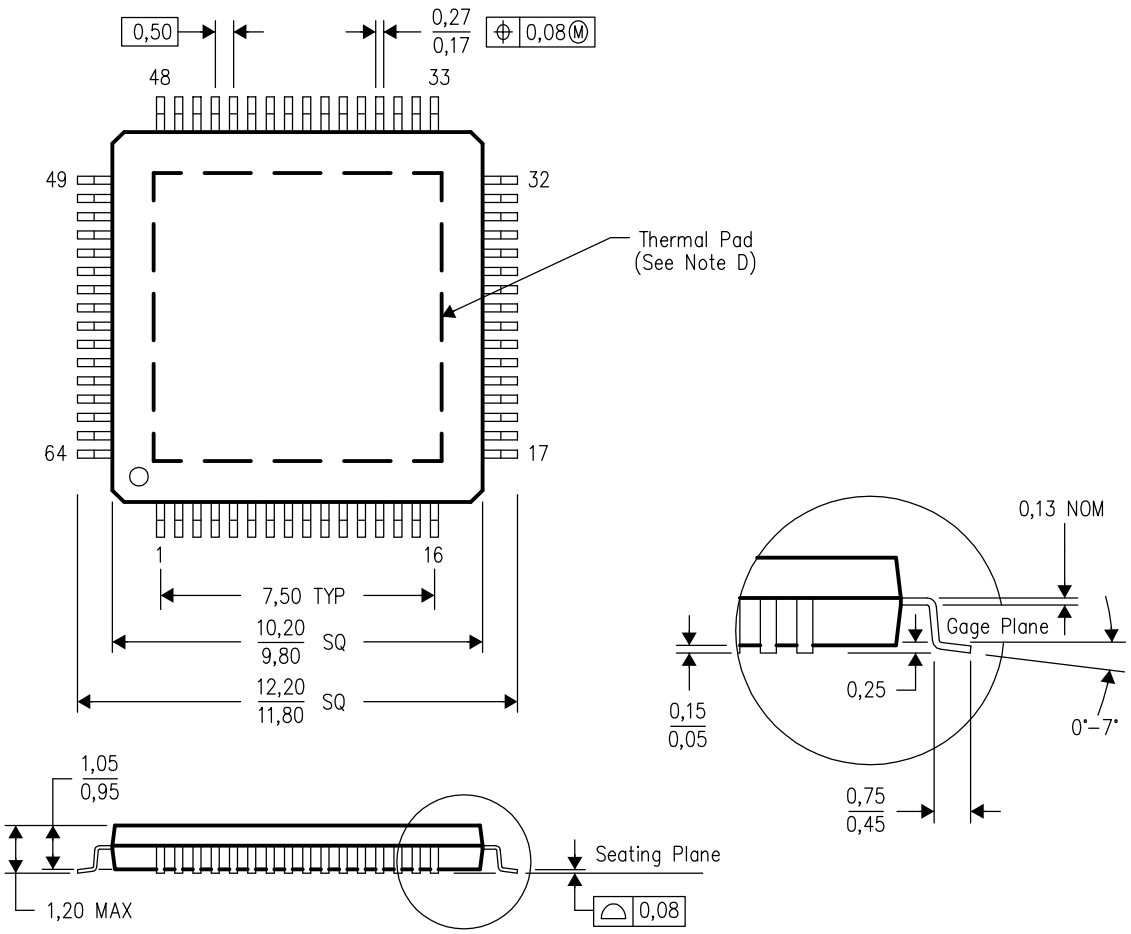
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC7812SPAPR	HTQFP	PAP	64	1000	367.0	367.0	55.0
AMC7812SRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
AMC7812SRGCT	VQFN	RGC	64	250	210.0	185.0	35.0

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

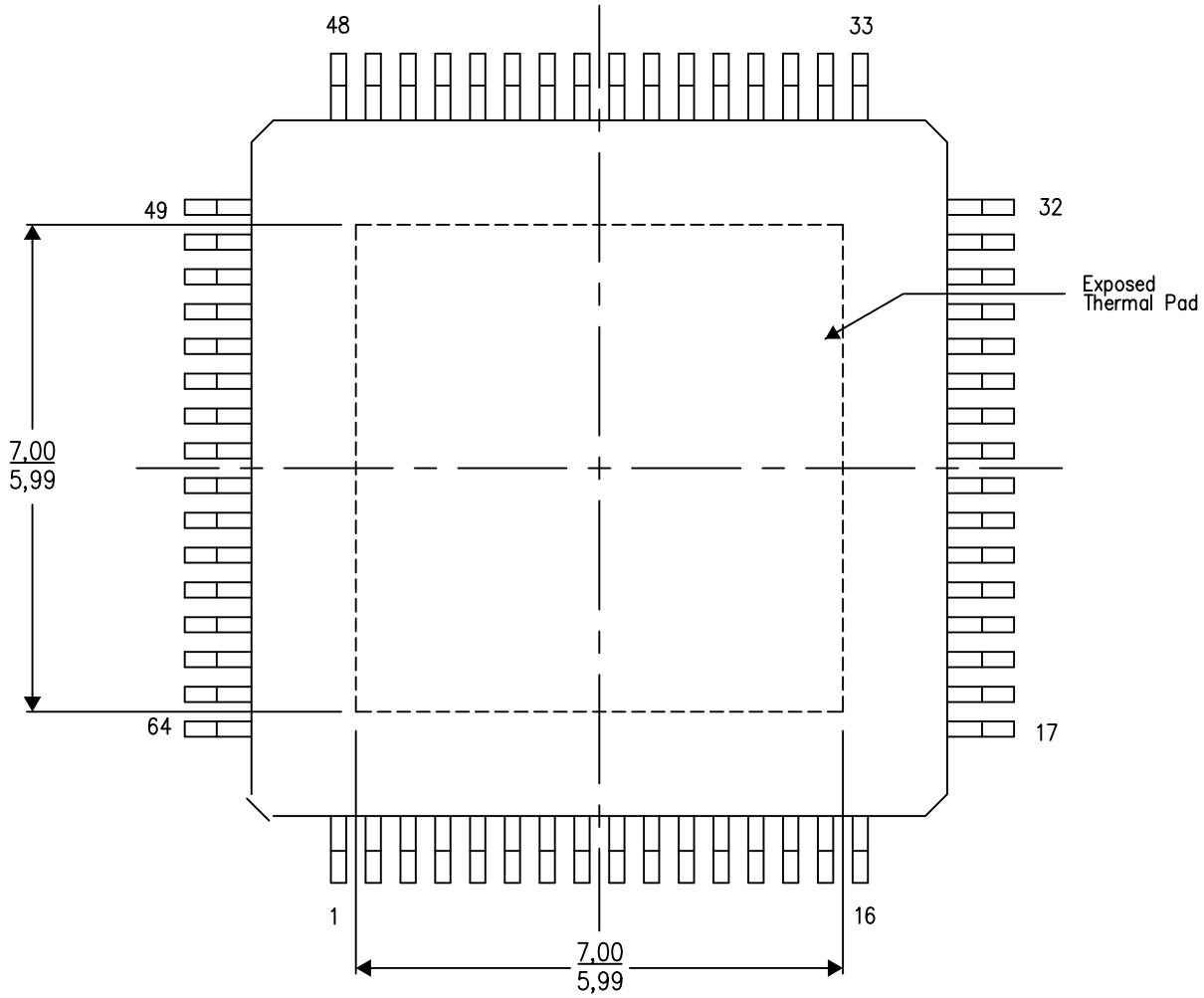
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206326–5/P 05/14

NOTES: A. All linear dimensions are in millimeters

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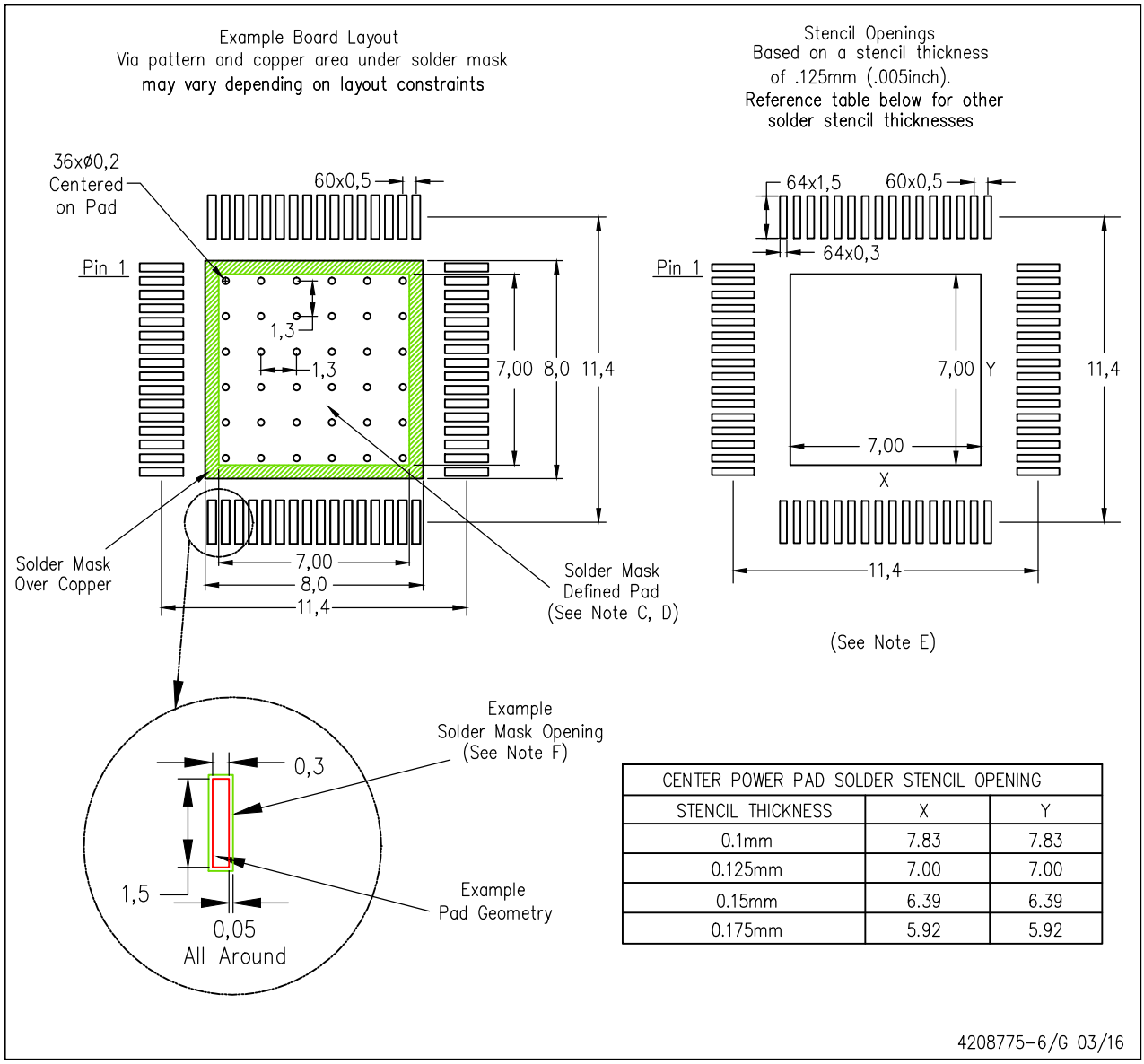
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	7.83	7.83
0.125mm	7.00	7.00
0.15mm	6.39	6.39
0.175mm	5.92	5.92

4208775–6/G 03/16

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

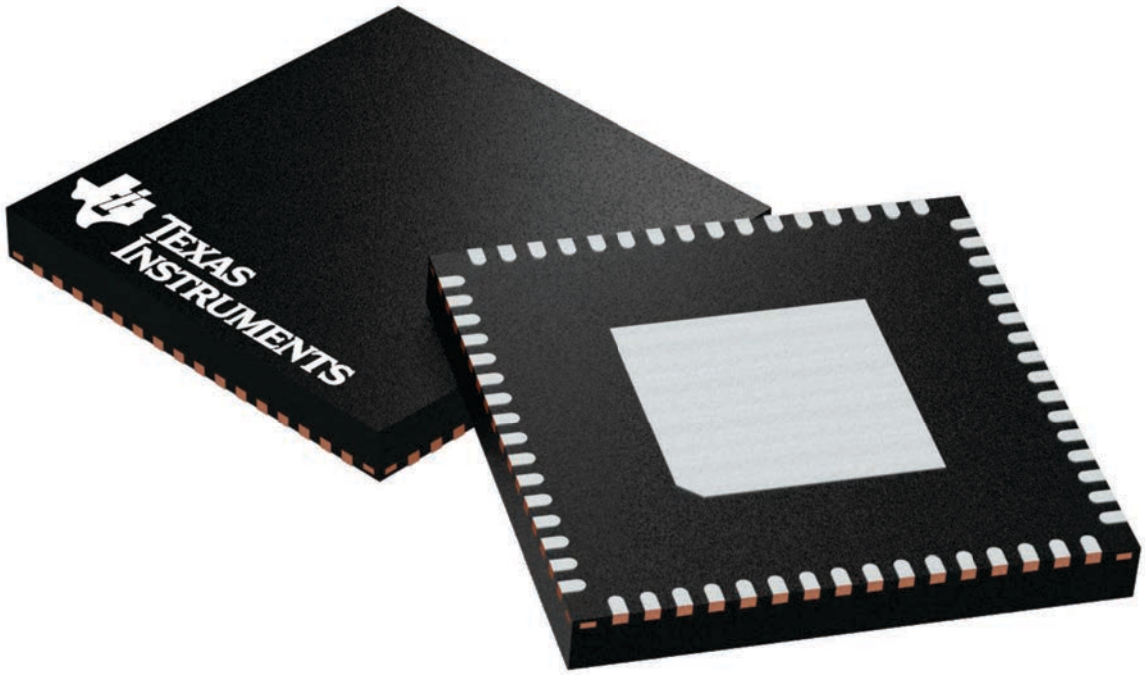
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

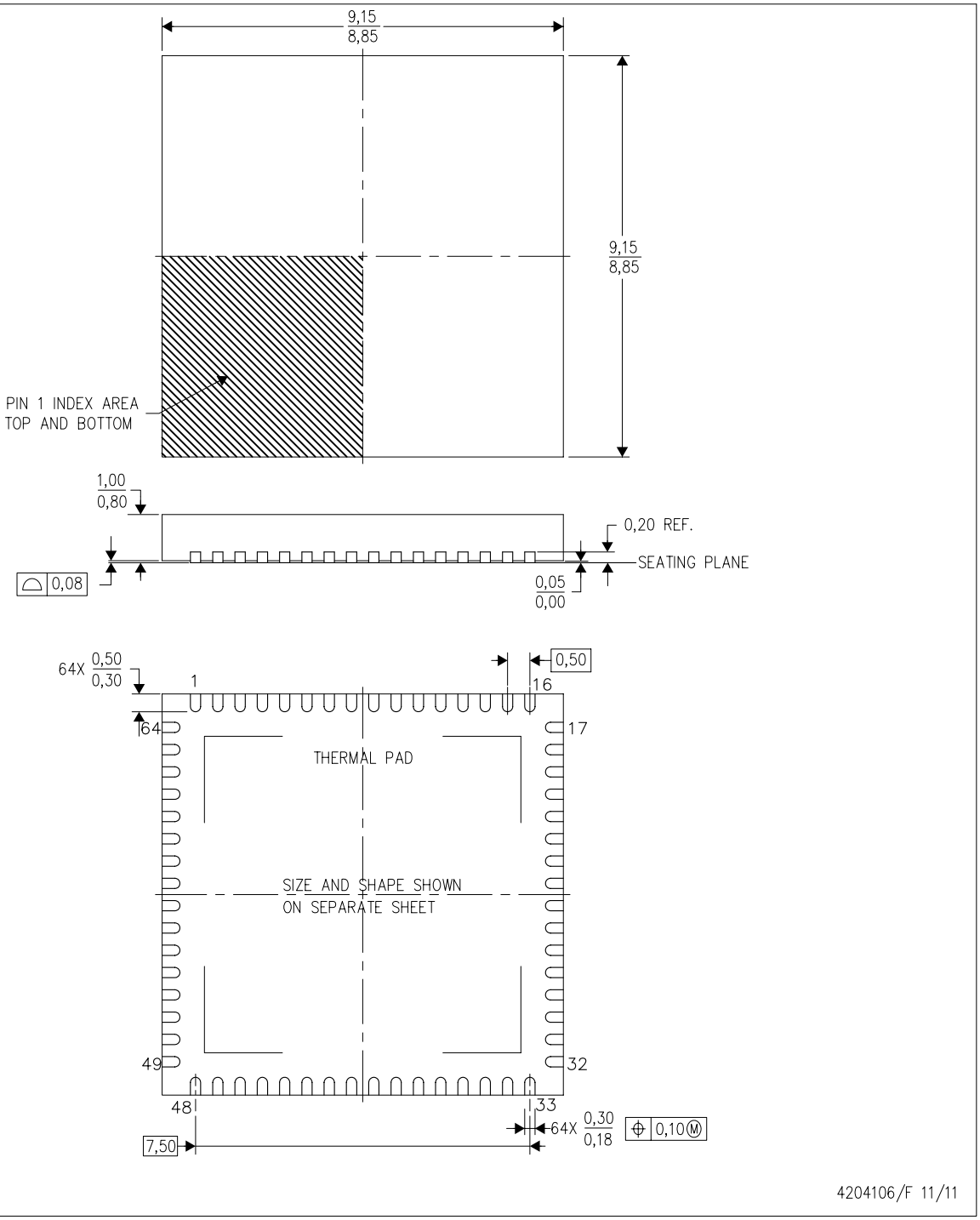
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224597/A

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

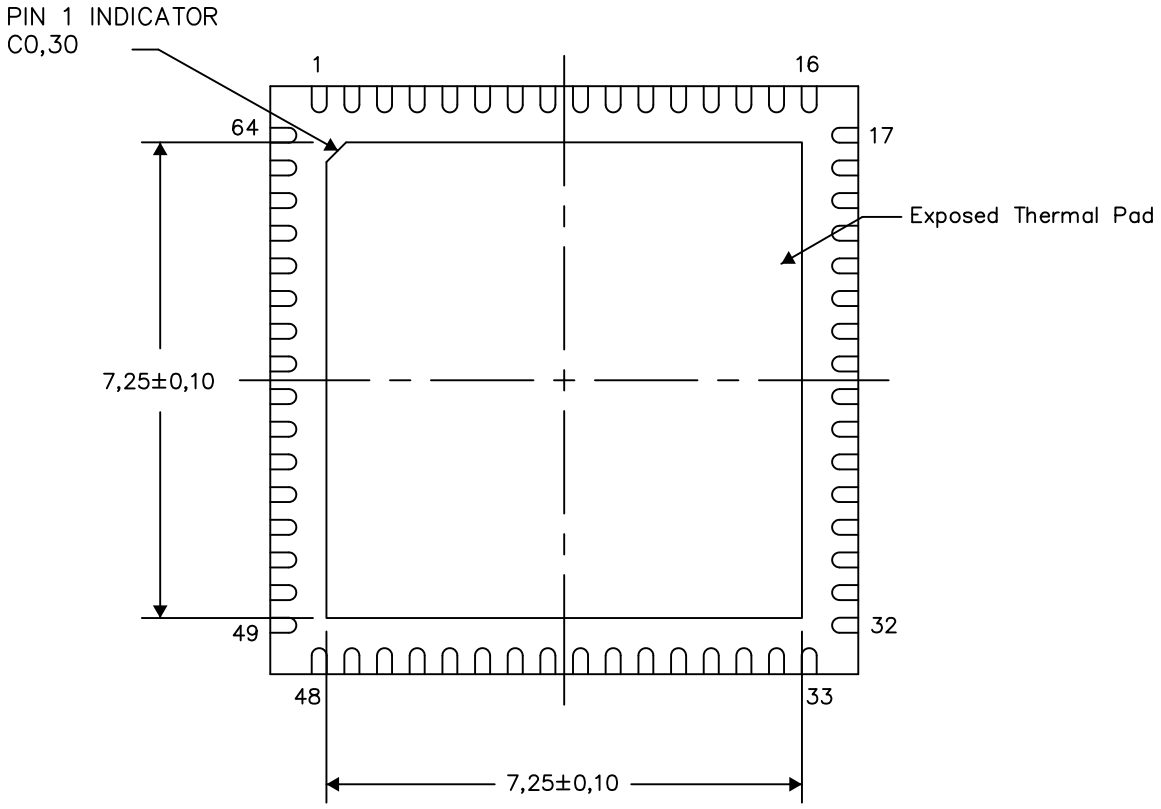
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206192–2/AE 03/15

NOTE: A. All linear dimensions are in millimeters

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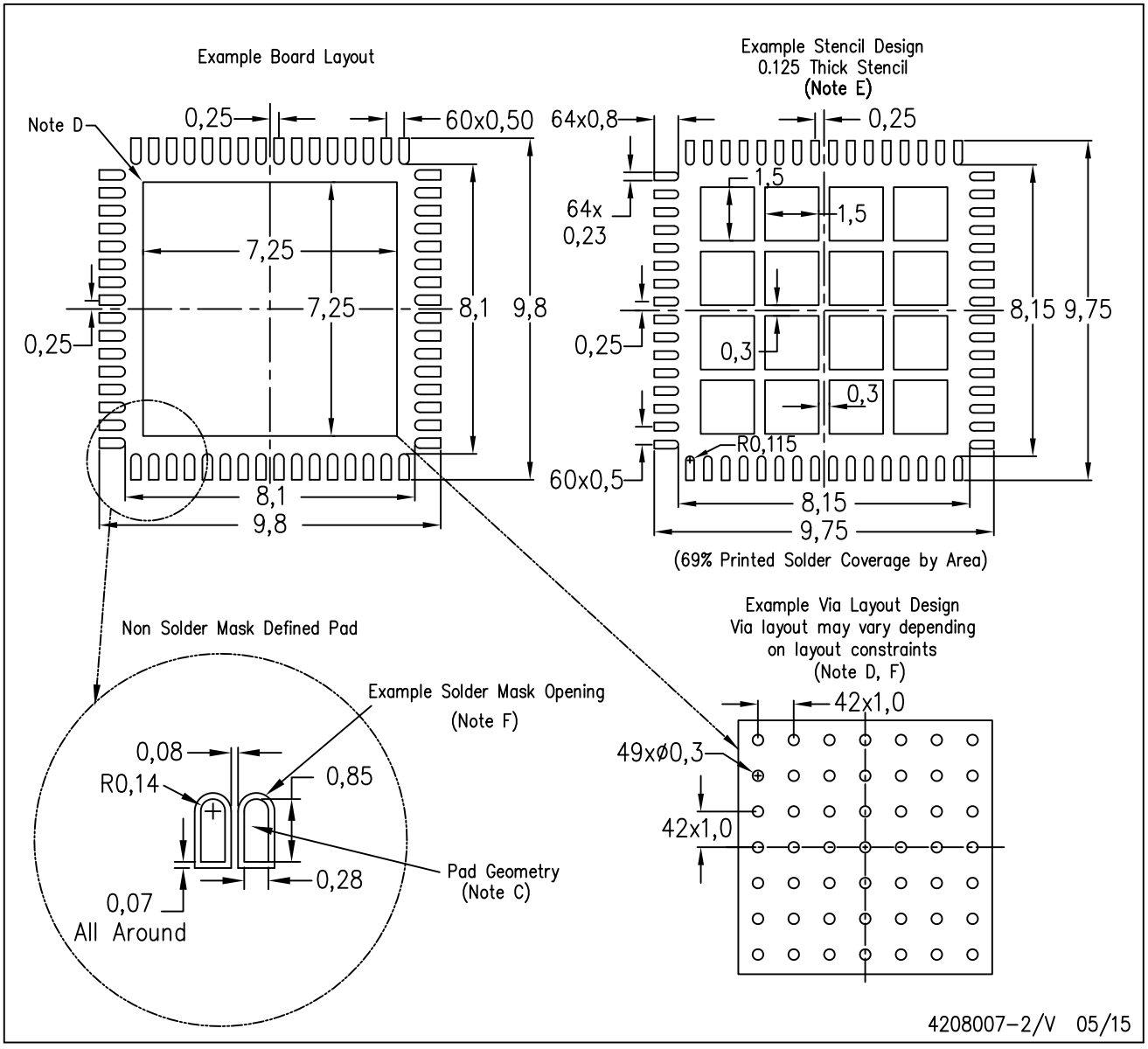

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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