THE DATASHEET OF

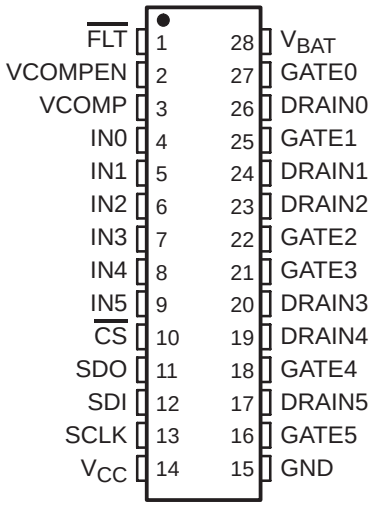
TPIC46L01DB

TPIC46L01, TPIC46L02, TPIC46L03
6-CHANNEL SERIAL AND PARALLEL LOW-SIDE PRE-FET DRIVER

SLIS055B – NOVEMBER 1996 – REVISED AUGUST 2001

- **6-Channel Serial-In/Parallel-In Low-side Pre-FET Driver**
- **Device Can Be Cascaded**
- **Internal 55-V Inductive Load Clamp and V_{GS} Protection Clamp for External Power FETs**
- **Independent Shorted-Load/Short-to-Battery Fault Detection on All Drain Terminals**
- **Independent Off-State Open-Load Fault Sense**
- **Over-Battery-Voltage Lockout Protection and Fault Reporting**
- **Under-Battery Voltage Lockout Protection for TPIC46L01 and TPIC46L02**
- **Asynchronous Open-Drain Fault Flag**
- **Device Output Can Be Wire-ORed With Multiple External Devices**
- **Fault Status Returned Through Serial Output Terminal**
- **Internal Global Power-On Reset of Device**
- **High-Impedance CMOS Compatible Inputs With Hysteresis**
- **TPIC46L01 and TPIC46L03 Disables the Gate Output When a Shorted-Load Fault Occurs**
- **TPIC46L02 Transitions the Gate Output to a Low-Duty Cycle PWM Mode When a Shorted-Load Fault Occurs**

DB PACKAGE
(TOP VIEW)



description

The TPIC46L01, TPIC46L02, and TPIC46L03 are low-side predrivers that provide serial input interface and parallel input interface to control six external field-effect transistor(FET) power switches such as offered in the Texas Instruments TPIC family of power arrays. These devices are designed primarily for low-frequency switching, inductive load applications such as solenoids and relays. Fault status for each channel is available in a serial-data format. Each driver channel has independent off-state open-load detection and on-state shorted-load/short-to-battery detection. Battery overvoltage and undervoltage detection and shutdown are provided. Battery and output load faults provide real-time fault reporting to the controller. Each channel also provides inductive-voltage-transient protection for the external FET.

These devices provide control of output channels through a serial input interface or a parallel input interface. A command to enable the output from either interface enables the respective channel GATE output to the external FET. The serial input interface is recommended when the number of signals between the control device and the predriver must be minimized, and the speed of operation is not critical. In applications where the predriver must respond very quickly or asynchronously, the parallel input interface is recommended.

description (continued)

For serial operation, the control device must transition $\overline{CS}$ from high to low to activate the serial input interface. When this occurs, SDO is enabled, fault data is latched into the serial input interface, and the $\overline{FLT}$ flag is refreshed.

Data is clocked into the serial registers on low-to-high transitions of SCLK through SDI. Each string of data must consist of 8 bits of data. In applications where multiple devices are cascaded together, the string of data must consist of 8 bits for each device. A high data bit turns the respective output channel on and a low data bit turns it off. Fault data for the device is clocked out of SDO as serial input data is clocked into the device. Fault data consists of fault flags for the over-battery voltage (bit 8), under-battery voltage (bit 7) (not on TPIC46L03), and shorted/open-load flags (bits 1-6) for each of the six output channels. A logic-high bit in the fault data indicates a fault and a logic-low bit indicates that no fault is present on that channel. Fault register bits are set or cleared asynchronously to reflect the current state of the hardware. The fault must be present when $\overline{CS}$ is transitioned from high to low to be captured and reported in the serial fault data. New faults cannot be captured in the serial register when $\overline{CS}$ is low. $\overline{CS}$ must be transitioned high after all of the serial data has been clocked into the device. A low-to-high transition of $\overline{CS}$ transfers the last 6 bits of serial data to the output buffer, puts SDO in a high-impedance state, and clears and reenables the fault register. The TPIC46L01/L02/L03 was designed to allow the serial input interfaces of multiple devices to be cascaded together to simplify the serial interface to the controller. Serial input data flows through the device and is transferred out SDO following the fault data in cascaded configurations.

For parallel operation, data is asynchronously transferred directly from the parallel input interface (IN0-IN5) to the respective GATE output. SCLK or $\overline{CS}$ are not required for parallel control. A 1 on the parallel input turns the respective channel on, where a 0 turns it off. Note that either the serial interface or the parallel interface can enable a channel. Under parallel operation, fault data must still be collected through the serial data interface.

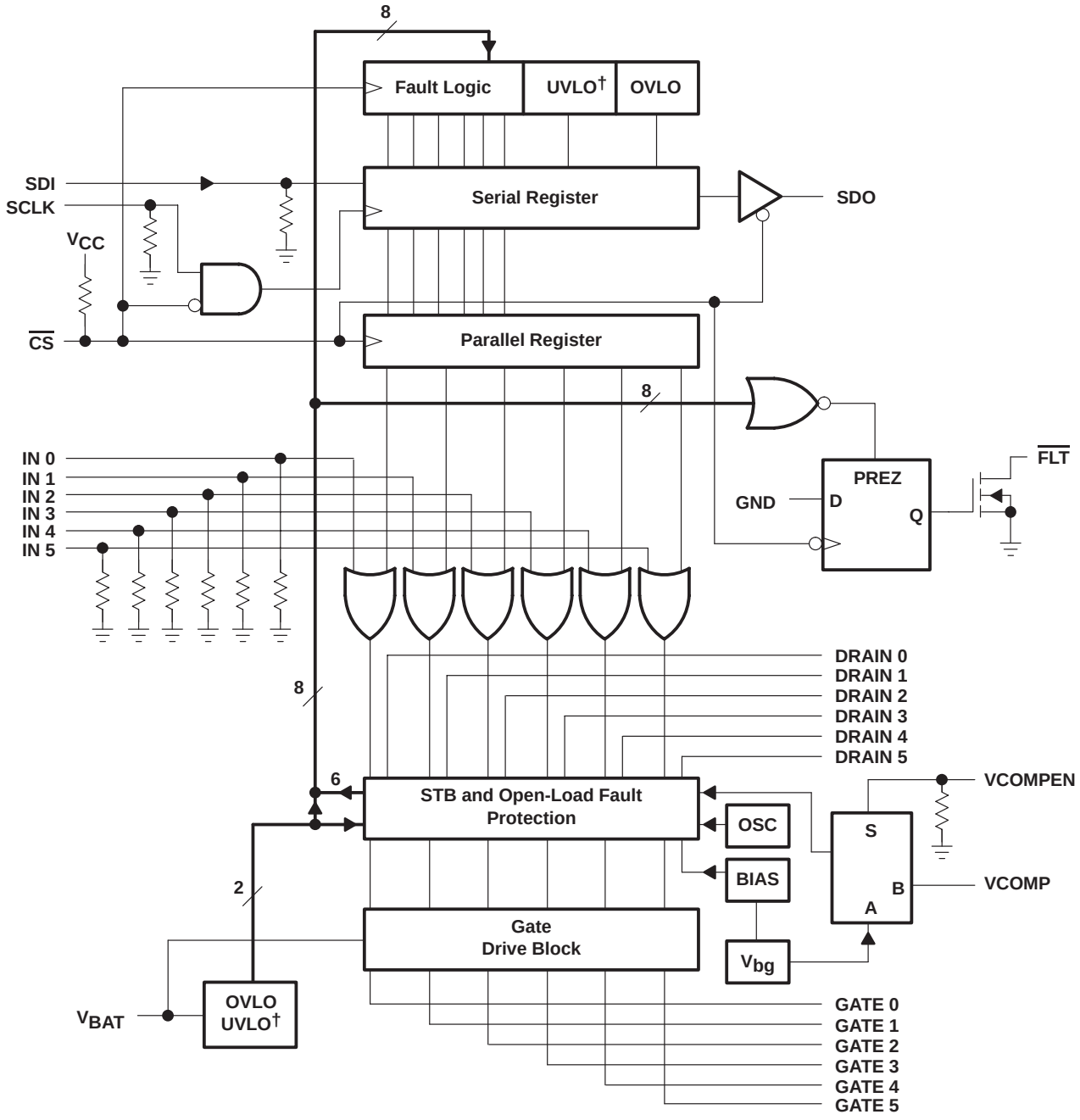
The predrivers monitor the drain voltage for each channel to detect shorted-load or open-load fault conditions in the on and off states respectively. These devices offer the option of using an internally generated fault-reference voltage or an externally supplied VCOMP for fault detection. The internal fault reference is selected by connecting VCOMPEN to GND and the external reference is selected by connecting VCOMPEN to V_{CC}. The drain voltage is compared to the fault-reference voltage when the channel is turned on to detect shorted-load conditions and when the channel is off to detect open-load conditions. When a shorted-load fault occurs using the TPIC46L01 or TPIC46L03, the channel is turned off and a fault signal is sent to $\overline{FLT}$ as well as to the serial fault-register bit. When a shorted-load fault occurs while using the TPIC46L02, the channel transitions into a low-duty cycle, pulse-width-modulated (PWM) signal as long as the fault is present. Shorted-load conditions must be present for at least the shorted-load deglitch time, $t_{(STBDG)}$, in order to be flagged as a fault. A fault signal is sent to $\overline{FLT}$ as well as the serial fault register bit. More detail on fault detection operation is presented in the device operation section of this data sheet.

The TPIC46L01 and TPIC46L02 provide protection from over-battery voltage and under-battery voltage conditions irrespective of the state of the output channels. The TPIC46L03 provides protection from over-battery voltage conditions irrespective of the state of the output channels When the battery voltage is greater than the overvoltage threshold or less than the undervoltage threshold (except for the TPIC46L03, which has no undervoltage threshold), all channels are disabled and a fault signal is sent to $\overline{FLT}$ as well as to the respective fault register bits. The outputs return to normal operation once the battery voltage fault has been corrected. When an over-battery/under-battery voltage condition occurs, the device reports the battery fault, but disables fault reporting for open and shorted-load conditions. Fault reporting for open and shorted-load conditions are reenabled after the battery fault condition has been corrected.

These devices provide inductive transient protection on all channels. The drain voltage is clamped to protect the FET. This clamp voltage is defined by the sum of V_{CC} and turn-on voltage of the external FET. The predriver also provides a gate-to-source voltage (V_{GS}) clamp to protect the GATE-source terminals of the power FET from exceeding their rated voltages.

These devices provide pulldown resistors on all inputs except $\overline{CS}$. A pullup resistor is used on $\overline{CS}$.

schematic diagram



† UVLO is not in TPIC46L03

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{CS}$	10	I	Chip select. A high-to-low transition on the $\overline{CS}$ enables SDO, latches fault data into the serial interface, and refreshes the fault flag. When $\overline{CS}$ is high, the fault registers can change fault status. On the falling edge of $\overline{CS}$, fault data is latched into the serial output register and transferred using SDO and SCLK. On a low-to-high transition of $\overline{CS}$, serial data is latched in to the output control register.
DRAIN0 DRAIN1 DRAIN2 DRAIN3 DRAIN4 DRAIN5	26 24 23 20 19 17	I	FET drain inputs. DRAIN0 through DRAIN5 are used for both open-load and short-circuit fault detection at the drain of the external FETs. They are also used for inductive transient protection.
$\overline{FLT}$	1	O	Fault flag. $\overline{FLT}$ is an open-drain output that provides a real-time fault flag for shorted-load/open-load/over-battery voltage/under-battery voltage faults. The device can be ORed with $\overline{FLT}$ on other devices for interrupt handling. $\overline{FLT}$ requires an external pullup resistor.
GATE0 GATE1 GATE2 GATE3 GATE4 GATE5	27 25 22 21 18 16	O	Gate drive output. GATE0 through GATE5 outputs are derived from the V_{BAT} supply. Internal clamps prevent the voltages on these nodes from exceeding the V_{GS} rating on most FETs.
GND	15	I	Ground and substrate
IN0 IN1 IN2 IN3 IN4 IN5	4 5 6 7 8 9	I	Parallel gate driver inputs. IN0 through IN5 are real-time controls for the gate predrive circuitry. They are CMOS compatible with hysteresis.
SCLK	13	I	Serial clock. SCLK clocks the shift register. Serial data is clocked into SDI and serial fault data is clocked out of SDO on the falling edge of the serial clock.
SDI	12	I	Serial data input. Output control data is clocked into the serial register through SDI. A 1 on SDI commands a particular gate output on and a 0 turns it off.
SDO	11	O	Serial data output. SDO is a 3-state output that transfers fault data to the controlling device. It also passes serial input data to the next stage for cascaded operation. SDO is taken to a high-impedance state when $\overline{CS}$ is in a high state.
V_{BAT}	28	I	Battery supply voltage input
V_{CC}	14	I	Logic supply voltage
VCOMPEN	2	I	Fault reference voltage select. VCOMPEN selects the internally generated fault reference voltage (0) or an external fault reference (1) to be used in the shorted- and open-load fault detection circuitry.
VCOMP	3	I	Fault reference voltage. VCOMP provides an external fault reference voltage for the shorted- and open-load fault detection circuitry.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
Battery supply voltage range, V_{BAT} . . . . . −0.3 V to 60 V
Input voltage range,V_I (at any input) . . . . . −0.3 V to 7 V
Output voltage range, V_O (SDO and $\overline{FLT}$) . . . . . −0.3 V to 7 V
Drain-to-source input voltage, V_{DS} . . . . . −0.3 V to 60 V
Output voltage, V_O . . . . . −0.3 V to 15 V
Operating case temperature range, T_C . . . . . −40°C to 125°C
Thermal resistance, junction to ambient, $R_{\theta JA}$ . . . . . 112°C/W
Operating virtual junction temperature range, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −40°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5	5.5	V
Battery supply voltage, V_{BAT}	8		24	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V_{CC}	V
Low-level input voltage, V_{IL}	0		0.15 V_{CC}	V
Setup time, SDI high before SCLK rising edge, t_{su} (see Figure 5)	10			ns
Hold time, SDI high after SCLK rising edge, t_h (see Figure 5)	10			ns
Case temperature, T_C	−40		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{BAT}	Supply current, V_{BAT}	All outputs off,	V_{BAT} = 12 V	300	500	700	µA
I_{CC}	Supply current, V_{CC}	All outputs off,	V_{BAT} = 5.5 V	1	2.6	4.2	mA
$V_{(turnon)}$	Turnon voltage, logic operational, V_{CC}	V_{BAT} = 5.5 V, Check output functionality		2.6	3.5	4.4	V
$V_{(ovsd)}$	Over-battery voltage shutdown	Gate disabled,	See Figure 16	32	34	36	V
$V_{hys(ov)}$	Over-battery voltage reset hysteresis			0.5	1	1.5	V
$V_{(uvsd)}$	Under-battery voltage shutdown, (TPIC46L01, L02 only)	Gate disabled,	See Figure 17	4.1	4.8	5.4	V
$V_{hys(uv)}$	Under-battery-voltage reset hysteresis, (TPIC46L01, L02 only)			100	200	300	mV
V_G	Gate drive voltage	8 V < V_{BAT} < 24 V,	I_O = 100 µA	7		13.5	V
		5.5 V < V_{BAT} < 8 V,	I_O = 100 µA	5		7	V
$I_{O(H)}$	Maximum current output for drive terminals, pullup	V_O = GND		0.5	1.2	2.5	mA
$I_{O(L)}$	Maximum current output for drive terminals, pulldown	V_O = 7 V		0.5	1.2	2.5	mA
$V_{(stb)}$	Short-to-battery/shorted-load/open-load detection voltage	VCOMPEN = L		1.1	1.25	1.4	V
$V_{hys(stb)}$	Short-to-battery hysteresis			40	100	150	mV
$V_{D(open)}$	Open-load off-state detection drain voltage threshold	VCOMPEN = L		1.1	1.25	1.4	V
$V_{hys(open)}$	Open-load hysteresis			40	100	150	mV
$I_{I(open)}$	Open-load off-state detection current			30	60	80	µA
$I_{I(PU)}$	Input pullup current ($\overline{CS}$)	V_{CC} = 5 V,	V_{IN} = 0 V		10		µA
$I_{I(PD)}$	Input pulldown current	V_{CC} = 5 V,	V_{IN} = 5 V		10		µA
$V_{I(hys)}$	Input voltage hysteresis	V_{CC} = 5 V		0.6	0.85	1.1	V
$V_{O(SH)}$	High-level serial output voltage	I_O = 1 mA		0.8 V_{CC}			V
$V_{O(SL)}$	Low-level serial output voltage	I_O = 1 mA			0.1	0.4	V
$I_{OZ(SD)}$	3-state current serial-data output	V_{CC} = 0 V to 5.5 V		-10	1	10	µA
$V_{O(CFLT)}$	Fault-interrupt output voltage	I_O = 1 mA			0.1	0.5	V
$V_{I(COMP)}$	Fault-external reference voltage, (TPIC46L01, L02 only)	VCOMPEN = H		0.25		3	V
$V_{I(COMP)}$	Fault-external reference voltage, (TPIC46L03 only)	VCOMPEN = H		1		3	V
V_C	Output clamp voltage, (TPIC46L01, L02 only)	dc < 1%,	t_W = 100 µs	47	55	63	V
V_C	Output clamp voltage, (TPIC46L03 only)	dc < 1%,	t_W = 100 µs	47		60	V

switching characteristics, V_{CC} = 5 V, V_{BAT} = 12 V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(STBFM)}$	Mask time, short-to-battery/shorted-load/open-load fault	See Figures 14 and 15			60		µs
$t_{(STBDG)}$	Deglitch time, short-to-battery/shorted-load	See Figure 14			8		µs
t_{PLH}	Propagation turnon delay time, $\overline{CS}$ or IN0-IN5 to GATE0–GATE5	$C_{(gate)}$ = 400 pF,	See Figure 1		4		µs
t_{PHL}	Propagation turnoff delay time, $\overline{CS}$ or IN0-IN5 to GATE0–GATE5	$C_{(gate)}$ = 400 pF,	See Figure 2		3.5		µs
$t_{r(1)}$	Rise time, GATE0–GATE5	$C_{(gate)}$ = 400 pF,	See Figure 3		3.5		µs
$t_{f(1)}$	Fall time, GATE0–GATE5	$C_{(gate)}$ = 400 pF,	See Figure 4		3		µs
$f_{(SCLK)}$	Serial clock frequency					10	MHz
$t_{rf(SB)}$	Refresh time, short-to-battery	TPIC46L02 only,	See Figure 14		10		ms
t_w	Short-to-battery refresh pulse width	TPIC46L02 only,	See Figure 14		68		µs
$t_{su(1)}$	Setup time, $\overline{CS}\downarrow$ to ↑SCLK	See Figure 5			10		ns
$t_{pd(1)}$	Propagation delay time, $\overline{CS}\downarrow$ to SDI valid	R_L = 10 kΩ, See Figure 6	C_L = 200 pF,		40		ns
$t_{pd(2)}$	Propagation delay time, SCLK↓ to SDI valid	See Figure 6			20		ns
$t_{pd(3)}$	Propagation delay time, $\overline{CS}\uparrow$ to SDO 3-state	R_L = 10 kΩ, See Figure 7	C_L = 50 pF,		2		µs
$t_{r(2)}$	Rise time, SDO 3-state to SDO valid	R_L = 10 kΩ to GND, C_L = 200 pF,	Over-battery fault, See Figure 8		30		ns
$t_{f(2)}$	Fall time, SDO 3-state to SDO valid	R_L = 10 kΩ to V_{CC}, C_L = 200 pF,	No faults, See Figure 9		20		ns
$t_{r(3)}$	Rise time, $\overline{FLT}$	R_L = 10 kΩ, See Figure 10	C_L = 50 pF,		1.2		µs
$t_{f(3)}$	Fall time, $\overline{FLT}$	R_L = 10 kΩ, See Figure 11	C_L = 50 pF,		15		ns

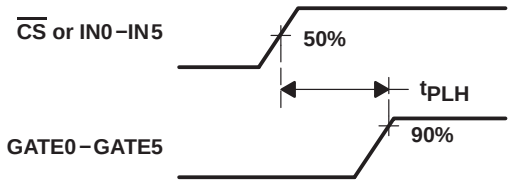


Figure 1

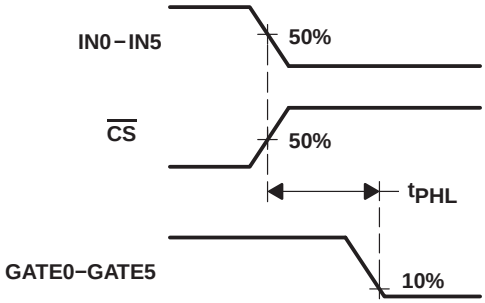


Figure 2

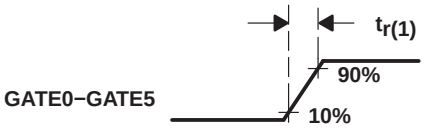


Figure 3

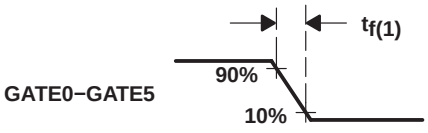


Figure 4

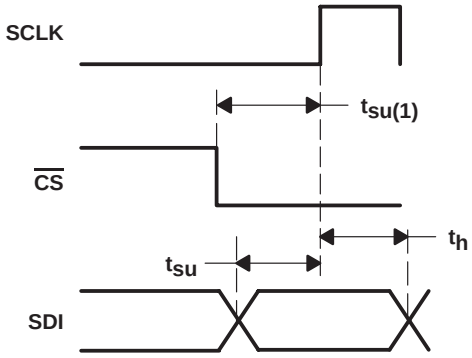


Figure 5

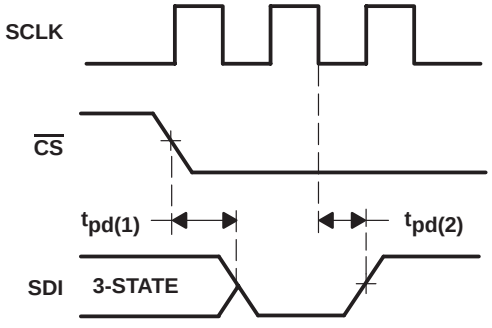


Figure 6

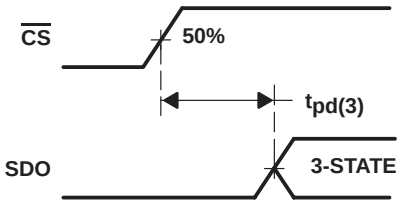


Figure 7

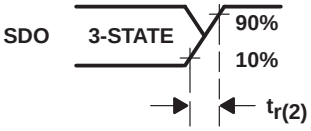


Figure 8

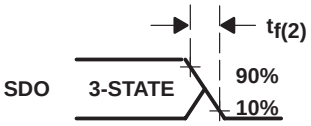


Figure 9

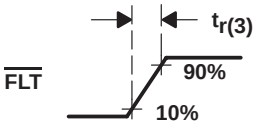


Figure 10

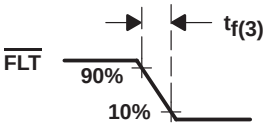


Figure 11

PRINCIPLES OF OPERATION

serial data operation

The TPIC46L01, TPIC46L02, and TPIC46L03 offer serial input interfaces to the microcontroller to transfer control data to the predriver and output fault data back to the controller. The serial input interface consists of:

- SCLK – Serial clock
- $\overline{CS}$ – Chip select
- SDI – Serial data input
- SDO – Serial data outpu

Serial data is shifted into the least significant bit (LSB) of the SDI shift register on the rising edge of the first SCLK after $\overline{CS}$ has transitioned from 1 to 0. Eight clock cycles are required to shift the first bit from the LSB to the most significant bit (MSB) of the shift register. Less than eight clock cycles result in fault data being latched into the output control buffer. The first two bits are unused and the last six bits are the output control data. A low-to-high transition on $\overline{CS}$ latches the contents of the serial shift register into the output control register. A 0 input to SDI turns the corresponding parallel output off and a 1 turns the output on (see Figure 12).

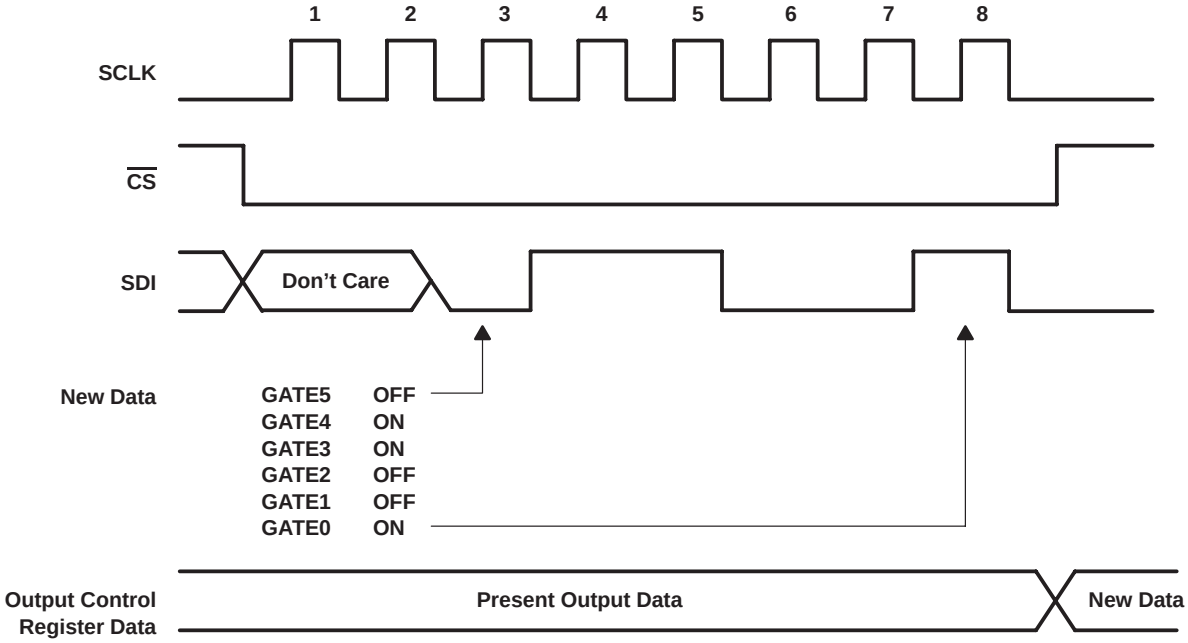
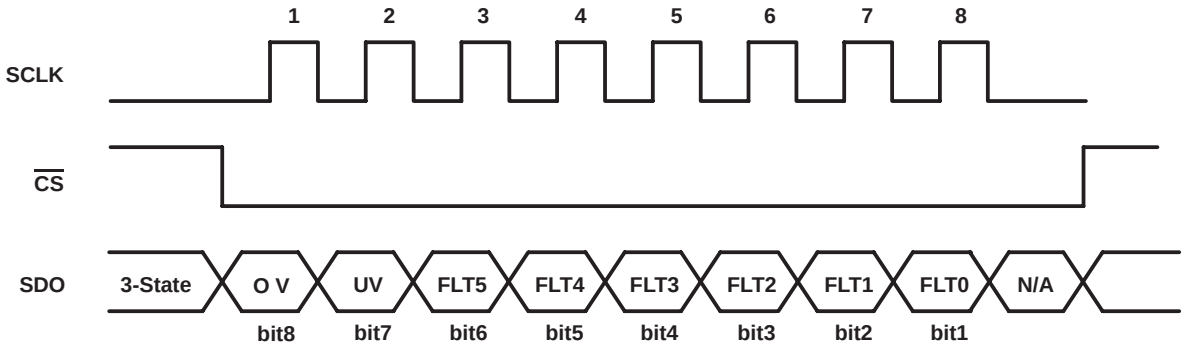


Figure 12

PRINCIPLES OF OPERATION

serial data operation (continued)

Data is shifted out of SDO on the falling edge of SCLK. The MSB of fault data is available when $\overline{CS}$ is transitioned low. The remaining 7 bits of fault data are shifted out on the following seven clock cycles. Fault data is latched into the serial register when $\overline{CS}$ is transitioned low. Fault data must be present on the high-to-low transition of $\overline{CS}$ to be captured by the device. The $\overline{CS}$ input must be transitioned to a high state after the last bit of serial data has been clocked into the device. $\overline{CS}$ puts SDO in a high-impedance state, inhibits SDI, latches the 6 bits of serial data into the output control register, and clears and reenables the serial fault registers (see Figure 13). When a shorted-load condition occurs with the TPIC46L01 or TPIC46L03, the controller must disable and reenable the channel to clear the fault register and fault flag. The TPIC46L02 automatically retries the output and $\overline{FLT}$ clears after the fault condition has been corrected.



OV	Over-Battery-Voltage Fault Bit
UV	Under-Battery-Voltage Fault Bit
FLT5	Shorted- or Open-Load Fault on Channel 5
FLT4	Shorted- or Open-Load Fault on Channel 4
FLT3	Shorted- or Open-Load Fault on Channel 3
FLT2	Shorted- or Open-Load Fault on Channel 2
FLT1	Shorted- or Open-Load Fault on Channel 1
FLT0	Shorted- or Open-Load Fault on Channel 0
N/A	Unknown Data

Figure 13

parallel input data operation

In addition to the serial input interface, the TPIC46L01 and TPIC46L02 also provides a parallel input interface to the microcontroller. The output turns on if either the parallel or the serial interface commands it to turn on. The parallel data pins are real-time control inputs for the output drivers. SCLK and $\overline{CS}$ are not required to transfer parallel input data to the output buffer. Fault data must be read over the serial data bus as described in the serial data operation section of this data sheet. The parallel input must be transitioned low and then high to clear and reenable a gate output that has been disabled due to a shorted-load fault condition.

PRINCIPLES OF OPERATION

chipset performance under fault conditions

The TPIC46L01, TPIC46L02, TPIC46L03, and power FET array's are designed for normal operation over a battery-voltage range of 8 V to 24 V with load fault detection from 4.8 V to 34 V. The TPIC46L01, TPIC46L02, and TPIC46L03 offer onboard fault detection to handle a variety of faults that may occur within a system. The circuits primary function is to prevent damage to the load and the power FETs in the event that a fault occurs. Unused DRAIN0−DRAIN5 inputs must be connected to V_{BAT} through a pullup resistor to prevent false reporting of open-load fault conditions. This circuitry detects the fault, shuts off the output to the FET, and reports the fault to the microcontroller. The primary faults under consideration are:

1. Shorted load
2. Open load
3. Over-battery voltage shutdown
4. Under-battery voltage shutdown

NOTE:

On the TPIC46L01 and TPIC46L02, an undervoltage fault may be detected when V_{CC} and V_{BAT} are applied to the device. The controller should initialize the fault register after power up to clear any false fault reports.

shorted-load fault condition

The TPIC46L01 and TPIC46L02 monitor the drain voltage of each channel to detect shorted-load conditions. The onboard deglitch timer starts running when the gate output to the power FET transitions from the off state to the on state. The timer provides a 60-µs deglitch time, $t_{(STBFM)}$, to allow the drain voltage to stabilize after the power FET has been turned on. The deglitch time is only enabled for the first 60 µs after the FET has been turned on. After the deglitch delay time, the drain voltage is checked to verify that it is less than the fault reference voltage. When it is greater than the reference voltage for at least the short-to-battery deglitch time, $t_{(STBDG)}$, then $\overline{FLT}$ flags the microcontroller that a fault condition exists and the gate output is automatically shut off (TPIC46L01 and TPIC46L03) until the error condition has been corrected.

An overheating condition on the FET occurs when the controller continually tries to reenable the output under shorted-load fault conditions. When a shorted-load fault is detected while using the TPIC46L02, the gate output is transitioned into a low-duty cycle PWM signal to protect the FET from overheating. The PWM rate is defined as $t_{(SB)}$ and the pulse with is defined as t_W. It remains in this low-duty cycle pulse state until the fault has been corrected or until the controller disables the gate output.

The microcontroller can read the serial port on the predriver to isolate which channel reported the fault condition. Fault bits 0−5 distinguish faults for each of the output channels. When a shorted-load condition occurs with the TPIC46L01, the controller must disable and reenable the channel to clear the fault register and fault flag. The TPIC46L02 automatically retries the output and the fault clears after the fault condition has been corrected. Figure 14 illustrates operation after a gate output has been turned on. The gate to the power FET is turned on and the deglitch timer starts running. Under normal operation T1 turns on and the drain operates below the reference point set at U1. The output of U1 is low and a fault condition is not flagged.

PRINCIPLES OF OPERATION

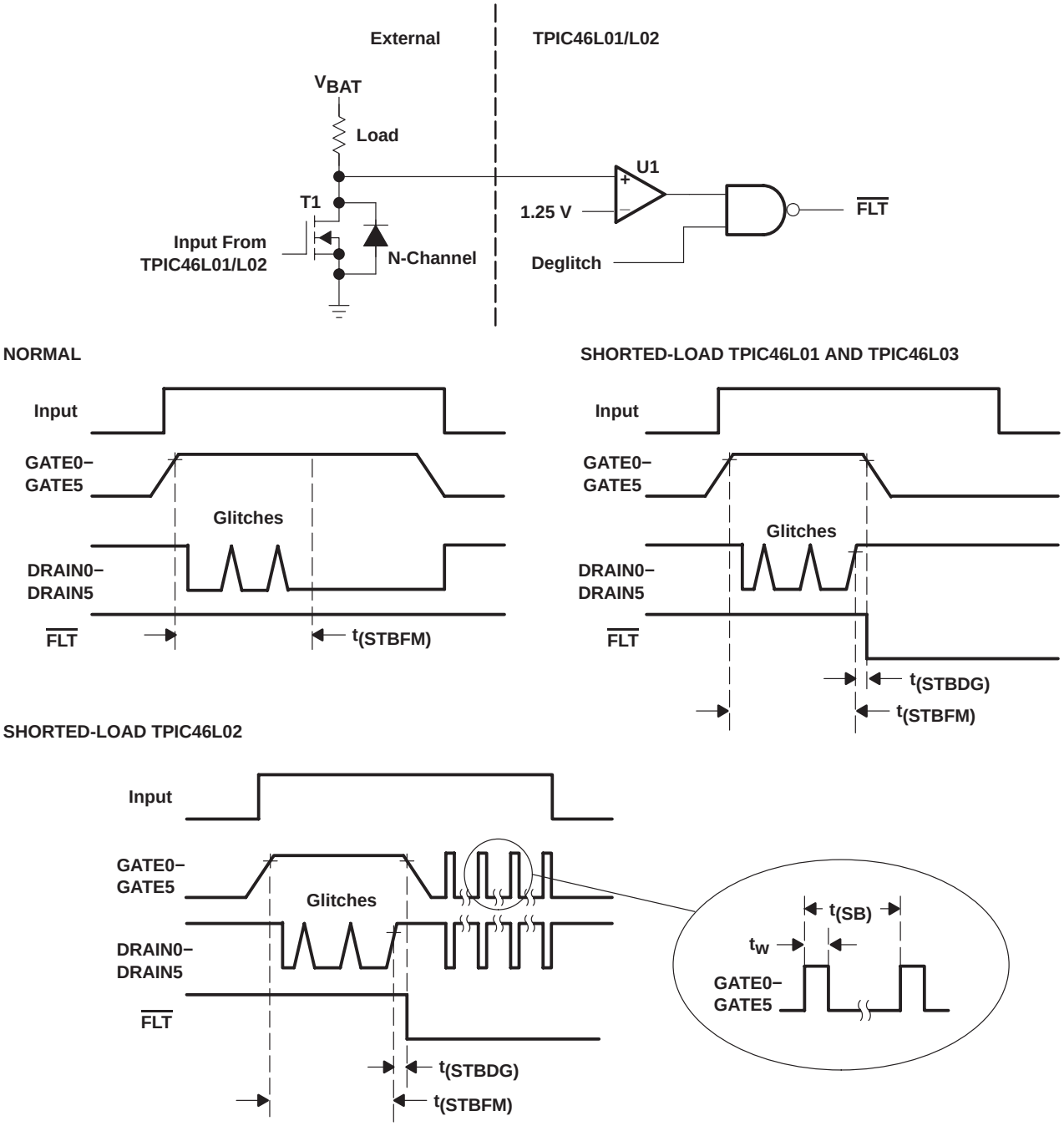


Figure 14

PRINCIPLES OF OPERATION

open load

The TPIC46L01, TPIC46L02, and TPIC46L03 monitor the drain of each power FET for open-circuit conditions that may exist. The 60-µA current source is provided to monitor open-load fault conditions. Open-load faults are detected when the power FET is turned off. When load impedance is open or substantially high, then the 60-µA current source has adequate drive to pull the drain of T1 below the fault reference threshold on the detection circuit. Unused DRAIN0−DRAIN5 inputs must be connected to V_{BAT} through a pullup resistor to prevent false reporting of open-load fault conditions. The onboard deglitch timer starts running when the TPIC46L01, TPIC46L02, and TPIC46L03 gate output to the power FET transitions to the off state. The timer provides a 60-µs deglitch time, $t_{(STBFM)}$, to allow the drain voltage to stabilize after the power FET has been turned off. The deglitch time is only enabled for the first 60 µs after the FET has been turned off. After the deglitch delay time, the drain is checked to verify that it is greater than the fault reference voltage. When it is less than the reference voltage, a fault is flagged to the microcontroller through $\overline{FLT}$ that an open-load fault condition exists. The microcontroller can then read the serial port on the TPIC46L01, TPIC46L02, and TPIC46L03 to isolate which channel reported the fault condition. Fault bits 0−5 distinguish faults for each of the output channels. Figure 15 illustrates the operation of the open-load detection circuit. This feature provides useful information to the microcontroller to isolate system failures and warn the operator that a problem exists. Examples of such applications would be warning that a light bulb filament may be open, solenoid coils may be open, etc.

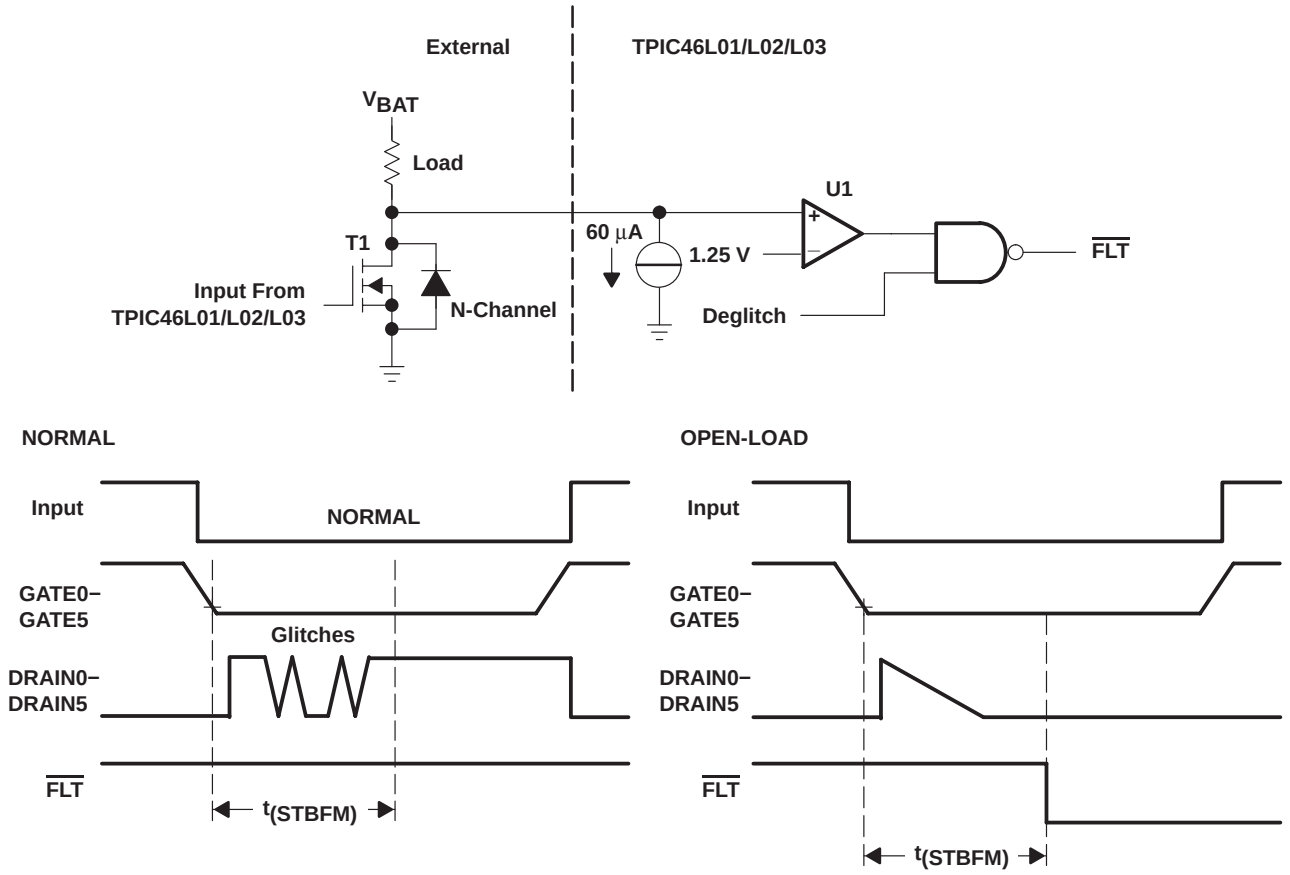


Figure 15

PRINCIPLES OF OPERATION

over-battery-voltage shutdown

The TPIC46L01, TPIC46L02, and TPIC46L03 monitor the battery voltage to prevent the power FETs from being turned on in the event that the battery voltage is too high. This condition may occur due to voltage transients resulting from a loose battery connection. The TPIC46L01/L02/L03 turns the power FETs off when the battery voltage is above 34 V, to prevent possible damage to the load and the FETs. The gate output goes back to normal operation after the overvoltage condition has been corrected. An over-battery voltage fault is flagged to the controller through the fault flag. Bit 8 of the serial-data fault word is set whenever an over-battery voltage condition is present. When an overvoltage condition occurs the device reports the battery fault, but disables fault reporting for open and shorted-load conditions. Fault reporting for open and shorted-load conditions reenables after the battery-fault condition has been corrected. When the fault condition is removed before the $\overline{CS}$ signal transitions low, then the fault condition is not captured in the serial fault register. $\overline{FLT}$ resets on the high-to-low transition of $\overline{CS}$ provided no other faults are present in the device. Figure 16 illustrates the operation of the over-battery voltage detection circuit.

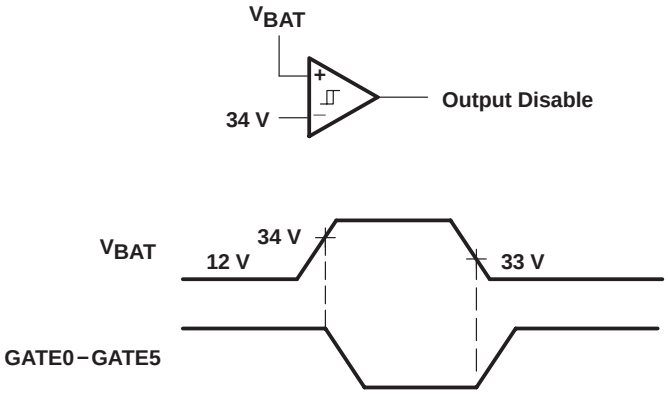


Figure 16

PRINCIPLES OF OPERATION

under-battery-voltage shutdown (TPIC46L01, and TPIC46L02 only)

The TPIC46L01 and TPIC46L02 monitor the battery voltage to prevent the power FETs from being turned on in the event that the battery voltage is too low. When the battery voltage is below 4.8 V, then GATE0−GATE5 outputs may not provide sufficient gate voltage to the power FETs to minimize the on-resistance that could result in a thermal stress on the FET. The output resumes normal operation after the under-voltage condition has been corrected. An under-battery voltage fault flags the controller through the fault flag. Bit 7 of the serial-data fault word is set whenever an under-battery voltage condition is present. When an under-battery voltage condition occurs the device reports the battery fault, but disables fault reporting for open- and shorted-load conditions. When the fault condition is removed before $\overline{CS}$ signal transitions low, the fault condition is not captured in the serial fault register. $\overline{FLT}$ resets on the high-to-low transition of $\overline{CS}$ provided no other faults are present in the device. Figure 17 illustrates the operation of the under-battery voltage detection circuit.

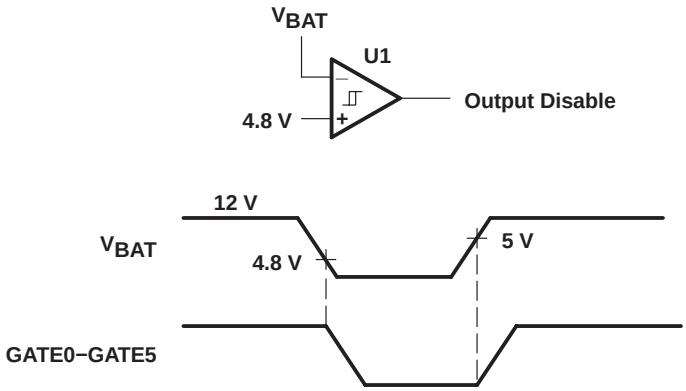


Figure 17

PRINCIPLES OF OPERATION

Inductive voltage transients

A typical application for the predriver/power FET circuit is to switch inductive loads. When an inductive load is switched off, a large voltage spike can occur. These spikes can exceed the maximum V_{DS} rating for the external FET and damage the device when proper protection is not in place. The FET can be protected from these transients through a variety of methods using external components. The TPIC46L01 and TPIC46L02 offer that protection in the form of a Zener diode stack connected between the drain input and GATE output (see Figure 18). Zener diode (Z1) turns the FET on to dissipate the transient energy. GATE diode (Z2) is provided to prevent the gate voltage from exceeding 13 V during normal operation and transient protection.

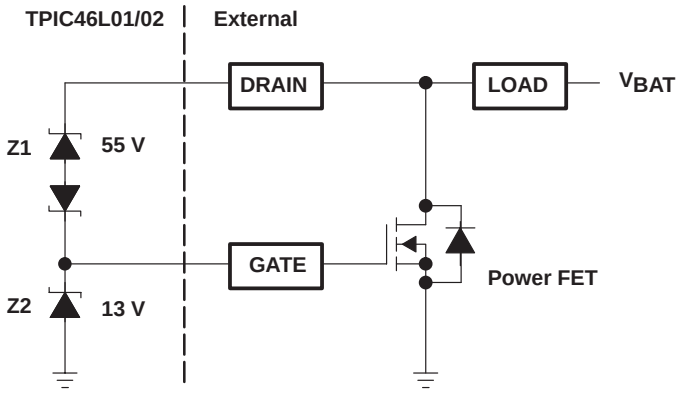


Figure 18

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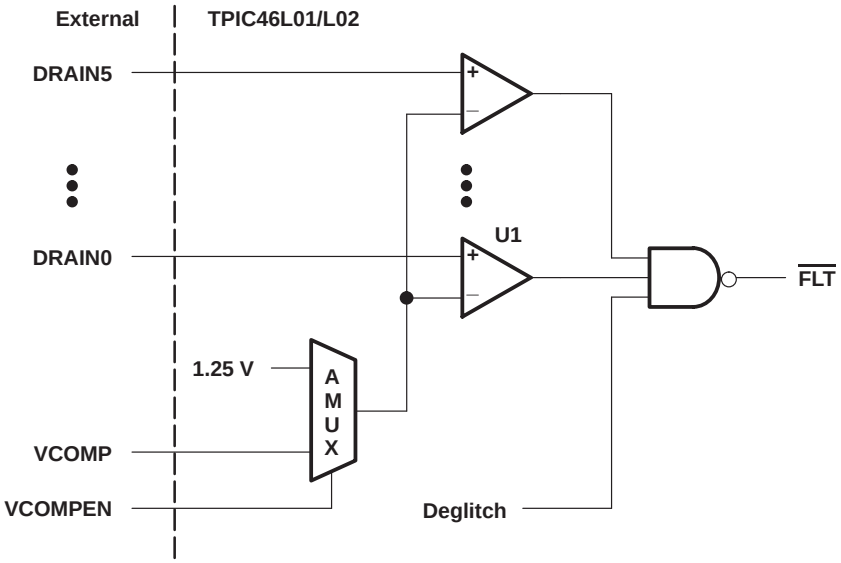
PRINCIPLES OF OPERATION

external fault reference input

The TPIC46L01, TPIC46L02, and TPIC46L03 compare each channel drain voltage to a fault reference to detect shorted-load and open-load conditions. The user has the option of using the internally generated 1.25-V fault reference or providing an external reference voltage through VCOMP. The internal reference voltage is selected by connecting VCOMPEN to GND and VCOMP is selected by connecting VCOMPEN to V_{CC} (see Figure 19). Proper layout techniques should be used in the grounding network for the VCOMP circuit and the TPIC46L01/L02/L03. The ground for the predriver and the VCOMP network should be connected to a Kelvin ground if available; otherwise, a single point connection should be maintained to the power ground of the FET array. Improper grounding techniques may result in inaccuracies in detecting faults.



	VCOMPEN
1.25 V	0
VCOMP	1

Figure 19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC46L01DB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC46L01	Samples
TPIC46L01DBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TPIC46L01	Samples
TPIC46L01DBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TPIC46L01	Samples
TPIC46L01DBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TPIC46L01	Samples
TPIC46L02DB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC46L02	Samples
TPIC46L02DBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TPIC46L02	Samples
TPIC46L02DBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC46L02	Samples
TPIC46L02DBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC46L02	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

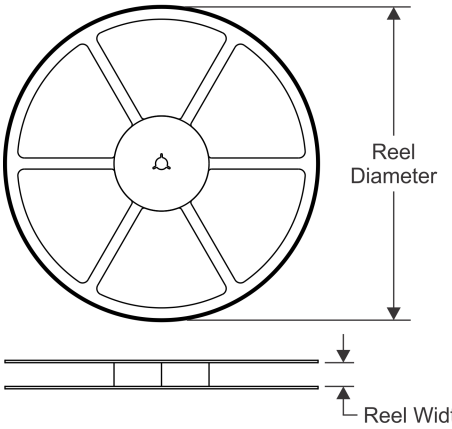
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

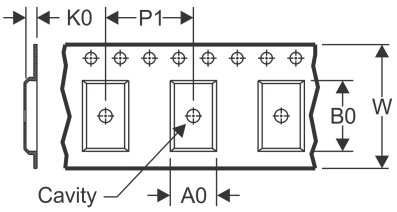
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

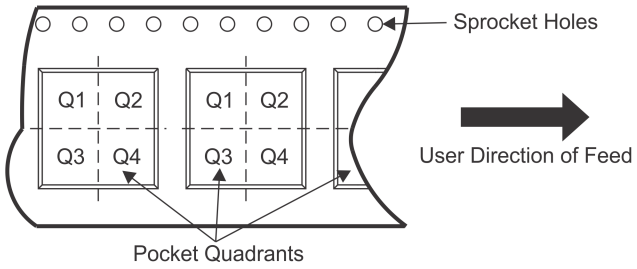


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

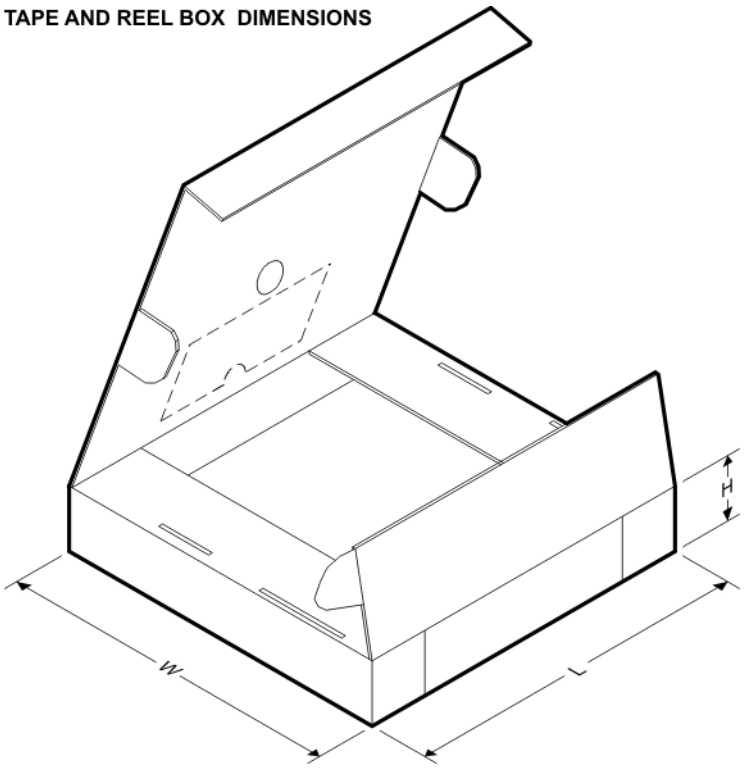
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC46L01DBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
TPIC46L01DBRG4	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TPIC46L02DBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TPIC46L02DBRG4	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

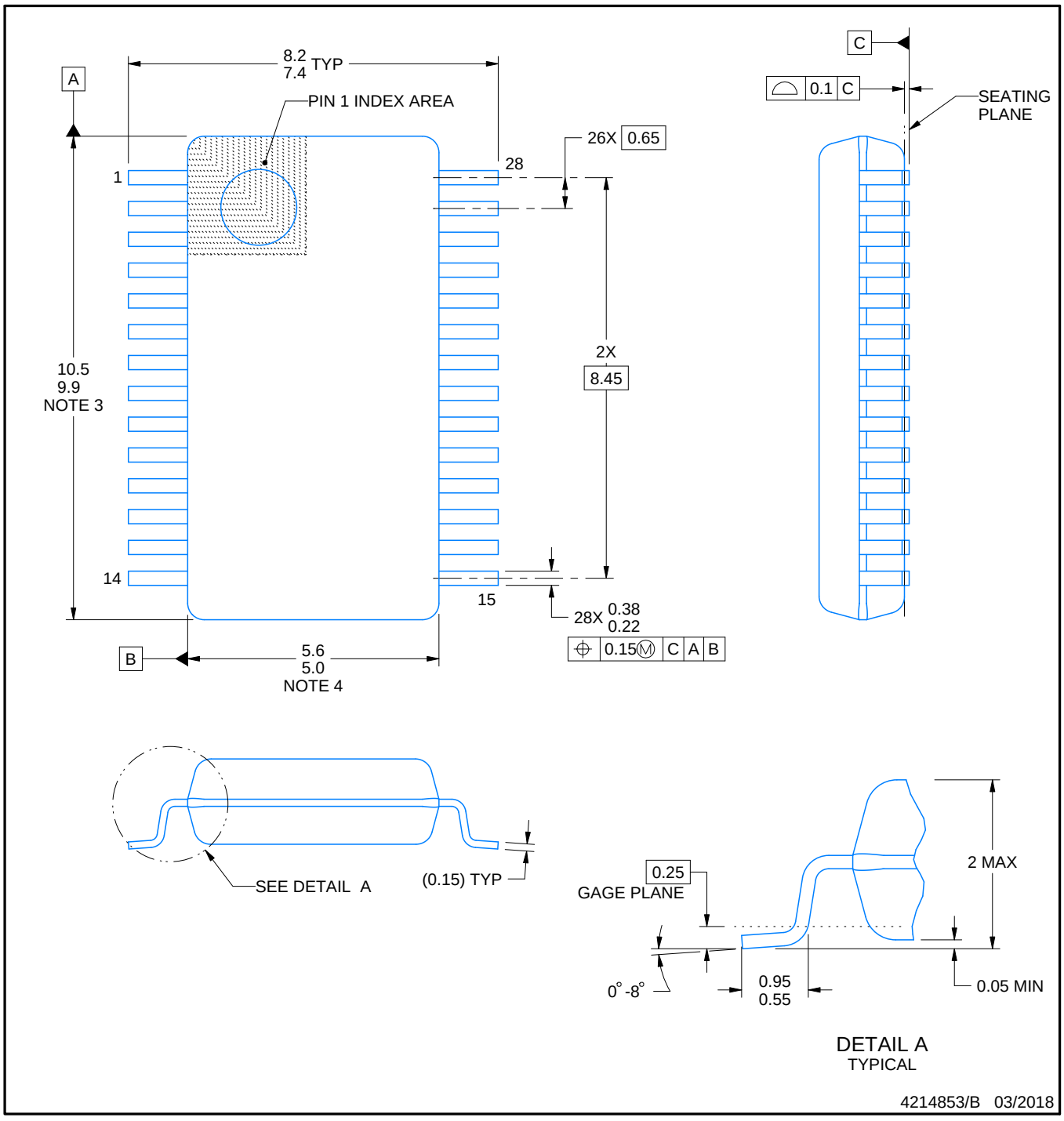
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC46L01DBR	SSOP	DB	28	2000	367.0	367.0	38.0
TPIC46L01DBRG4	SSOP	DB	28	2000	367.0	367.0	38.0
TPIC46L02DBR	SSOP	DB	28	2000	367.0	367.0	38.0
TPIC46L02DBRG4	SSOP	DB	28	2000	367.0	367.0	38.0

PACKAGE OUTLINE

DB0028A

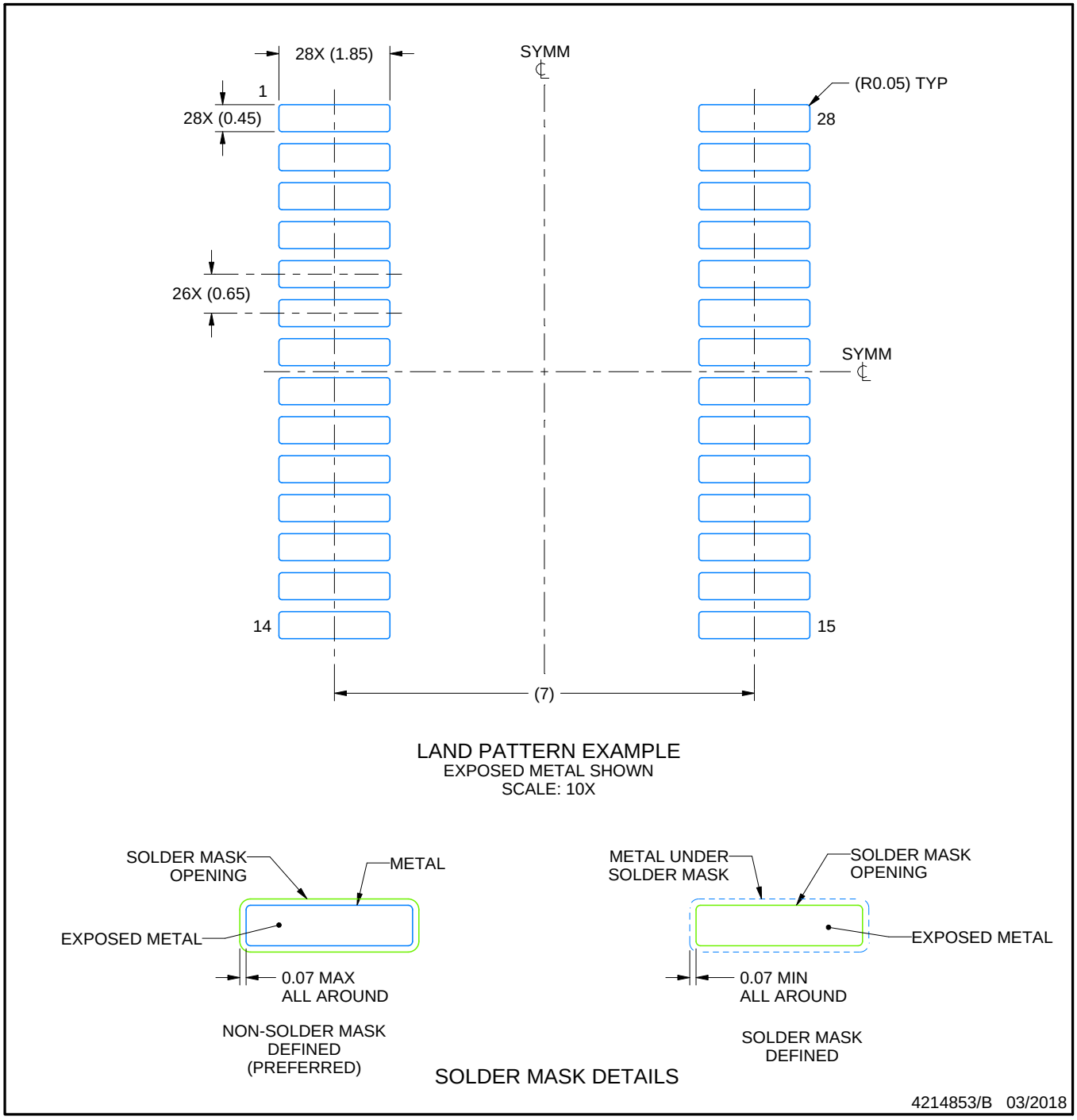
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



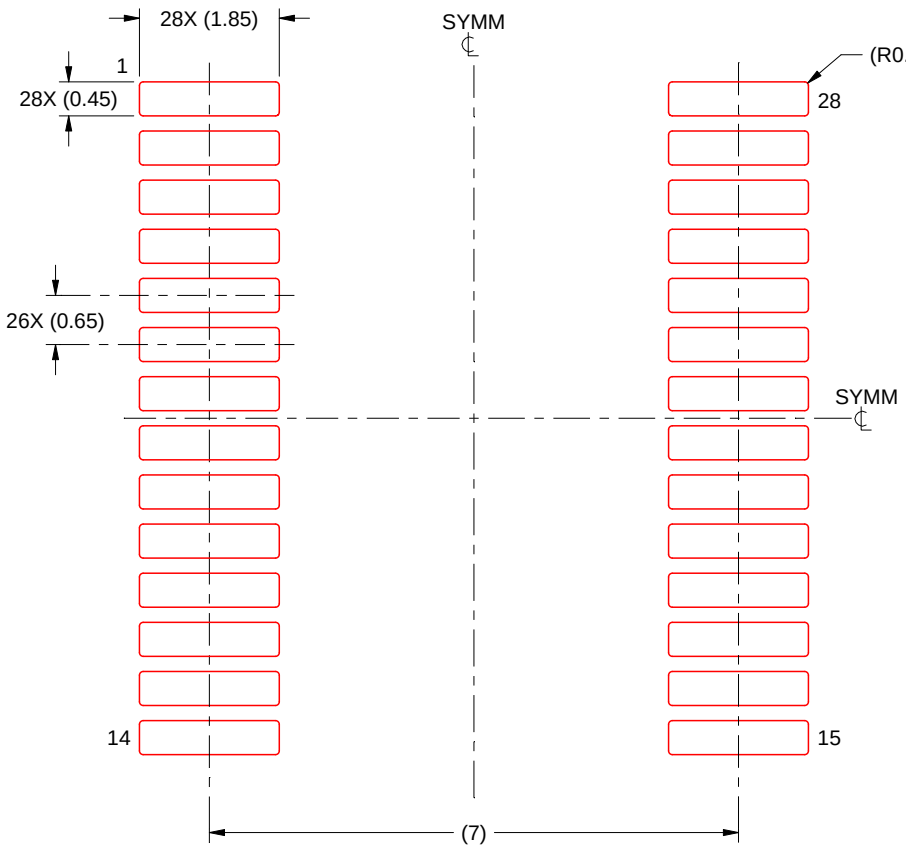
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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