THE DATASHEET OF

TMDS461PZTR

1080p – Deep Color 4-to-1 HDMI/DVI Switch with Adaptive Equalization

FEATURES

- 4:1 Switch Supporting DVI Above 1920 × 1200 and HDMI HDTV Resolutions up to 1080p With 16-bit Color Depth
- Designed for Signaling Rates up to 3 Gbps
- HDMI1.3a Spec Compliant
- Adaptive Equalization to Support up to 20-m HDMI Cable
- TMDS Input Clock-Detect Circuit
- DDC Repeater Function
- <2 mW Low-Power Mode
- Local I^2C or GPIO Configurable
- Enhanced ESD. HBM: 10 kV on All Input TMDS, DDC I^2C pins
- 3.3-Volt Power Supply
- Temperature Range: 0°C to 70°C
- Automatic Port Select Feature
- Robust TMDS Receive Stage That Can Work With Non-Compliant Input Common-Mode HDMI Signals

APPLICATIONS

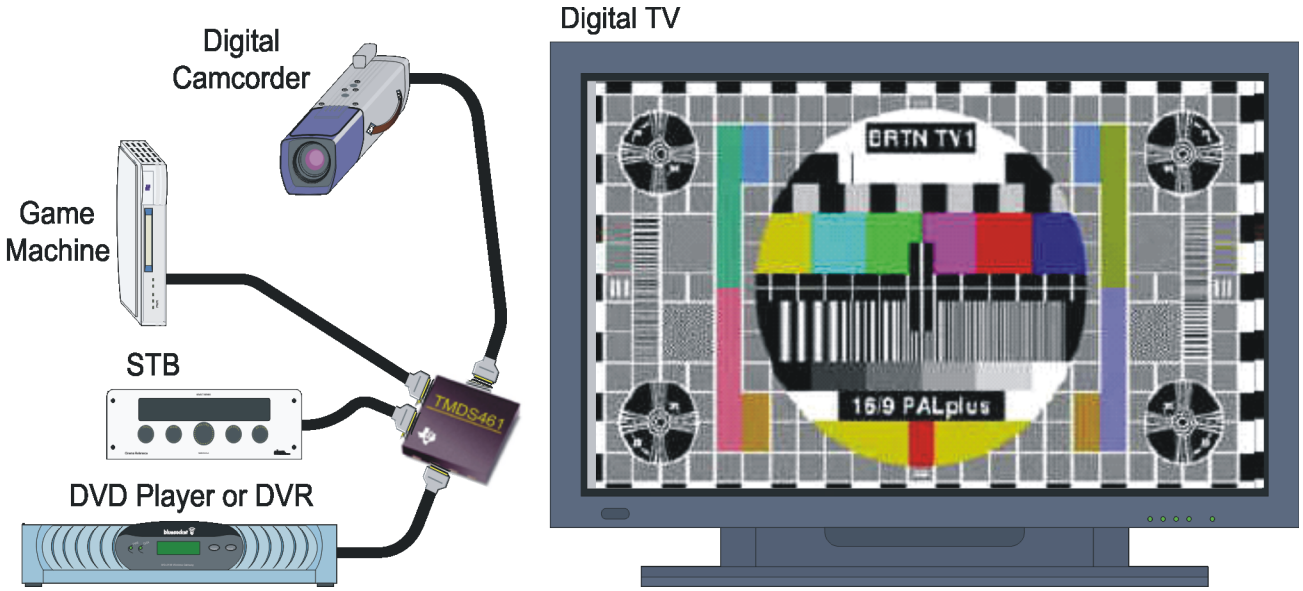
- High-Definition Digital TV
  - LCD
  - Plasma
  - DLP®

DESCRIPTION

The TMDS461 is a 4-port digital video interface (DVI) or high-definition multimedia interface (HDMI) switch that allows up to four DVI or HDMI ports to be switched to a single display terminal. Four TMDS channels, one hot-plug detector, and a digital display control (DDC) interface are supported on each port. Each TMDS channel supports signaling rates up to 3 Gbps to allow 1080p resolution in 16-bit color depth.

The TMDS461 provides an analog adaptive equalizer for different ranges of cable lengths. The equalizer automatically compensates for intersymbol interference [ISI] loss of an HDMI/DVI cable for up to 20 dB at 3 Gbps (see Figure 19).

TYPICAL APPLICATION



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DESCRIPTION (CONTINUED)

When any input port is selected, the integrated terminations (50-Ω termination resistors pulled up to VCC) are switched on for the TMDS clock channel, the TMDS clock-detection circuit is enabled, and the DDC repeater is enabled. After a valid TMDS clock is detected, the integrated termination resistors for the data lines are enabled, and the output TMDS lines are enabled. When an input port is not selected, the integrated terminations are switched off, the TMDS receivers are disabled, and the DDC repeater is disabled. Clock-detection circuitry provides an automatic power-management feature, because if no valid TMDS clock is detected, the terminations on the input TMDS data lines are disconnected and the TMDS outputs are placed in a high-impedance state.

The TMDS461 is designed to be controlled via a local I^2C interface or GPIO interface based on the status of the I2C_SEL pin. The local I^2C interface in TMDS461 is a slave-only I^2C interface. (See the I2C INTERFACE NOTES section.)

I^2C Mode: When the I2C_SEL pin is set high, the device is in I^2C mode. Refer to Table 7 to Table 13 for I^2C register description. With local I^2C, the interface port status can be read and the advanced configurations of the device such as TMDS output edge rate control, DDC I^2C buffer output-voltage-select (OVS) settings (See the DDC I2C Function Description for detailed description on DDC I^2C buffer description and OVS description), device power management, TMDS clock-detect feature, **Automatic Port Selection** and TMDS input-port selection can be set. In I^2C mode when any system level change such as change in 5V_PWR on the source side, a change in the selected port, or a change in the selected port's valid clock detect is detected, TMDS461 can issue an Interrupt Request via IRQ pin (refer IRQ Section). A micro-controller connected to TMDS461 can read I^2C register address 0X01, (See Table 7) to obtain the current status of 5V_PWR, the selected port, and clock-detect status. Once the micro-controller has read I^2C register 0x01, the IRQ pin returns to low.

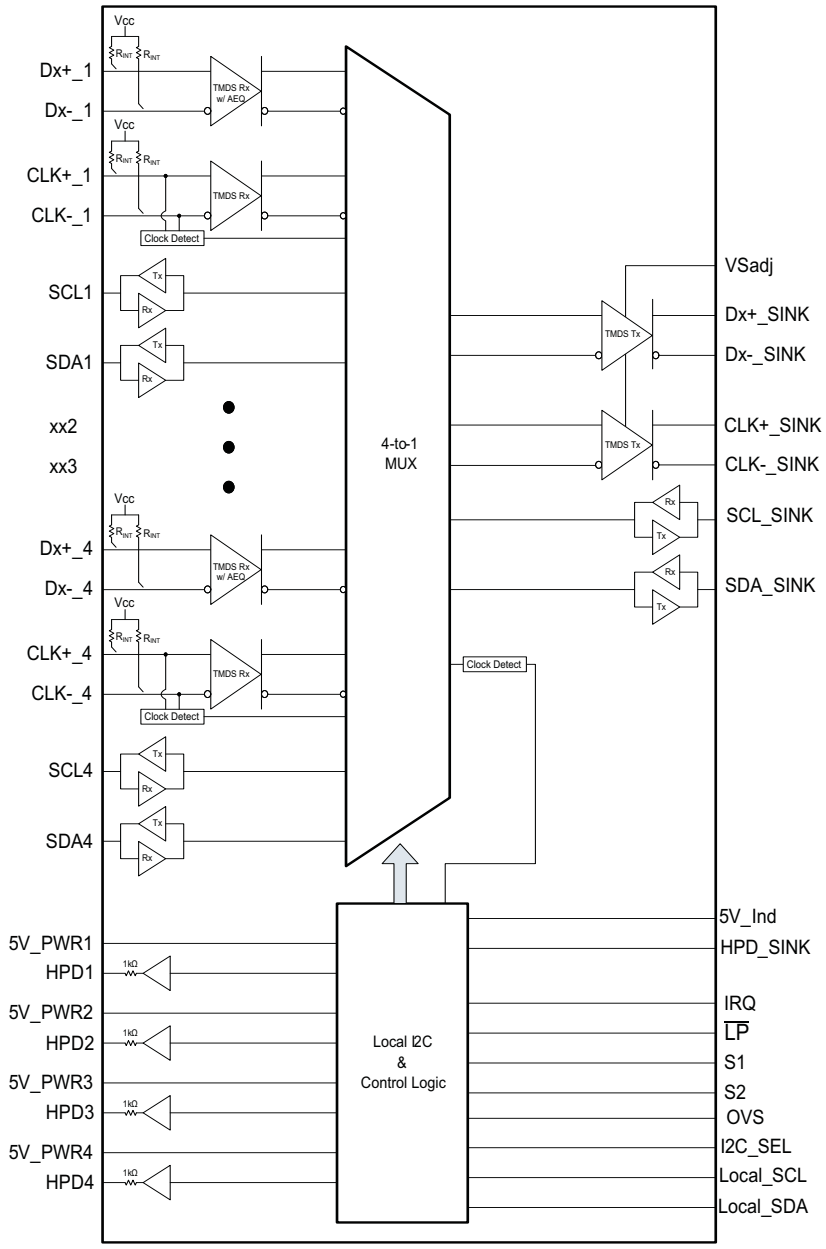
GPIO mode: When the I2C_SEL pin is set low, the device is in GPIO control mode. The port selection is controlled with source selectors, S1 and S2. The power-saving mode is controlled through the LP pin. In GPIO mode, the default TMDS output edge rate that is the fastest setting of rise and fall time is set. The DDC I^2C buffer OVS setting can be changed through OVS GPIO pin, see Table 2. In GPIO mode, IRQ pin reflects the status of the selected port's clock detect. If a valid clock is detected by the clock detect circuit, IRQ goes high. If no valid clock is detected, IRQ is driven low.

Following are some of the key features (advantages) that TMDS461 provides to the overall sink-side system (HDTV).

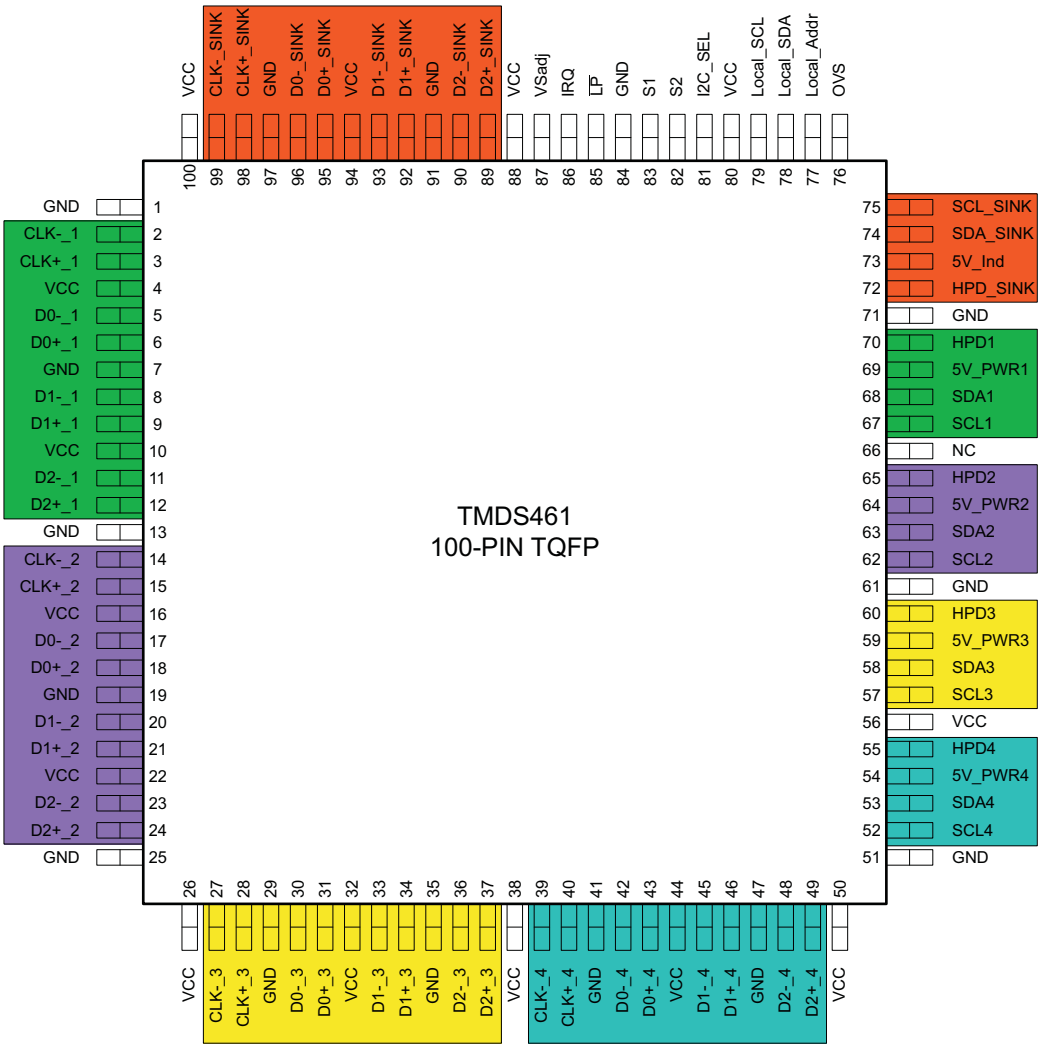
- 4:1 switch that supports TMDS data rates up to 3 Gbps on all four input ports.
- ESD: Built-in support for high ESD protection (up to 10 kV on the TMDS and DDC I^2C pins). The HDMI source-side pins on the TMDS461 are connected via the HDMI/DVI exterior connectors and cable to the HDMI/DVI sources (e.g., DVD player). In TV applications, it can be expected that the source side may be subjected to higher ESD stresses compared to the sink side that is connected internally to the HDMI receiver.
- Adaptive equalization: The built-in analog adaptive equalization support compensates for intersymbol interference [ISI] loss of up to 20 dB, which represents a typical 20-m HDMI/DVI cable at 3 Gbps. Analog Adaptive equalization adjusts the equalization gain **automatically**, based on the cable length and the incoming TMDS data rate.
- TMDS clock-detect circuitry: This feature provides an automatic power-management feature and also ensures that the TMDS output port is turned on only if there is a valid TMDS input signal. TMDS clock-detect feature can be by-passed in I^2C Mode, (See Table 9). It is recommended to enable TMDS clock-detect circuitry during normal operation. However, for HDMI compliance testing (TMDS Termination Voltage Test), the clock detect feature should be disabled by using the I^2C mode control. To comply with the TMDS Termination Voltage Test in the GPIO mode (default TMDS clock-detect circuitry enabled), a valid TMDS clock will need to be provided. With the clock present, the internal terminations are present providing the correct termination voltage.
- DDC I^2C buffer: This feature provides isolation on the source side and sink side DDC I^2C capacitance, thus helping the sink system to pass system-level compliance.
- Robust TMDS receive stage: This feature ensures that the TMDS461 can work with TMDS input signals which have common-mode voltage levels that can be either compliant or non-compliant with HDMI/DVI specifications
- VSadj: This feature adjusts the TMDS output swing and can help the sink system to tune the output TMDS swing of the TMDS461 (if needed) based on the system requirements.
- GPIO or local I^2C interface to control the device features

- TMDS output edge-rate control: This feature adjusts the TMDS461 TMDS output rise and fall times. There are four settings that can be chosen. The default setting is the fastest rise and fall time; the other three settings are slower. Slower edge transitions can potentially help the sink system (HDTV) in passing regulatory EMI compliance.
- Automatic Port Select Feature available in I^2C mode
- 5V_PWR detect for each port connected, Hot Plug Detect (HPD) of non selected port follows 5V_PWR, whereas HPD of selected port follows HPD_SINK.

FUNCTIONAL BLOCK DIAGRAM



PZT PACKAGE



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
SIGNAL	NO.		
TMDS INPUT PINS			
CLK+_1 CLK-_1	3 2	I	Port-1 TMDS differential clock
D[0:2]+_1 D[0:2]-_1	6, 9, 12 5, 8, 11	I	Port-1 TMDS differential data inputs
CLK+_2 CLK-_2	15 14	I	Port-2 TMDS differential clock
D[0:2]+_2 D[0:2]-_2	18, 21, 24, 17, 20, 23	I	Port-2 TMDS differential data inputs
CLK+_3 CLK-_3	28 27	I	Port-3 TMDS differential clock
D[0:2]+_3 D[0:2]-_3	31, 34, 37 30, 33, 36	I	Port-3 TMDS differential data inputs
CLK+_4 CLK-_4	40 39	I	Port-4 TMDS differential clock

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
SIGNAL	NO.		
D[0:2]+_4 D[0:2]-_4	43, 46, 49 42, 45, 48	I	Port-4 TMDS differential data inputs
TMDS OUTPUT PINS			
CLK+_SINK CLK-_SINK	98 99	O	TMDS sink differential clock
D[0:2]+_SINK D[0:2]-_SINK	95, 92, 89 96, 93, 90	O	TMDS sink differential data outputs
HOT-PLUG-DETECT STATUS PINS			
HPD[1:4]	70, 65, 60, 55	O	Source port hot-plug-detect output
HPD_SINK	72	I	Sink hot plug detect input
DDC PINS			
SCL[1:4]	67, 62, 57, 52	I/O	TMDS port bidirectional DDC clock
SDA[1:4]	68, 63, 58, 53	I/O	TMDS port bidirectional DDC data
SCL_SINK	75	I/O	TMDS sink side bidirectional DDC clock
SDA_SINK	74	I/O	TMDS sink side bidirectional DDC data
STATUS PINS			
IRQ	86	O	Interrupt Request
5V_PWR[1:4]	69, 64, 59, 54	I	Source Port 5V Signal Input
5V_Ind	73	O	Selected Port 5V Power Indicator
CONTROL PINS			
$\overline{LP}$	85	I	Low-power select bar
S[1:2]	83,82	I	Source Selection GPIO
I2C_SEL	81	I	Local I^2C control select
Local_SCL	79	I	Local I^2C clock
Local_SDA	78	I/O	Local I^2C data
Local_Addr	77	I	Local I^2C address
VSadj	87	I	TMDS compliant voltage swing control
OVS	76	I	DDC offset selector
NC	66		No Connect
SUPPLY AND GROUND PINS			
VCC	4, 10, 16, 22, 26, 32, 38, 44, 50, 56, 80, 88, 94, 100		3.3 V supply
GND	1, 7, 13, 19, 25, 29, 35, 41, 47, 51, 61, 71, 84, 91, 97		Ground

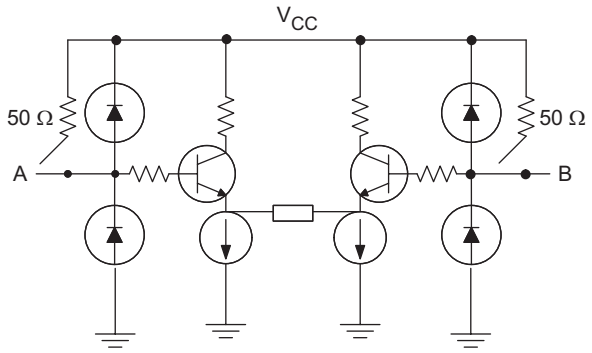
Table 1. Source Selection Lookup(1)

CONTROL PINS		I/O SELECTED		HOT-PLUG DETECT STATUS				Power Mode
S2	S1	Port Selected	SCL_SINK SDA_SINK	HPD1	HPD2	HPD3	HPD4	
L	L	Port 1 Terminations of port 2, 3 and 4 are disconnected.	SCL1 SDA1	HPD_SINK	5V_PWR2	5V_PWR3	5V_PWR4	Normal mode
L	H	Port 2 Terminations of port 1, 3 and 4 are disconnected.	SCL2 SDA2	5V_PWR1	HPD_SINK	5V_PWR3	5V_PWR4	Normal mode
H	L	Port 3 Terminations of port 1, 2 and 4 are disconnected.	SCL3 SDA3	5V_PWR1	5V_PWR2	HPD_SINK	5V_PWR4	Normal mode
H	H	Port 4 Terminations of port 1, 2 and 3 are disconnected.	SCL4 SDA4	5V_PWR1	5V_PWR2	5V_PWR3	HPD_SINK	Normal mode

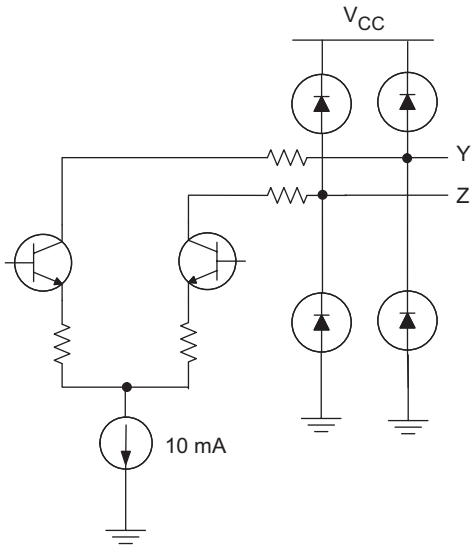
(1) H: Logic high; L: Logic low

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

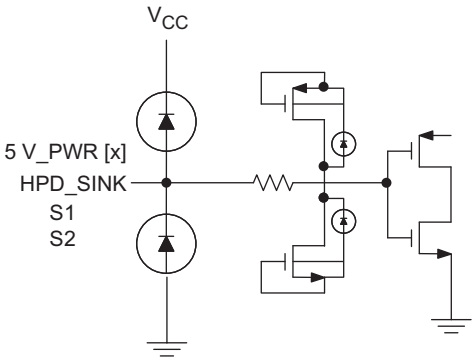
TMDS Input Stage



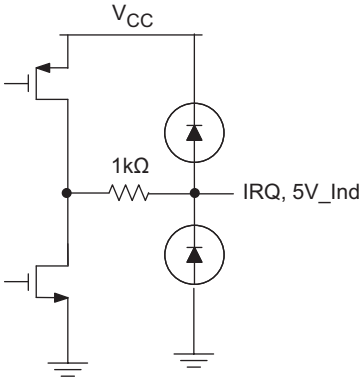
TMDS Output Stage



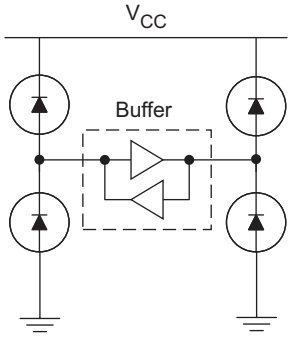
Status and Source Selector



Output Stage



DDC Buffer



HPD Output Stage

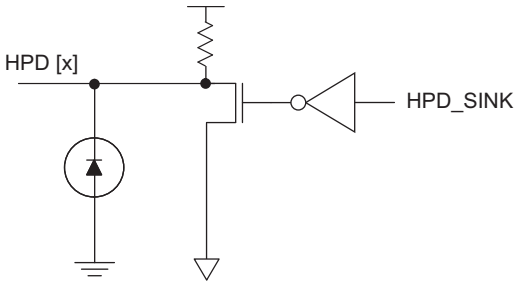


Table 2. Control Pin Lookup Table(1)

SIGNAL	LEVEL		STATE	DESCRIPTION
$\overline{LP}$	H		Normal Mode	Normal operational mode for device.
	L		Low-power mode	Device is forced into a low power state, causing the inputs and outputs to go to a high-impedance state. All other inputs are ignored.
S[2:1] GPIO Mode	S2	S1		
	L	L	Port 1	Port 1 is selected as the active port; all other ports are disabled.
	L	H	Port 2	Port 2 is selected as the active port; all other ports are disabled.
	H	L	Port 3	Port 3 is selected as the active port; all other ports are disabled.
	H	H	Port 4	Port 4 is selected as the active port; all other ports are disabled.
I2C_SEL	H		I^2C	Device is configured by I^2C logic.
	L		GPIO	Device is configured by GPIO.
Local_Addr	H		0101101	The 7-bit address for the local I^2C logic is 0101101
	L		0101100	The 7-bit address for the local I^2C logic is 0101100
OVS	H		Offset 1	DDC sink side VOL and VIL offset range 1, $V_{IL1\ (max)}$: 0.4V, $V_{OL1\ (max)}$: 0.7V
	L		Offset 2	DDC sink side VOL and VIL offset range 2, $V_{IL2\ (max)}$: 0.4V, $V_{OL2\ (max)}$: 0.6V
	Hi-Z		Offset 3	DDC sink side VOL and VIL offset range 3, $V_{IL3\ (max)}$: 0.3V, $V_{OL3\ (max)}$: 0.5V
VSadj	4.02 kΩ		Compliant Voltage Swing	Driver output voltage swing precision control to aid with system compliance. VSadj resistor value could be selected to be 4.02 kΩ ±10% based on the system requirement to pass HDMI compliance.

(1) (H) Logic high; (L) Logic low

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
TMDS461PZTR	TMDS461	100-pin TQFP reel
TMDS461PZT	TMDS461	100-pin TQFP tray

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage range(2)	VCC	–0.3 to 3.6	V
Voltage range	TMDS I/O	–0.3 to 4	V
	HPD and DDC I/O	–0.3 to 5.5	
	Control and status I/O	–0.3 to 5.5	
Electrostatic discharge	Human body model(3) on SCL[1:4], SDA[1:4], D[0:2]+_[1:4], D[0:2]–_[1:4], CLK+_[1:4], CLK–_[1:4] pins	±10,000	V
	Human body model(3) on all other pins	±6,000	
	Charged-device model(4)	±1500	
	Machine model(5)	±200	
Continuous power dissipation		See Dissipation Ratings table	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \le 25°C$	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
100-pin TQFP (PZT)	Low-K	1329 mW	13.2 mW/°C	731 mW
	High-K	1631 mW	16.3 mW/°C	897 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance			37.13		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			15.3		°C/W
$P_{D(1)}$	Device power dissipation in normal mode	$\overline{LP}$ = HIGH TMDS: $V_{ID(pp)}$ = 1200 mV, 3 Gbps TMDS data pattern; HPD_SINK = HIGH, S1/S2 = LOW/LOW, LOW/HIGH, HIGH/HIGH, HIGH/LOW.		666	792	mW
$P_{D(2)}$	Device power dissipation in standby mode	$\overline{LP}$ = HIGH, TMDS: $V_{ID(pp)}$ = 1200 mV, 3 Gbps TMDS data pattern; HPD_SINK = HIGH, (See Table 8, Register 0x02[7:6] =[0:1]. Note that standby power mode is only available when TMDS461 is configured in I^2C mode.		10	20	mW
P_{SD}	Device power dissipation in low-power mode	$\overline{LP}$ = LOW.		1	2	mW
P_{NCLK}	Device power dissipation in normal mode with no active TMDS input clock	$\overline{LP}$ = HIGH, No TMDS input clock, HPD_SINK =HIGH, S1/S2 = LOW/LOW, LOW/HIGH, HIGH/HIGH, HIGH/LOW.		61.2	72	mW

(1) The maximum rating is simulated under 3.6V VCC across worse case temperature and process variation, Typical conditions are simulated at 3.3V VCC, 25 °C with nominal process material.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	0		70	°C
TMDS DIFFERENTIAL OUTPUT PINS					
$V_{ID(pp)}$	Peak-to-peak input differential voltage	0.15		1.56	V
V_{IC}	Input common mode voltage	V_{CC} –0.4		V_{CC} + 0.01	V
AV_{CC}	TMDS output termination voltage	3	3.3	3.6	V
d_R	Data rate			3	Gbps
R_{VSADJ}	Resistor for TMDS compliant voltage swing range	3.66	4.02	4.47	KΩ
R_t	Termination resistance	45	50	55	Ω
DDC PINS					
V_I	Input voltage	0		5.5	V
$d_{R(I2C)}$	I^2C data rate			100	Kbps
HPD_SINK, 5V_PWR[x], S1, S2, OVS					
V_{IH}	High-level input voltage: HPD_SINK, 5V_PWR[x], S1, S2	2		5.5	V
V_{IL}	Low-level input voltage: HPD_SINK, 5V_PWR[x], S1, S2	0		0.8	V
V_{IHOVS}	High-level input voltage: OVS	3		5.5	V
V_{ILOVS}	Low-level input voltage: OVS	0		0.5	V

DEVICE POWER

The TMDS461 is designed to operate from a single 3.3-V supply voltage. The TMDS461 has three power modes of operation. These three modes are referred to as normal mode, standby mode, and low-power mode.

Normal mode is designed to be used during typical operating conditions. In normal mode, the device is fully functional and consumes the greatest amount of power.

Standby mode is designed to be used when reduced power is desired, but DDC and HPD communication must be maintained. Standby mode can be enabled via the I^2C interface (See Table 8) only. In standby mode, the high-speed TMDS data and clock channels are disabled to reduce power consumption. The internal I^2C logic and DDC function normally. HPD[1:4] of the selected port follows HPD_SINK. HPD[1:4] of the non-selected port follows 5V_PWR[1:4].

Low-power mode is designed to consume the least possible amount of power while still applying 3.3 V to the device. Low-power mode can be enabled by either the $\overline{LP}$ pin or by local I^2C (See Table 8). In low-power mode, all of the inputs and outputs are disabled with the exception of the internal I^2C logic and $\overline{LP}$ pin.

The clock-detect feature in the TMDS461 provides an automatic power-management feature in normal mode. if no valid TMDS clock is detected, the terminations on the input TMDS data lines are disconnected, and the TMDS outputs are high-Z. As soon as a valid TMDS clock is detected, the terminations on the TMDS data lines are connected, the TMDS outputs come out of high-Z, and the device is fully functional and consumes the greatest amount of power.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Normal-mode supply current	$\overline{LP}$ = HIGH TMDS: $V_{ID(pp)}$ = 1200 mV, 3 Gbps TMDS data pattern; HPD_SINK = HIGH, S1/S2 = LOW/LOW, LOW/HIGH, HIGH/HIGH, HIGH/LOW.		185	220	mA
I_{STBY}	Standby supply current	$\overline{LP}$ = HIGH, TMDS: $V_{ID(pp)}$ = 1200 mV, 3 Gbps TMDS data pattern; HPD_SINK = HIGH, (See Table 8, Register 0x02[7:6] =[0:1]. Note that standby power mode is only available when TMDS461 is configured in I^2C mode.		3	5.5	mA
I_{SD}	Shutdown current	$\overline{LP}$ = LOW.		300	555	µA
I_{NCLK}	Normal-mode supply current, with no active TMDS input clock	$\overline{LP}$ = HIGH, No TMDS input clock, HPD_SINK =HIGH, S1/S2 = LOW/LOW, LOW/HIGH, HIGH/HIGH, HIGH/LOW.		17	20	mA

5V DETECT and HOT PLUG DETECT

5V DETECT: TMDS461 incorporates 5V detect logic on each input port. 5V_PWR is the 5V that an HDMI/DVI source provides to an HDMI/DVI sink. As soon as TMDS461 detects a high on any of the 5V_PWR[1:4] signals, the 5V_Ind pin which is 5V Power detect indicator goes high. In I^2C mode, a micro controller connected to TMDS461 can read the status of 5V_PWR[x] signals by reading (See Table 7) I^2C register 0x01.

Hot Plug Detect: The TMDS461 is designed to support the Hot Plug indication to the input ports. For the selected port, the state of the Hot Plug output (HPD[1:4]) follows the state of the Hot Plug input (HPD_SINK). For the non selected ports, the state of the Hot Plug outputs follows logic state of 5V_PWR. (See Table 1). HPD[x] are internally connected to 5V_PWR[x] via 1KΩ resistor as shown in Figure 1(b). Thus even if the TMDS461 is powered off, HPD[x] will still follow 5V_PWR[x]. When the HDMI transmitter does not have the capability of detecting the TMDS receiver termination, using the HPD signal as a reference for sensing port selections is the only possible method. Thus it is recommended that HPD_SINK can be held low before port selection is done and then forced high after port selection, this ensures that HPD[x] of the selected port is pulsed High-to-Low at port selection before HPD[x] follows HPD_SINK.

In Standby power savings mode, HPD functions similar to normal mode. In low ($\overline{LP}$) power savings mode, the HPD[x] follows 5V_PWR[x].

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(HPD[x])}$	High-level output voltage	5V_PWR =4.5-5.5V			5V_PWR	V
$V_{OL(HPD[x])}$	Low-level output voltage	5V_PWR =4.5-5.5V	0		0.4	V
$I_{H(HPD\_SINK)}$	High-level input current	V_{IH} = 2V, V_{CC} = 3.6 V	–10		10	µA
$I_{L(HPD\_SINK)}$	Low-level input current	V_{IL} = 0.8V, V_{CC} = 3.6 V	–10		10	µA
$I_{H(5V\_PWR[x])}$	High-level input current	V_{IH} = 5.5V, V_{CC} = 3.6 V	–10		10	µA
$V_{OH(5V\_Ind)}$	High-level output voltage	I_{OH} = 100 µA	2.4		VCC	V
$V_{OL(5V\_Ind)}$	Low-level output voltage	I_{OL} = 100 µA	0		0.4	V
$R_{L(HPD[x])}$	Output source impedance	$R_{L(HPD[x])}$ is connected between 5V_PWR[x] and HPD[x].	800	1000	1200	kΩ

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD1(HPD)}$	HPD_SINK propagation delay	HPD_SINK to HPD[1:4]			40	ns
$t_{PD2(HPD)}$	5V_PWR to HPD propagation delay	5V_PWR[1:4] to HPD[1:4].			30	ns
$t_{S1(HPD)}$	Selecting port HPD switch time	S[1:2] to HPD[1:4]			40	ns
$t_{S2(HPD)}$	De-selecting port HPD switch time	S[1:2] to HPD[1:4]			25	ns
$t_{Z(HPD)}$	$\overline{LP}$ to HPD[x] switch time	$\overline{LP}$ to HPD[x]			40	ns
$t_{PD3(5v)}$	5V_PWR to 5V_Ind propagation delay	5V PWR to 5V_Ind propagation Delay (Load on 5V_Ind: 5 pF)			30	ns

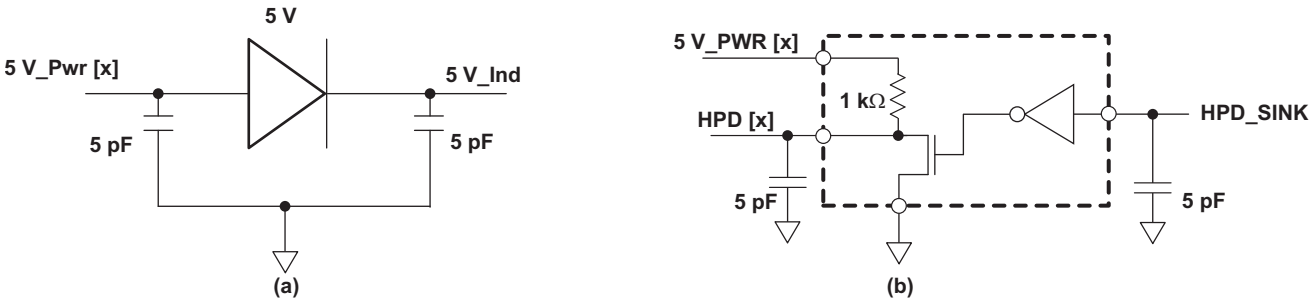


Figure 1. 5V_PWR and HPD Test Circuit

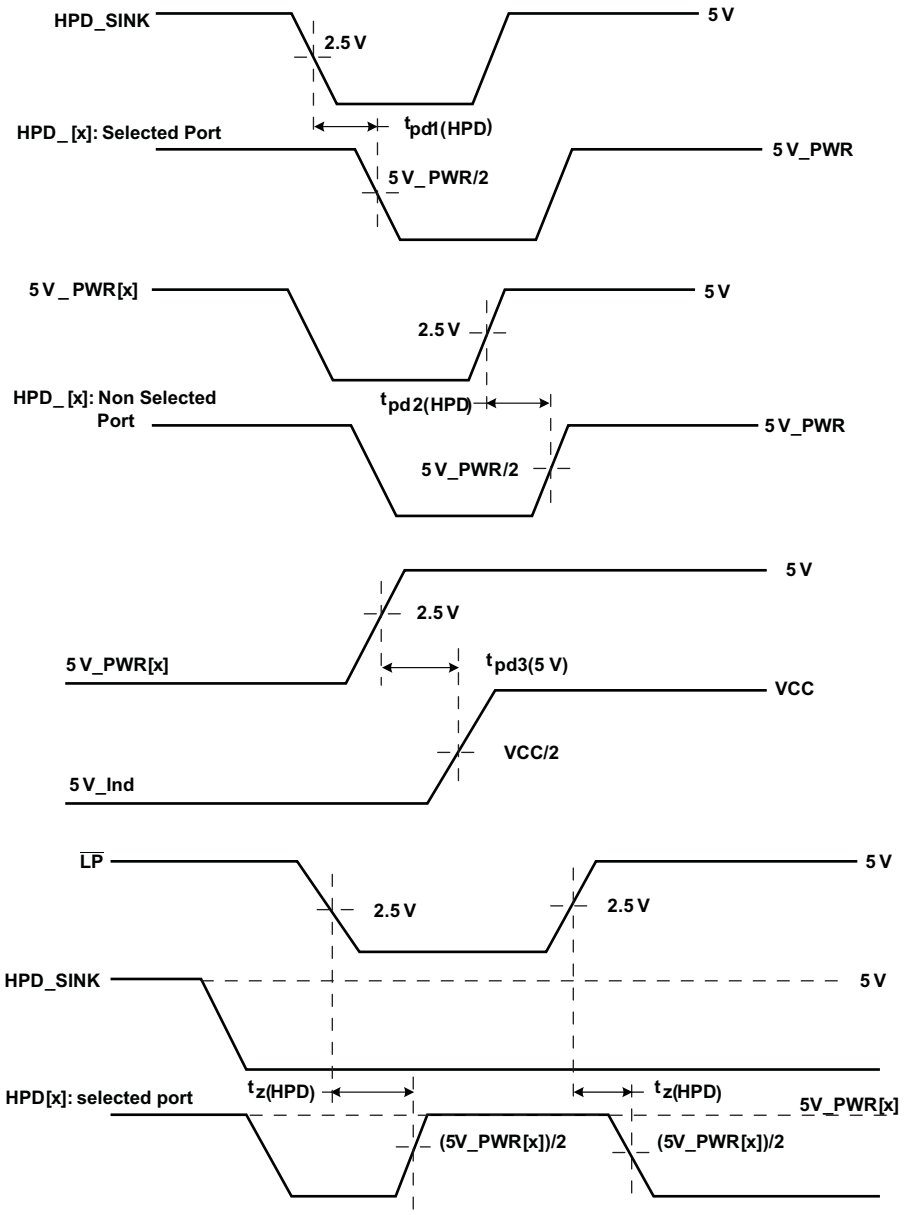


Figure 2. HPD Timing Diagram #1

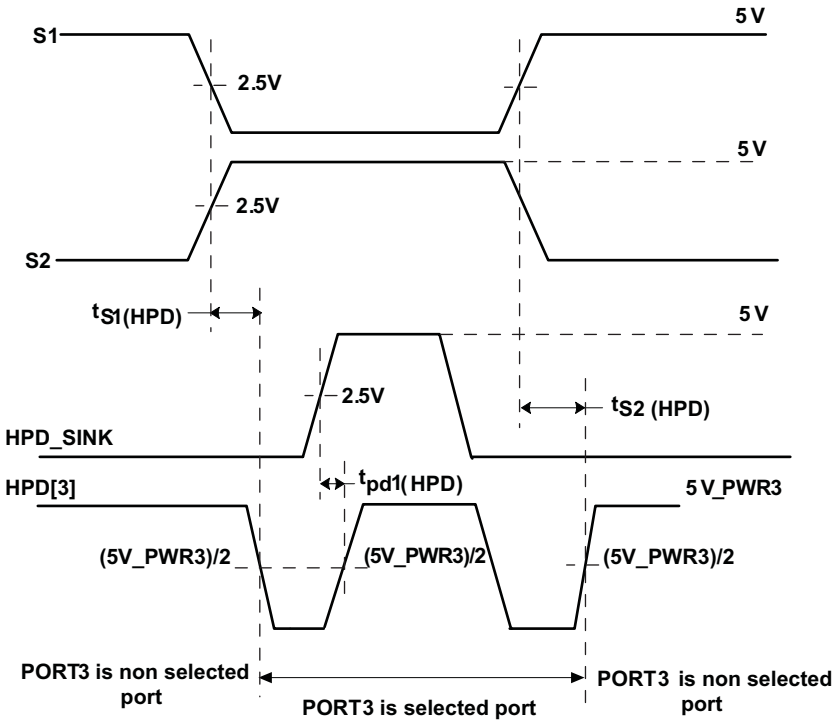


Figure 3. HPD Timing Diagram #2

IRQ

I²C mode: When TMDS461 is configured in I²C mode, the IRQ pin in TMDS461 functions as a system level interrupt indicator pin. The TMDS461 issues Interrupt Requests by raising the IRQ pin from low to high, which can be detected by the sink micro-controller. An Interrupt Request occurs when any system level change is detected by TMDS461, which is a change in 5V_PWR on the source side, a change in the selected port, or a change in the selected port's valid clock detect. The micro-controller can read I²C register address 0x01 to obtain the current status of 5V_PWR, the selected port, and clock detect status. Once the micro-controller has read 0x01, the IRQ pin returns to low.

It is desired that as soon as the sink micro-controller gets an Interrupt Request, it reads I²C register address 0x01

GPIO mode: When TMDS461 is configured in GPIO mode, the IRQ pin in TMDS461 functions as a clock-detect indicator pin for the selected port. If a valid clock is detected by the clock detect circuit, IRQ goes high. If no valid clock is detected, IRQ is driven low. Refer to (TMDS Main Link Switching Characteristics) t_{CLK1} for valid clock enable time and (TMDS Main Link Switching Characteristics) t_{CLK2} for valid clock disable time.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(IRQ)}$	High-level output voltage	I_{OH} = 100 µA	2.4		V_{CC}	V
$V_{OL(IRQ)}$	Low-level output voltage	I_{OL} = 100 µA	0		0.4	V
$R_{L(IRQ)}$	Output source impedance		800	1000	1200	kΩ

Automatic Port Select Feature

TMDS461 incorporates an AutoSelect Feature that is available in I^2C mode only. Refer to Table 8, bits 3, 4, 5. If the TMDS461 is configured in AutoSelect Mode, then the port selection is done based on the priority bit (Refer to Table 8 , bit 3, 4) and 5V_PWR[x] (See Table 7, bit 0, 1, 2, 3) as indicated in Figure 4, Figure 5, Figure 6, and Figure 7 .

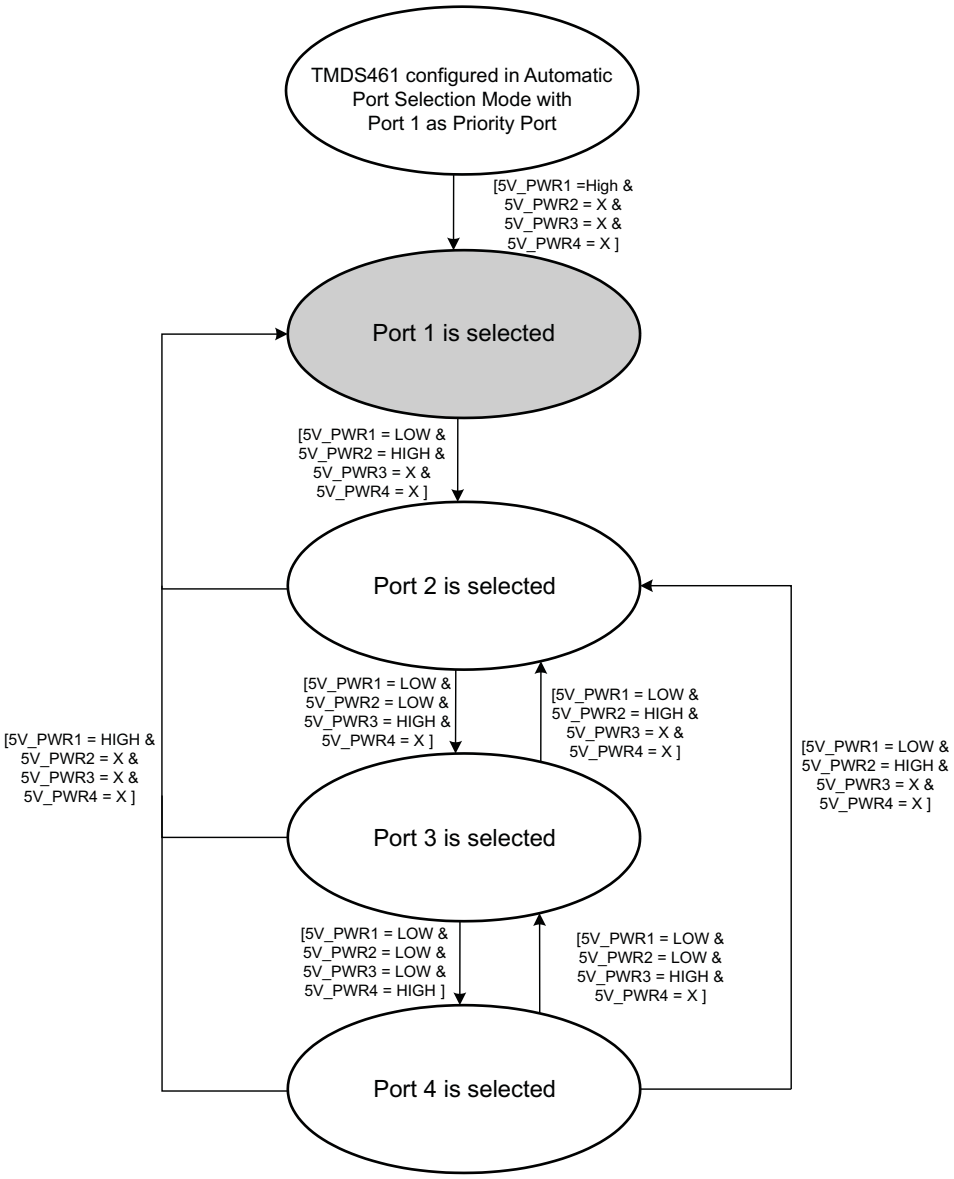


Figure 4. TMDS461 Configured in AutoSelect Mode, with Port 1 as Priority Port

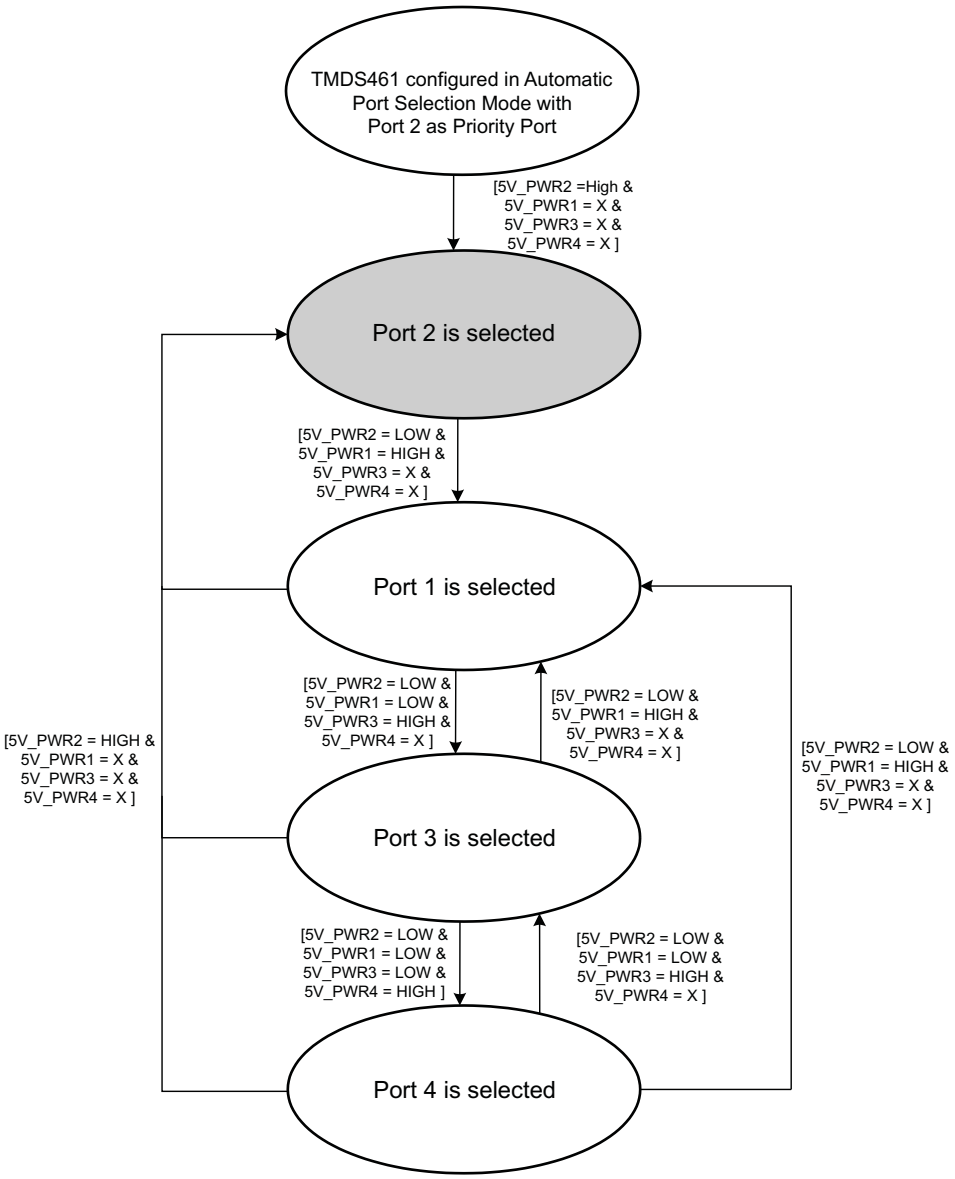


Figure 5. TMDS461 Configured in AutoSelect Mode, with Port 2 as Priority Port

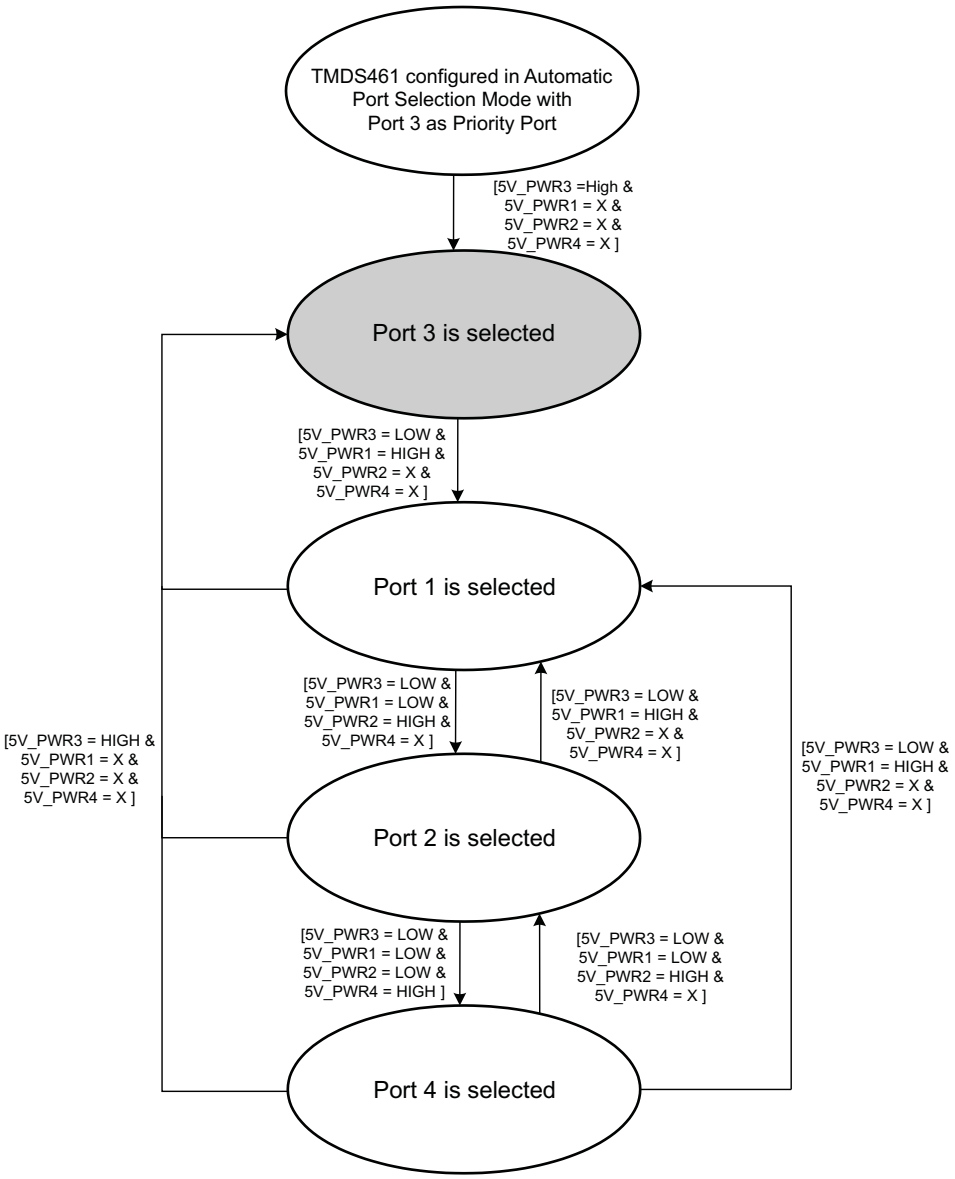


Figure 6. TMDS461 Configured in AutoSelect Mode, with Port 3 as Priority Port

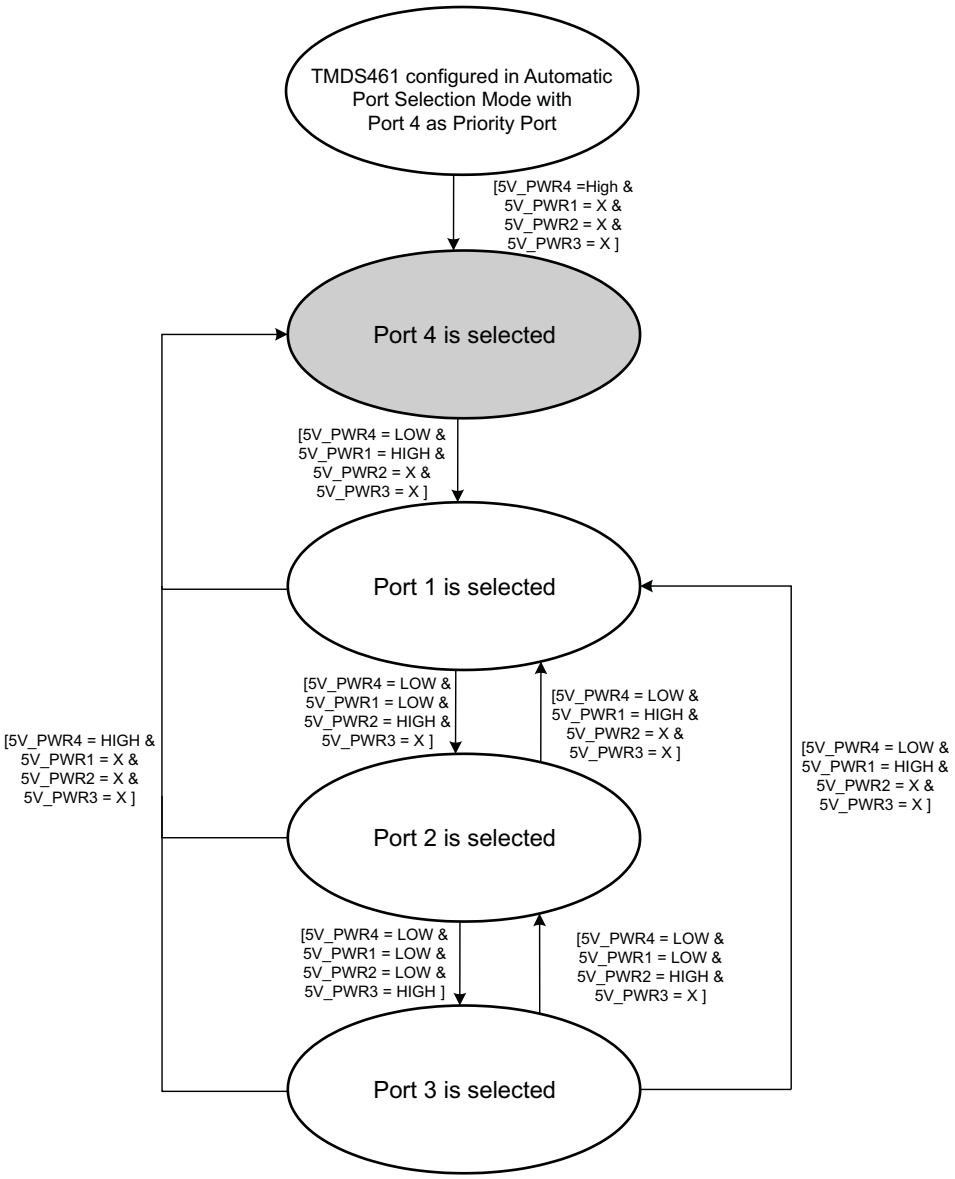


Figure 7. TMDS461 Configured in AutoSelect Mode, with Port 4 as Priority Port

TMDS DDC and Local I²C Pins

DDC I²C Buffer or Repeater: The TMDS461 provides buffering on the DDC I²C interface for each of the input ports connected. This feature isolates the capacitance on the source side from the sink side and thus helps in passing system-level compliance. See the DDC I2C Function Description section for a detailed description on how the DDC I²C buffer operates. Note that a key requirement on the sink side is that the $V_{IL(Sink)}$ (input to TMDS461) should be less than 0.4 V. This requirement should be met for the DDC I²C buffer to function properly. There are three settings of $V_{IL(Sink)}$ and $V_{OL(Sink)}$ that can be chosen based on OVS settings (See Table 9).

Local I²C Interface: The TMDS461 includes a slave I²C interface to control device features like TMDS input port selection, TMDS output edge-rate control, power management, DDC buffer OVS settings, etc. See Table 7 through Table 13. The TMDS461 is designed to be controlled via a local I²C interface or GPIO interface, based on the status of the I2C_SEL pin. The local I²C interface in the TMDS461 is only a slave I²C interface. See the I2C INTERFACE NOTES section for a detailed description of I²C functionality.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_L	Low-level input current		VCC = 3.6 V, V_I = 0 V	–10		10	µA
$I_{lkg(Sink)}$	Input leakage current	Sink pins	VCC = 3.6 V, V_I = 4.95 V	–10		10	µA
$C_{IO(Sink)}$	Input/output capacitance	Sink pins	DC bias = 2.5 V, AC = 3.5 Vp-p, f = 100 kHz			15	pF
$V_{IH(Sink)}$	High-level input voltage	Sink pins		2.1		5.5	V
$V_{IL1(Sink)}$	Low-level input voltage	Sink pins	OVS 1	–0.2		0.4	V
$V_{OL1(Sink)}$	Low-level output voltage	Sink pins	I_O = 3 mA, OVS = HIGH	0.6		0.7	V
$V_{IL2(Sink)}$	Low-level input voltage	Sink pins	OVS 2	–0.2		0.4	V
$V_{OL2(Sink)}$	Low-level output voltage	Sink pins	I_O = 3 mA, OVS = LOW	0.5		0.6	V
$V_{IL3(Sink)}$	Low-level input voltage	Sink pins	OVS 3	–0.2		0.3	V
$V_{OL3(Sink)}$	Low-level output voltage	Sink pins	I_O = 3 mA, OVS = high-Z	0.4		0.5	V
$I_{lkg(I2C)}$	Input leakage current	Port[1:4] pins	VCC = 3.6 V, V_I = 4.95 V	–10		10	µA
$C_{IO(I2C)}$	Input/output capacitance	Port[1:4] pins	DC bias = 2.5 V, AC = 3.5 Vp-p, f = 100 kHz			15	pF
$V_{IH(I2C)}$	High-level input voltage	Port[1:4] pins		2.1		5.5	V
$V_{IL(I2C)}$	Low-level input voltage	Port[1:4] pins		–0.2		1.5	V
$V_{OL(I2C)}$	Low-level output voltage	Port[1:4] pins	I_O = 3 mA			0.2	V

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH2}	Propagation delay time, low to high	Source to sink	80		251	ns
t_{PHL2}	Propagation delay time, high to low	Source to sink	35		200	ns
t_{PLH1}	Propagation delay time, low to high	Sink to source	204		459	ns
t_{PHL1}	Propagation delay time, high to low	Sink to source	35		200	ns
t_{f1}	Output signal fall time	Sink side	20		72	ns
t_{f2}	Output-signal fall time	Source side	20		72	ns
f_{SCL}	SCL clock frequency for internal register	Local I^2C			100	kHz
$t_{W(L)}$	Clock LOW period for I^2C register	Local I^2C	4.7			µs
$t_{W(H)}$	Clock HIGH period for internal register	Local I^2C	4			µs
t_{SU1}	Internal register setup time, SDA to SCL	Local I^2C	250			ns
$t_{h(1)}$ *1	Internal register hold time, SCL to SDA	Local I^2C	0			µs
$t_{(buf)}$	Internal register bus free time between STOP and START	Local I^2C	4.7			µs
$t_{su(2)}$	Internal register setup time, SCL to START	Local I^2C	4.7			µs
$t_{h(2)}$	Internal register hold time, START to SCL	Local I^2C	4			µs
$t_{su(3)}$	Internal register hold time, SCL to STOP	Local I^2C	4			µs

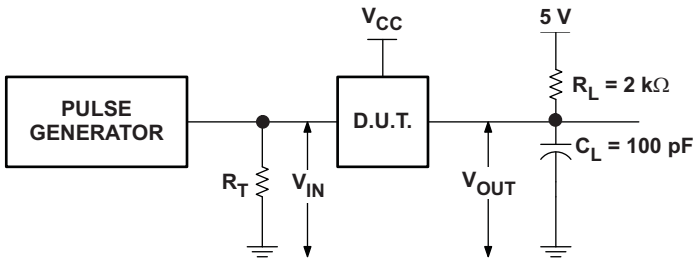


Figure 8. Sink-Side Test Circuit

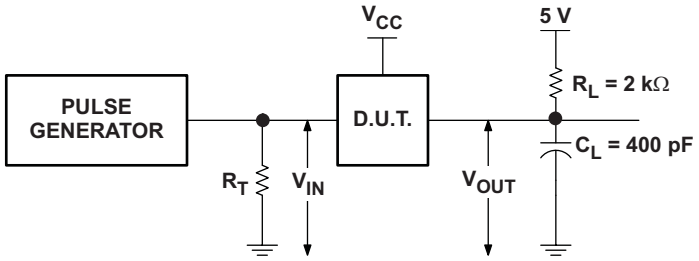


Figure 9. Source-Side Test Circuit

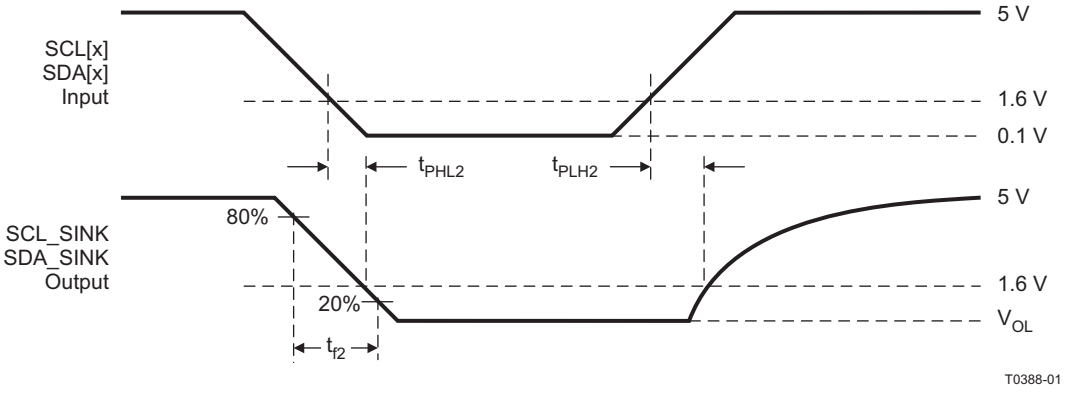


Figure 10. Sink-Side Output AC Measurements

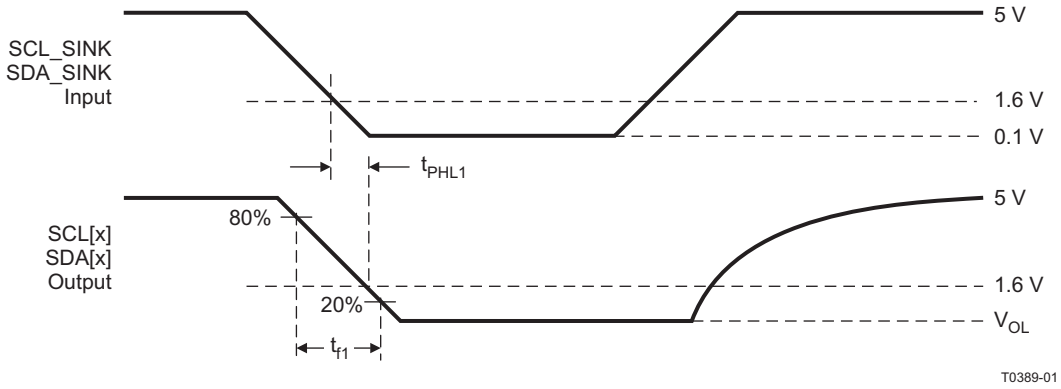


Figure 11. Source-Side Output AC Measurements

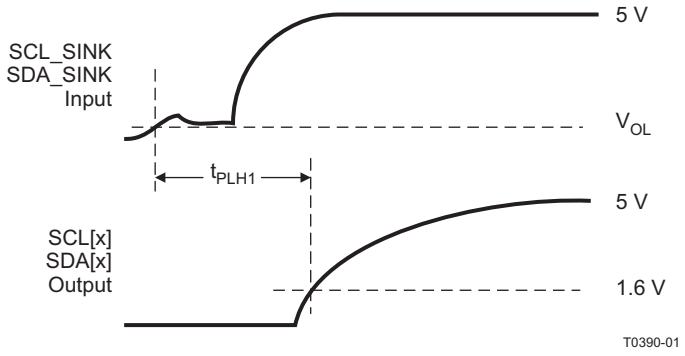


Figure 12. Source-Side Output AC Measurements Cont.

TMDS Main Link Pins

The TMDS port of the TMDS461 is designed to be compliant with the Digital Video Interface (DVI) 1.0 and High Definition Multimedia Interface (HDMI) 1.3a specifications. The differential output voltage swing can be fine-tuned with the VSadj resistor.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Single-ended HIGH-level output voltage	AVCC = 3.3 V, R_T = 50 Ω. See Figure 13	AVCC – 10		AVCC + 10	mV
V_{OL}	Single-ended LOW-level output voltage		AVCC – 600		AVCC – 400	mV
V_{SWING}	Single-ended output voltage swing		400		600	mV
$V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states				5	mV
$V_{OD(pp)}$	Peak-to-peak output differential voltage		800		1200	mV
$V_{(O)SBY}$	Single-ended standby output voltage		AVCC – 10		AVCC + 10	mV
$I_{(O)OFF}$	Single-ended power-down output current	0 V ≤ VCC ≤ 1.5 V, AVCC = 3.3 V, R_T = 50 Ω	–10		10	µA
I_{OS}	Short-circuit output current	See Figure 20	–15	12	15	mA
$V_{CD(pp)}$	Minimum valid clock differential voltage (peak-to-peak)	Input TMDS clock frequency = 300 MHz	100			mV

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time	AVCC = 3.3 V, R_T = 50 Ω. See Figure 13 and Figure 14.	250		800	ps
t_{PHL}	Propagation delay time		250		800	ps
t_{R1}	Rise time, fastest mode (default setting): Fastest Setting		84	110	140	ps
t_{F1}	Fall time, fastest mode (default setting): Fastest Setting		84	110	140	ps
t_{R2}	Rise time, fastest mode + 50 ps (approximately)		142	160	190	ps
t_{F2}	Fall time, fastest mode + 50 ps (approximately)		142	160	190	ps
t_{R3}	Rise time, fastest mode + 100 ps (approximately)		187	210	230	ps
t_{F3}	Fall time, fastest mode + 100 ps (approximately)		187	210	230	ps
t_{R4}	Rise time, fastest mode + 120 ps (approximately): Slowest Setting		216	230	260	ps
t_{F4}	Fall time, fastest mode + 120 ps (approximately): Slowest Setting		216	230	260	ps
$t_{SK(P)}$	Pulse skew (see (2))			8	15	ps
$t_{SK(D)}$	Intra-pair skew	AVCC = 3.3 V, R_T = 50 Ω. See Figure 15.		10	30	ps
$t_{SK(O)}$	Inter-pair skew (see (3))				100	ps
$t_{JITD(PP)}$	Peak-to-peak output residual data jitter	AVCC = 3.3 V, R_T = 50 Ω, dR = 2.25 Gbps. See Figure 18 for measurement setup; residual jitter is the total jitter measured at TTP4 minus the jitter measured at TTP1. See Figure 19 for the loss profile of the cable used for $t_{JITD(PP)}$ measurement. Also see Typical Characteristics for $t_{JITD(PP)}$ across cable length and input TMDS data rate.		40	88	ps

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between t_{PLH} and t_{PHL} of a specified terminal.
(3) $t_{sk(o)}$ is the magnitude of the difference in propagation delay times between any specified terminals of a sink-port bank when inputs of the active source port are tied together.

SWITCHING CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{JITC(PP)}$	Peak-to-peak output residual clock jitter	AVCC = 3.3 V, R_T = 50 Ω, input TMDS clock frequency = 225 MHz. See Figure 18 for measurement setup; residual jitter is the total jitter measured at TTP4 minus the jitter measured at TTP1. See Figure 19 for the loss profile of the cable used for $t_{JITC(PP)}$ measurement.		10	35	ps
t_{CLK1}	Valid clock-detect enable time	AVCC = 3.3 V, R_T = 50 Ω, input TMDS clock frequency = 300 MHz. See Figure 17.		300	500	ns
t_{CLK2}	Invalid clock-detect disable time	AVCC = 3.3 V, R_T = 50 Ω, input TMDS clock frequency = 1 MHz. See Figure 17.		500	800	ns
t_{SEL1}	Port selection time (see (4))	AVCC = 3.3 V, R_T = 50 Ω		300	500	ns
t_{SEL2}	Port deselection time (see (5))	AVCC = 3.3 V, R_T = 50 Ω		40	50	ns
f_{CD}	Clock-detect frequency	AVCC = 3.3 V, R_T = 50 Ω. See Figure 17.	25		300	MHz

(4) t_{SEL1} includes the time for the valid clock detect enable time and $t_{S1(HPD)}$, because the $t_{S1(HPD)}$ event happens in parallel with t_{SEL1}; thus, the t_{SEL1} time is primarily the t_{CLK1} time.
(5) t_{SEL2} is primarily the $t_{S2(HPD)}$ time.

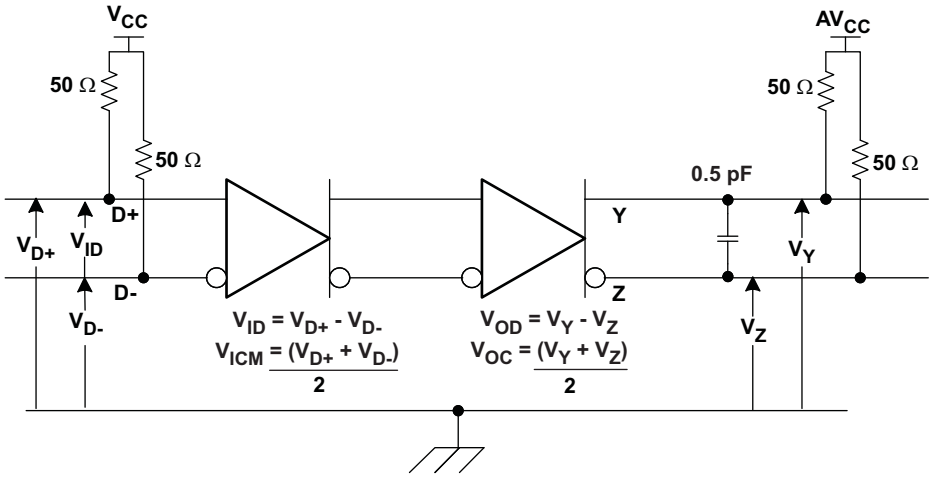


Figure 13. TMDS Main Link Test Circuit

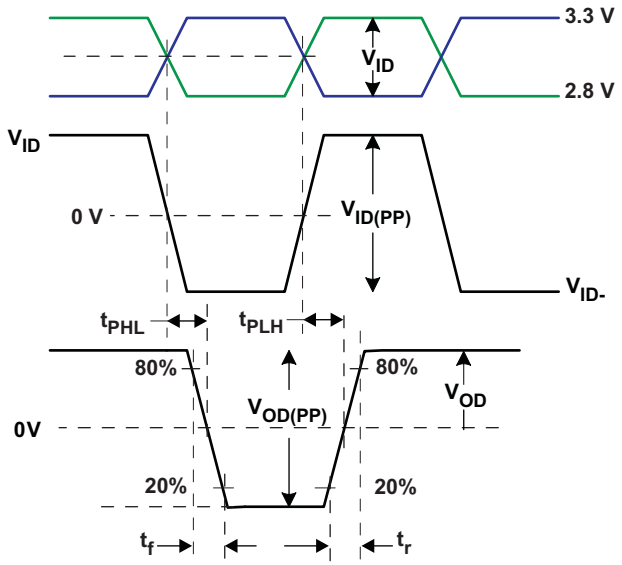


Figure 14. TMDS Main Link Timing Measurements

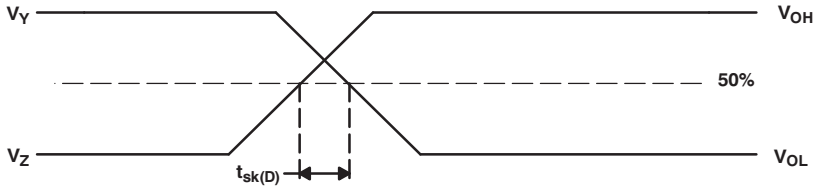


Figure 15. Definition of Intra-Pair Differential Skew

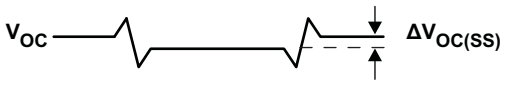


Figure 16. TMDS Main Link Common Mode Measurements

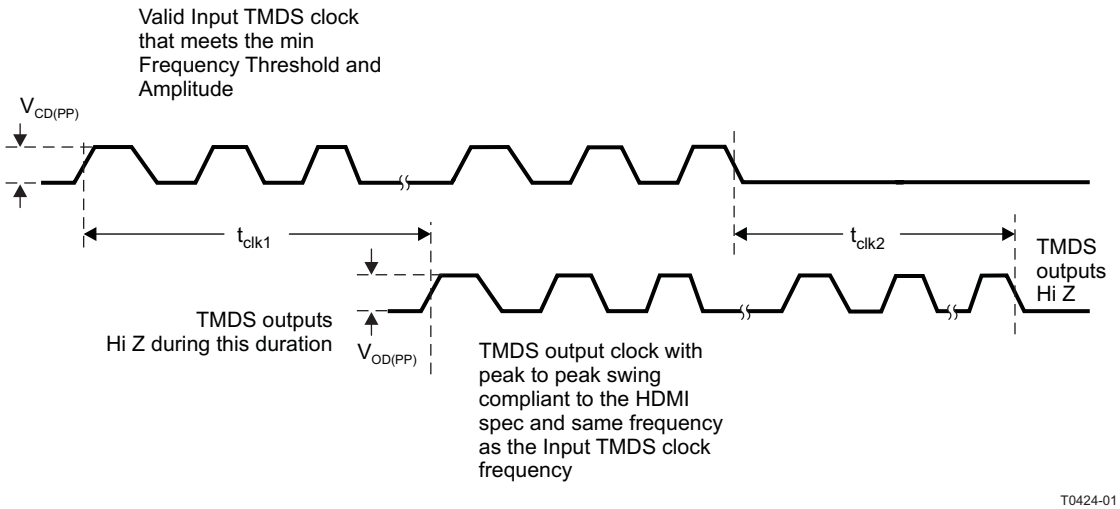
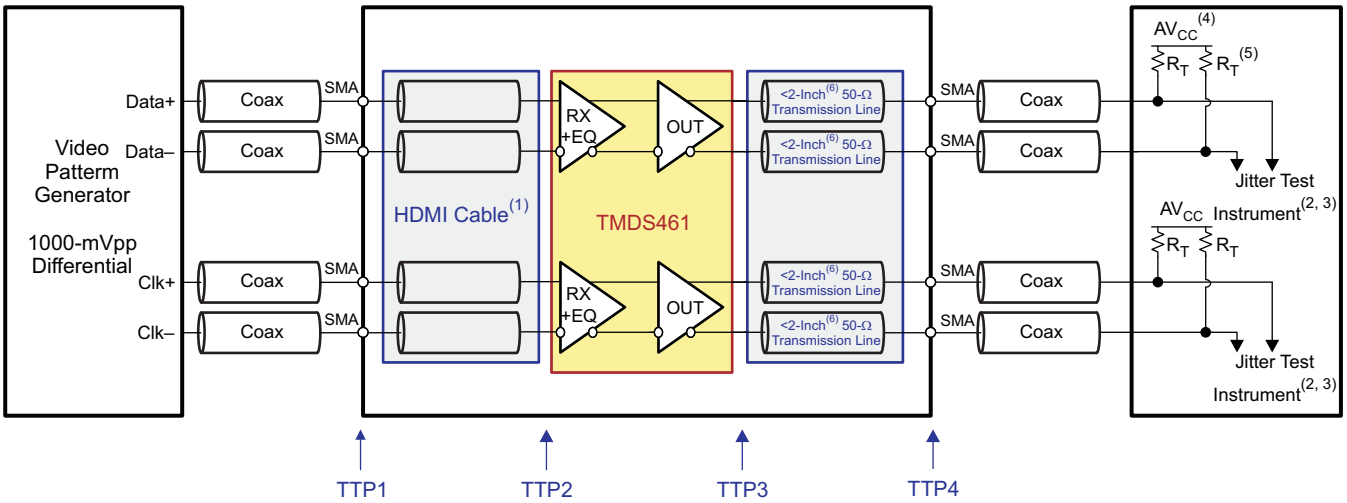


Figure 17. Clock-Detect Timing Diagram



(1) The HDMI cable between TTP1 and TTP2 is 20 m. See Figure 19 for the loss profile of the cable.
(2) All jitter is measured at a BER of 10^{-9}.
(3) Residual jitter is the total jitter measured at TTP4 minus the jitter measured at TTP1.
(4) AVCC = 3.3 V.
(5) R_T = 50 Ω.
(6) 2 inches = 5.08 cm.

Figure 18. TMDS Jitter Measurements

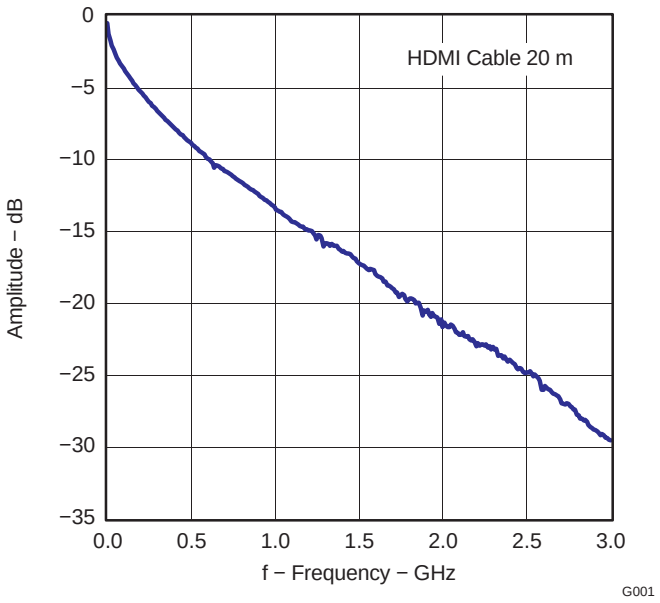


Figure 19. Loss Profile of 20-m Cable

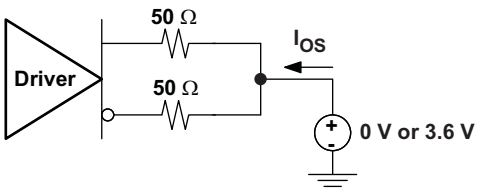


Figure 20. TMDS Main Link Short Circuit Output Circuit

TYPICAL CHARACTERISTICS

AVCC = 3.3 V, R_T = 50 Ω

POWER vs AMBIENT TEMPERATURE

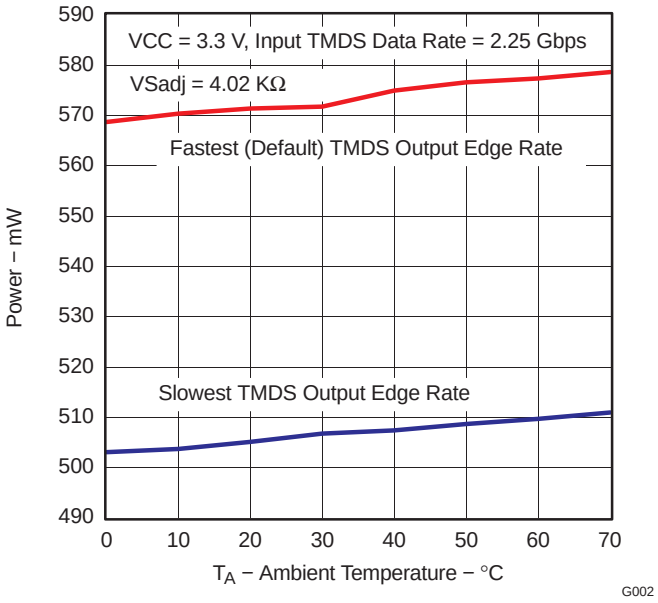


Figure 21.

POWER vs INPUT TMDS DATA RATE

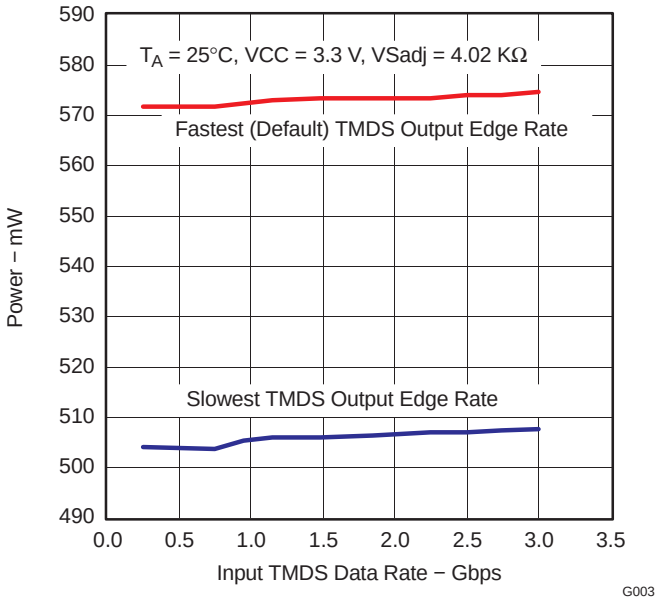


Figure 22.

PEAK-PEAK RESIDUAL DATA JITTER vs INPUT TMDS DATA RATE

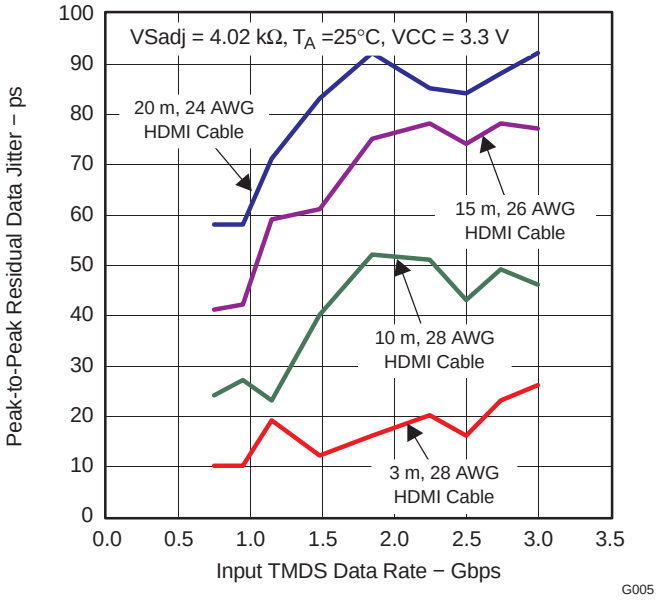


Figure 23.

PEAK-PEAK RESIDUAL DATA JITTER vs HDMI CABLE LENGTH

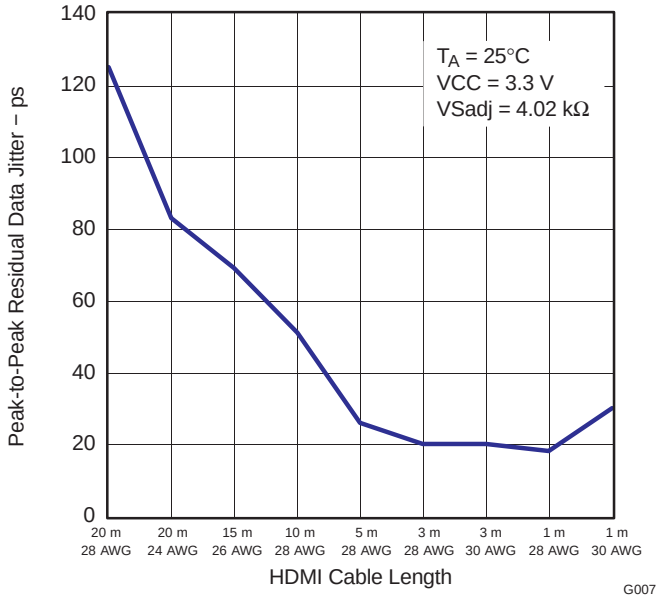


Figure 24.

TYPICAL CHARACTERISTICS (continued)

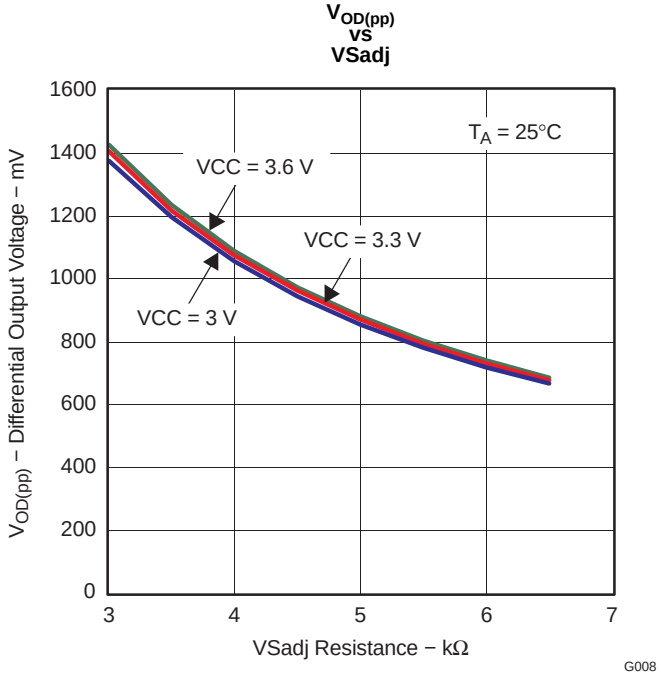


Figure 25.

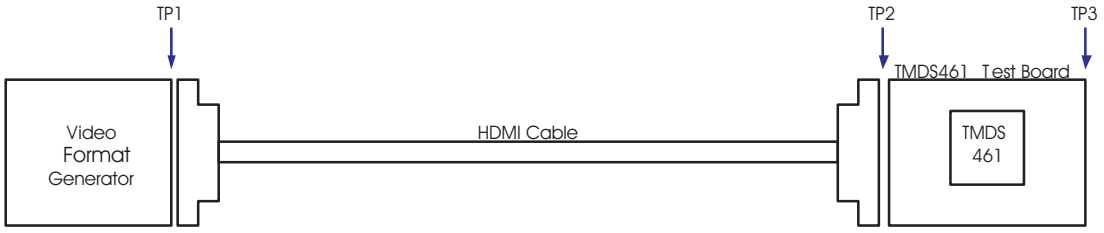


Figure 26. HDMI Cable Test-Point Configuration

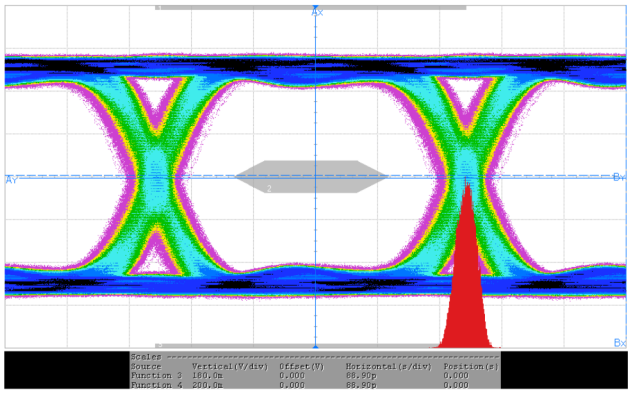


Figure 27. Eye at TP3 (output of TMDS461) with 20 m, 24 AWG HDMI cable, 2.25 Gbps Input TMDS data Rate, Fastest Rise and Fall Time Setting on TMDS outputs

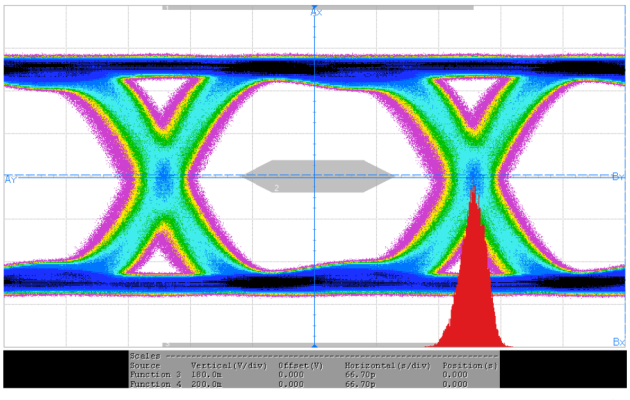
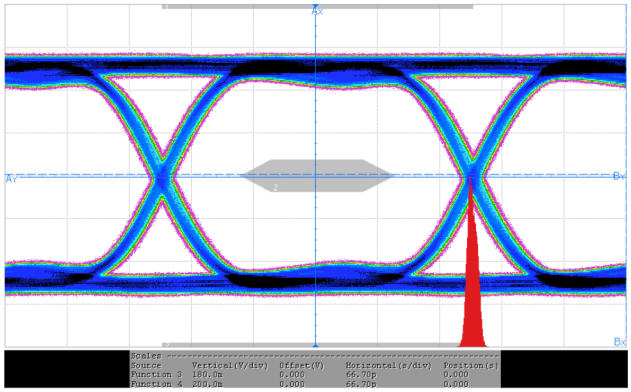


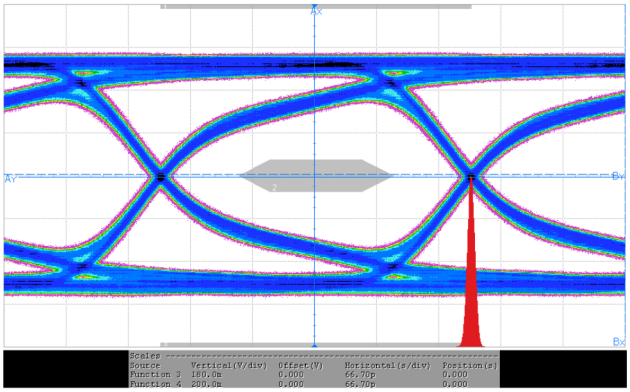
Figure 28. Eye at TP3 (output of TMDS461) with 20 m, 24 AWG HDMI cable, 3 Gbps Input TMDS data Rate, Fastest Rise and Fall Time Setting on TMDS outputs

TYPICAL CHARACTERISTICS (continued)



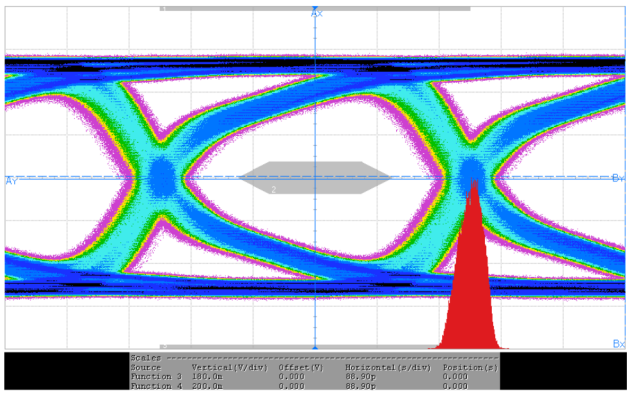
C003

Figure 29. Eye at TP3 (output of TMDS461) with 3 m, 28 AWG HDMI cable, 3 Gbps Input TMDS data Rate, Fastest Rise and Fall Time Setting on TMDS outputs



C004

Figure 30. Eye at TP3 (output of TMDS461) with 3 m, 28 AWG HDMI cable, 3 Gbps Input TMDS data Rate, Slowest Rise and Fall Time Setting on TMDS outputs



C005

Figure 31. Eye at TP3 (output of TMDS461) with 20 m, 24 AWG HDMI cable, 2.25 Gbps Input TMDS data Rate, Slowest Rise and Fall Time Setting on TMDS outputs

APPLICATION INFORMATION

Supply Voltage

The TMDS461 is powered up with a single power source that is 3.3-V VCC for the TMDS circuitry for HPD, DDC, and most of the control logic.

TMDS Input Fail-Safe

The TMDS461 incorporates clock-detect circuitry. If there is no valid TMDS clock from the connected HDMI/DVI source, the TMDS461 does not switch on the terminations on the source-side data channels. Additionally, the TMDS outputs are placed in the high-impedance state. This prevents the TMDS461 from turning on its outputs if there is no valid incoming HDMI/DVI data.

TMDS Outputs

A 10% precision resistor, 4.02-kΩ, is recommended to control the output swing to the HDMI-compliant 800-mV to 1200-mV range $V_{OD(pp)}$ (1000 mV typical).

DDC I^2C Function Description

The TMDS461 provides buffers on the DDC I^2C lines on all four input ports. This section explains the operation of the buffer. For representation, the source side of the TMDS461 is represented by RSCL/RSDA, and the sink side is represented by TSCL/TSDA. The buffers on the RSCL/RSDA and TSCL/TSDA pins are 5-V tolerant when the device is powered off and high-impedance under low supply voltage, 1.5 V or below. If the device is powered up, the driver T (see Figure 32) is turned on or off depending on the corresponding R-side voltage level.

When the R side is pulled low below 1.5 V, the corresponding T-side driver turns on and pulls the T side down to a low level output voltage, V_{OL}. The value of V_{OL} and V_{IL} on the T side or the sink side of the TMDS461 switch depends on the output-voltage select (OVS) control settings. OVS control can be changed by the slave I^2C, see Table 9. When the OVS1 setting is selected, V_{OL} is typically 0.7 V and V_{IL} is typically 0.4 V. When the OVS2 setting is selected, V_{OL} is typically 0.6 V and V_{IL} is typically 0.4 V. When OVS3 setting (default) is selected, V_{OL} is typically 0.5 V and V_{IL} is typically 0.3 V. V_{OL} is always higher than the driver-R input threshold, V_{IL} on the T side or the sink side, preventing lockup of the repeater loop. The TMDS461 is targeted primarily as a switch in the HDTV market and is expected to be a companion chip to an HDMI receiver; thus, the OVS control has been provided on the sink side, so that the requirement of V_{IL} to be less than 0.4 V can be met. The V_{OL} value can be selected to improve or optimize noise margins between V_{OL} and V_{IL} of the repeater itself or V_{IL} of some external device connected on the T side.

When the R side is pulled up, above 1.5 V, the T-side driver turns off and the T-side pin is high-impedance.

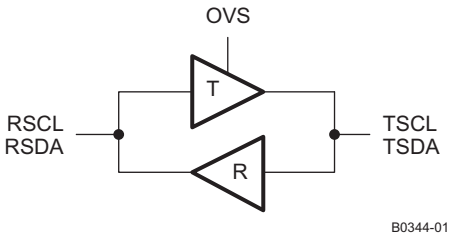


Figure 32. I^2C Drivers in the TMDS461 = Side Is the HDMI Source Side, T Side Is the HDMI Sink Side)

When the T side is pulled below 0.4 V by an external I^2C driver, both drivers R and T are turned on. Driver R pulls the R side to near 0 V, and driver T is on, but is overridden by the external I^2C driver. If driver T is already on, due to a low on the R side, driver R just turns on.

When the T side is released by the external I^2C driver, driver T is still on, so the T side is only able to rise to the V_{OL} of driver T. Driver R turns off, because V_{OL} is above its 0.4-V V_{IL} threshold, releasing the R side. If no external I^2C driver is keeping the R side low, the R side rises, and driver T turns off once the R side rises above 1.5 V, see Figure 33.

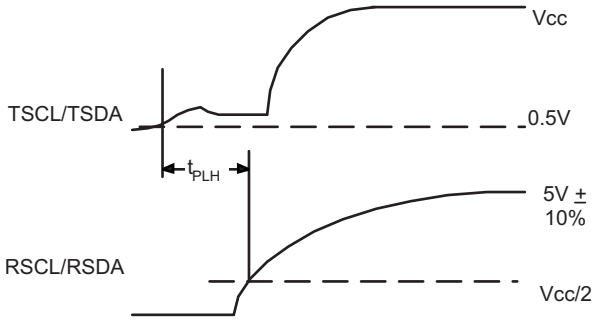


Figure 33. Waveform of Driver T Turning Off

It is important that any external I^2C driver on the T side is able to pull the bus below 0.4 V to achieve full operation. If the T side cannot be pulled below 0.4 V, driver R may not recognize and transmit the low value to the R side.

DDC I^2C Behavior

The typical application of the TMDS461 is as a 4:1 switch in a TV connecting up to four HDMI input sources to an HDMI receiver. The I^2C repeater is 5-V tolerant, and no additional circuitry is required to translate between 3.3-V and 5-V bus voltages. In the following example, the system master is running on an R-side I^2C-bus while the slave is connected to a T-side bus. Both buses run at 100 kHz, supporting standard-mode I^2C operation. Master devices can be placed on either bus.

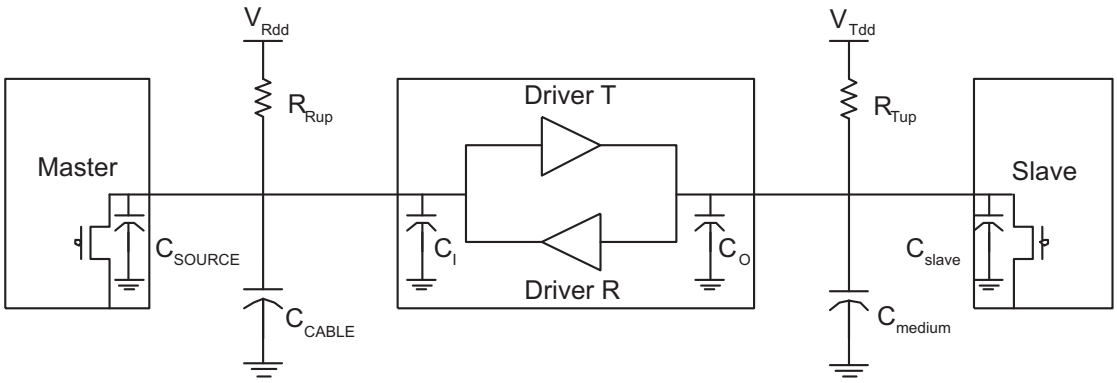


Figure 34. Typical Application

Figure 35 illustrates the waveforms seen on the R-side I^2C-bus when the master writes to the slave through the I^2C repeater circuit of the TMDS461. This looks like a normal I^2C transmission, and the turnon and turnoff of the acknowledge signals are slightly delayed.

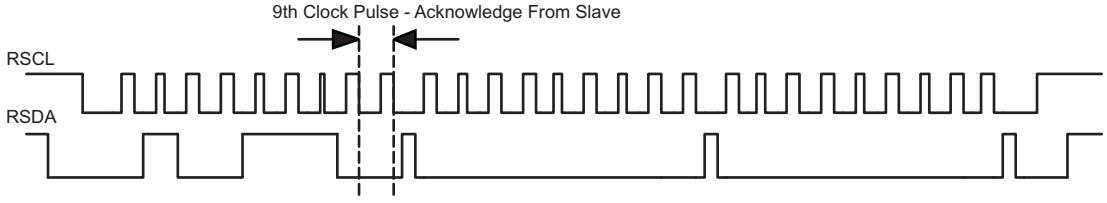


Figure 35. Bus-R Waveform

Figure 36 illustrates the waveforms seen on the T-side I^2C-bus under the same operation as in Figure 35. On the T-side of the I^2C repeater, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the driver T. After the 8th clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in this example. At the end of the acknowledge, the slave device releases and the bus level rises back to the V_{OL} set by the driver until the R-side rises above VCC/2, after which it continues to be high. It is important to note that any arbitration or clock-stretching events require that the low level on the T-side bus at the input of the TMDS461 I^2C repeater is below 0.4 V to be recognized by the device and then transmitted to the R-side I^2C bus.

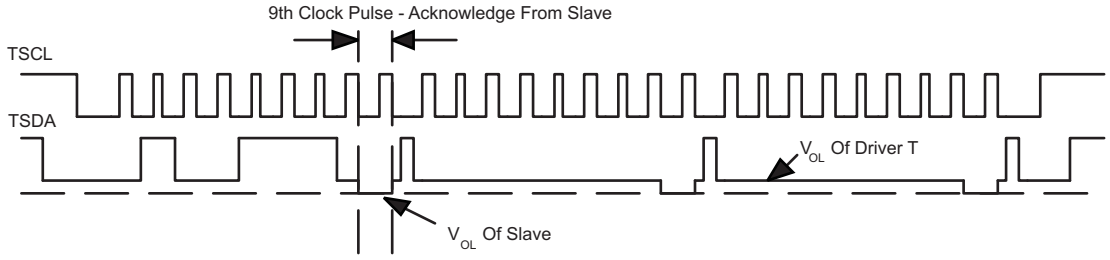


Figure 36. Bus T Waveform

I^2C Pullup Resistors

The pullup resistor value is determined by two requirements:

1. The maximum sink current of the I^2C buffer is 3 mA or slightly higher for an I^2C driver supporting standard-mode I^2C operation.

$$R_{up(min)} = V_{DD}/Isink \quad (1)$$

2. The maximum transition time, T, of an I^2C on the bus is set by an RC time constant, where R is the pullup resistor value and C is the total load capacitance. The parameter, k, can be calculated from Equation 3 by solving for t, the times at which certain voltage thresholds are reached. Different input threshold combinations introduce different values of t. Table 3 summarizes the possible values of k under different threshold combinations.

$$T = k \times RC \quad (2)$$

$$V(t) = V_{DD}(1 - e^{-t/RC}) \quad (3)$$

Table 3. Value of k for Different Input Threshold Voltages

V_{th-}|V_{th+}	0.7 V_{DD}	0.65 V_{DD}	0.6 V_{DD}	0.55 V_{DD}	0.5 V_{DD}	0.45 V_{DD}	0.4 V_{DD}	0.35 V_{DD}	0.3 V_{DD}
0.1 V_{DD}	1.0986	0.9445	0.8109	0.6931	0.5878	0.4925	0.4055	0.3254	0.2513
0.15 V_{DD}	1.0415	0.8873	0.7538	0.6360	0.5306	0.4353	0.3483	0.2683	0.1942
0.2 V_{DD}	0.9808	0.8267	0.6931	0.5754	0.4700	0.3747	0.2877	0.2076	0.1335
0.25 V_{DD}	0.9163	0.7621	0.6286	0.5108	0.4055	0.3102	0.2231	0.1431	0.0690
0.3 V_{DD}	0.8473	0.6931	0.5596	0.4418	0.3365	0.2412	0.1542	0.0741	—

From Equation 1, $R_{up(min)}$ = 5.5 V/3 mA = 1.83 kΩ to operate the bus under a 5-V pullup voltage and provide less than 3 mA when the I^2C device is driving the bus to a low state. If a higher sink current, for example 4 mA, is allowed, $R_{up(min)}$ can be as low as 1.375 kΩ.

Given a 5-V I^2C device with input low and high threshold voltages at 0.3 V_{dd} and 0.7 V_{dd}, respectively, the value of k is 0.8473 from Table 3. Taking into account the 1.83-kΩ pullup resistor, the maximum total load capacitance is $C_{(total-5V)}$ = 645 pF. $C_{cable(max)}$ should be restricted to be less than 545 pF if C_{source} and C_I can be as high as 50 pF. Here the C_I is treated as C_{sink}, the load capacitance of a sink device.

Fixing the maximum transition time from Table 3, T = 1 µs, and using the k values from Table 3, the recommended maximum total resistance of the pullup resistors on an I^2C bus can be calculated for different system setups.

To support the maximum load capacitance specified in the HDMI spec, $C_{cable(max)}$ = 700 pF/C_{source} = 50 pF/C_I = 50 pF, $R_{(max)}$ can be calculated as shown in Table 4.

Table 4. Pullup Resistor for Different Threshold Voltages and 800-pF Load

V_{th-}/V_{th+}	0.7 V_{DD}	0.65 V_{DD}	0.6 V_{DD}	0.55 V_{DD}	0.5 V_{DD}	0.45 V_{DD}	0.4 V_{DD}	0.35 V_{DD}	0.3 V_{DD}	UNIT
0.1 V_{DD}	1.14	1.32	1.54	1.80	2.13	2.54	3.08	3.84	4.97	kΩ
0.15 V_{DD}	1.20	1.41	1.66	1.97	2.36	2.87	3.59	4.66	6.44	kΩ
0.2 V_{DD}	1.27	1.51	1.80	2.17	2.66	3.34	4.35	6.02	9.36	kΩ
0.25 V_{DD}	1.36	1.64	1.99	2.45	3.08	4.03	5.60	8.74	18.12	kΩ
0.3 V_{DD}	1.48	1.80	2.23	2.83	3.72	5.18	8.11	16.87	—	kΩ

Or, limiting the maximum load capacitance of each cable to 400 pF to accommodate with I^2C spec version 2.1. $C_{cable(max)}$ = 400 pF/C_{source} = 50 pF/C_I = 50 pF, the maximum values of $R_{(max)}$ are calculated as shown in Table 5.

Table 5. Pullup Resistor Upon Different Threshold Voltages and 500-pF Loads

V_{th-}/V_{th+}	0.7 V_{DD}	0.65 V_{DD}	0.6 V_{DD}	0.55 V_{DD}	0.5 V_{DD}	0.45 V_{DD}	0.4 V_{DD}	0.35 V_{DD}	0.3 V_{DD}	UNIT
0.1 V_{DD}	1.82	2.12	2.47	2.89	3.40	4.06	4.93	6.15	7.96	kΩ
0.15 V_{DD}	1.92	2.25	2.65	3.14	3.77	4.59	5.74	7.46	10.30	kΩ
0.2 V_{DD}	2.04	2.42	2.89	3.48	4.26	5.34	6.95	9.63	14.98	kΩ
0.25 V_{DD}	2.18	2.62	3.18	3.92	4.93	6.45	8.96	13.98	28.99	kΩ
0.3 V_{DD}	2.36	2.89	3.57	4.53	5.94	8.29	12.97	26.99	—	kΩ

Obviously, to accommodate the 3-mA drive current specification, a narrower threshold voltage range is required to support a maximum 800-pF load capacitance for a standard-mode I^2C bus.

When the input low- and high-level threshold voltages, V_{th-} and V_{th+}, are 0.7 V and 1.9 V, respectively, which is 0.15 V_{DD} and 0.4 V_{DD}, approximately. With V_{DD} = 5 V from Table 4, the maximum pullup resistor is 3.59 kΩ. The allowable pullup resistor is in the range of 1.83 kΩ and 3.59 kΩ.

Layout Considerations

The high-speed differential TMDS inputs are the most critical paths for the TMDS461. There are several considerations to minimize discontinuities on these transmission lines between the connectors and the device:

- Maintain 100-Ω differential transmission line impedance into and out of the TMDS461.
- Keep an uninterrupted ground plane beneath the high-speed I/Os.
- Keep the ground-path vias to the device as close as possible to allow the shortest return current path.
- Keep the trace lengths of the TMDS signals between connector and device as short as possible.

Using the TMDS461 in Systems with CEC Link Requirements

The TMDS461 supports a DTV with up to four HDMI inputs when used in conjunction with a signal-port HDMI receiver. The CEC is an optional feature of the HDMI interface for centralizing and simplifying user control instructions from multiple audio/video products in an interconnected system, even when all the audio/video products are from different manufacturers. This feature minimizes the number of remote controls in a system, as well as reducing the number of times buttons must be pressed.

In TMDS461, the HPD[x] of non-selected port follows the 5V_PWR[x] in normal operation. In Low Power mode ($\overline{LP}$ mode) or if the TMDS461 is powered off, the HPD[x] will still follow 5V_PWR[x] from source, thus if it is desired for the source to read the E-EDID memory in $\overline{LP}$ mode, a possible configuration in Figure 37 is recommended.

A DTV Supporting an Active CEC Link

In Figure 37, the CEC PHY and CEC LOGIC functions are included. The DTV can initiate and/or react to CEC signals from its remote control or other audio/video products on the same CEC bus. All sources must have their own CEC physical address to support the full functionality of the CEC link.

A source reads its CEC physical address stored its E-EDID memory after receiving a logic-high from the HPD feedback. When HPD is high, the sink-assigned CEC physical address should be maintained. Otherwise, when HPD is low, the source sets CEC physical address value to (F.F.F.F).

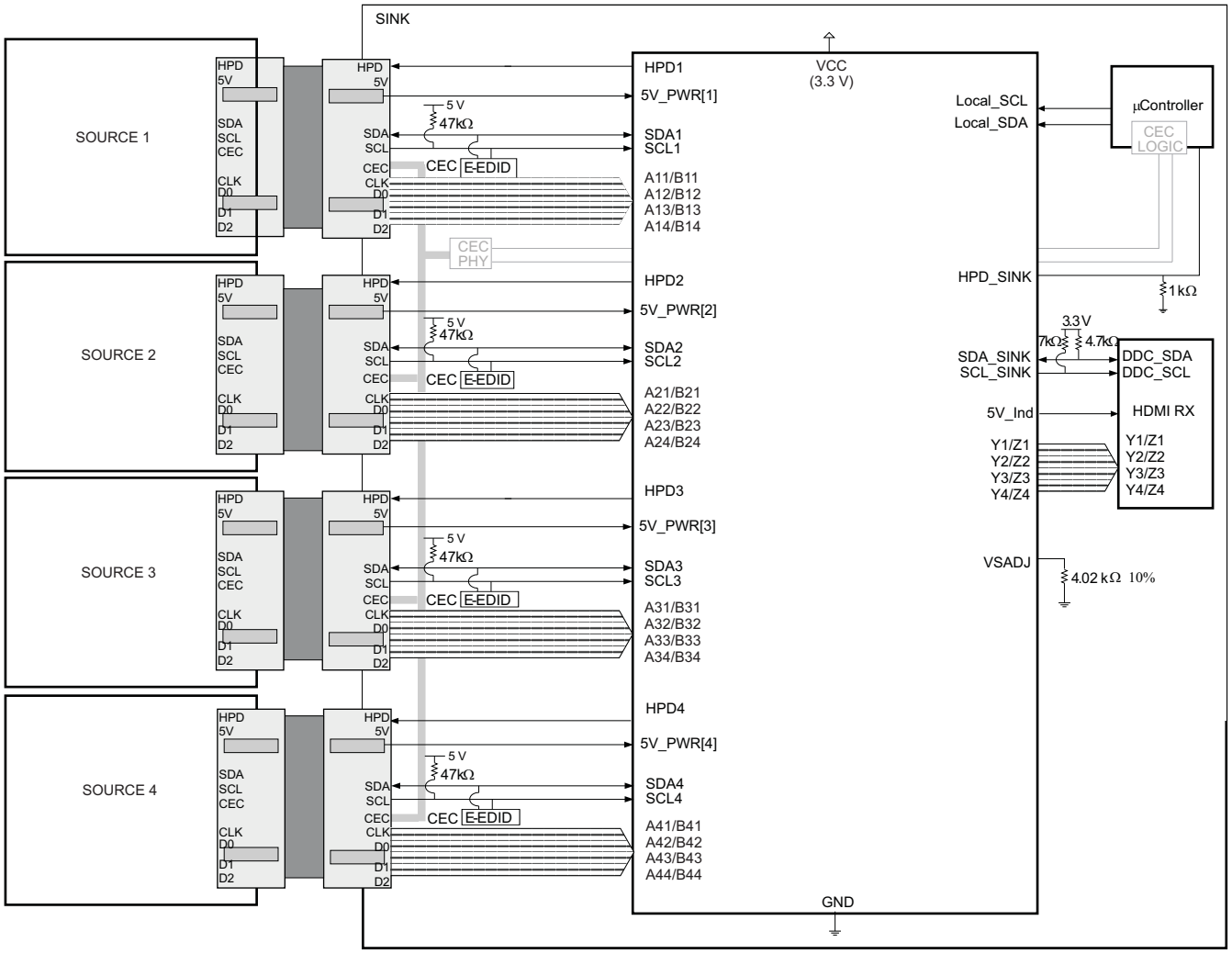


Figure 37. Four-Port HDMI-Enabled DTV With TMDS461 – CEC Commands Active

I²C INTERFACE NOTES

The I²C interface is used to access the internal registers of the TMDS461. I²C is a two-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through open-drain I/O pins, SDA and SCL. A master device, usually a micro controller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addressing information. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device. The TMDS461 works as a slave and supports standard-mode transfer (100 kbps).

The basic I^{2}C start and stop access cycles are shown in Figure 38.

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

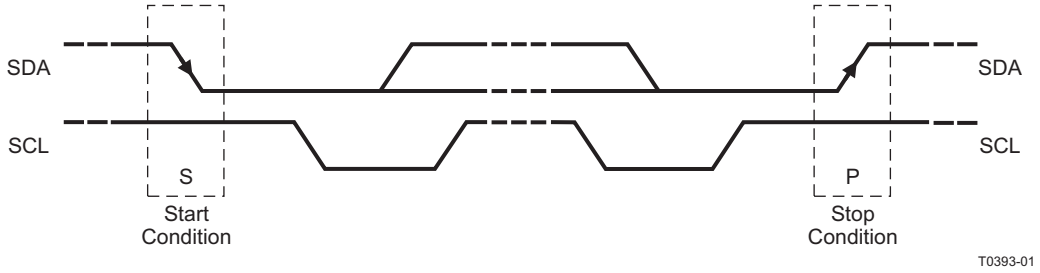


Figure 38. I^{2}C Start and Stop Conditions

GENERAL I^{2}C PROTOCOL

- The *master* initiates data transfer by generating a *start condition*. The *start condition* is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 38. All I^{2}C-compatible devices should recognize a *start condition*.
- The master then generates the SCL pulses and transmits the 7-bit address and the *read/write direction bit* R/W on the SDA line. During all transmissions, the master ensures that data is *valid*. A *valid data* condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 39). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see Figure 40) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.
- The master generates further SCL cycles to either *transmit* data to the slave (R/W bit 0) or *receive* data from the slave (R/W bit 1). In either case, the *receiver* must acknowledge the data sent by the *transmitter*. So an acknowledge signal can be generated either by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (See Figure 42 through Figure 45).
- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see Figure 38). This releases the bus and stops the communication link with the addressed slave. All I^{2}C compatible devices must recognize the stop condition. Upon the receipt of a *stop condition*, all devices know that the bus is released, and they wait for a *start condition* followed by a matching address.

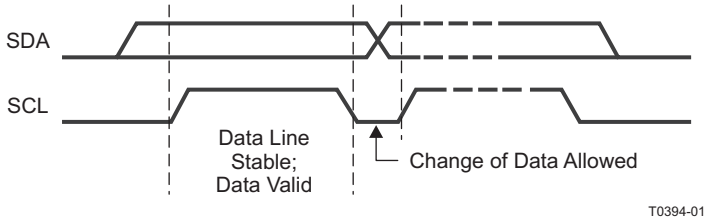


Figure 39. I^{2}C Bit Transfer

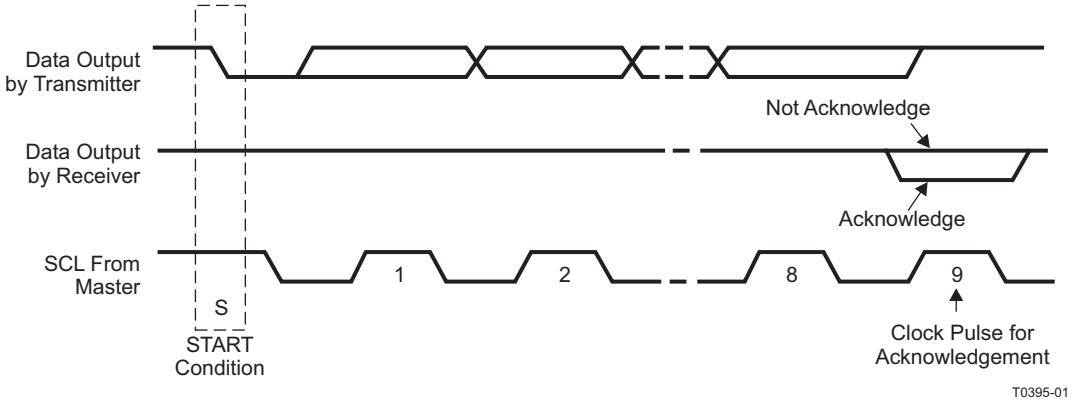


Figure 40. I²C Acknowledge

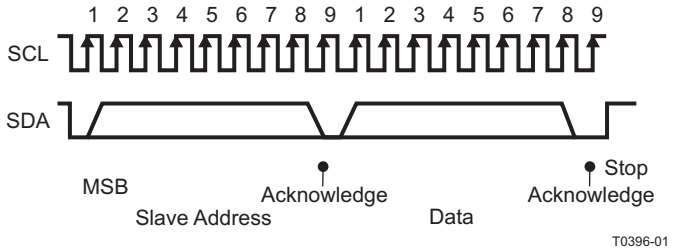


Figure 41. I²C Address, Data Cycle(s), and Stop

During a write cycle, the transmitting device must not drive the SDA signal line during the acknowledge cycle so that the receiving device may drive the SDA signal low. After each byte transfer following the address byte, the receiving device pulls the SDA line low for one SCL clock cycle. A stop condition is initiated by the transmitting device after the last byte is transferred. An example of a write cycle can be found in Figure 42 and Figure 43. Note that the TMDS461 allows multiple write transfers to occur. See the *Example – Writing to the TMDS461* section for more information.

During a read cycle, the slave receiver acknowledges the initial address byte if it decodes the address as its address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not-acknowledge ($\overline{A}$) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop (P) condition. This sequence terminates a read cycle as shown in Figure 44 and Figure 45. See the *Example – Reading from the TMDS461* section for more information.

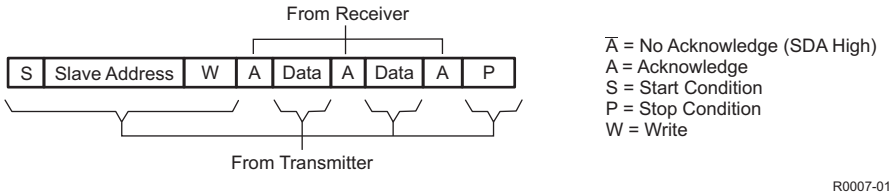


Figure 42. I²C Write Cycle

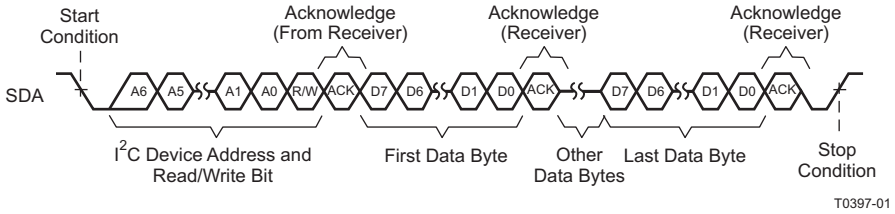


Figure 43. Multiple-Byte Write Transfer

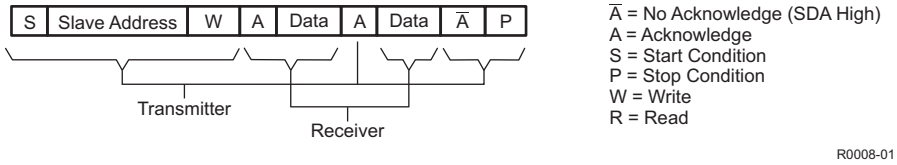


Figure 44. I²C Read Cycle

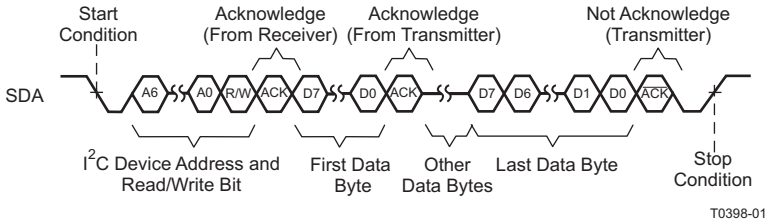


Figure 45. Multiple-Byte Read Transfer

Slave Address

Both SDA and SCL must be connected to a positive supply voltage via a pullup resistor. These resistors should comply with the I²C specification that ranges from 2 kΩ to 19 kΩ. When the bus is free, both lines are high. The address byte is the first byte received following the START condition from the master device. The 7-bit address is factory preset to 0101100 or 0101101 based on the status of the Local_Addr pin . Table 6 lists the calls to which the TMDS461 responds.

Table 6. TMDS461 Slave Address

FIXED ADDRESS							READ/WRITE BIT
Bit 7 (MSB)	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (R/W)**
0	1	0	1	1	0	0 (Local_Addr pin =LOW) 1 (Local_Addr pin = HIGH)	1/0

EXAMPLE – WRITING TO THE TMDS461

The proper way to write to the TMDS461 is illustrated as follows:

An I²C master initiates a write operation to the TMDS461 by generating a start condition (S) followed by the TMDS461 I²C address (as shown following, in MSB-first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the TMDS461, the master presents the subaddress (sink port) to be written, consisting of one byte of data, MSB-first. The TMDS461 acknowledges the byte after completion of the transfer. Finally, the master presents the data to be written to the register (sink port), and the TMDS461 acknowledges the byte. The master can continue presenting data to be written after TMDS461 acknowledges the previous byte (steps 6, 7). After the last byte to be written has been acknowledged by TMDS461, the I²C master then terminates the write operation by generating a stop condition (P).

Step 1	0
I²C start (master)	S

Step 2	7	6	5	4	3	2	1	0
I²C general address (master)	0	1	0	1	1	0	0 (Local_Addr pin =LOW) 1 (Local_Addr pin = HIGH)	0

Step 3	8
I²C acknowledge (slave)	A

Step 4	7	6	5	4	3	2	1	0
I²C write sink logic address (master)	0	0	0	0	Addr	Addr	Addr	Addr

Step 5	8
I²C acknowledge (slave)	A

Step 6	7	6	5	4	3	2	1	0
I²C write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

Data is the register address or register data to be written

Step 7	8
I²C acknowledge (slave)	A

Step 8	0
I²C stop (master)	P

An example of the proper bit control for selecting port 2 is:

Step 4: 0000 0011

Step 6: 00101000

EXAMPLE – READING FROM THE TMDS461

The read operation consists of two phases. The first phase is the address phase. In this phase, an I²C master initiates a write operation to the TMDS461 by generating a start condition (S) followed by the TMDS461 I²C address, in MSB-first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledges from the TMDS461, the master presents the subaddress of the register to be read. After the cycle is acknowledged (A), the master may optionally terminate the cycle by generating a stop condition (P).

The second phase is the data phase. In this phase, an I²C master initiates a read operation to the TMDS461 by generating a start condition followed by the TMDS461 I²C address (as shown following for a read operation), in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the TMDS461, the I²C master receives one byte of data from the TMDS461. The master can continue receiving data byes by issuing an acknowledge after each byte read (steps 10, 11). After the last data byte has been transferred from the TMDS461 to the master, the master generates a not-acknowledge followed by a stop.

TMDS461 Read Phase 1

Step 1	0
I²C start (master)	S

Step 2	7	6	5	4	3	2	1	0
I²C general address (master)	0	1	0	1	1	0	0 (Local_Addr pin =LOW) 1 (Local_Addr pin = HIGH)	0

Step 3	8
I²C acknowledge (slave)	A

Step 4	7	6	5	4	3	2	1	0
I^2C write sink logic address (master)	0	0	0	0	Addr	Addr	Addr	Addr

Where Addr is determined by the values shown in Table 6.

Step 5	8
I^2C acknowledge (slave)	A

Step 6	0
I^2C stop (master)	P

Step 6 is optional.

TMDS461 Read Phase 2

Step 7	0
I^2C start (master)	S

Step 8	7	6	5	4	3	2	1	0
I^2C general address (master)	0	1	0	1	1	0	0 (Local_Addr pin =LOW) 1 (Local_Addr pin = HIGH)	1

Step 9	8
I^2C acknowledge (slave)	A

Step 10	7	6	5	4	3	2	1	0
I^2C read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

Where data is determined by the logic values contained in the internal registers.

Step 11A	8
I^2C acknowledge (master)	A

If Step 11A is executed, go to step 10. If Step 11B is executed, go to Step 12.

Step 11B	8
I^2C not acknowledge (master)	$\overline{A}$

Step 12	0
I^2C stop (master)	P

Table 7. I²C Register 0x01 Lookup Table(1)

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7	0	RSVD	X	Reserved
6:5	Bit 6	Bit 5		Port Select Status Indicator
	0	0	X	Indicates Port 1 is selected as the active port, all other ports are disabled
	0	1		Indicates Port 2 is selected as the active port, all other ports are disabled
	1	0		Indicates Port 3 is selected as the active port, all other ports are disabled
	1	1		Indicates Port 4 is selected as the active port, all other ports are disabled
4	1	Valid TMDS Clock Detected		A valid TMDS clock signal is detected on the selected input port. If clock-detect circuit is disabled in I²C register 0x03, then bit 4 of I²C register 0x01 will always be 1.
	0	No Valid TMDS Clock Detected	X	The selected port does not have a valid TMDS clock signal
3	1	Port 4 5V_PWR Detected		5V_PWR is detected as HIGH on Port 4
	0	Port 4 5V_PWR not Detected	X	5V_PWR is detected as LOW on Port 4
2	1	Port 3 5V_PWR Detected		5V_PWR is detected as HIGH on Port 3
	0	Port 3 5V_PWR not Detected	X	5V_PWR is detected as LOW on Port 3
1	1	Port 2 5V_PWR Detected		5V_PWR is detected as HIGH on Port 2
	0	Port 2 5V_PWR not Detected	X	5V_PWR is detected as LOW on Port 2
0	1	Port 1 5V_PWR Detected		5V_PWR is detected as HIGH on Port 1
	0	Port 1 5V_PWR not Detected	X	5V_PWR is detected as LOW on Port 1

(1) I²C register 0x01 is Read Only. This register is supposed to be read by the sink micro-controller on IRQ interrupt (IRQ goes high). The register values get updated in real time. IRQ will be reset (IRQ goes low) once the sink micro controller has completed reading this register.

Table 8. I²C Register 0x02 Lookup Table(1)

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7:6	Bit 7	Bit 6		Power Mode
	1	0		Device enters low power mode ($\overline{LP}$ mode)
	1	1		Device enters low power mode ($\overline{LP}$ mode)
	0	1		Device is in Standby mode
	0	0	X	Device is in normal power mode
5	1	Automatic Port Select On		Port Selection will be automatic based on state of 5V_PWR[1:4] as indicated by I²C register 0x01:bits[3:0] and priority bit which is I²C register 0x02:bits [4:3]
	0	Automatic Port Select Off	X	Port Selection based on I²C register 0x03:bits [6:5]

(1) During switching of modes between Auto-select on/off, it is required that the sink micro controller reads the register 0x01 to determine which port is selected. Register 0x02 is Read/Write.

Table 8. I²C Register 0x02 Lookup Table (continued)

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
4:3	Bit 4	Bit 3		Priority Select
	0	0	X	Port 1 is the priority port
	0	1		Port 2 is the priority port
	1	0		Port 3 is the priority port
	1	1		Port 4 is the priority port
2	0	Reserved	X	Reserved (Do not write a 1 to this bit)
1:0	Bit 1	Bit 0		Output Edge Rate Control
	1	1		Fastest TMDS output rise and fall time setting + 120 ps approximately (slowest rise and fall time setting)
	1	0		Fastest TMDS output rise and fall time setting + 100 ps approximately
	0	1		Fastest TMDS output rise and fall time setting + 50 ps approximately
	0	0	X	Fastest TMDS output rise and fall time setting

Table 9. I²C Register 0x03 Lookup Table(1)

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7	0	Clock Detect Enabled	X	Clock Detect Circuit Enabled. It is recommended that TMDS461 is used in this default mode in the normal operation, where clock-detect circuit is enabled. The terminations on the TMDS input data lines are connected only when valid TMDS clock is detected on the selected port.
	1	Clock Detect Disabled		Clock Detect Circuit Disabled. For HDMI compliance testing (TMDS Termination Voltage Test), clock-detect feature should be disabled. In this mode the terminations on the TMDS input data lines are always connected when the port is selected.
6:5	Bit 6	Bit 5		Port select I²C mode
	0	0	X	Port 1 is selected as the active port, all other ports disabled.
	0	1		Port 2 is selected as the active port, all other ports disabled.
	1	0		Port 3 is selected as the active port, all other ports disabled.
	1	1		Port 4 is selected as the active port, all other ports disabled.
4:3	Bit 4	Bit 3		OVS Control
	0	0		DDC sink side VOL and VIL offset range 2: $V_{IL2\ (max)}$: 0.4V, $V_{OL2\ (max)}$: 0.6V
	0	1	X	DDC sink side VOL and VIL offset range 3: $V_{IL3\ (max)}$: 0.3V, $V_{OL3\ (max)}$: 0.5V
	1	1		DDC sink side VOL and VIL offset range 1: $V_{IL1\ (max)}$: 0.4V, $V_{OL1\ (max)}$: 0.7V
2:0	0	RSVD	X	Reserved

(1) Register 0x03 is Read/Write.

Table 10. I²C Register 0x04 Lookup Table(1)

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7:0	—	RSVD	X	Reserved. Read-only, value is indeterministic.

(1) Register x04 is TI internal usage only.

Table 11. I²C Register 0x05 Lookup Table(1)

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7:0	—	RSVD	X	Reserved. Read-only, value is indeterministic.

(1) Register x05 is TI internal usage only.

Table 12. I²C Register 0x06 Lookup Table(1)

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7:0	—	RSVD	X	Reserved. Read-only, value is indeterministic.

(1) Register x06 is TI internal usage only.

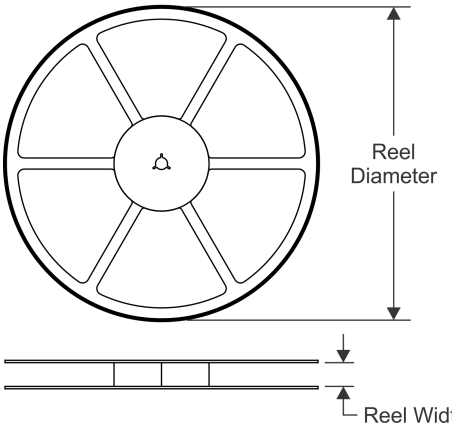
Table 13. I²C Register 0x07 Lookup Table(1)

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7:6	0	RSVD	X	Reserved
5	1	Port Select Changed		The selected port has changed since reading 0x01
	0	Port Select Unchanged	X	The selected port has not changed since reading 0x01
4	1	Clock-Detect Changed		The selected port's clock detect status has changed since reading 0x01
	0	Clock-Detect Unchanged	X	The selected port's clock detect status has not changed since reading 0x01
3	1	Port 4 5V_PWR Changed		5V_PWR on Port 4 has changed since reading 0x01
	0	Port 4 5V_PWR Unchanged	X	5V_PWR on Port 4 has not changed since reading 0x01
2	1	Port 3 5V_PWR Changed		5V_PWR on Port 3 has changed since reading 0x01
	0	Port 3 5V_PWR Unchanged	X	5V_PWR on Port 3 has not changed since reading 0x01
1	1	Port 2 5V_PWR Changed		5V_PWR on Port 2 has changed since reading 0x01
	0	Port 2 5V_PWR Unchanged	X	5V_PWR on Port 2 has not changed since reading 0x01
0	1	Port 1 5V_PWR Changed		5V_PWR on Port 1 has changed since reading 0x01
	0	Port 1 5V_PWR Unchanged	X	5V_PWR on Port 1 has not changed since reading 0x01

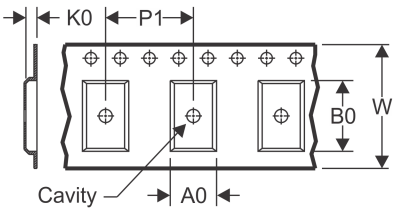
(1) I²C register 0x07 is Read Only. The register values get latched whenever a system-level interrupt occurs (IRQ goes high); and, the register values are cleared when the IRQ gets cleared upon reading register 0x01. This I²C register can be used for debug purposes, if needed. If register 0x01 is not read, then the latched values in register x07, will keep on updating based on any system level event.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

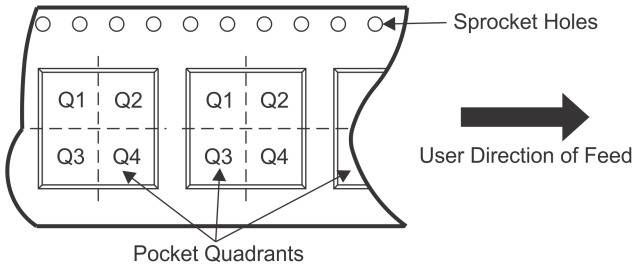


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

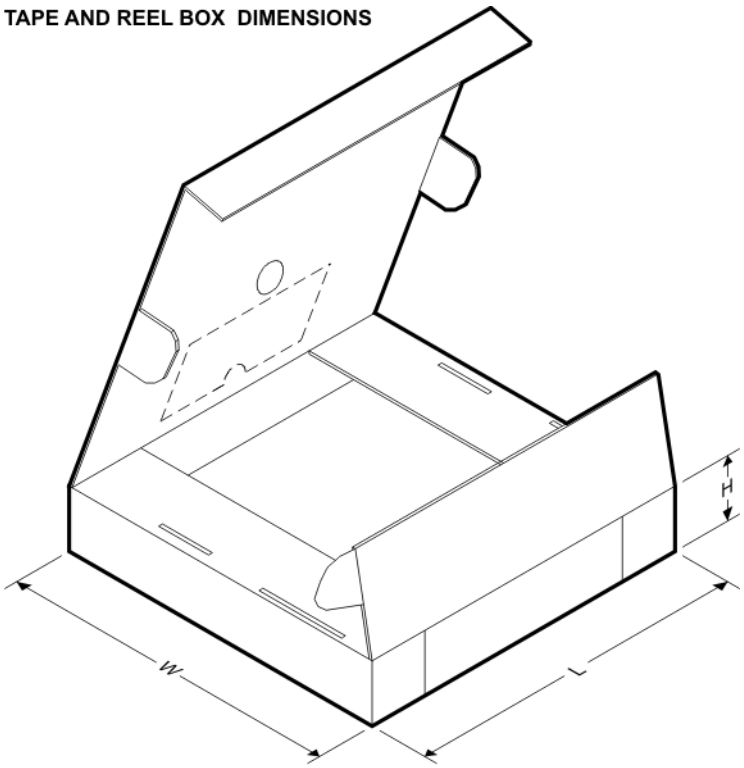
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMDS461PZTR	TQFP	PZT	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMDS461PZTR	TQFP	PZT	100	1000	350.0	350.0	43.0

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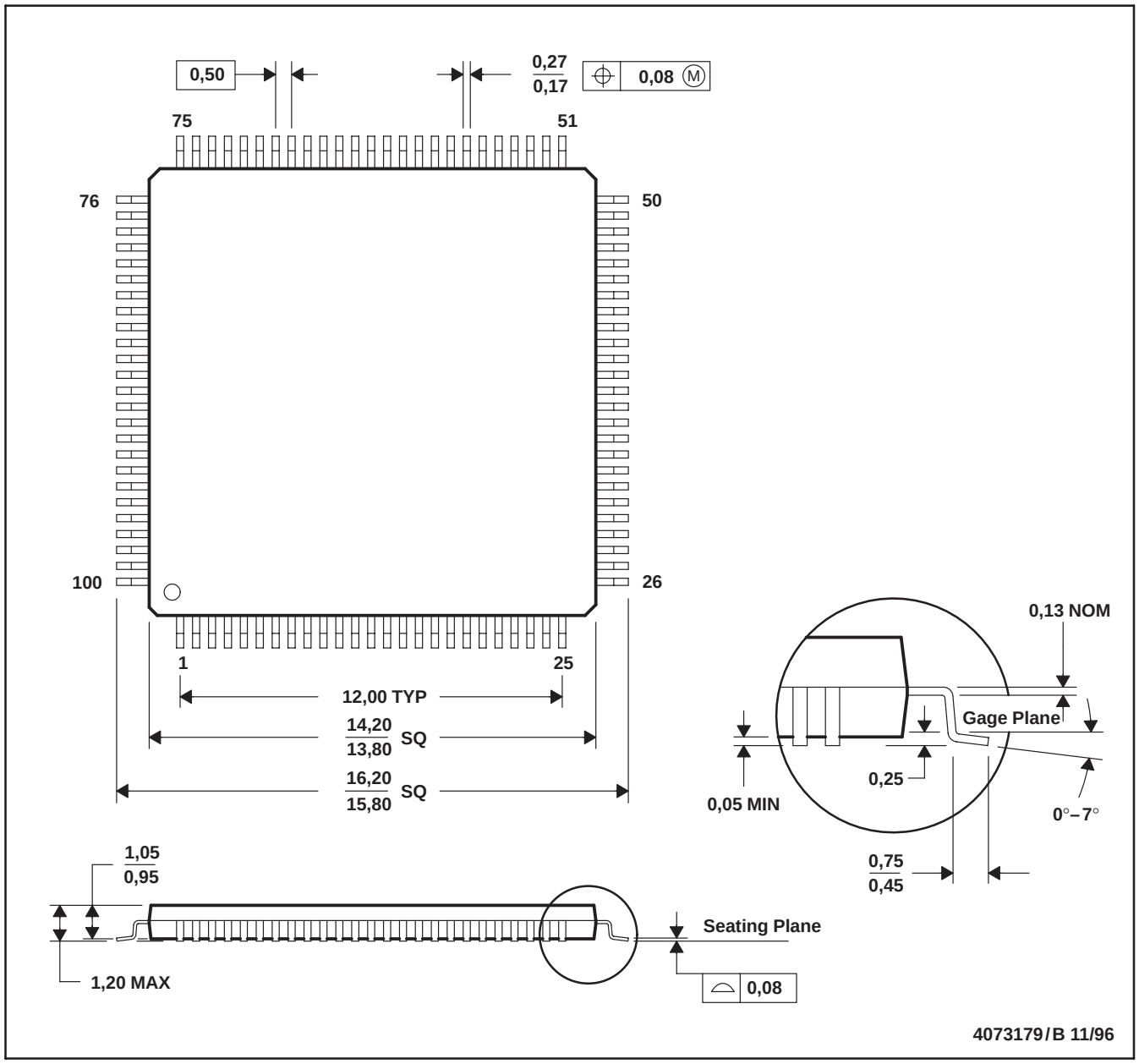
PZT (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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