THE DATASHEET OF

SN74LVCH16652ADGGR

SN74LVCH16652A 16-Bit Bus Transceiver and Register with 3-State Outputs

1 Features

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.3 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial-Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pull-up or Pull-down Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1500-V Charged-Device Model

2 Applications

- Servers
- PCs, Notebooks
- Network switches
- Telecom Infrastructure
- I/O Expanders

3 Description

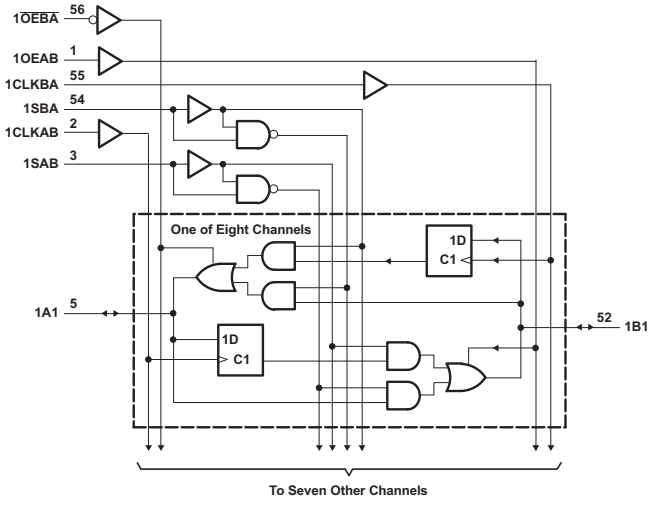
This 16-bit bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

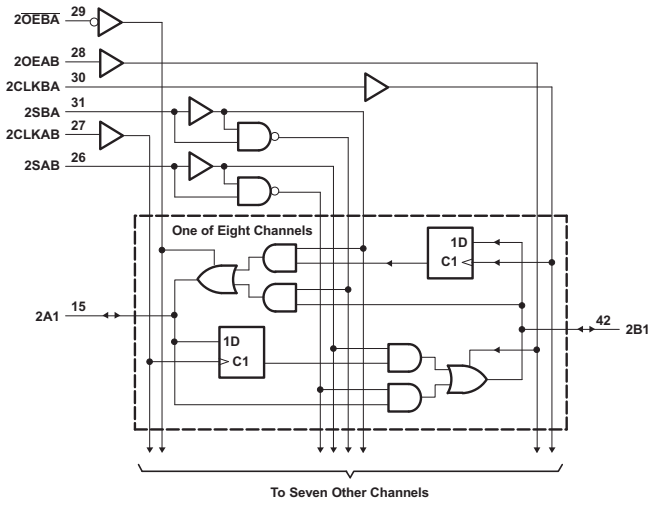
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVCH16652A	SSOP (56)	18.40 mm x 7.50 mm
	TSSOP (56)	14.00 mm x 6.10 mm
	TVSOP (56)	11.30 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic





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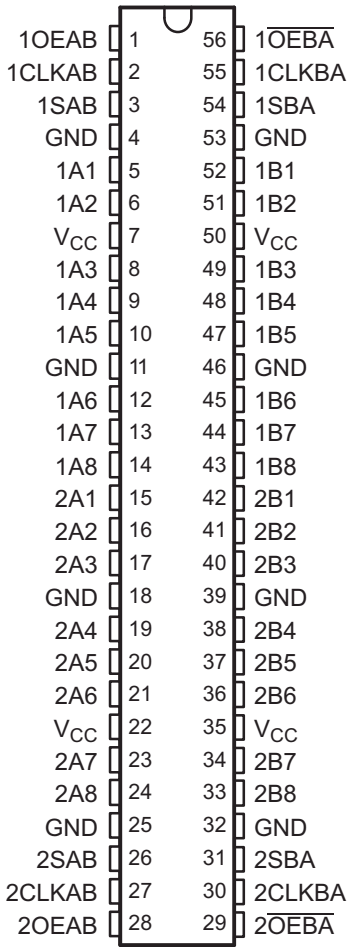
5 Revision History

Changes from Revision I (March 2005) to Revision J **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1
- Changed MAX operating temperature in *Recommended Operating Conditions* table. ... 6

6 Pin Configuration and Functions

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	1OEAB	I	1OEAB Input. Active-high enable for A-to-B directional data.
2	1CLKAB	I	1CLKAB Input. Clock input for D flip-flop from A to B.
3	1SAB	I	1SAB Input. Data select from A to B: A high level selects stored data and a low-level selects real-time data.
4	GND	—	GND
5	1A1	I/O	1A1 Input/Output
6	1A2	I/O	1A2 Input/Output
7	V_{CC}	—	Power Pin
8	1A3	I/O	1A3 Input/Output
9	1A4	I/O	1A4 Input/Output
10	1A5	I/O	1A5 Input/Output
11	GND	—	Ground Pin
12	1A6	I/O	1A6 Input/Output
13	1A7	I/O	1A7 Input/Output
14	1A8	I/O	1A8 Input/Output

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
15	2A1	I/O	2A1 Input/Output
16	2A2	I/O	2A2 Input/Output
17	2A3	I/O	2A3 Input/Output
18	GND	—	Ground Pin
19	2A4	I/O	2A4 Input/Output
20	2A5	I/O	2A5 Input/Output
21	2A6	I/O	2A6 Input/Output
22	V_{CC}	—	Power Pin
23	2A7	I/O	2A7 Input/Output
24	2A8	I/O	2A8 Input/Output
25	GND	—	Ground Pin
26	2SAB	I	2SAB Input. Data select from A to B: A high level selects stored data and a low-level selects real-time data.
27	2CLKAB	I	2CLKAB Input. Clock input for D flip-flop from A to B.
28	2OEAB	I	2OEAB Input. Active-high enable for A-to-B directional data.
29	$2\overline{OEBA}$	I	$2\overline{OEBA}$ Input. Active-low enable for B-to-A directional data.
30	2CLKBA	I	2CLKBA Input. Clock input for D flip-flop from B to A.
31	2SBA	I	2SBA Input. Data select from B to A: A high level selects stored data and a low-level selects real-time data.
32	GND	—	Ground Pin
33	2B8	I/O	2B8 Input/Output
34	2B7	I/O	2B7 Input/Output
35	V_{CC}	—	Power Pin
36	2B6	I/O	2B6 Input/Output
37	2B5	I/O	2B5 Input/Output
38	2B4	I/O	2B4 Input/Output
39	GND	-	Ground Pin
40	2B3	I/O	2B3 Input/Output
41	2B2	I/O	2B2 Input/Output
42	2B1	—	2B1 Input/Output
43	1B8	I/O	1B8 Input/Output
44	1B7	I/O	1B7 Input/Output
45	1B6	I/O	1B6 Input/Output
46	GND	—	Ground Pin
47	1B5	I/O	1B5 Input/Output
48	1B4	I/O	1B4 Input/Output
49	1B3	I/O	1B3 Input/Output
50	V_{CC}	—	Power Pin
51	1B2	I/O	1B2 Input/Output
52	1B1	I/O	1B1 Input/Output
53	GND	—	Ground Pin
54	1SBA	i	1SBA Input. Data select from B to A: A high-level selects stored data and a low-level selects real-time data.
55	1CLKBA	I	1CLKBA Input. Clock input for D flip-flop from B to A.
56	$1\overline{OEBA}$	I	$1\overline{OEBA}$ Input. Active-low enable for B-to-A directional data.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–40	125	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

7.4 Thermal Information

THERMAL METRIC(1)		SN74LVCH16652A			UNIT
		DGG	DGV	DL	
		56 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	72.8	53.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.9	27.5	18.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	29.4	38.3	25.8	
ψ_{JT}	Junction-to-top characterization parameter	0.8	1.7	1.4	
ψ_{JB}	Junction-to-board characterization parameter	29.1	37.8	25.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
					MIN	TYP(1)	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –100 µA		1.65 V to 3.6 V	V_{CC} – 0.2			V_{CC} – 0.2		V_{CC} – 0.2		V
		I_{OH} = –4 mA		1.65 V	1.2			1.2		1.2		
		I_{OH} = –8 mA		2.3 V	1.7			1.7		1.7		
		I_{OH} = –12 mA		2.7 V	2.2			2.2		2.2		
				3 V	2.4			2.4		2.4		
		I_{OH} = –24 mA		3 V	2.2			2.2		2.2		
V_{OL}		I_{OL} = 100 µA		1.65 V to 3.6 V			0.2		0.2		0.2	V
		I_{OL} = 4 mA		1.65 V			0.45		0.45		0.45	
		I_{OL} = 8 mA		2.3 V			0.7		0.7		0.7	
		I_{OL} = 12 mA		2.7 V			0.4		0.4		0.4	
		I_{OL} = 24 mA		3 V			0.55		0.55		0.55	
I_I	Control inputs	V_I = 0 to 5.5 V		3.6 V			±5		±5		±5	µA
$I_{I(hold)}$	A or B ports	V_I = 0.58 V		1.65 V	See(2)			See(2)		See(2)		µA
		V_I = 1.07 V			See(2)			See(2)		See(2)		
		V_I = 0.7 V		2.3 V	45			45		45		
		V_I = 1.7 V			–45			–45		–45		
		V_I = 0.8 V		3 V	75			75		75		
		V_I = 2 V			–75			–75		–75		
		V_I = 0 to 3.6 V(3)		3.6 V			±500		±500		±500	
I_{off}		V_I or V_O = 5.5 V		0			±10		±10		±10	µA
I_{OZ} (4)		V_O = 0 V or (V_{CC} to 5.5 V)		2.3 V to 3.6 V			±5		±5		±5	µA
I_{CC}		V_I = V_{CC} or GND	I_O = 0	3.6 V			20		20		20	µA
		3.6 V ≤ V_I ≤ 5.5 V(5)					20		20		20	
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500		500		500	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		5						pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		8						pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This information was not available at the time of publication.
(3) This is the bus-hold maximum dynamic current required to switch the input from one state to another.
(4) For the total leakage current in an I/O port, please consult the $I_{I(hold)}$ specification for the input voltage condition 0 V < V_I < V_{CC}, and the I_{OZ} specification for the input voltage conditions V_I = 0 V or V_I = V_{CC} to 5.5 V. The bus-hold current, at input voltage greater than V_{CC}, is negligible.
(5) This applies in the disabled state only.

7.6 Timing Requirements, 40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

		V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		120		150		150		150	MHz
t_w	Pulse duration, CLK high or low	See (1)		See (1)		3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	5		3.8		3.4		3		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0.7		0.5		0		0.2		ns

(1) This information was not available at the time of publication.

7.7 Timing Requirements, 40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

		V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		120		150		150		150	MHz
t_w	Pulse duration, CLK high or low	See (1)		See (1)		3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	5.3		3.5		3.4		3		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0.8		0.5		0		0.2		ns

(1) This information was not available at the time of publication.

7.8 Switching Characteristics, 40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}				120		150		150		150	MHz
t_{pd}	A or B	B or A	9.1	11.8	6.9	8.6	6.4		1.4	6.3	ns
	CLKAB or CLKBA	A or B		10.4		7.3	7.3		2.4	6.4	
	SAB or SBA	B or A		12.5		9.6	8.8		1.9	7.4	
t_{en}	$\overline{OE}$ or OE	A or B		23.4		9.3	6.6		1.6	6.3	ns
t_{dis}	$\overline{OE}$ or OE	A or B		15.9		8.2	6.6		1.2	6.2	ns

7.9 Switching Characteristics, 40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}				120		150		150		150	MHz
t_{pd}	A or B	B or A		10		7.6	6.4		1.4	6.3	ns
	CLKAB or CLKBA	A or B		11.6		9.1	7.3		2.4	6.4	
	SAB or SBA	B or A		13.1		9.9	8.8		1.9	7.4	
t_{en}	$\overline{OE}$ or OE	A or B		2.1		8.5	6.6		1.6	6.3	ns
t_{dis}	$\overline{OE}$ or OE	A or B		18.6		8.2	6.6		1.2	6.2	ns

7.10 Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	f = 10 MHz	See (1)	See (1)	55	pF
		Outputs disabled		See (1)	See (1)	12	

(1) This information was not available at the time of publication.

7.11 Typical Characteristics

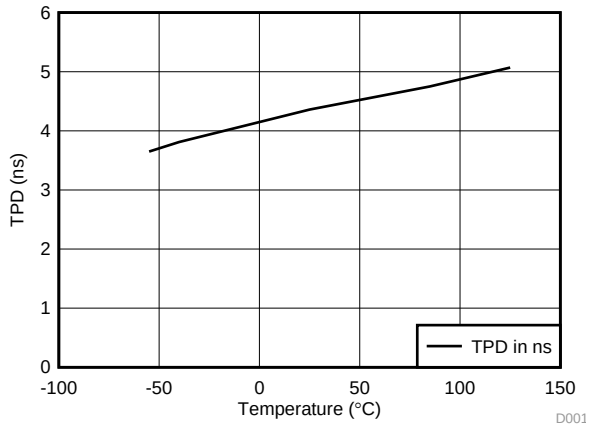


Figure 1. TPD vs Temperature

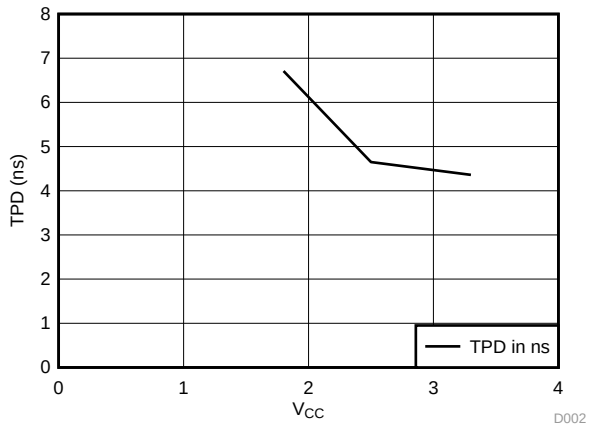
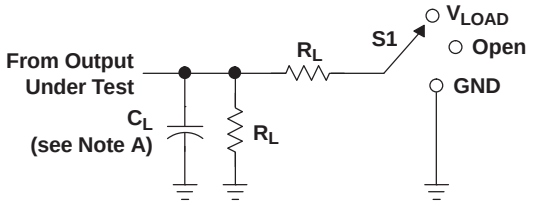


Figure 2. TPD vs V_{CC} at 25°C

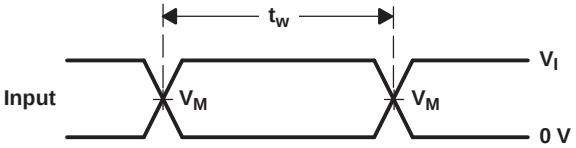
8 Parameter Measurement Information



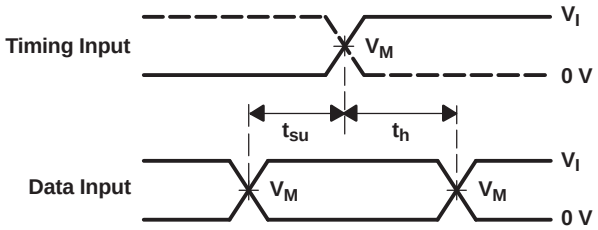
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

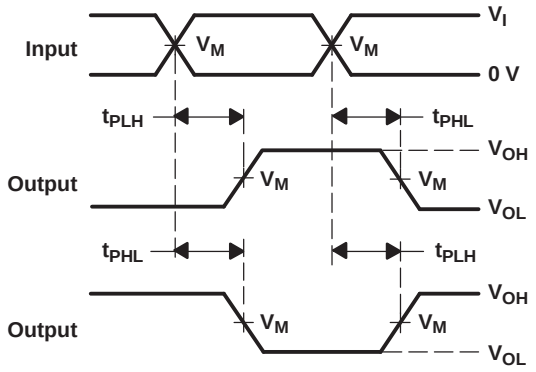
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



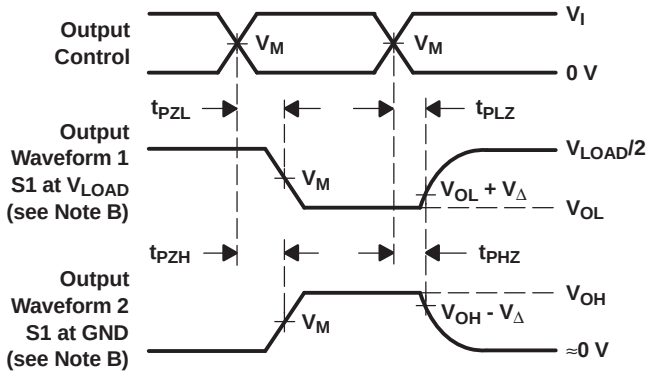
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

This 16-bit bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16652A device consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and $\overline{\text{OEBA}}$) inputs control the transceiver functions. Select-control (SAB and SBA) inputs select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 5 illustrates the four fundamental bus-management functions that can be performed with SN74LVCH16652A.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it also is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last level configuration.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pull-up resistor and OEAB should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by $\overline{\text{OE}}$ or DIR.

9.2 Functional Block Diagram

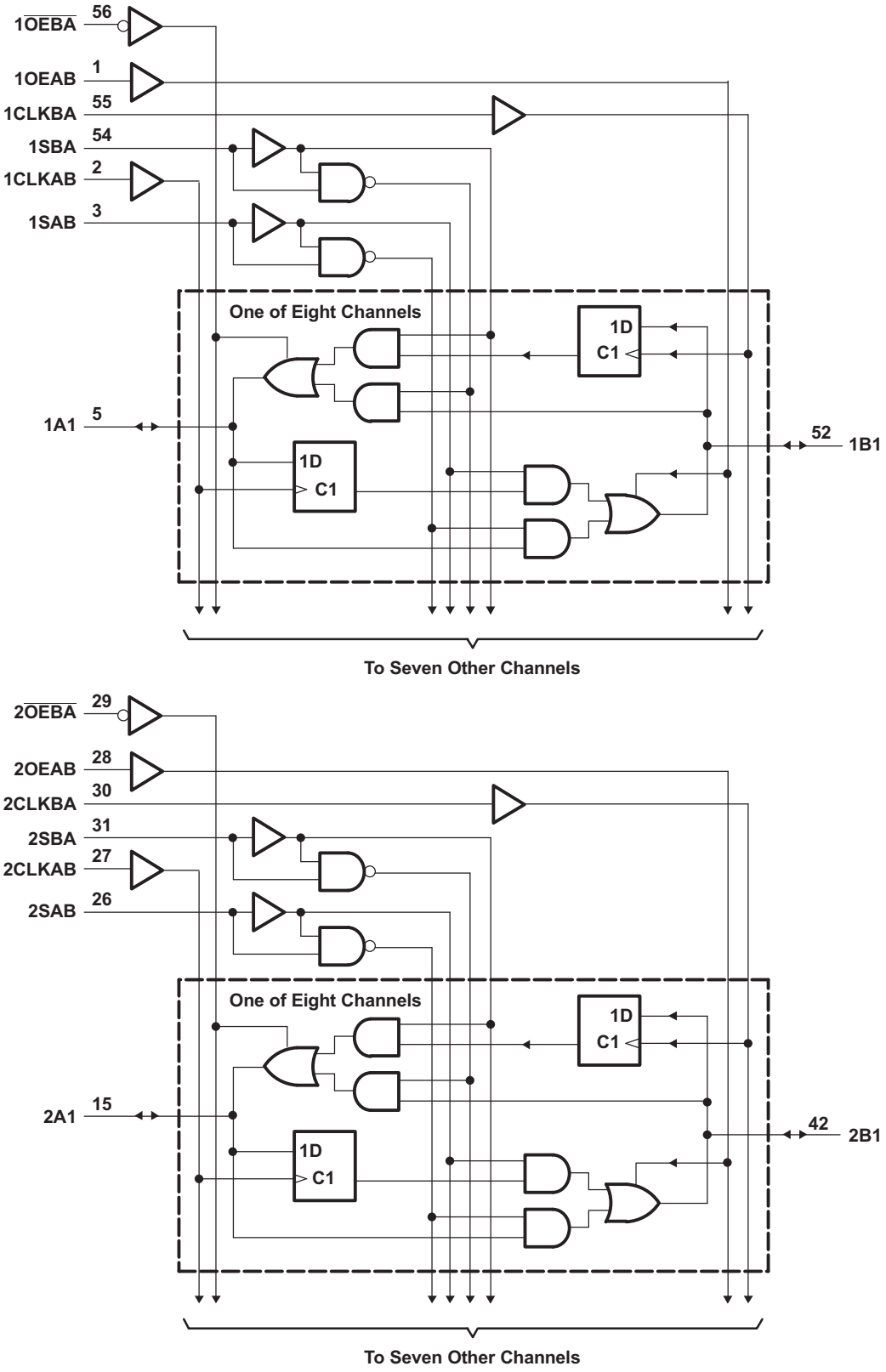


Figure 4. Logic Diagram (Positive Logic)

9.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
  - Inputs accept voltages to 5.5 V
- I_{off} feature
  - Allows voltages on the inputs and outputs when V_{CC} is 0 V
- Bus hold on data Inputs eliminates the need for external pull-up/pull-down resistors

9.4 Device Functional Modes

Table 1. Function Table

INPUTS						DATA I/O(1)		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified(2)	Store A, hold B
H	H	↑	↑	X(2)	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified(2)	Input	Hold A, store B
L	L	↑	↑	X	X(2)	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

(1) The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or $\overline{OEBA}$. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.
(2) Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered to load both registers.

10 Application and Implementation

10.1 Application Information

SN74LVCH16652A is a high-drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be retained or latched. It can produce 24 mA of drive current at 3.3 V, making it Ideal for driving multiple outputs and good for high-speed applications up to 100 MHz. To ensure the high-impedance state during power up or power down, $\overline{OEBA}$ should be tied to V_{CC} through a pull-up resistor and OEAB should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver. Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment. Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by any control pin.

10.2 Typical Application

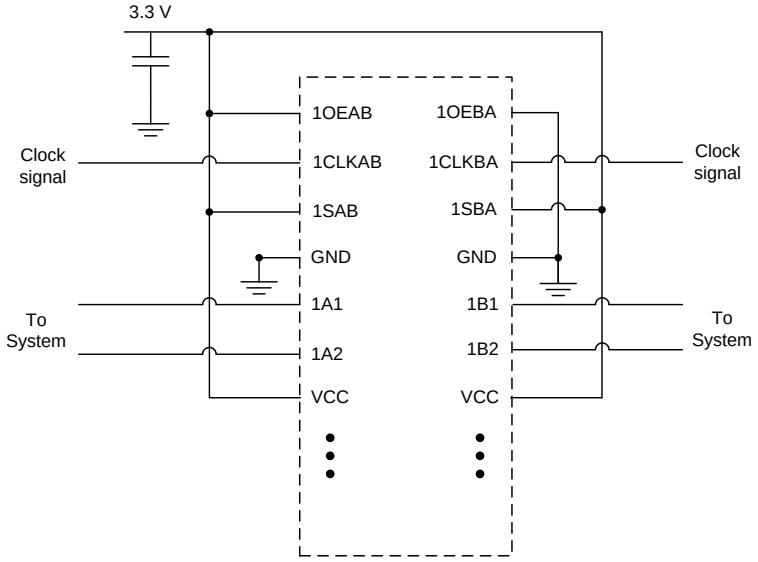


Figure 5. Bus-Management Functions

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *Recommended Operating Conditions* table.
   - For specified High and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions
   - Load currents should not exceed 50 mA per output and 100 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

Typical Application (continued)

10.2.3 Application Curves

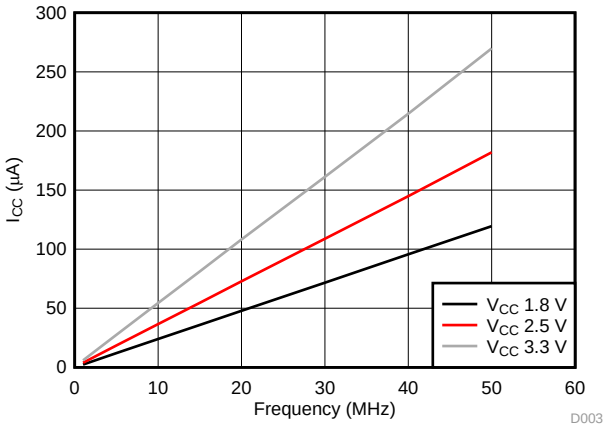


Figure 6. I_{CC} vs Frequency

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver.

12.2 Layout Example

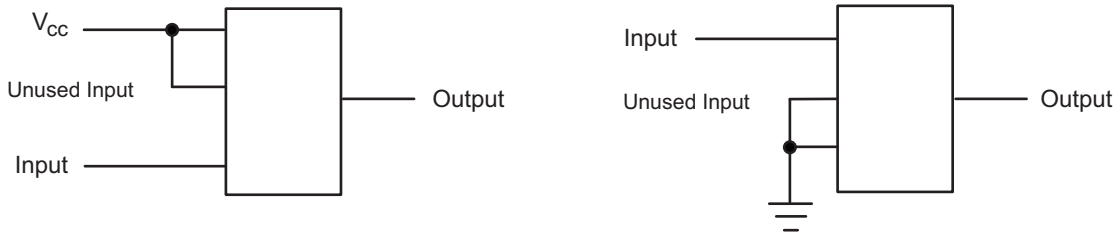


Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

Widebus is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCH16652ADGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH16652A	Samples
SN74LVCH16652ADGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LDH652A	Samples
SN74LVCH16652ADL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH16652A	Samples
SN74LVCH16652ADLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH16652A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LVCH16652A :

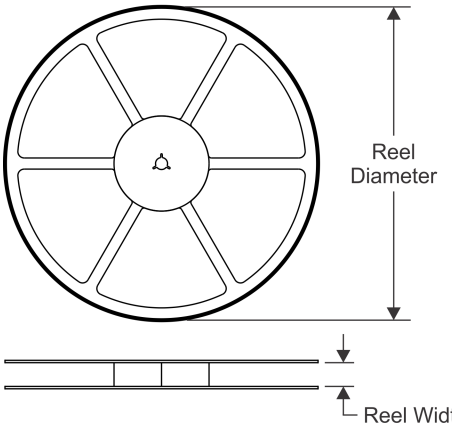
- Enhanced Product: SN74LVCH16652A-EP

NOTE: Qualified Version Definitions:

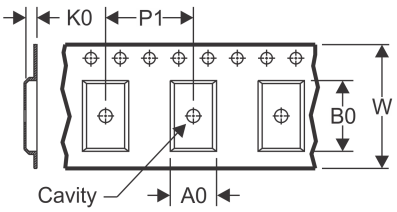
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

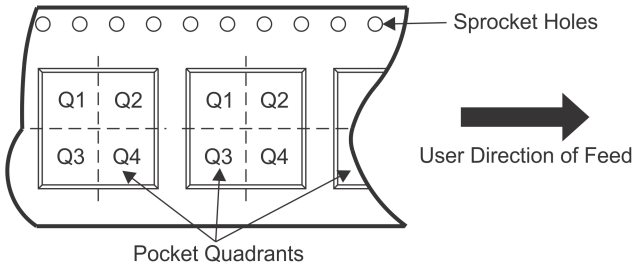


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

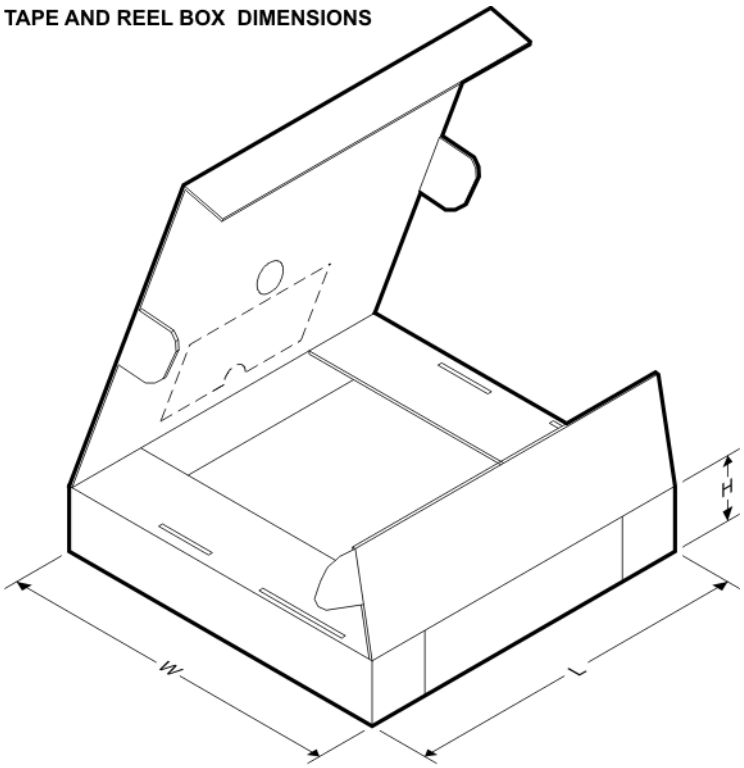
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCH16652ADGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74LVCH16652ADGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

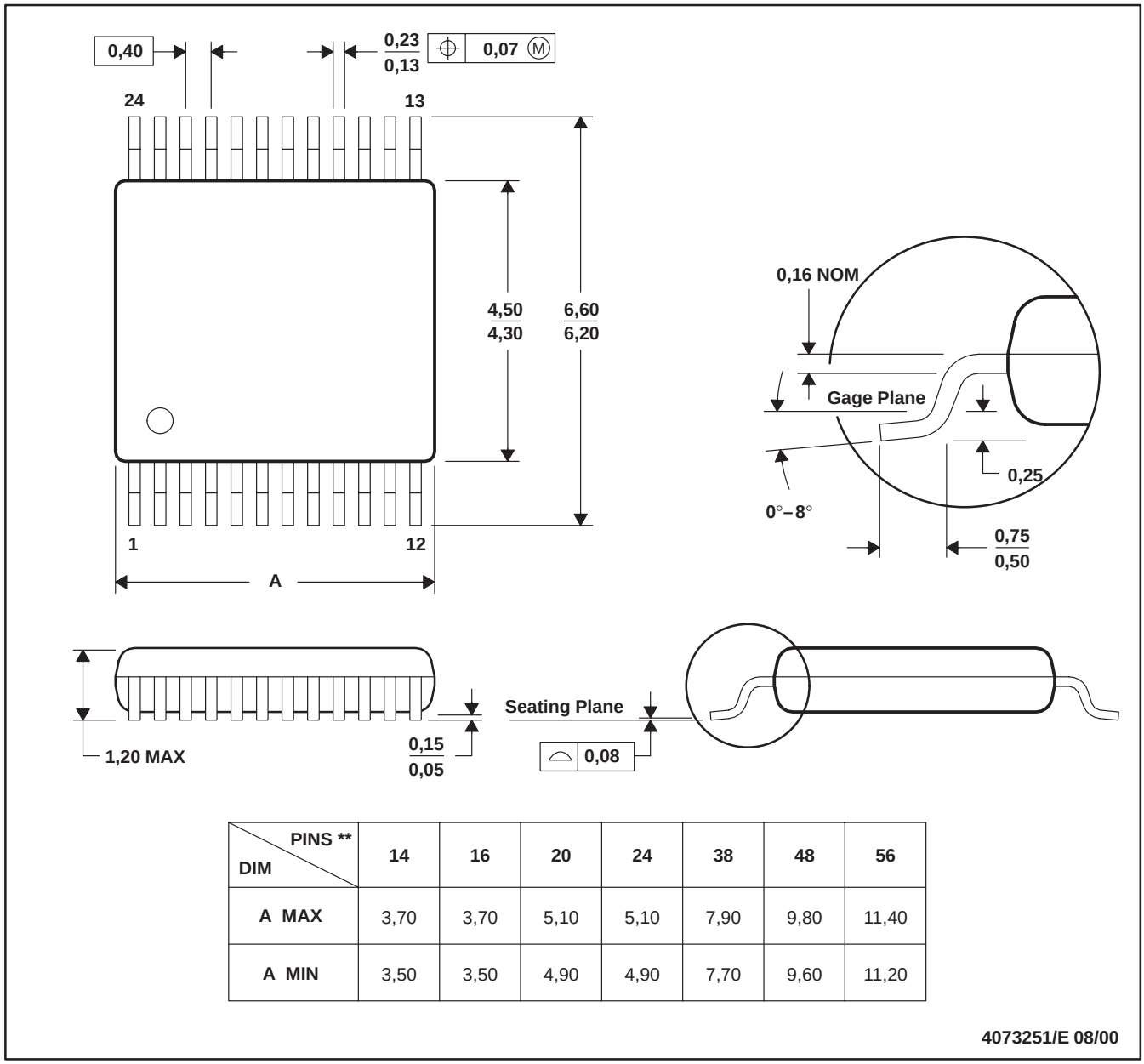


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCH16652ADGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74LVCH16652ADGVR	TVSOP	DGV	56	2000	367.0	367.0	45.0

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

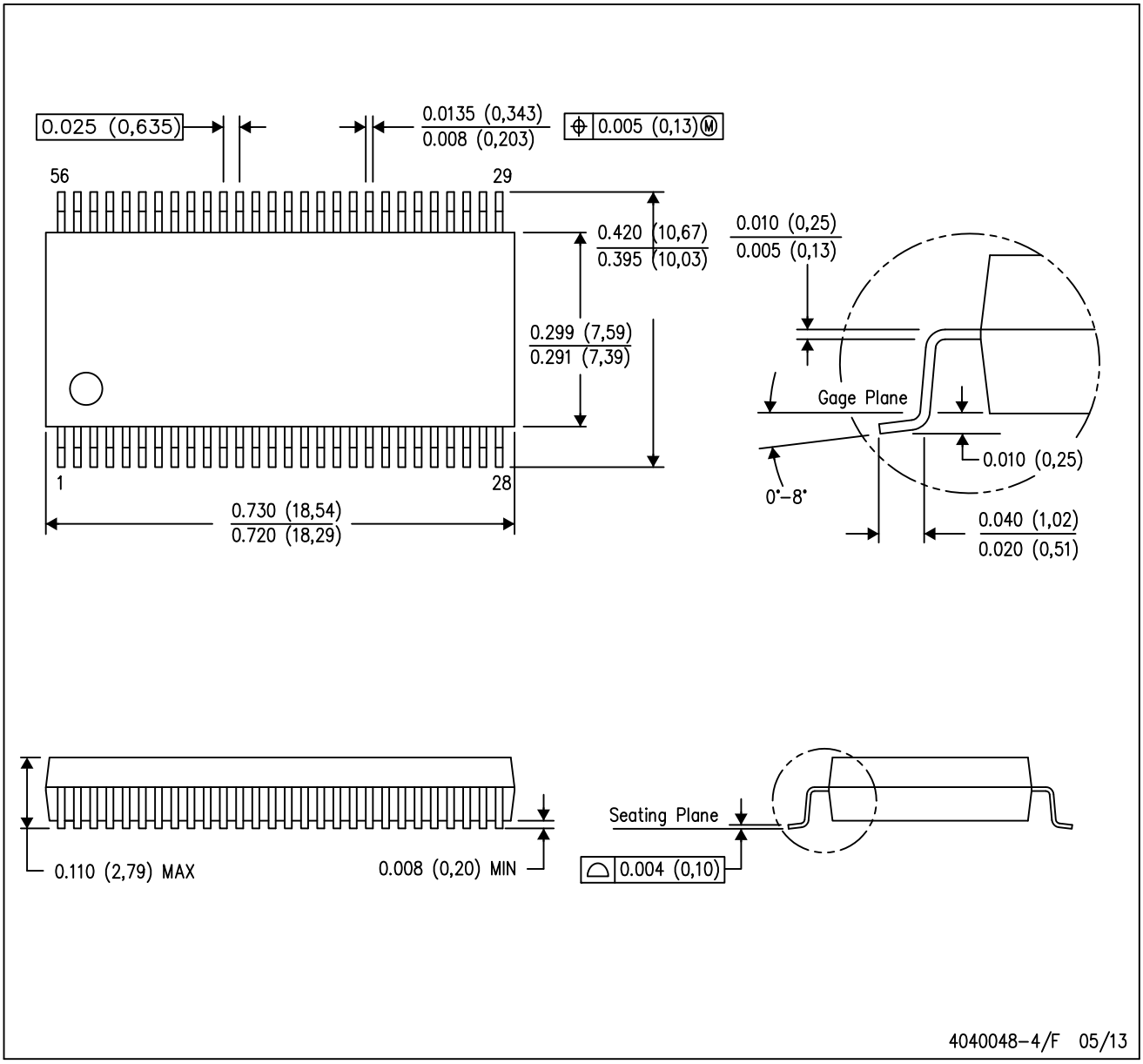


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

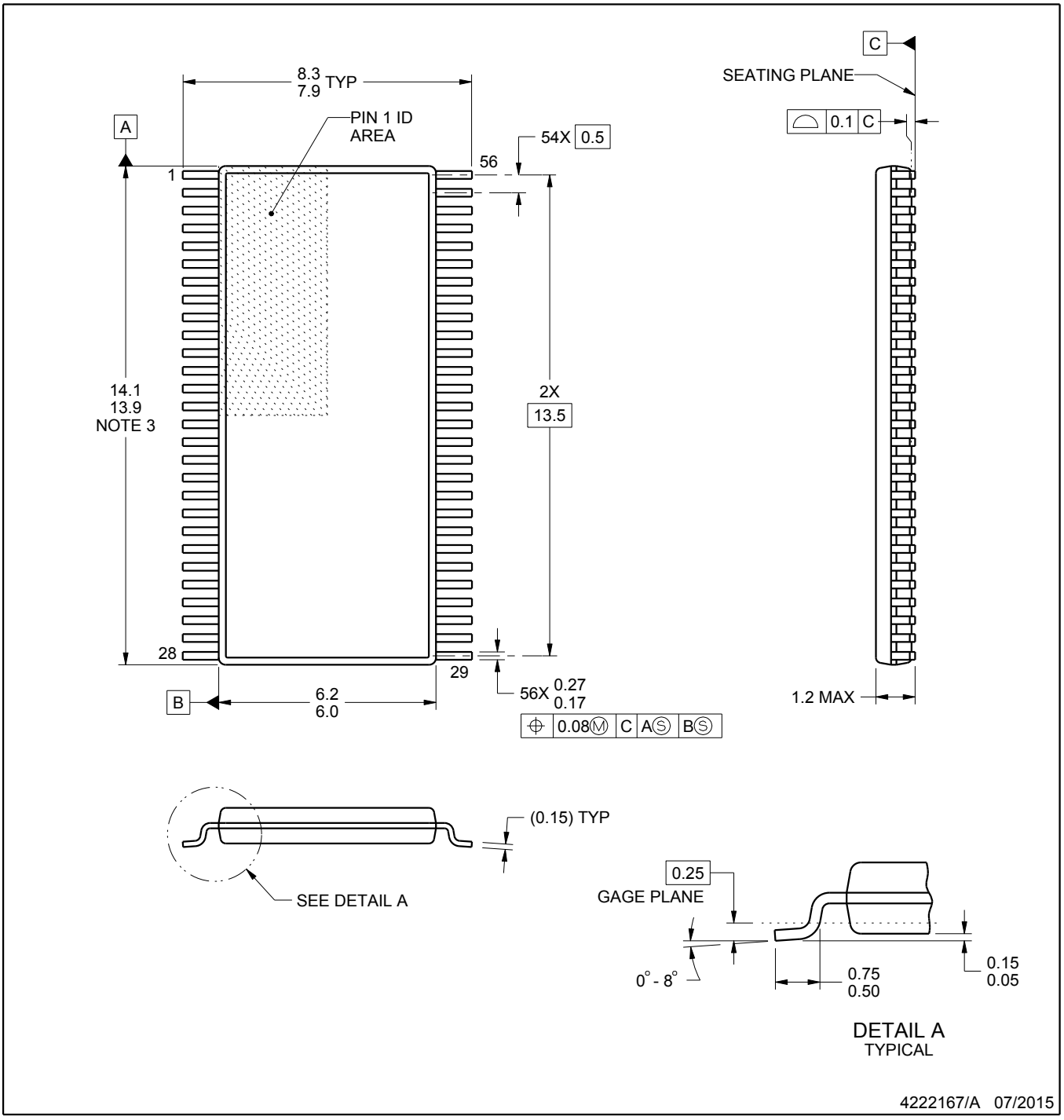
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DGG0056A

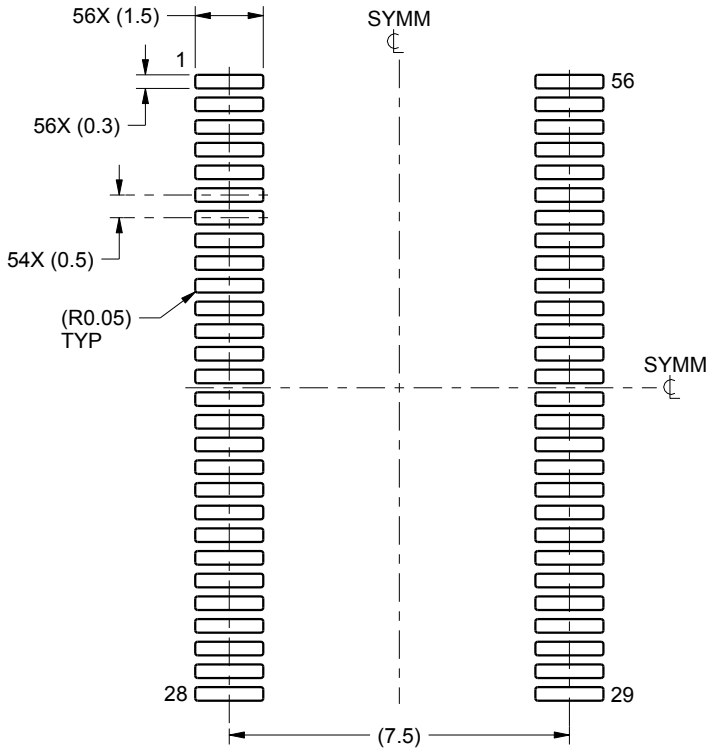
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

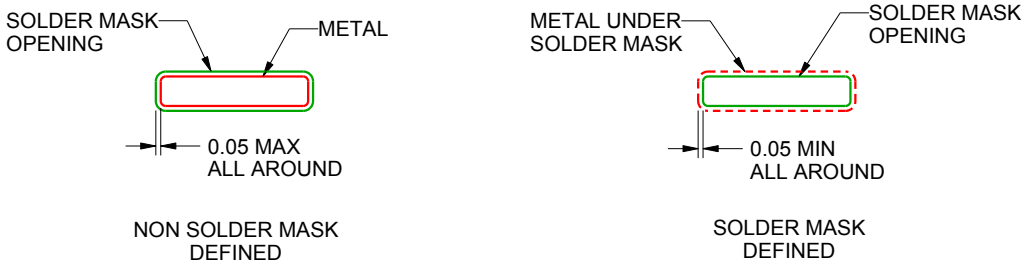


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

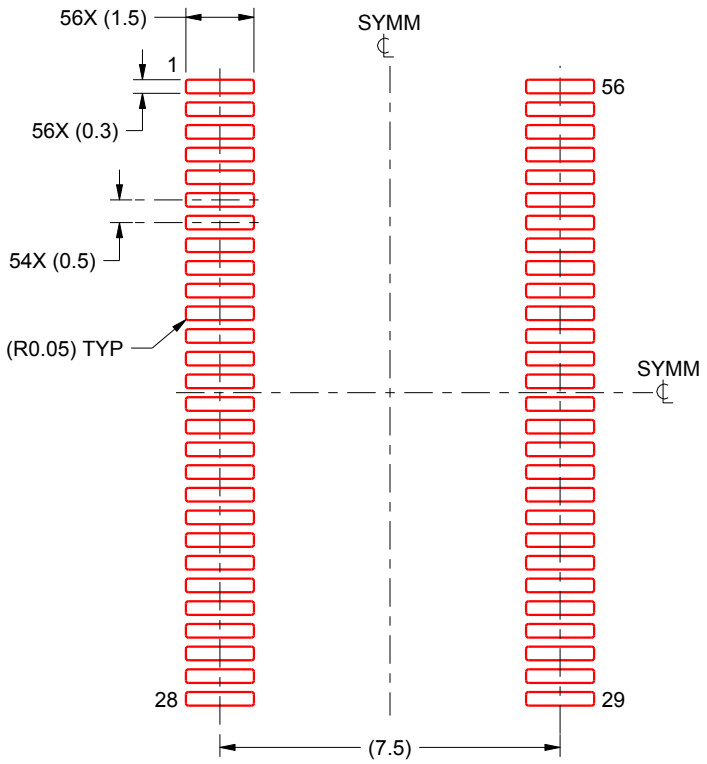


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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