THE DATASHEET OF

CDCVF2510APWRG4

3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH POWER DOWN MODE

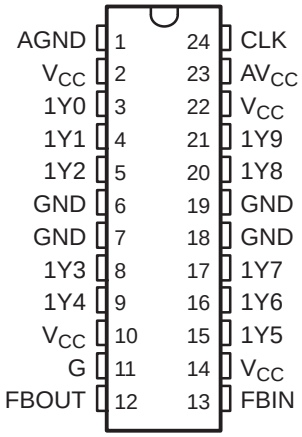
FEATURES

- **Designed to Meet and Exceed PC133 SDRAM Registered DIMM Specification Rev. 1.1**
- **Spread Spectrum Clock Compatible**
- **Operating Frequency 20 MHz to 175 MHz**
- **Static Phase Error Distribution at 66 MHz to 166 MHz is ±125 ps**
- **Jitter (cyc–cyc) at 66 MHz to 166 MHz is |70| ps**
- **Advanced Deep Submicron Process Results in More Than 40% Lower Power Consumption vs Current Generation PC133 Devices**
- **Auto Frequency Detection to Disable Device (Power-Down Mode)**
- **Available in Plastic 24-Pin TSSOP**
- **Distributes One Clock Input to One Bank of 10 Outputs**
- **External Feedback (FBIN) Terminal is Used to Synchronize the Outputs to the Clock Input**
- **25-Ω On-Chip Series Damping Resistors**
- **No External RC Network Required**
- **Operates at 3.3 V**

APPLICATIONS

- **DRAM Applications**
- **PLL Based Clock Distributors**
- **Non-PLL Clock Buffer**

PW PACKAGE
(TOP VIEW)



DESCRIPTION

The CDCVF2510A is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. The CDCVF2510A uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDCVF2510A operates at a 3.3-V V_{CC} and also provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of 10 outputs provides 10 low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50%, independent of the duty cycle at CLK. Outputs are enabled or disabled via the control (G) input. When the G input is high, the outputs switch in phase and frequency with CLK; when the G input is low, the outputs are disabled to the logic-low state. The device automically goes into power-down mode when no input signal (< 1 MHz) is applied to CLK; the outputs go into a low state.

Unlike many products containing PLLs, the CDCVF2510A does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDCVF2510A requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, a fixed-phase signal at CLK, or following any changes to the PLL reference or feedback signals. The PLL can be bypassed by strapping AV_{CC} to ground to use as a simple clock buffer.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

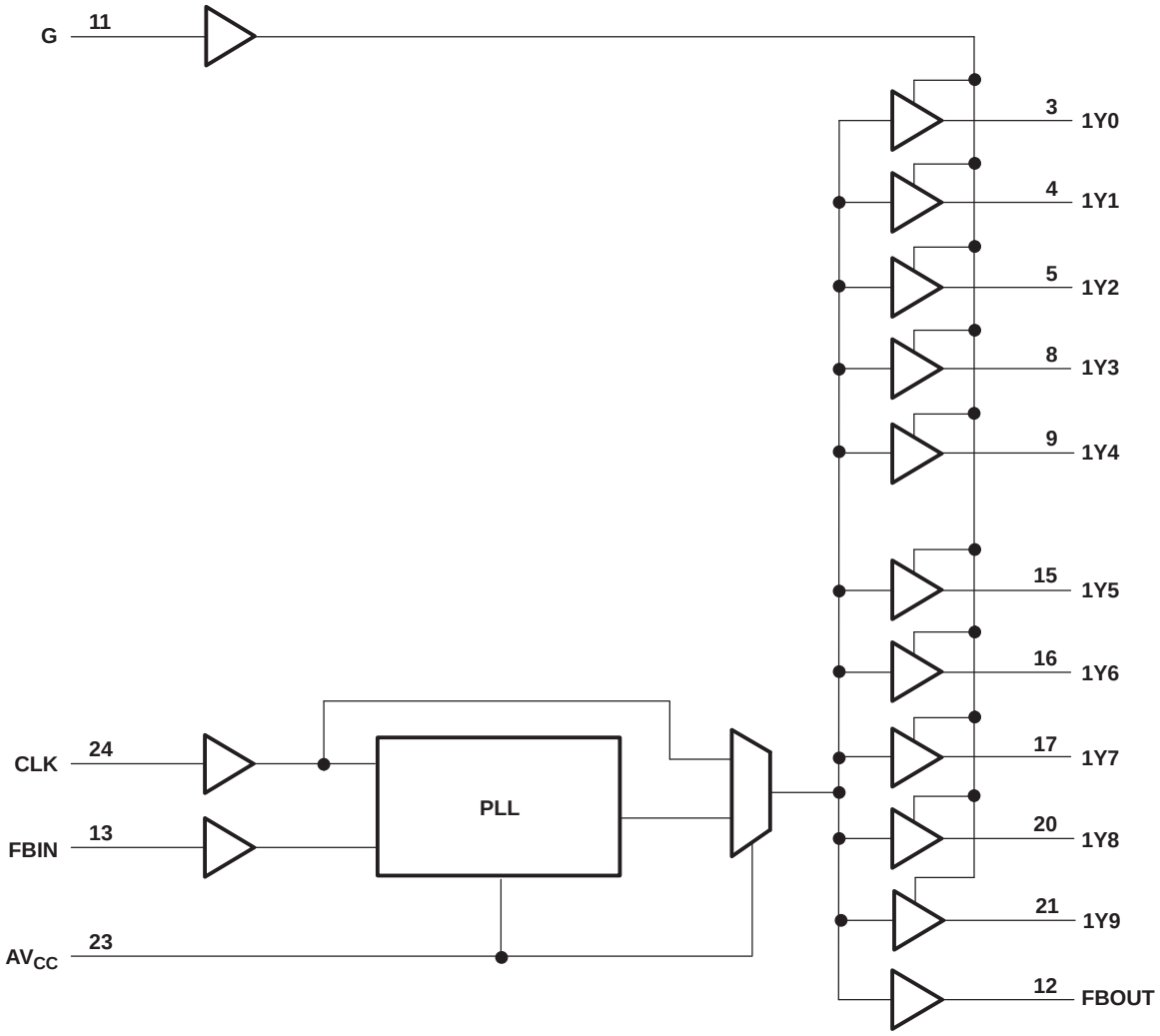
The CDCVF2510A is characterized for operation from 0°C to 85°C.

For application information see the application reports *High Speed Distribution Design Techniques for CDC509/516/2509/2510/2516* (literature number SLMA003) and *Using CDC2509A/2510A PLL With Spread Spectrum Clocking (SSC)* (literature number SCAA039).

FUNCTION TABLE

INPUTS			OUTPUTS		PLL
AVDD	**G**	**CLK**	**1Y(0:9)**	**FBOUT**	
GND	L	Signal	L	Signal (delayed)	Bypassed / Off
GND	H	Signal	Signal (delayed)	Signal (delayed)	Bypassed / Off
3.3 V (nom)	L	CLK > 1 MHz	L	CLK (in phase)	On
3.3 V (nom)	H	CLK > 1 MHz	CLK (in phase)	CLK (in phase)	On
3.3 V (nom)	X	CLK < 1 MHz	L	L	Off

FUNCTIONAL BLOCK DIAGRAM



AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (PW)
0°C to 85°C	CDCVF2510APWR
	CDCVF2510APW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CDCVF2510A clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
G	11	I	Output bank enable. G is the output enable for outputs 1Y(0:9). When G is low, outputs 1Y(0:9) are disabled to a logic-low state. When G is high, all outputs 1Y(0:9) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has an integrated 25-Ω series-damping resistor.
1Y (0:9)	3, 4, 5, 8, 9, 15, 16, 17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:9) is enabled via the G input. These outputs can be disabled to a logic-low state by deasserting the G control input. Each output has an integrated 25-Ω series-damping resistor.
AV_{CC}	23	Power	Analog power supply. AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	2, 10, 14, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

AV_{CC}	Supply voltage range (1)	$AV_{CC} < V_{CC} + 0.7$ V
V_{CC}	Supply voltage range	-0.5 V to 4.3 V
V_I	Input voltage range (2)	-0.5 V to 4.6 V
V_O	Voltage range applied to any output in the high or low state (2)(3)	–0.5 V to V_{CC} + 0.5 V
I_{IK}	Input clamp current, ($V_I < 0$)	–50 mA
I_{OK}	Output clamp current, ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
I_O	Continuous output current, ($V_O = 0$ to V_{CC})	±50 mA
	Continuous current through each V_{CC} or GND	±100 mA
$Z_{\theta JA}$	Junction-to-ambient package thermal impedance (4)	114.5°C/W
$Z_{\theta JC}$	Junction-to-case thermal impedance (4)	25.7°C/W
T_J	Maximum allowable junction temperature	125°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) AV_{CC} must not exceed V_{CC} + 0.7 V.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance and junction-to-case thermal impedance are calculated in accordance with JESD51 (no air flow condition) and JEDEC252P (high-k board).

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	MAX	UNIT
V_{CC}, AV_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current,		12	mA
f_{clk}	Clock frequency(2)	20	175	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time		1	ms

(1) Unused inputs must be held high or low to prevent them from floating.
(2) Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the *switching characteristics* table are not applicable. This parameter does not apply for input modulation under SSC application.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}, AV_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA	3 V			-1.2	V
V_{OH}	High-level output voltage	I_{OH} = –100 µA	MIN to MAX	V_{CC}–0.2			V
		I_{OH} = –12 mA	3 V	2.1			
		I_{OH} = –6 mA	3 V	2.4			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA	MIN to MAX			0.2	V
		I_{OL} = 12 mA	3 V			0.8	
		I_{OL} = 6 mA	3 V			0.55	
I_{OH}	High-level output current	V_O= 1 V	3 V	–28			mA
		V_O = 1.65 V	3.3 V		–36		
		V_O = 3.135 V	3.6 V			-8	
I_{OL}	Low-level output current	V_O= 1.95 V	3 V	30			mA
		V_O = 1.65 V	3.3 V		40		
		V_O = 0.4 V	3.6 V			10	
I_I	Input current	V_I = V_{CC} or GND	3.6 V			±5	µA
I_{CC}(2)	Supply current (static, output not switching)	V_I = V_{CC} or GND, I_O = 0, Outputs: low or high	3.6 V, 0 V			40	µA
ΔI_{CC}	Change in supply current	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3.3 V to 3.6 V			500	µA
C_i	Input capacitance	V_I = V_{CC} or GND	3.3 V		2.5		pF
C_o	Output capacitance	V_O = V_{CC} or GND	3.3 V		2.8		pF

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) For dynamic I_{CC} vs Frequency, see Figure 9 and Figure 10.

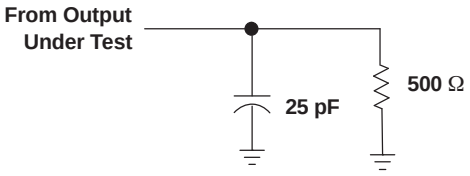
SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature, C_L = 25 pF (see Note (1) and Figure 1 and Figure 2)(2)

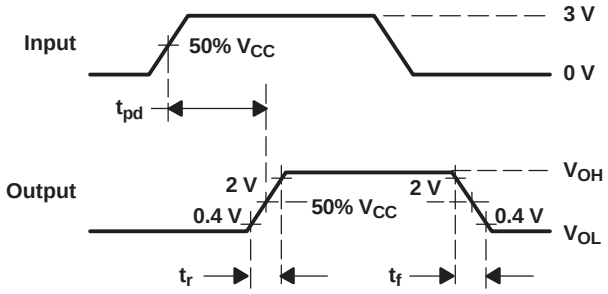
PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}, AV_{CC} = 3.3 V ± 0.3 V			UNIT
				MIN	TYP	MAX	
$t_{(\phi)}$	Phase error time-static (normalized) (see Figure 4 through Figure 7)	CLK↑ = 25 MHz to 65 MHz	FBIN↑	–150		150	ps
		CLK↑ = 66 MHz to 175 MHz		–125		125	
$t_{sk(o)}$	Output skew time(3)	Any Y	Any Y			100	ps
	Phase error time-jitter (4)	CLK = 66 MHz to 175 MHz	Any Y or FBOUT	–50		50	ps
	$Jitter_{(cycle-cycle)}$(see Figure 8)	CLK = 25 MHz to 40 MHz	Any Y or FBOUT			500	ps
		CLK = 41 MHz to 59 MHz				200	
		CLK = 60 MHz to 175 MHz			65	125	
$t_{d(\phi)}$	Dynamic phase offset(5)	CLK↑ = 25 MHz to 65 MHz	FBIN↑			1.5	ns
		CLK↑ = 66 MHz to 175 MHz				0.4	
	Duty cycle	$f_{(CLK)}$ > 60 MHz	Any Y or FBOUT	45%		55%	
t_r	Rise time	V_O = 0.4 V to 2 V	Any Y or FBOUT	0.3		1.1	ns/V
t_f	Fall time	V_O = 2 V to 0.4 V	Any Y or FBOUT	0.3		1.1	ns/V
t_{PLH}	Low-to-high propagation delay time, bypass mode	CLK	Any Y or FBOUT	1.8		3.9	ns
t_{PHL}	High-to-low propagation delay time, bypass mode	CLK	Any Y or FBOUT	1.8		3.9	ns

(1) The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
(2) These parameters are not production tested.
(3) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
(4) Calculated per PC DRAM SPEC ($t_{phase\ error}$, static - $jitter_{(cycle-to-cycle)}$).
(5) The parameter is assured by design but cannot be 100% production tested.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 133 MHz, Z_O = 50 Ω, t_r ≤ 1.2 ns, t_f ≤ 1.2 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

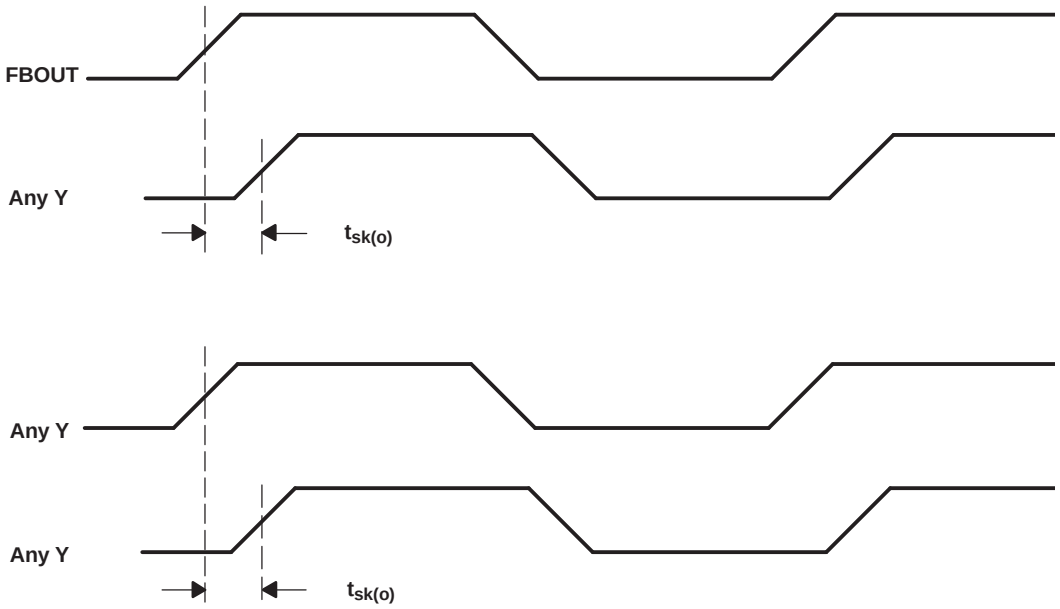
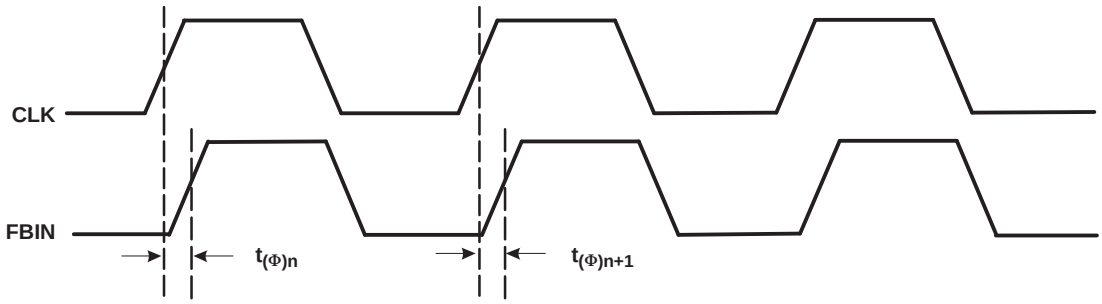
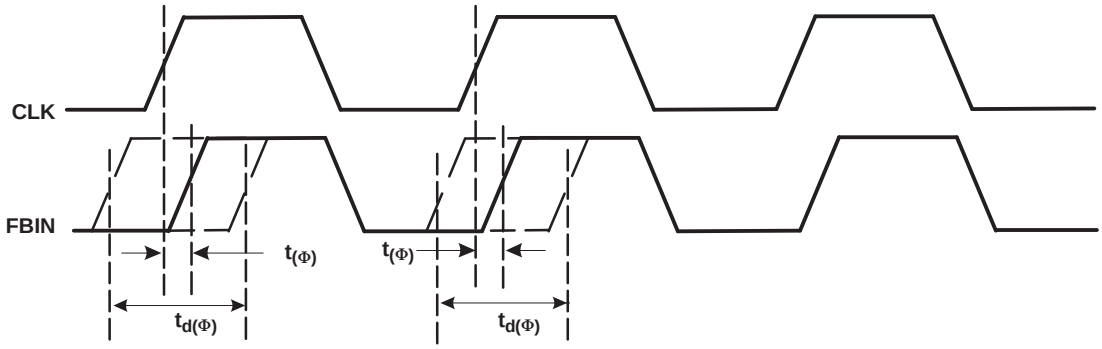


Figure 2. Skew Calculations



$$t_{(\Phi)} = \frac{\sum_{1}^{n=N} t_{(\Phi)n}}{N}$$ (N is a large number of samples)

a) Static Phase Offset



b) Dynamic Phase Offset

Figure 3. Static and Dynmaic Phase Offset

TYPICAL CHARACTERISTICS

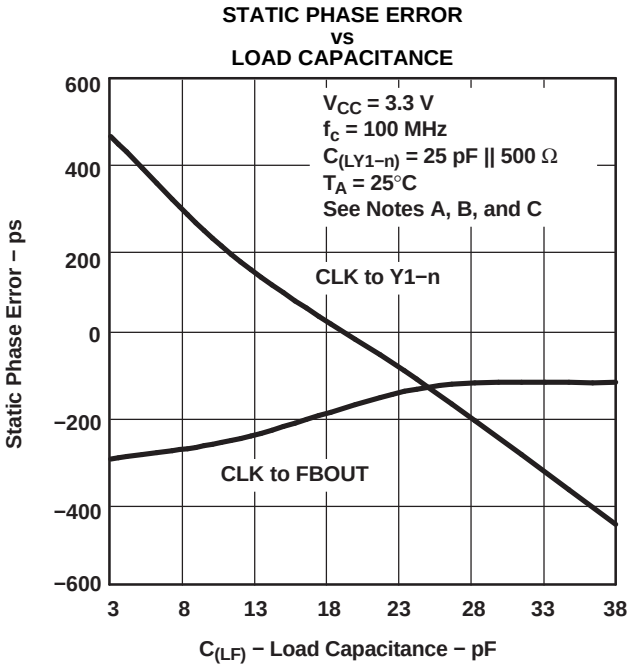


Figure 4.

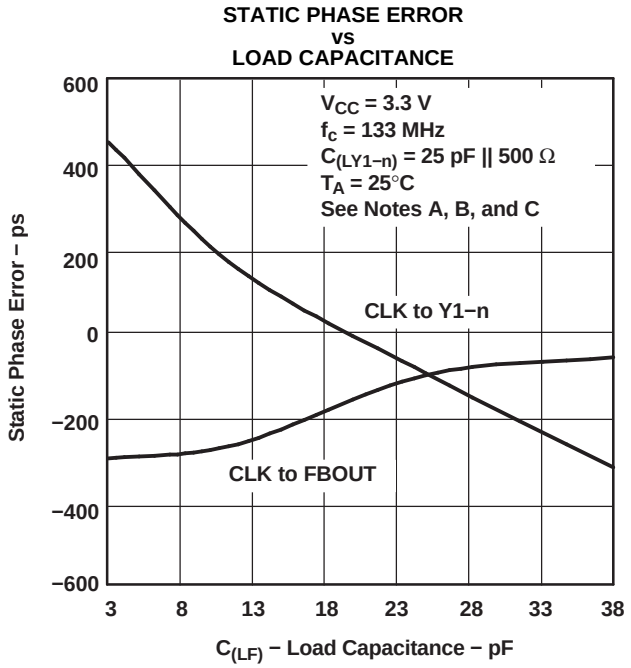


Figure 5.

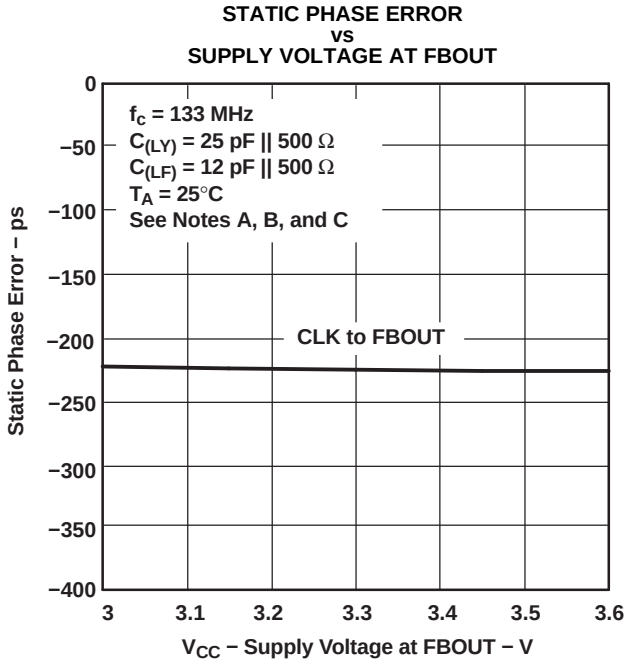


Figure 6.

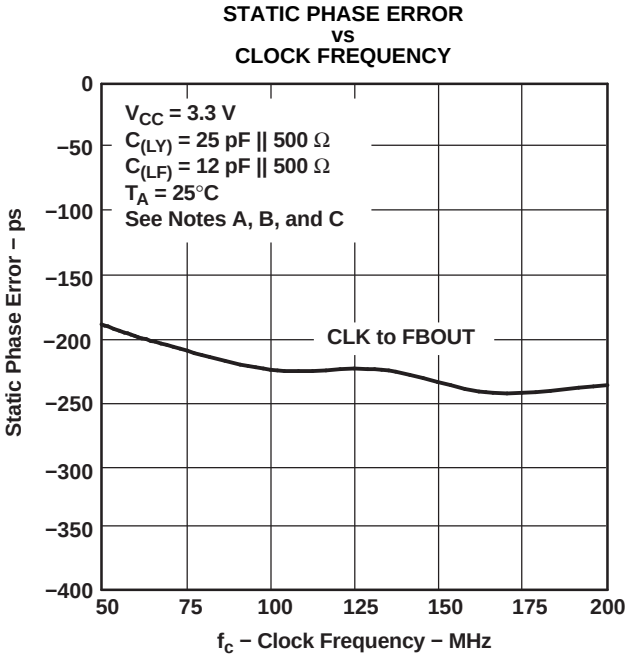


Figure 7.

A. Trace length FBOUT to FBIN = 5 mm, Z_O = 50Ω

B. $C_{(LY)}$ = Lumped capacitive load Y_{1-n}

C. $C_{(LFx)}$ = Lumped feedback capacitance at FBOUT = FBIN

TYPICAL CHARACTERISTICS (continued)

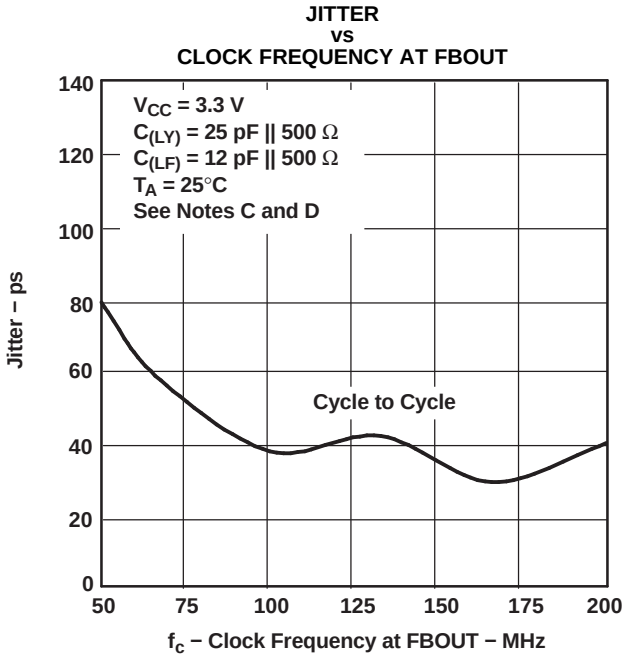


Figure 8.

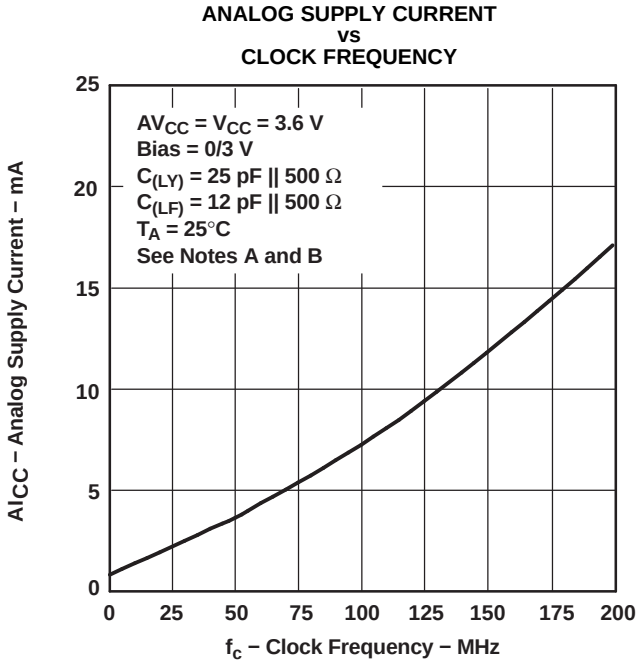


Figure 9.

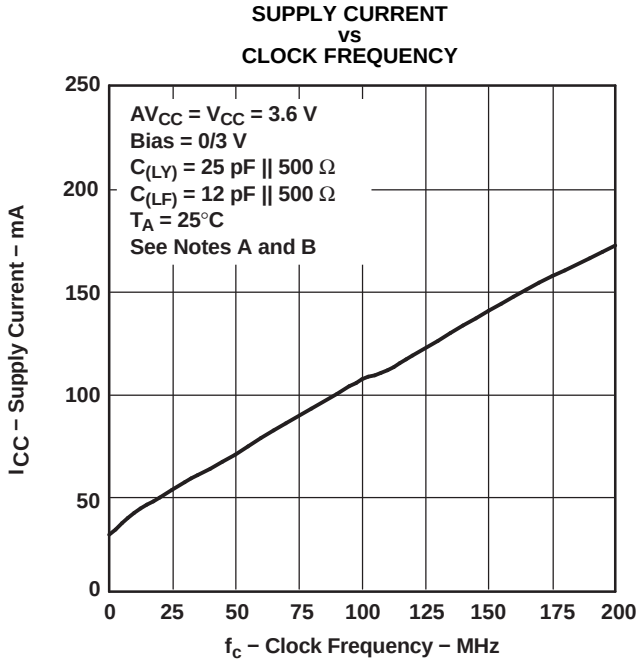


Figure 10.

A. Trace length FBOUT to FBIN = 5 mm, Z_O = 50Ω

B. $C_{(LY)}$ = Lumped capacitive load Y_{1-n}

C. $C_{(LFx)}$ = Lumped feedback capacitance at FBOUT = FBIN

D. $C_{(LFx)}$ = Lumped feedback capacitance at FBOUT = FBIN

Revision History

Table 1. Revision History

Date	Rev	Page	Section	Description
04/11/05	B	6	Switching Characteristics	Added static phase error - 25 MHz to 65 MHz
				Added jitter - 25 MHz to 65 MHz
				Added Dynamic Phase Offset specification
		7	Figure 2	Revised into two figures
		8	Figure 3	Added Figure 3 for a diagram of dynamic phase offset
2/09/09	C	2	Function Table	Revised for clarity

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCVF2510APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	CKV2510A	Samples
CDCVF2510APWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	CKV2510A	Samples
CDCVF2510APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	CKV2510A	Samples
CDCVF2510APWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	CKV2510A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

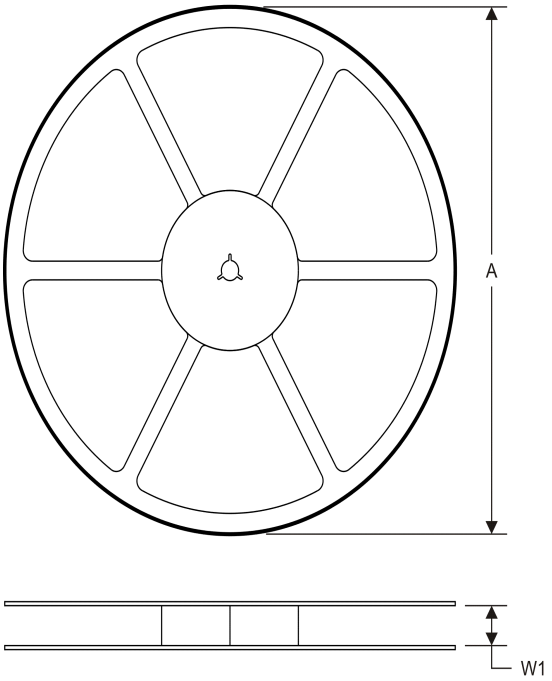
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

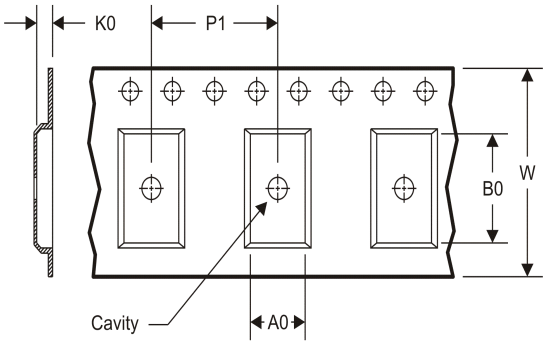
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



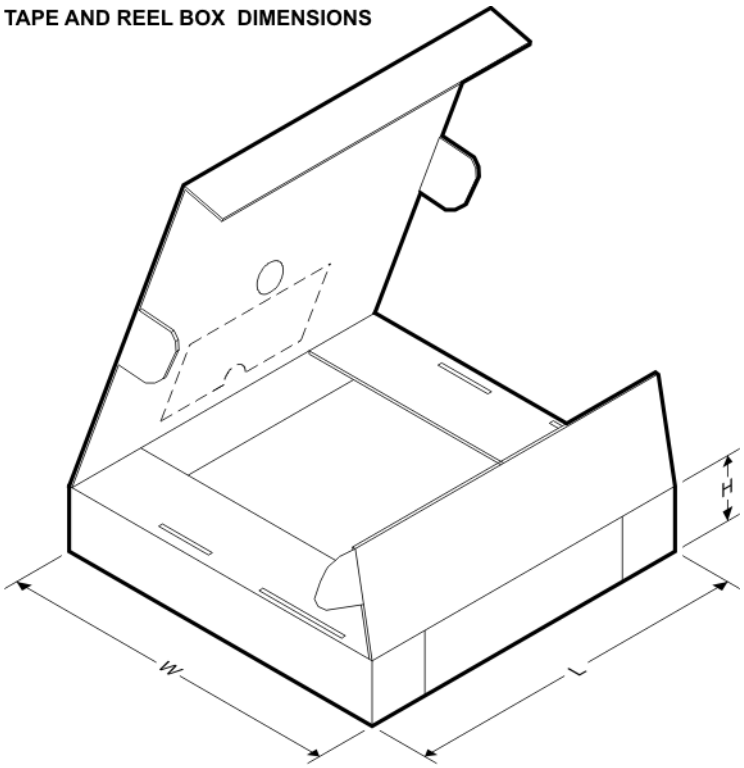
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF2510APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

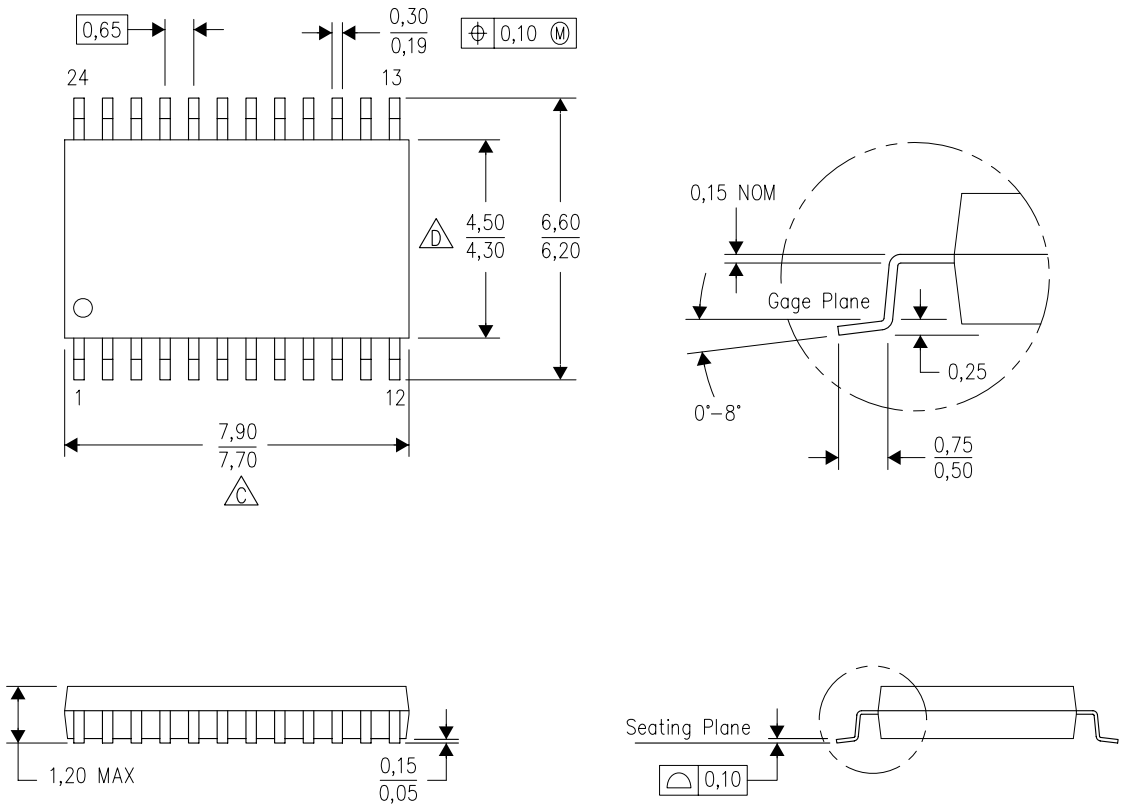
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF2510APWR	TSSOP	PW	24	2000	367.0	367.0	38.0

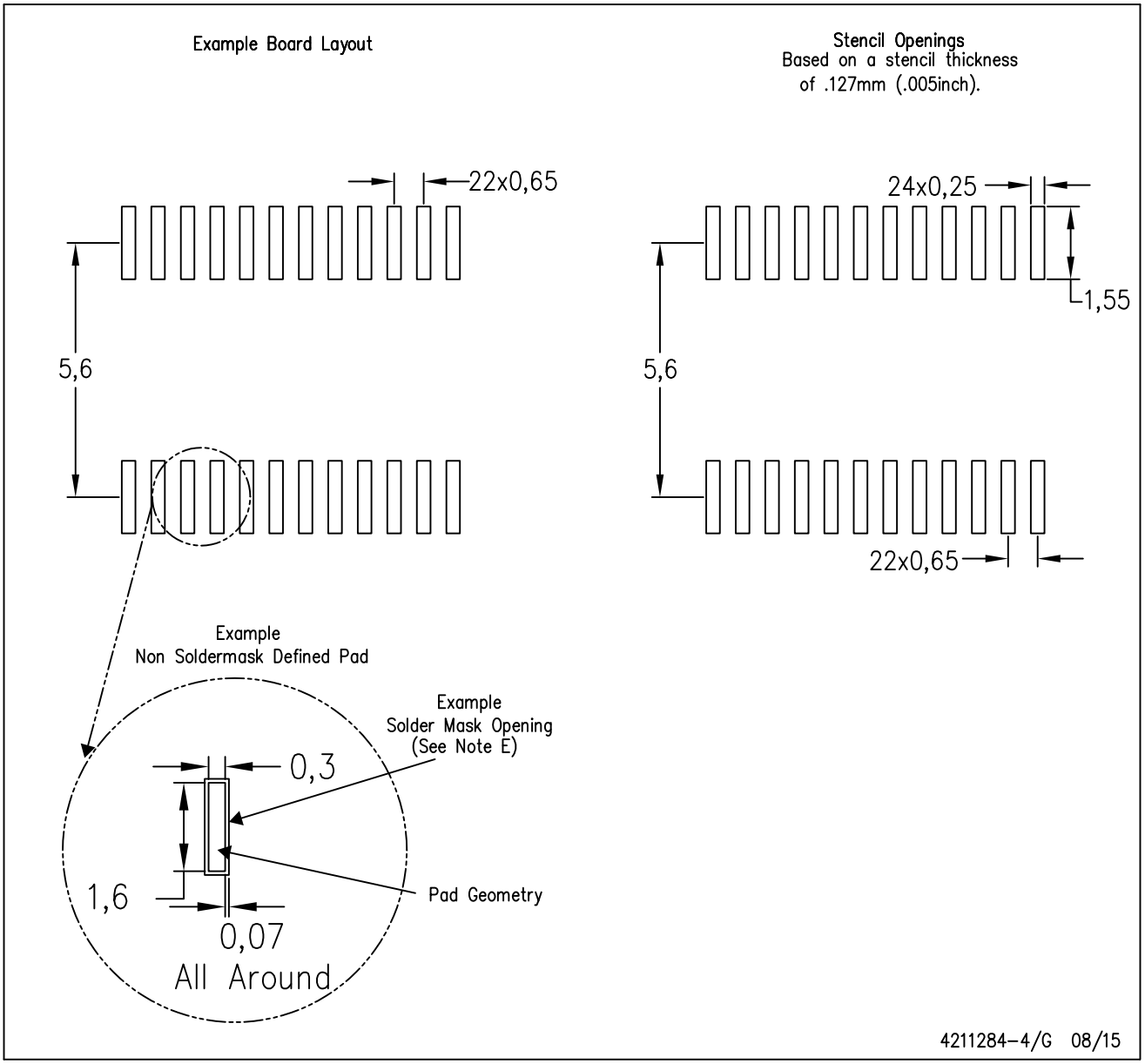
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

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