THE DATASHEET OF

UCC3973PWTRG4

BiCMOS Cold Cathode Fluorescent Lamp Driver Controller

FEATURES

- 1mA Typical Supply Current
- Accurate Lamp Current Control
- Analog or Low Frequency Dimming Capability
- Open Lamp Protection
- Programmable Startup Delay
- 4.5V to 25V Operation
- PWM Frequency Synchronized to External Resonant Tank
- 8 Pin TSSOP and SOIC Packages Available
- Internal Voltage Clamp Protects Transformer from Over-voltage (UCC3973)

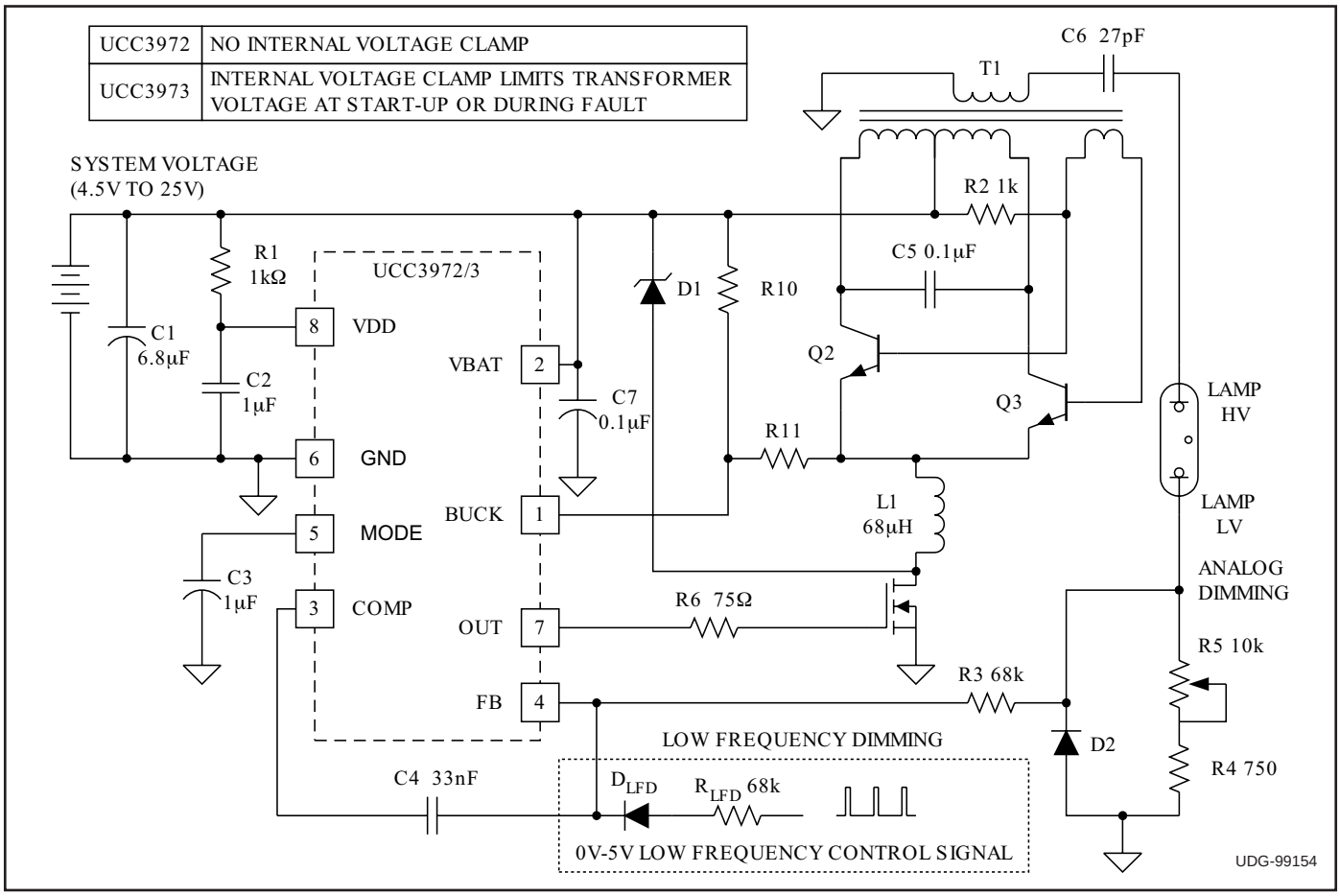
DESCRIPTION

Design goals for a Cold Cathode Fluorescent Lamp (CCFL) converter used in a notebook computer or portable application include small size, high efficiency, and low cost. The UCC3972/3 CCFL controllers provide the necessary circuit blocks to implement a highly efficient CCFL backlight power supply in a small footprint 8 pin TSSOP package. The BiCMOS controllers typically consume less than 1mA of operating current, improving overall system efficiency when compared to bipolar controllers requiring 5mA to 10mA of operating current.

External parts count is minimized and system cost is reduced by integrating such features as a feedback controlled PWM driver stage, open lamp protection, startup delay and synchronization circuitry between the buck and push-pull stages. The UCC3972/3 include an internal shunt regulator, allowing the part to operate with input voltages from 4.5V up to 25V. The part supports both analog and externally generated low frequency dimming modes of operation.

The UCC3973 adds a programmable voltage clamp at the BUCK pin. This feature can be used to protect the transformer from overvoltage during startup or when an open lamp occurs. Transformer voltage is controlled by reducing duty cycle when an over-voltage is detected.

TYPICAL APPLICATION CIRCUIT



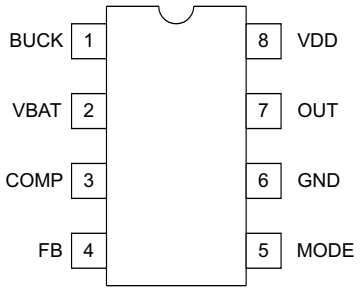
ABSOLUTE MAXIMUM RATINGS

VBAT . . . . . +27V
VDD Maximum Forced Current 30mA
Maximum Forced Voltage 17V
BUCK . . . . . –5V to VBAT
MODE . . . . . –0.3V to 4.0V
MODE Maximum Forced Current 300μA
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C

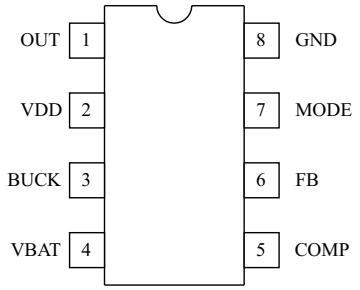
Unless otherwise indicated, currents are positive into, negative out of the specified terminal. Pulse is defined as less than 10% duty cycle with a maximum duration of 500μs. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

CONNECTION DIAGRAMS

TSSOP-8 (TOP VIEW)
PW Package



DIL-8 (TOP VIEW)
J, N Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified these specifications hold for T_A=0°C to +70°C for the UC3972/3, –40°C to +85°C for the UC2972/3, and –55°C to +125°C for the UC1972/3; T_A=T_J; VDD=VBAT=VBUCK=12V; MODE=OPEN. For any tests with VBAT>17V, place a 1k resistor from VBAT to VDD.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input supply					
VDD Supply Current	VDD = 12V		1	1.5	mA
	VBAT = 25V		7	10.5	mA
VBAT Supply Current	VBAT = 12V		30	60	μA
	VBAT = 25V		70	140	μA
VDD Regulator Turn-on Voltage	I_{SOURCE} = 2mA to 10mA	17	18	19	V
VDD UVLO Threshold	Low to high	3.6	4	4.4	V
UVLO Threshold Hysteresis		100	200	300	mV
Output Section					
Pull Down Resistance	I_{SINK} = 10mA to 100mA		25	50	Ω
Pull Up Resistance	I_{SOURCE} = 10mA to 100mA		25	50	Ω
Output Clamp Voltage	VBAT = 25V, Shunt Regulator on		16	18	V
Output Low	MODE = 0.5V, I_{SINK} = 1mA		0.05	0.2	V
Rise Time	CL = 1nF, Note 1		200		ns
Fall Time	CL = 1nF, Note 1		200		ns

ELECTRICAL CHARACTERISTICS: Unless otherwise specified these specifications hold for T_A=0°C to +70°C for the UC3972/3, –40°C to +85°C for the UC2972/3, and –55°C to +125°C for the UC1972/3; T_A=T_J; VDD=VBAT=VBUCK=12V; MODE=OPEN. For any tests with VBAT>17V, place a 1k resistor from VBAT to VDD.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Synchronizable Frequency (See Note 2.)	BUCK = VBAT– 2, V_{BAT} = 12V to 25V, T_A = –40°C to +85°C	80	-	160	kHz
	BUCK = VBAT–2, V_{BAT} = 12V to 25V T_A = –55°C to +125°C	80	-	145	kHz
Maximum Duty Cycle	FB = 1V, T_A < 0°C	84			%
	FB = 1V, T_A = 0°C to 70°C	90	95		%
Minimum Duty Cycle	FB = 2V			0	%
BUCK Input Bias Current	BUCK = VBAT = 12V		40	90	µA
	BUCK = VBAT = 25V		80	110	µA
Zero Detect Threshold	Measured at BUCK w/respect to VBAT, VBAT=12V to 25V, T_A < 0°C	–2.4	–1	–0.3	V
	Measured at BUCK w/respect to VBAT, VBAT=12V to 25V, T_A = 0°C to 70°C	–2.0	–1	–0.3	V
Error Amplifier					
Input Voltage	COMP = 2V, T_A = 0°C to +70°C	1.465	1.5	1.535	V
	COMP = 2V	1.455		1.545	V
Line Regulation		–2	2	10	mV
Input Bias Current		–500	–100		nA
Open Loop Gain	COMP = 0.5V to 3.0V	60	80		dB
Output High Voltage	FB = 1V	3.3	3.7	4.1	V
Output Low Voltage	FB = 2V		0.15	0.35	V
Output Source Current	FB = 1V, COMP = 2V		–1.2	–0.4	mA
Output Sink Current	FB = 2V, COMP = 2V	2	4		mA
Output Source Current	FB = 1V, COMP = 2V, MODE = 0.5V	–1		1	µA
Output Sink Current	FB = 2V, COMP = 2V, MODE = 0.5V	–1		1	µA
Unity Gain Bandwidth	T_J = 25C, Note 1		2		MHz
Mode Select					
Output Enable Threshold		0.85	1	1.15	V
Open Lamp Detect Enable Threshold		2.75	3	3.25	V
Mode Output Current	MODE = 0.5V	15	20	25	µA
MODE Clamp Voltage	MODE = OPEN	3.3	3.7	4	V
Open Lamp					
Open Lamp Detect Threshold	Measured at BUCK with respect to VBAT, VBAT=12V to 25V	–8	–7	–6	V
Over-voltage Clamp Threshold (UCC3973)	Measured at BUCK with respect to VBAT, VBAT=12V to 25V, I_{FB} = 100µA	–10.3	–9	–7.7	V

Note 1. Ensured by design. Not 100% tested in production.

Note 2. Oscillator operates at 2x transformer switching frequencey.

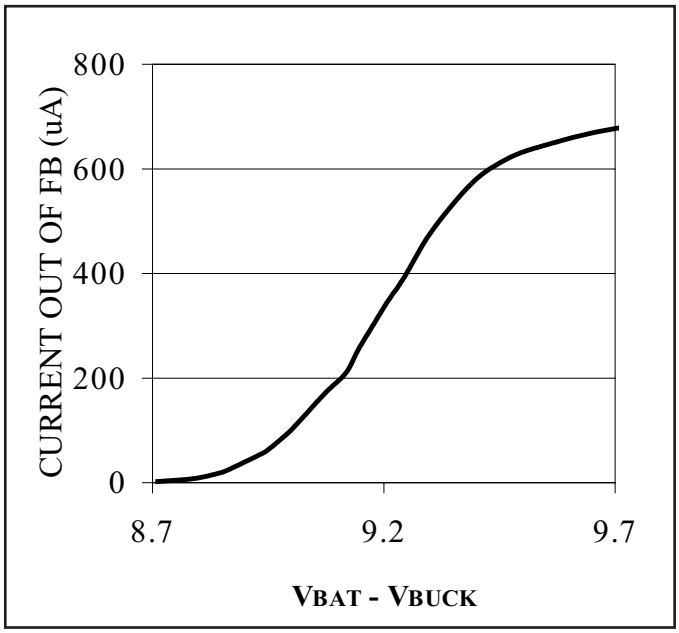
PIN DESCRIPTIONS

BUCK: Senses the voltage on the top side of the inductor feeding the resonant tank. The voltage at this point is used to synchronize the internally generated ramp and to detect whether an open lamp condition exists. An open lamp condition exists when this voltage is below the specified threshold for seven clock cycles. If the MODE pin is held below the open lamp detect enable threshold, this protective feature is disabled.

On the UCC3973, this pin is also used to sense an over-voltage across the transformer primary. If the voltage at this pin exceeds the clamp threshold, current will be sourced fron the FB pin.

COMP: Output of the error amplifier.Compensation components set the bandwidth of the entire system and are normally connected between COMP and FB. The error amplifier averages lamp current against a fixed internal reference. The resulting voltage on the COMP pin is compared to an internally generated ramp, setting the PWM duty cycle. During UVLO, this pin is actively pulled low.

FB: This pin is the inverting input to the error amplifier. On the UCC3973, current is sourced form this pin if the clamp threshold is exceeded at the BUCK pin (see below). The sourced current will reduce OUT duty cycle to control transformer primary voltage. The source current is disabled on the UCC3972.



Clamp current vs. tank voltage for UCC3973.

GND: Ground reference for the IC.

MODE: The voltage on this pin is used to control start-up and various modes of operation for the part (refer to the table in the block diagram).

When the voltage is below 1V, OUT is forced low, open lamp detection is disabled and the error amplifier is tri-stated.

When the voltage is between 1V and 3V, OUT is enabled and the error amplifier output is connected to COMP. Open lamp detection is still disabled and a constant 20 A current is sourced from this pin. Placing an appropriate value external capacitor between this pin and ground allows the user to disable open lamp detection for a set period of time at start-up to allow the lamp to strike.

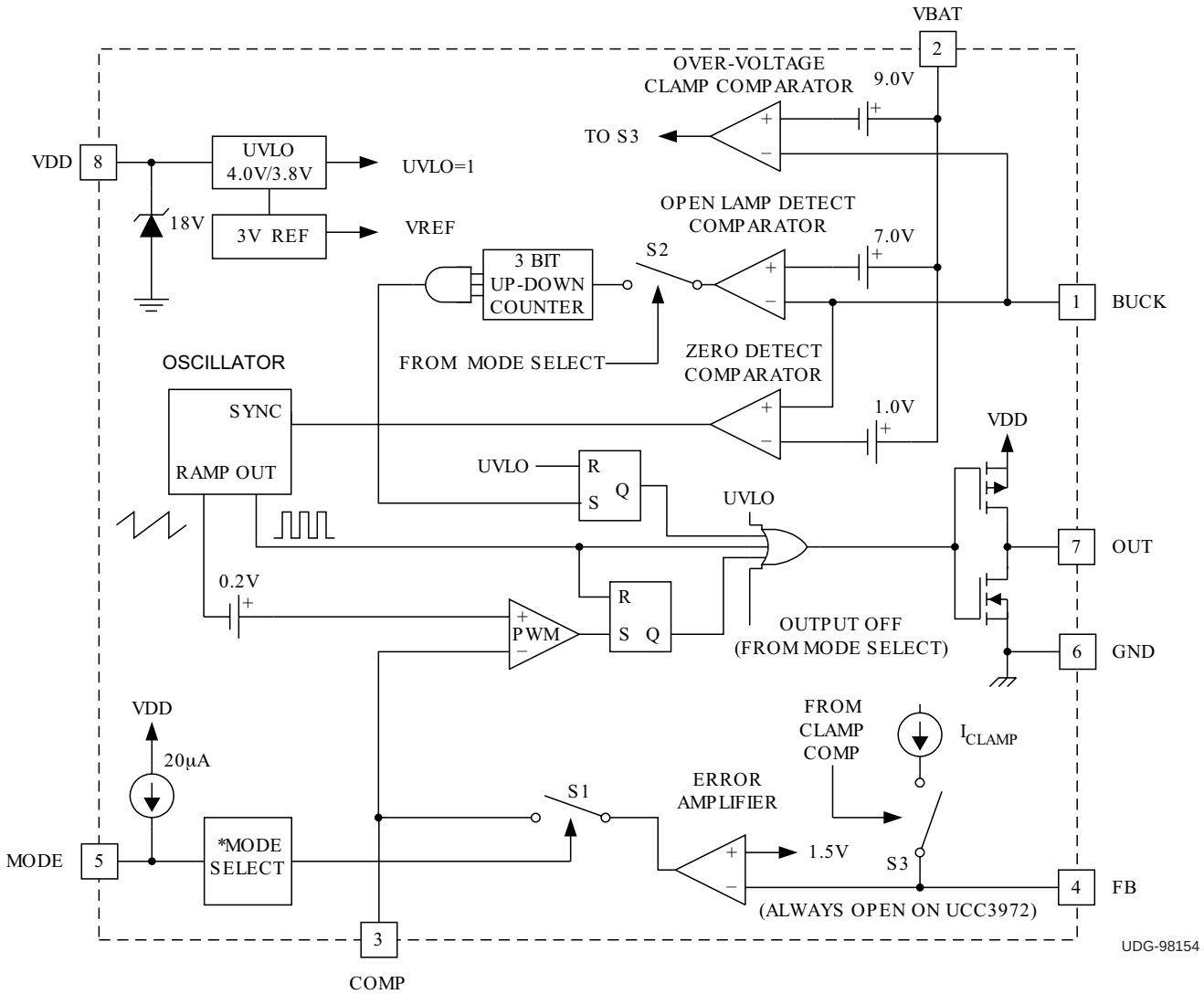
When MODE reaches 3V, open lamp detection is enabled and normal operation is activated.

OUT: Drives the buck regulator N-channel MOSFET. OUT turn-on is synchronized to twice the tank resonant frequency. OUT is actively pulled low when in UVLO, an open lamp condition has been detected or MODE is less than 1V.

VBAT: Positive input supply to power stage. This voltage is required by internal control circuitry to provide open-lamp detection and synchronization. Operating range is from 4.5V to 25V.

VDD: This pin connects to the battery voltage from which the CCFL inverter will operate. If the potential on VBAT can exceed 18V in the application, a series resistor must be placed between VBAT and this pin (see applications section). The voltage at the VDD pin will then be regulated to 18V. This pin should be bypassed with a minimum capacitance of 0.1μF.

BLOCK DIAGRAM



*MODE	Output	Open Lamp Detection	S2	Error Amplifier Output	S1
<1V	OFF	DISABLED	OPEN	DISCONNECTED FROM COMP	OPEN
1V< MODE< 3V	ON	DISABLED	OPEN	CONNECTED TO COMP	CLOSED
>3V	ON	ENABLED	CLOSED	CONNECTED TO COMP	CLOSED

APPLICATION INFORMATION

Introduction

Cold Cathode Fluorescent Lamps (CCFL) are frequently used as the backlight source for Liquid Crystal Displays (LCDs). These displays are found in numerous applications such as notebook computers, portable instrumentation, automotive displays, and retail terminals. Fluorescent lamps provide superior light output efficiency, making their use ideal for power sensitive portable applications where the backlight circuit can consume a significant portion of the battery's capacity. The backlight converter must produce the high voltage needed to strike and operate the lamp. Although CCFLs can be operated with a DC voltage, a symmetrical AC operating voltage is recommended to maintain the rated life of the lamp. Sinusiodal voltage and current lamp waveforms are also recommended to achieve optimal electrical to light conversion and to reduce high voltage electromagnetic interference (EMI). A topology that provides these requirements while maintaining efficient operation is presented below.

APPLICATION INFORMATION (cont.)

Circuit Operation

A current fed push-pull topology is used to power the CCFL backlight shown in Fig. 1. This topology accommodates a wide input voltage and dimming range while retaining sinusoidal operation of the lamp. The converter consists of a resonant push-pull stage, a high voltage output stage, and a buck pre-stage used to regulate current in the converter.

Referring to Fig. 1, the push-pull stage consists of C_{RES}, Q1, Q2, R_B, and T1's primary and auxiliary windings. The output stage consists of $C_{BALLAST}$, the lamp, the current sense resistor R_S, and T1's secondary. The resonant frequency of the tank is set by the primary inductance of T1, along with the resonant capacitor (C_{RES}), and the reflected secondary impedance. The secondary impedance includes the lamp, the ballast capacitor ($C_{BALLAST}$), the distributed winding capacitance of T1, and the stray capacitance which forms between the lamp, lamp wires, and the backlight reflector. Since the lamp impedance is nonlinear with operating current, the tank resonant frequency will vary slightly with load (typically 1.5:1).

The resonant tank consisting of C_{RES} and T1 produces sinusoidal currents (I_{RES}) and voltages and is fed by a controlled DC current (I_{BUCK}) from the buck stage. Note that the BUCK node voltage is ½ the primary tank voltage, as VBAT is located at the center tap of the transformer. The high turns ratio transformer (T1) amplifies the sinusoidal tank voltage to produce a sinusoidal secondary voltage that is divided between the lamp and ballast capacitor.

Transistors Q1 and Q2 are driven out of phase at 50 percent duty cycle with an auxiliary winding on T1. The winding provides a floating AC voltage source at the resonant frequency that is used to drive the transistor bases alternately on and off. One leg of the auxiliary winding is tied to the input voltage through base resistor R_B, which is sized to provide sufficient base current to the transistors. The transistors channel the buck inductor current into opposing ends of the tank at the resonant frequency, supplying energy for the lamp and system losses.

The buck power stage consists of inductor L_{BUCK}, MOSFET switch S_{BUCK}, and flyback diode D_{BUCK}. In order to prevent interactions between multiple switching

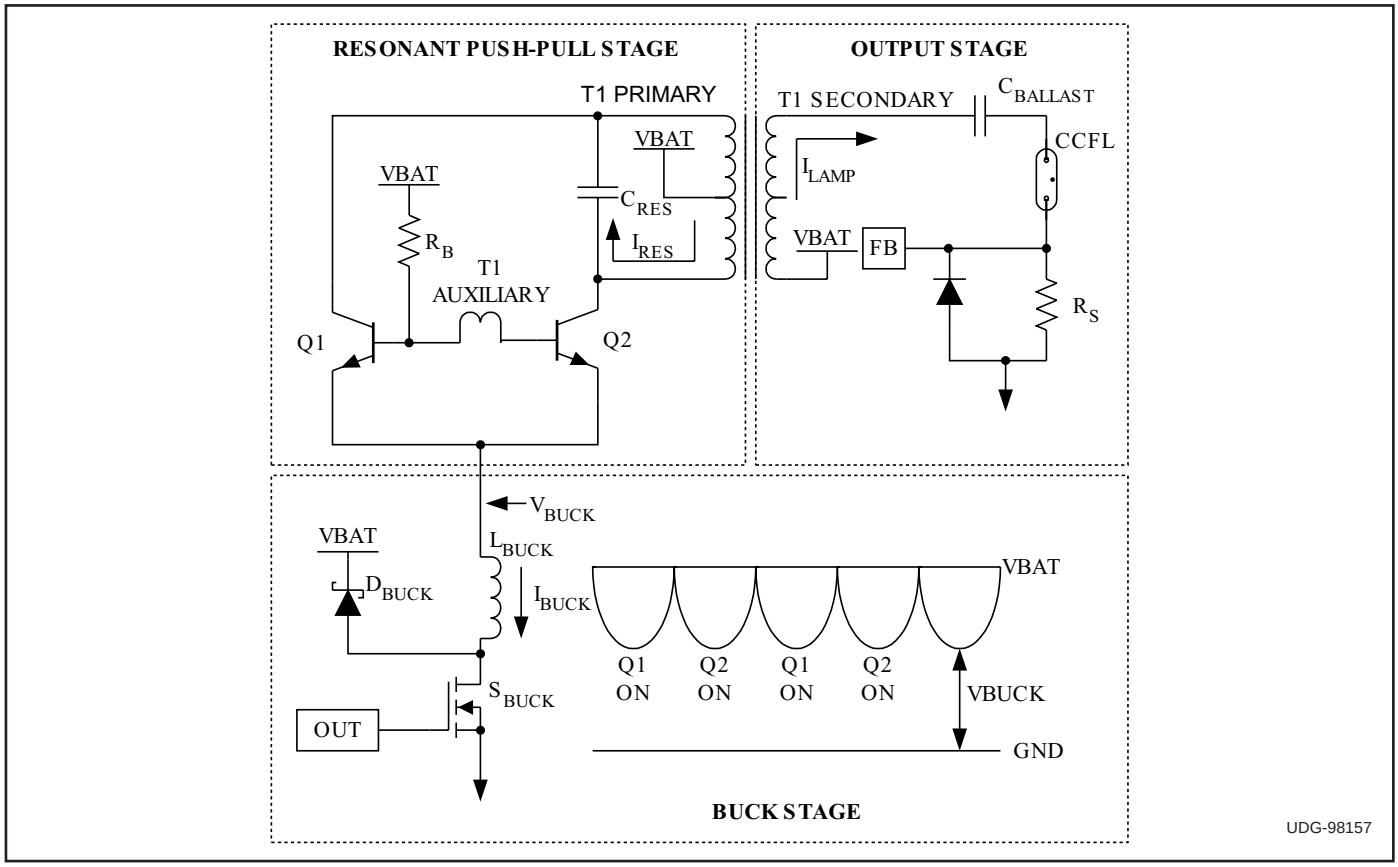


Figure 1. Push-pull, output, and buck stages.

APPLICATION INFORMATION (cont.)

frequencies, the UCC3972/3 synchronizes the buck frequency to the frequency of the push-pull stage. The traditional buck topology is inverted to take advantage of the lower $R_{DS(on)}$ characteristics of an N-Channel MOSFET switch (S_{BUCK}). With a sinusoidal voltage across the tank, the resulting output of the buck stage (V_{BUCK}) becomes a full-wave rectified voltage referenced to VBAT as shown in Fig. 1.

Lamp current is sensed directly with R_S and a parallel diode on each half cycle. The resulting voltage across the sense resistor R_S is kept at a 1.5V average by the error amplifier, which in turn controls the duty cycle of S_{BUCK}. The buck converter typically operates in continuous current mode but can operate with discontinuous current as the CCFL is dimmed.

Design Procedure

A notebook computer backlight circuit will be presented here to illustrate a design based on the UCC3972/3 controller. The converter will be designed to drive a single cold cathode fluorescent lamp (CCFL) with the following specifications:

Table 1. Lamp Specifications

Lamp Length	250mm (10”)
Lamp Diameter	6mm
Striking Voltage (20°C)	1000V (PEAK)
Operating Voltage (5mA)	375V (RMS)
Full Rated Current	5mA
Full Rated Power	1.9W

Input Voltage Range:
The notebook computer will be powered by a 4 cell Lithium-Ion battery pack with an operational voltage range of 10V to 16.8V. When the pack is being charged, the back light converter is powered from an AC adapter whose DC output voltage can be as high as 22V.

Resonant Tank and Output Circuit

The selection of components to be used in the resonant tank of the converter is critical in trading off the electrical and optical efficiencies of the system. The value of the output circuit’s ballast capacitor plays a key role in this trade-off. The voltage across the ballast capacitor is a function of the resonant frequency and secondary lamp current:

$$V_{CB} = \frac{I_{LAMP}}{2 \bullet \pi \bullet C_{BALLAST} \bullet F_{RESONANT}} \quad (1)$$

A voltage drop across $C_{BALLAST}$ many times the lamp voltage will make the secondary current insensitive to distortions caused by the non-linear behavior of the lamp, providing a high impedance sinusoidal current source with which to drive the CCFL. This approach improves the optical efficiency of the system, as capacitive leakage effects are minimized due to reduced harmonic content in the voltage waveforms. Unfortunately, from an electrical efficiency standpoint, an increased tank voltage produces increased flux losses in the transformer and increased circulating currents in the tank. In practice, the voltage drop across the ballast capacitor is selected to be approximately twice the lamp voltage (750V in our case) at rated lamp current. Assuming a 50kHz resonant frequency and 5mA operating current, a ballast capacitance of 22pF is selected. Since the lamp and ballast capacitor impedance are 90 degrees out of phase, the vector sum of lamp and capacitor voltages determine the secondary voltage on the transformer.

$$V_{SEC} = \sqrt{\left(V_{CB}\right)^2 + \left(V_{LAMP}\right)^2} \quad (2)$$

The resulting secondary voltage at rated lamp current is 820V. Since the capacitor dominates the secondary impedance, the lamp current maintains a sinusiodal shape despite the non-linear behavior of the lamp. As the CCFL is dimmed, lamp voltage begins to dominate the secondary impedance and current becomes less sinusiodal. Transformer secondary voltage is reduced, however, so high frequency capacitive losses are less pronounced. The value of ballast capacitor has no effect on current regulation since the average lamp current is sensed directly by the controller.

Once the ballast capacitor is selected, the resonant frequency of the push-pull stage can be determined from the transformer’s inductance (L), turns ratio (N), and the selection of resonating capacitor (C_{RES}).

$$F_{RESONANT} = \frac{1}{2\pi \sqrt{L_{PRIMARY}\left(C_{RES} + \left(N^2 \bullet C_{BALLAST}\right)\right)}} \quad (3)$$

Output distortion is minimized by keeping the independent resonant frequencies of the primary and secondary circuits equal. This is achieved by making the resonant capacitor equal to the ballast capacitance times the turns ratio squared:

$$C_{RES} = N^2 \bullet C_{BALLAST} = (67)^2 \bullet 22pF = 0.1\mu F \quad (4)$$

The resulting resonant frequency is about 50kHz, this frequency will vary depending upon the lamp load and amount of stray capacitance in the system. Since the UCC3972/3 has an internal oscillator, it is important that

APPLICATION INFORMATION (cont.)

the operating frequencies of a particular design are within the synchronizable frequencies of the controller.

Component Selection for the Resonant Tank and Output Circuit

Since high efficiency is a primary goal of the backlight converter design, the selection of each component must be carefully evaluated. Losses in the ballast capacitor are usually insignificant, however, its value determines the tank voltage which influences the losses in the resonant capacitor and transformer. Since the resonant capacitor has high circulating currents, a capacitor with low dissipation factor should be selected. Power loss in the resonant tank capacitor will be:

$$C_{RES\_LOSS}(watts) = \left(V_{TANK}\right)^2 \bullet 2\pi \bullet F_{RESONANT} \bullet C_{RES} \bullet Dissipation\ Factor \quad (5)$$

Polypropylene foil film capacitors give the lowest loss; metalized polypropylene or even NPO ceramic may give acceptable performance in a lower cost surface mount (SMT) package. Table 2 gives possible choices for the resonant and high voltage ballast capacitors.

The transformer is physically the largest component in the converter, making the tradeoff of transformer size and efficiency a critical choice. The transformer's efficiency will be determined by a combination of wire and core losses. A Coiltronics transformer (CTX110600) was chosen for this application because of its small size, low profile, and overall losses of about 5% at 1W. Low profile CCFL transformers are also available from Toko (847)-297-0070 in Mt. Prospect, IL or Sumida (408)-982-9660 in Santa Clara, CA.

Wire losses are determined by the RMS current and the ESR of the windings. The primary winding resistance for the Coiltronics transformer is 0.16Ω. The RMS current of the primary winding includes the sinusoidal resonant current and the DC buck current on alternate half cycles (i.e. only ½ of the primary winding sees the buck current depending upon which transistor is on). Maximum resonant current is equal to:

$$I_{RES} = \frac{V_{PRIMARY}}{\sqrt{\frac{L_{PRIMARY}}{C_{RES}}}} = \frac{820}{67 \bullet \sqrt{\frac{44}{0.1}}} = 600\,mA \quad (6)$$

Buck inductor current is calculated in the next section. Secondary current is simply the lamp current, the secondary winding has 176Ω of resistance.

Core losses are a function of core material, cross sectional area of the core, operating frequency, and transformer voltage. For ferrite material, the hysteresis core losses increase with voltage by a cubed factor; for a given core cross sectional area, doubling the tank voltage will cause the losses to increase by a factor of 8. This makes the selection of the ballast capacitor a critical decision for efficiency.

Other elements influencing the resonant tank and output circuit efficiency include the push-pull transistors, the base drive and sense resistors, as well as the lamp. High gain low V_{CESAT} bipolar transistor such as Zetek's FZT849 allow high efficiency operation of the push-pull stage. These SOT223 package parts have a typical current transfer ratio (h_{FE}) of 200 and a forward drop (V_{CESAT}) of just 35mV at 500mA. Rohm's 2SC5001 transistors provide similar performance. For low power, size sensitive applications, a SOT23 transistor is available from Zetek (FFMT619) with approximately twice the forward drop at 500mA. The base drive resistor R_B is sized to provide full V_{CE} saturation for all operating conditions assuming a worst case h_{FE}. For efficiency reasons, the base resistor should be selected to have the highest possible value. A 1kΩ resistor was selected in this application. Losses scale with buck voltage as:

$$R_{B(LOSS)} = \frac{V^2_{BUCK}}{R_B} \quad (7)$$

Table 2. Capacitor selection

Manufacturer	Capacitance Type	Series	Dissipation Factor (1kHz)
Ballast Capacitor			
Cera-Mite (414) 377-3500	High Voltage Disk Capacitor (3kV)	564C	
NOVA-CAP (805) 295-5920	SMT 1808 (3kV)	COG	
Murata Electronics	SMT 1808 (3kV)	GHM	
Resonant Capacitor			
Wima (914)347-2474	Polypropylene foil film FKP02	FKP02	0.0003
	Metalized Polypropylene	MKP2	0.0005
	SMT Metalized polyphenylene-sulfide	MKI	0.0015
Paccom (800)426-6254	SMT Metalized polyphenylene-sulfide	CHE	0.0006
NOVA-CAP	SMT Ceramic	COG	0.001

APPLICATION INFORMATION (cont.)

The current sense resistor R_S provides direct control of lamp current. Since the current sense resistor voltage is controlled to a 1.5V reference, its power loss is inversely proportional to its value at a given lamp current.

Synchronizing the Stages

An internal comparator at the BUCK node is used to synchronize the PWM buck frequency to twice the resonant tank frequency. Synchronization is accomplished with sync pulse that is generated each time the BUCK node voltage is within 1.0V of VBAT; the UCC3972/3 uses this sync pulse to reset the PWM oscillator's saw-tooth ramp. The syn circuit will operate at 2 X the transform switching frequency.

Buck Stage Design

The PWM output controls current in the buck inductor. The UCC3972/3's buck power stage differs from a traditional buck topology in a few respects:

- The topology is inverted using a ground referenced N-Channel MOSFET rather than a VDD referenced P-Channel.
- The output voltage is a full wave rectified sinewave at the switching frequency, rather than DC.

Referring back to Fig. 1, when OUT turns S_{BUCK} on, the BUCK node voltage V_{BUCK} is placed across the inductor. This voltage is typically positive and current ramps up in the inductor (it is possible for the BUCK node voltage to go negative if VBAT is low and the lamp current is near maximum). When S_{BUCK} is turned off, VBAT-V_{BUCK}+V_{DBUCK} is placed across the inductor with opposite polarity. As with any buck converter, the volt-seconds across the inductor must be reversed on each switching cycle to maintain constant current. The duty cycle (D) relationship is complicated somewhat by the fact the output voltage is changing within a switching cycle. The equations below determine the relationship between on and off times in continuous conduction mode where T is the switching period, D = t_{ON}/T, and t_{OFF} = T-t_{ON}.

$$\int_0^{t_{ON}} V_{BUCK} \bullet dt = \int_{t_{ON}}^{T} \left(VBAT - V_{BUCK} + V_D\right) \bullet dt \quad (8)$$

Selecting the buck inductor:
Maximum ripple current in the inductor occurs when frequency and duty cycle are at a minimum, which corresponds to VBAT and lamp current being a maximum. The average value of V_{BUCK} at rated lamp current is equal to:

$$V_{BUCK\_AVE} = V_{BAT} - \frac{V_{SEC} \bullet \sqrt{2}}{N \bullet \pi} \quad (9)$$
$$= V_{BAT} - \frac{820 \bullet \sqrt{2}}{67 \bullet \pi} = V_{BAT} - 5.5 \bullet Volts$$

The approximate on time using the maximum 22V input voltage (V_{BUCK_AVE} = 16.4), a 100kHz switching frequency (two times the resonant frequency), and ignoring the diode drop can be calculated from the following:

$$\frac{t_{ON}}{T - t_{ON}} = \frac{VBAT - V_{BUCK\_AVE}}{V_{BUCK\_AVE}} \quad (10)$$

The resulting on time is 2.5µs. A 150µH inductor will result in a peak to peak ripple current of 280mA. Average inductor current (with maximum lamp current) can be calculated by taking the lamp power divided by the tank efficiency and the RMS buck voltage.

$$I_{BUCK} = \quad (11)$$
$$\left(\frac{V_{LAMP} \bullet I_{LAMP}}{Efficiency}\right) \bullet \left(\frac{2 \bullet N}{V_{SEC}}\right) = \frac{375 \bullet 0.005 \bullet 2 \bullet 67}{0.8 \bullet 820}$$
$$= 380\,mA$$

The resulting inductor ripple is less than 50%. A list of possible inductors are given below along with ESR and current rating (losses in the inductor are calculated with RMS current).

The choice of a MOSFET for the buck switch should take into consideration conduction and switching losses. The $R_{DS(on)}$ and gate charge are typically at odds, however, where minimizing one will typically result in the other increasing. An International Rectifier IRFL014 was selected (SOT-223 package) in this application with a gate charge of 11nC and $R_{DS(on)}$ of 0.2Ω. A Schottky diode should be used for the buck diode in order to minimize forward drop.

Table 3. Inductor Suppliers

Vendor	L	Part Number	ESR	Current Rating
Coilcraft (847) 639-6400	150µH	DO3316-154	0.38	1A
Coiltronics (407) 241-7876	150µH	CTX150-4	0.175	0.72A
Sumida (847) 956-0666	150µH	CDR125-151	0.4	0.85A
Toko (847) 297-0070	150µH	646CY-151	0.73	0.4A

APPLICATION INFORMATION (cont.)

Dimming Techniques

Analog Dimming:

A control circuit that implements analog dimming with a potentiometer (R_{ADJ}) is shown in Fig. 2. When the secondary has a positive polarity current, D1 is reversed biased and lamp current is sensed directly through R_L and R_{ADJ}. When the current reverses direction, D1 conducts and the voltage on the sense node V_X is clamped to the forward drop of the diode. The resulting waveform at V_X is a half wave rectified sinusoid whose voltage is proportional to lamp current.

$$I_{LAMP} = \frac{\left[1.5 + \frac{V_D}{2}\right]\pi}{\sqrt{2}\left(R_L + R_{ADJ}\right)} \quad (12)$$

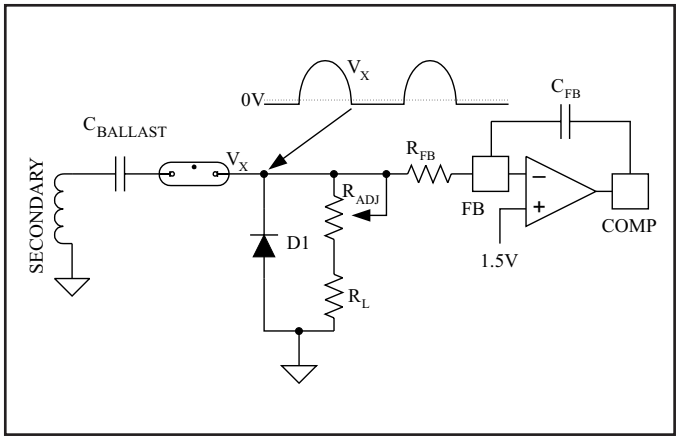


Figure 2. Analog dimmer with potentiometer.

This voltage is averaged by the feedback components (R_{FB}, C_{FB}) and held to 1.5V by the error amplifier when the control loop is active. The resulting voltage at the output of the error amplifier (COMP) sets the duty cycle of PWM stage. Average lamp current is controlled by adjusting R_{ADJ} to the appropriate value. Resistor R_L sets the high current level of the lamp.

Analog Dimming by PWM or D/A Control Signal:

Analog dimming control of the lamp can be achieved by providing a digital pulse stream (or DC control voltage) from the system microprocessor as shown in Fig. 3. For this technique, the lamp current sense resistor (R1) is fixed and the V_X node voltage is averaged against the digital pulse stream of the microprocessor. The averaging circuit consists of R2, R3, and C_{FB}. A higher average value from the pulse stream will result in less average lamp current. The frequency of the digital pulse stream should be high enough to maintain a constant DC value across the feedback capacitor. If a D/A converter is available in the system, a DC output can be used in place of the pulse stream.

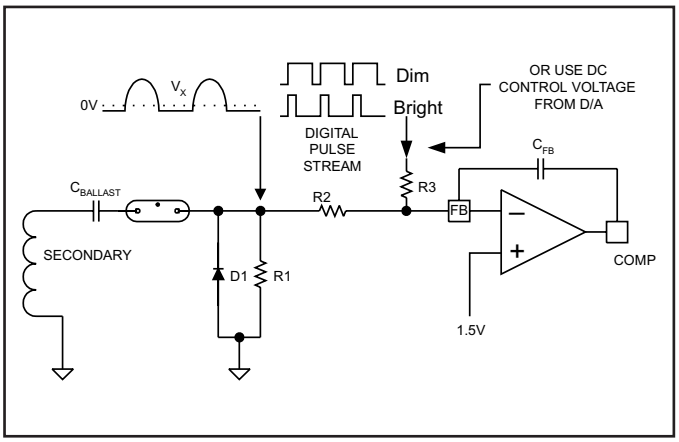


Figure 3. Analog dimming control from micro- processor.

Low Frequency Dimming (LFD):

Analog dimming techniques described previously can provide excellent dimming over a 10:1 range, depending upon the physical layout and the amount of stray capacitance in the backlight's secondary circuitry. Beyond this level the lamp may begin to exhibit the "thermometer effect" causing uneven illumination across the tube.

Low frequency dimming (LFD) is accomplished by operating the lamp at rated current and gating the lamp on and off at a low frequency. Since the lamp is operated at full intensity when on, the system layout has little effect on dimming performance. The average lamp intensity is a function of the duty cycle and period of the gating signal. The duty cycle can be controlled to a low minimum value, allowing a very wide dimming range. Low frequency dimming can be implemented by summing a PWM signal into the feedback node to turn the lamp off as shown in Fig. 4. A 68kΩ resistor is used for R_{FB} and R_{LFD}, C_{FB} is reduced to 6.8nF to speed up the lamp re-strike. The repetition rate of the signal should be greater than 120Hz to avoid visible flicker.

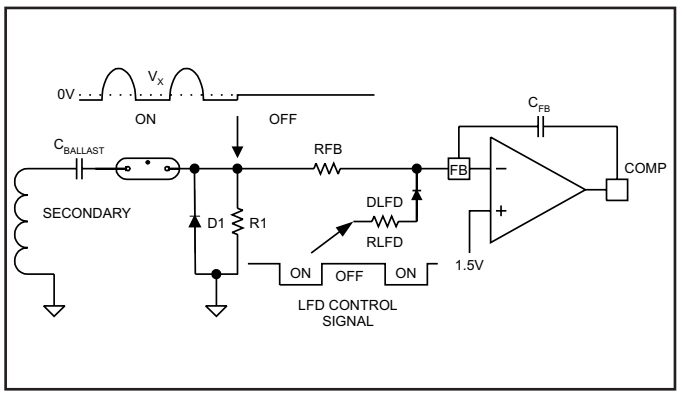


Figure 4. Low frequency dimming by forcing lamp current off through the FB pin.

APPLICATION INFORMATION (cont.)

Referring to Fig. 5, at time t0 the control signal is brought low and the voltage in the resonant tank begins to build. At time t1 there is sufficient voltage for the lamp to strike and the feedback loop controls the lamp at rated current using a fixed current sense resistor. When the LFD signal is brought low at time T2, the COMP output is low and the OUT pin stops switching. The resonant tank voltage decays until the lamp extinguishes. If the on time were extended to t3 the average lamp intensity would be increased accordingly, the next low frequency cycle begins at time t4.

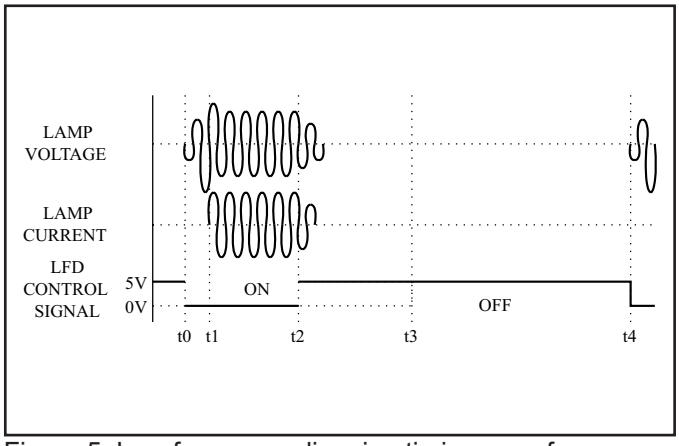


Figure 5. Low frequency dimming timing waveforms.

The time relationship between the resonant and gating frequency has been exaggerated so that the sinusoidal waveforms can be depicted. In order to avoid visible lamp flicker, the low frequency gating rate (t0-t4) should be greater than 100Hz. To prevent "beat" frequency interference, it may be advantageous to synchronize the gating frequency to a multiple of the monitor scan rate of the LCD display. This can be accomplished by controlling the duty cycle with a timer routine within the LCD's software program.

LFD waveforms at 200Hz and 50% duty cycle are shown in Fig. 6a. Fig. 6b show a time expanded photo of the same waveforms. Channel 1 is lamp voltage at 500V /div, Channel 2 is lamp current at 20mA / div, and Channel 3 is the LFD control voltage. Since the photos are from a digital oscilloscope, alias exists in the waveforms.

Lamp Current Control Loop

The current control loop for the CCFL circuit is discussed in detail in Unitrode Application Note U-148 and is briefly repeated here for completeness. A block diagram for the current control loop is shown in Fig. 7.

The PWM modulator small signal gain is inversely proportional to the internal saw tooth ramp and proportional to the input voltage (the inductor's current slope increases as VBAT increases). The resonant tank and buck inductor form a RLC filter at the center point of the push pull transformer. The effective L of the filter is dominated by buck inductor and the effective C is approximately 8 times the resonant capacitor (C_{RES}) value. This occurs because the reflected ballast capacitance is equal to C_{RES} and the equivalent capacitance at the push-pull center point is four times the capacitance across the tank. The equivalent resistance at the push-pull center point is equal to ¼ the tank voltage squared divided by the lamp power. The corner frequency and Q of the filter are:

$$F_{CORNER} = \frac{1}{2\pi\sqrt{L_{BUCK} \bullet 8 \bullet C_{RES}}} \quad (13)$$

$$Q = \frac{2\pi F_{FILTER} L_{BUCK}}{R_{FILTER}} \quad (14)$$

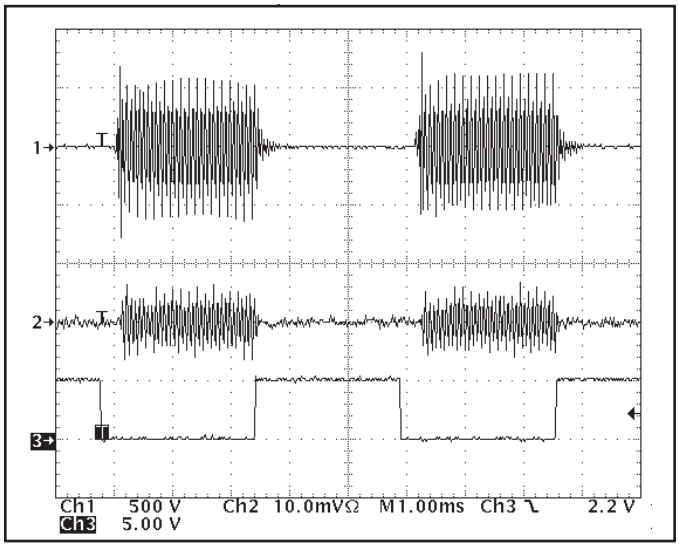


Figure 6a. LFD at 50% duty cycle.

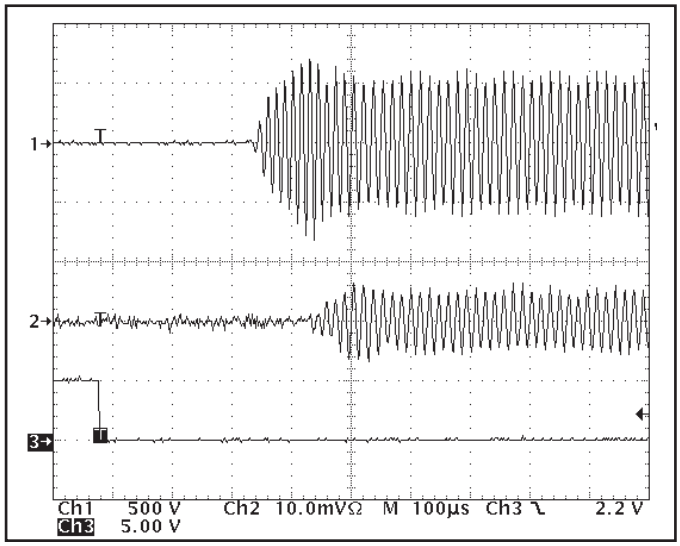


Figure 6b. Time expanded showing lamp strike and feedback delay.

APPLICATION INFORMATION (cont.)

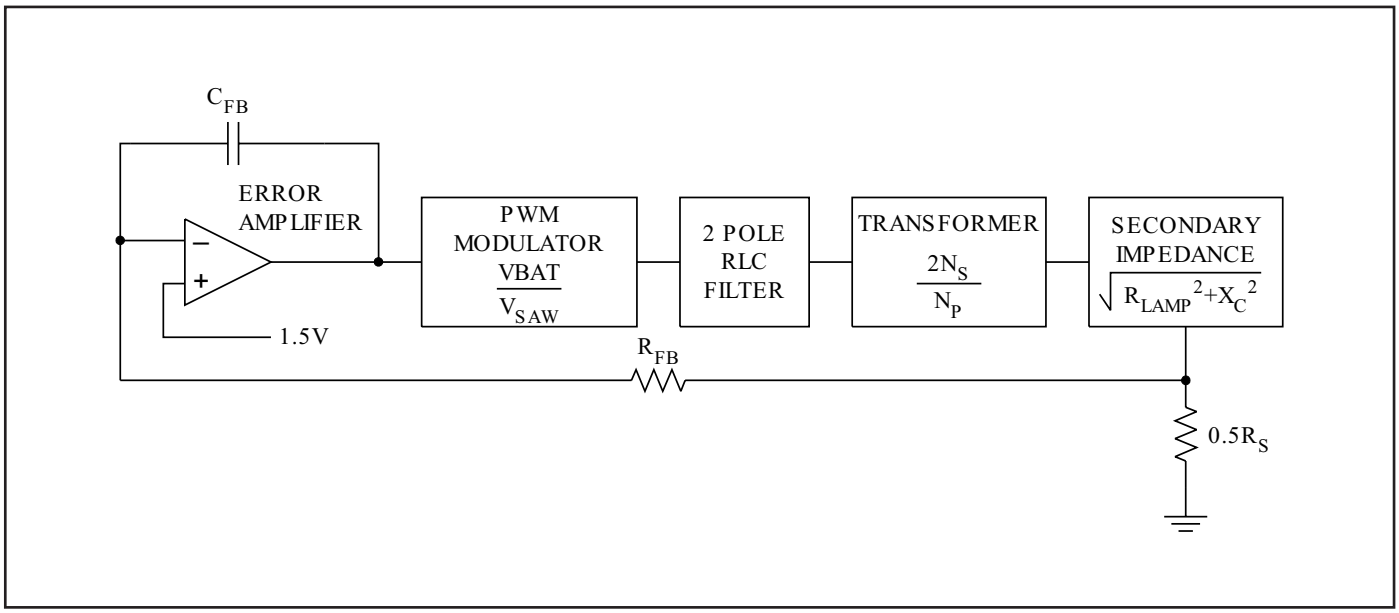


Figure 7. Current control loop block diagram.

The resulting gain of the filter is unity below the 15kHz corner frequency, peaking up at the corner frequency with Q, and rolling off with a 2-pole response above the corner frequency. As shown in Fig. 7, the transformer turns ratio provides a voltage gain and the output circuit (whose impedance includes the lamp and ballast capacitor) converts the voltage into a current. The current sense resistor produces a voltage on each half cycle, leaving the error amplifier as the final gain block.

Loop gain is greatest at minimum lamp current and maximum input voltage. With a 22V input, a 2V saw-tooth, and 1:67 turns transformer, the low frequency voltage gain of the PWM, RLC filter, and Transformer is 1500. With a 375V lamp and 1mA of lamp current (using a 22pF ballast capacitor and 50kHz switching frequency) the secondary impedance is 400kΩ. R_{SENSE} at 1mA is 4kΩ (equation 12), resulting in a low frequency power loop gain of 7.5. The error amplifier is configured as an integrator, giving a single pole roll-off and a high gain at DC. A 68k resistor and 33nF capacitor give a 70Hz crossover frequency for the feedback network, yielding a maximum crossover frequency of 500Hz for the total loop avoiding stability problems with the Q of the resonant tank. For 5mA of lamp current with a 22V input the total loop crossover is 200Hz, for low frequency dimming applications C_{FB} can be reduced to 6.8nF with no instability (1kHz crossover).

Striking the Lamp

Before the lamp is struck, the lamp presents an impedance much larger than the ballast capacitor and the full output voltage of the transformer secondary is across the lamp. Since the buck converter must reverse the volt-seconds on the buck inductor, the average tank voltage at the primary can be no greater than the DC input voltage. This constraint along with the turns ratio of the push-pull transformer sets the peak voltage available to strike the lamp:

$$V_{STRIKE} = N_{S:P} \bullet \pi \bullet V_{INPUT} \quad (15)$$

The Coiltronics transformer has a 67:1 turns ratio, giving 2100 peak volts available to strike the lamp with the minimum 10V input. In our example this is more than sufficient for the 1000V required to strike the lamp. With the 22V maximum charger input, the available striking voltage could theoretically reach 5000V! The possibility of breaking down the transformer's secondary insulation becomes a real concern at this voltage.

Voltage Clamp Circuit (UCC3972)

An external voltage clamp circuit consisting of D4, Q4, R7, R8, and R9 can be added to the typical application circuit as shown in Fig. 8. This circuit limits the maximum transformer voltage during startup, allowing an extended time period for striking the lamp while protecting the transformer from over voltage. For fixed input voltage designs, this circuit is optional since the transformer turns can be optimized at one voltage.

APPLICATION INFORMATION (cont.)

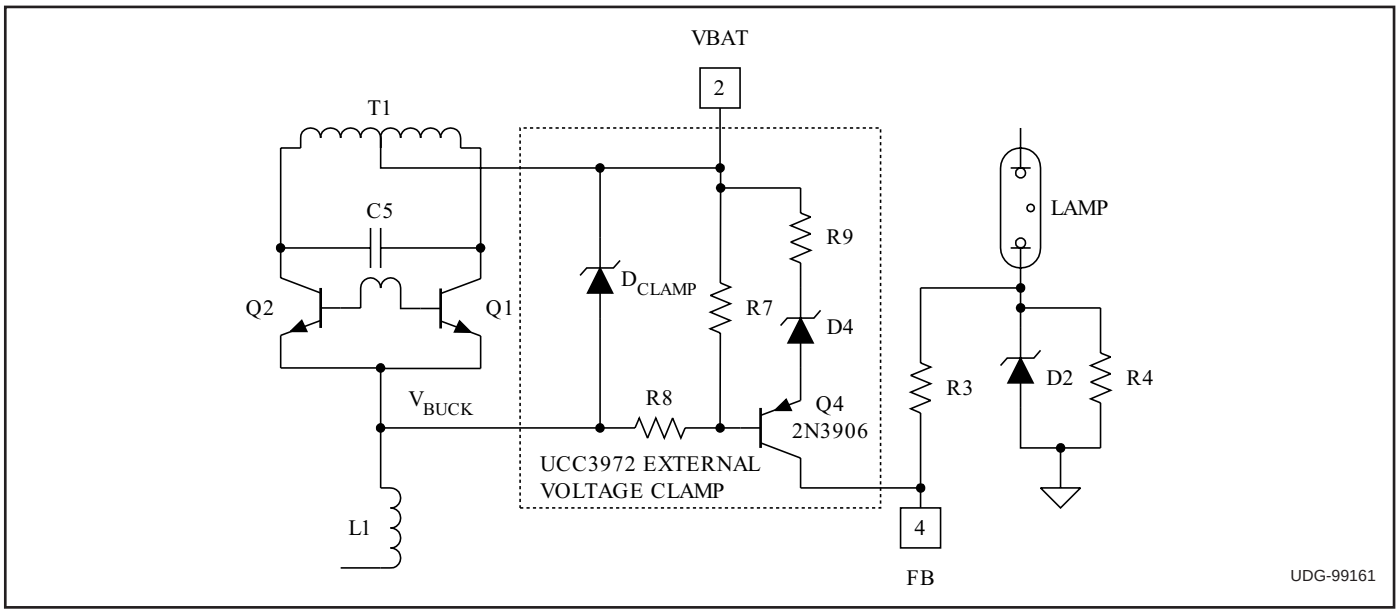


Figure 8. Optional voltage clamp circuit. For UCC3972. (Not required for UCC3973)

The clamp circuit works as follows:
If the voltage at the base of Q4 is equal to the zener (D4) voltage plus the V_{BE} of Q4, the clamp circuit will activate limiting the voltage in the resonant tank. When the clamp activates, Q4 is turned on and additional current (set by R9) is allowed into the feedback capacitor. The peak clamp voltage is given by:

$$V_{CLAMP} = V_{IN} - V_{BUCK} = \frac{R7+R8}{R7} \bullet \left(V_{ZENER} + V_{BEQ4}\right) \; PEAK \qquad (16a)$$

Internal Voltage Clamp Circuit for UCC3973

The over-voltage function is provided internally on the UCC3973. As shown in the block diagram of the UCC3972/3, an internal comparitor monitors the instantaneous voltage between VBAT and BUCK. If this voltage exceeds the over-voltage clamp level (9V nominal), a current will be sourced from the FB pin to reduce duty cycle. The source current level increases with over-voltage, but is typically 100μA at the threshold voltage. As with the Open Lamp Trip Level, the Voltage Clamp Threshold is programmed with external resistors R10 and R11.

$$V_{CLAMP} = \left(\frac{R10+R11}{R10}\right) \bullet 9V_{PEAK} \qquad (16b)$$

A 2k resistor for R10 and a 1k resistor for R11 will result in a peak (VBAT–V_{BUCK}) level of 13.5V. With a 1:67 turns ration transformer, the secondary voltage will be clamped to 1280 V_{RMS}.

The FB pin source current is disabled in the UCC3972.

An optional zener diode D_{CLAMP} can be added to either UCC3972 or UCC3973 designs as shown in Fig. 8. The zener provides a high speed clamp when power is initially applied to the circuit and before the voltage clamp can regulate the feedback loop. D_{CLAMP} can be a small 250mW zener since it will only conduct for a few resonant cycles before the voltage clamp takes effect. D_{CLAMP}'s value should be a few volts greater than the voltage clamp.

Setting the Time Period for Blanking Open Lamp Detection

A capacitor on the MODE pin of the UCC3972/3 is used to blank the open lamp protection circuitry during the initial lamp startup. When the IC is initially powered-up, a 20μA current out of the MODE pin charges the capacitor C_{MODE} from ground potential. Since the PWM output is disabled when the MODE pin is between 0V-1V, open lamp blanking occurs as C_{MODE} is charged from 1V-3V, giving a soft start period of:

$$T_{SS} = \frac{C_{MODE}}{10\mu F} \bullet SEC \qquad (17)$$

The time required for lamp strike is application dependent, and a 10μF capacitor allows 1 second in which to strike the lamp. Fig. 9 shows the voltage at the V_{BUCK} node with a 20V input and a 13.5V peak level for the internal voltage clamp (UCC3972 requires and external clamp) under an open lamp fault condition. After the 1 second period, the open lamp detection circuit trips and the UCC3972/3 shuts down until power is cycled on the chip.

APPLICATION INFORMATION (cont.)

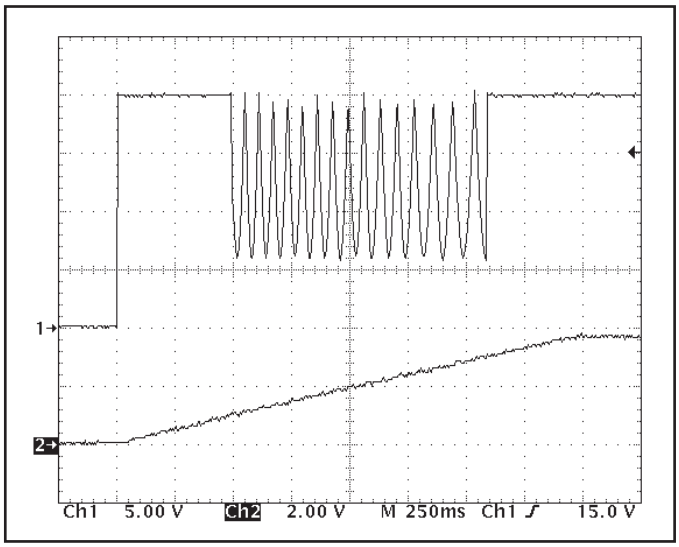


Figure 9. V_{BUCK} and MODE pin voltages during an open lamp fault start-up.

Normal Startup

In practice, the lamp will typically strike in much less than 1 second (usually within the first few cycles) and the voltage at the transformer voltage will collapse to below the open lamp trip level. Difficulty in striking the lamp usually results from one or a combination of the following:

Insufficient transformer turns ratio or input voltage.

Increase in required striking voltage at cold temperature.

The lamp has set for a long period of time.

Transformer secondary voltage is reduced due to voltage division between parasitic secondary capacitance and the ballast capacitor.

Setting the Open Lamp Trip Level

The buck voltage is monitored by an internal 7V comparator to detect an open lamp. The actual trip voltage across the resonant tank is set with an external resistor divider R10 and R11.

$$V_{OPENLAMP} = V_{IN} - V_{BUCK} = \left(\frac{R10+R11}{R10}\right) \bullet 7V \quad PEAK \tag{18}$$

R10 and R11 should be in the 1kΩ-5kΩ range, to guarantee sharp zero crossing edges at the buck pin of the IC. In most applications the peak clamp voltage would be set to a higher level than the open lamp trip voltage, ensuring the converter would shut down after the one second blank time if a true open lamp existed. If the open lamp voltage is increased, the peak clamp circuit voltage (equation 16) would need to be increased accordingly. A peak VBAT-Vbuck voltage of 10.5V has been set for open lamp detection in this example. (R10 = 2k, R11 = 1k).

Voltage Regulator

The UCC3972/3 controller contains an internal 18V shunt regulator that provides a 5% accurate voltage clamp for the MOSFET gate drive while allowing the controller to operate in applications with input voltages up to 25V. Since only the VBAT and BUCK pins are rated for 25V, the shunt regulator limits the voltage on the VDD and OUT pins to 18V. The MODE, CS, and COMP pin voltages are typically less than 5V. If the UCC3972/3 is to be used in an application with input voltages greater than 18V, a resistor from VBAT to VDD is required to limit the current into the VDD pin. The resistor should be sized to allow sufficient current to operate the controller and drive the external MOSFET gate, while minimizing the voltage drop across the resistor. A bypass capacitor should be connected at the VDD pin to provide a constant operating voltage.

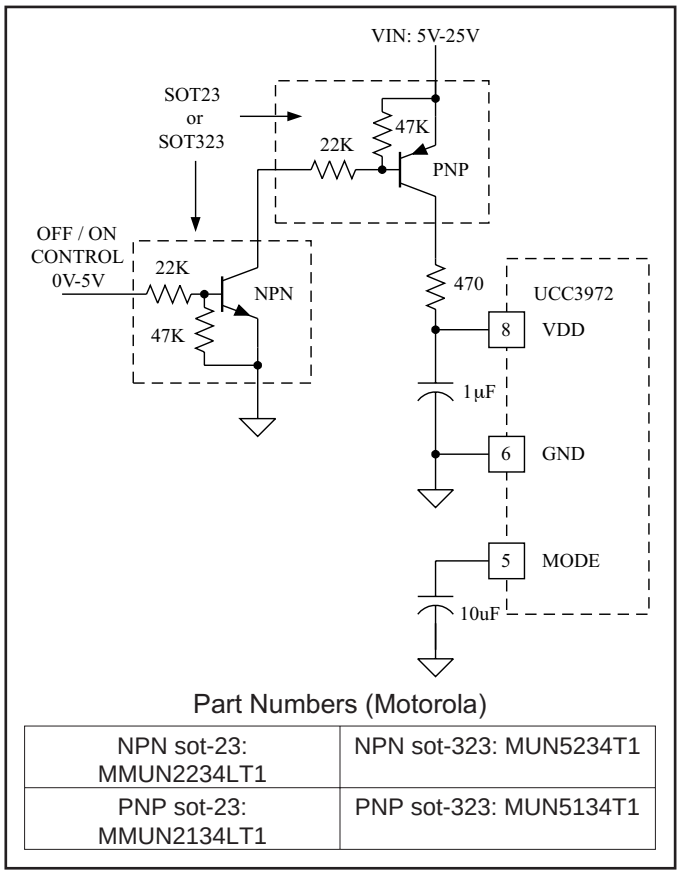
Selecting the Shunt Resistor:
The first step in selecting the shunt resistor is to determine the current requirements for the application. With a 100kHz switching frequency and a maximum gate charge of 11nC for the IRFL014 , the gate drive circuit requires 1.1mA of average current. The UCC3972/3 requires an additional maximum quiescent current of 1.5mA. The shunt resistor must therefore supply 2.6mA of current over the operating voltage of the part.

The application's maximum input voltage is 22V. With a regulator clamp voltage of 18V, the maximum value for the shunt resistor becomes 1.5kΩ [(22-18)V/2.6mA]. This resistor will minimize losses at maximum input voltage, but could produce a 4V drop (from VBAT to VDD) even when the regulator is not clamped. This drop reduces the available gate drive voltage, leaving only 6V with the minimum input voltage of 10V. Since the efficiency of the shunt regulator is not of primary importance when the charger is running, a smaller value of shunt resistor is selected to improve the available gate drive voltage. A 470 shunt resistor will produce a maximum 1.2V drop from VBAT to VDD when the shunt regulator is not clamped. When the regulator is clamped at 18V and the charger voltage is at its maximum of 22V, the power across the shunt resistor will be 35mW [(4V x 4V)/470].

APPLICATION INFORMATION (cont.)

Low Current Shutdown Circuit:

Since the shunt regulator circuitry needs to remain active, even when the MODE pin is less than 1V and the output is not switching, a low current shutdown is not provided in the UCC3972/3. The following is a simple on/off control requiring only two transistors with internal bias resistors to disconnect V_{IN} providing a low current shutdown. VBAT and BUCK pins will consume a small current in this mode because they have 430kΩ of internal resistance.



Part Numbers (Motorola)

NPN sot-23: MMUN2234LT1	NPN sot-323: MUN5234T1
PNP sot-23: MMUN2134LT1	PNP sot-323: MUN5134T1

Figure 10. Optional low current shutdown circuit.

Cold Cathode Lamp Characteristics

Before beginning a CCFL converter design, it is important to become familiar with the characteristics of the lamp. The lamp presents a non-linear load to the converter resulting in unique voltage vs. current (VI) characteristics. The length, diameter, and physical construction of the lamp determine its performance, and thus impact the design of the converter. Fig. 11 shows the VI characteristics collected from various lengths of 6mm diameter lamps, where Fig. 12 shows the characteristics of several 3mm-diameter lamps.

It is interesting to note how the operating and striking voltages (V_{STRIKE}) of the lamps are related to length as well as lamp diameter. Since equal length CCFLs of different diameters have about the same lumens per watt efficiency, the smaller diameter lamps actually produce more light when driven at a given current since they operate at a higher voltage. The lamps have regions of positive and negative resistance with the voltage peaking at 4mA for the 6mm diameter lamps and at 1mA for the 3mm diameter lamps.

In order to successfully dim the lamp, the converter's resonant tank and step up transformer must provide enough voltage to keep the lamp operating over the whole range of operating current, this requirement becomes more difficult with longer length and smaller diameter lamps. Since the lamp characteristics will vary with the manufacturing technique, it is a good idea to collect data from several lamp manufacturers and to include design margin for process variations.

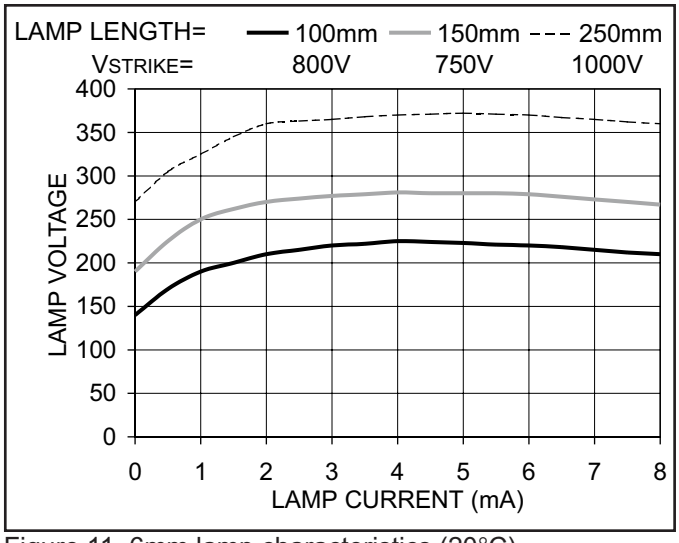


Figure 11. 6mm lamp characteristics (20°C).

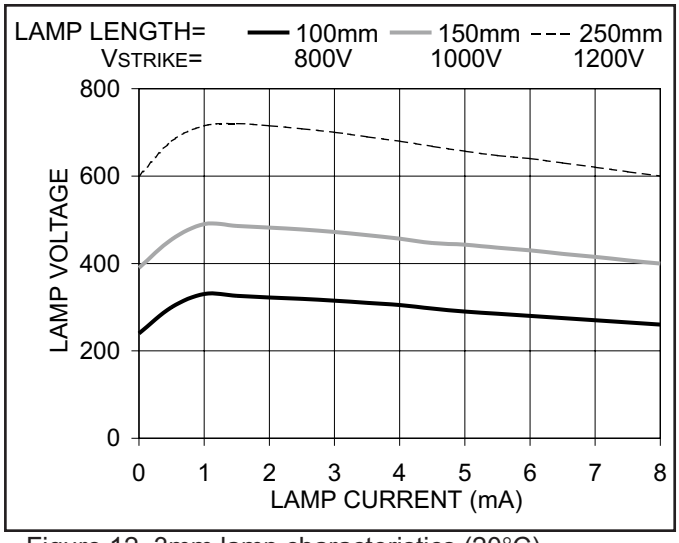


Figure 12. 3mm lamp characteristics (20°C).

APPLICATION INFORMATION (cont.)

Since a fluorescent lamp is a pressurized gas filled tube (usually Argon and Mercury vapor), it shouldn't be surprising that temperature plays a major role in the lamp characteristics. Fig. 13 depicts the variations in striking and operating voltage for a 150 x 3mm lamp over temperature, illustrating the importance of taking temperature effects into account when designing the converter. The lumen output of the backlight system is temperature dependent as well, and may need to be accounted for in applications requiring tight lumens regulation over a wide temperature range. Fig. 14 shows the temperature effects on lumens for the lamp operated at 5mA.

Since lamp current is roughly proportional to luminosity, it may be tempting to operate the lamp at a RMS current higher than specified in the manufacturer's data sheet. While the lamp will continue to operate tens of percent above the rated current, the luminosity gain becomes less pronounced as the lamp is over-driven as shown in Fig. 15. The expected life of the lamp will also degrade, as illustrated in Fig. 16, when the lamp is operated above rated current.

Cold Cathode Fluorescent Lamp Efficiency Trade-Offs

Although CCFLs offer high output light efficiency compared to other lamp types such as incandescent, only a percentage of the input energy is converted to light. As illustrated in Fig. 17, 35% of the energy is lost in the electrodes, 26% as conducted heat along the tube. A portion of the Ultra Violet energy gets converted into visible light by the lamp phosphor, where the remainder is converted into radiated heat. Finally, Mercury atoms convert 3% of the initial energy into visible light. The result is typically 15% overall electrical to optical energy conversion in the lamp.

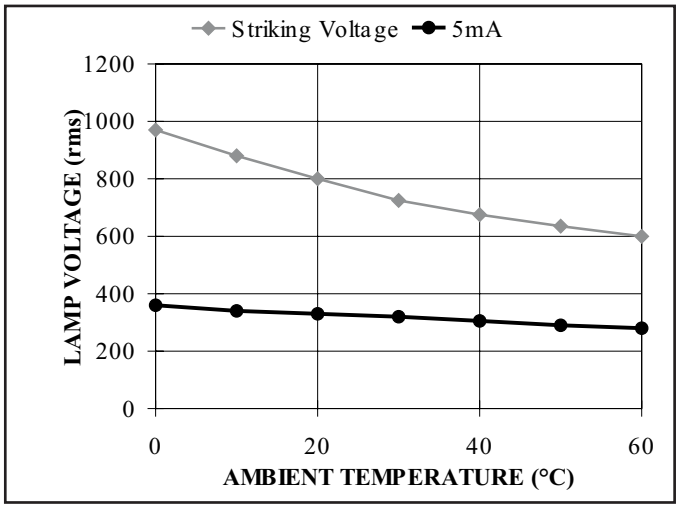


Figure 13. Temperature effects on voltage.

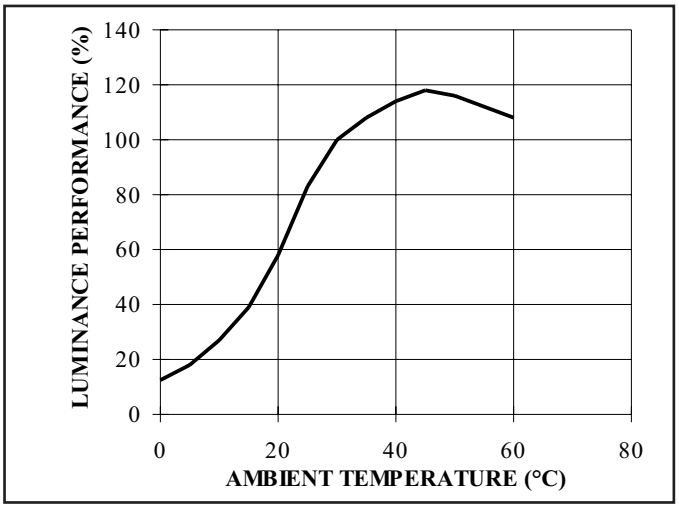


Figure 14. Temperature effects on lumens.

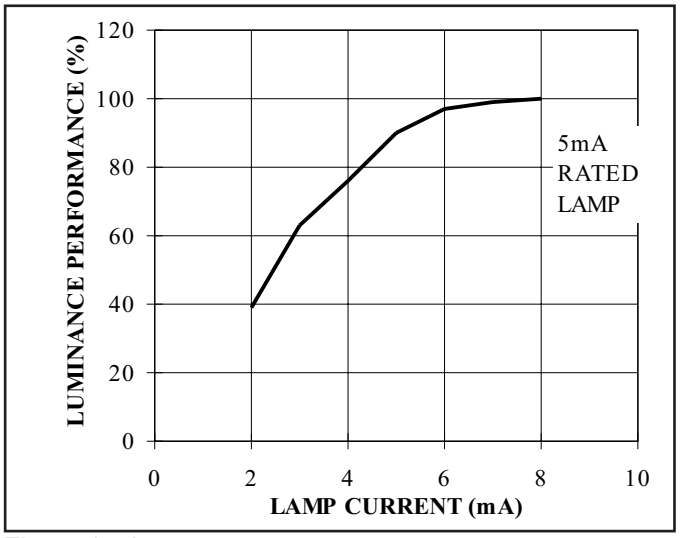


Figure 15. Lumens output versus current.

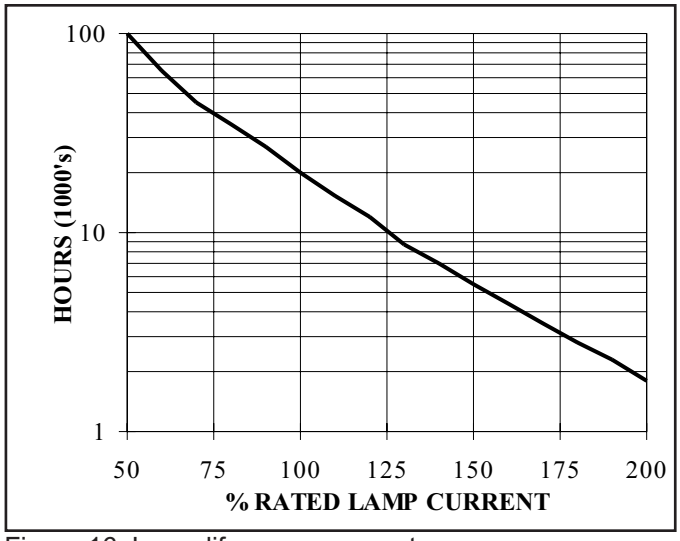


Figure 16. Lamp life versus current.

APPLICATION INFORMATION (cont.)

In a practical backlight design, the physical spacing between the lamp and high voltage secondary wiring with respect to the foil reflector and LCD frame can be tight. With this tight spacing, distributed stray capacitance will form as shown in Fig. 17. The stray capacitance causes leakage currents from the high voltage secondary to circuit ground. Although the current through stray capacitance doesn't directly translate into losses, the extra current through the transformer, primary resonant tank, and switching devices does. A poor layout with excessive stray capacitance can reduce system efficiency by tens of percent. High frequency harmonics in the secondary voltage waveform impact efficiency even further, since capacitive reactance decreases as frequency increases. This is why a pure sinusoid gives the best electrical to optical efficiency, minimizing harmonic losses. Sinusoidal waveforms require more circulating current in the resonant tank, however, lowering the electrical efficiency of the converter.

The trade-off of electrical and optical efficiencies must be optimized to achieve the best design. System electrical efficiencies of 75-85% are easily achievable in a typical UCC3972/3 based design while still maintaining good optical conversion. Efficiencies will vary with external component selection, input voltage, and lamp power. Fig. 18 and 19 show system electrical efficiencies versus input voltage and output power for the 375V lamp design.

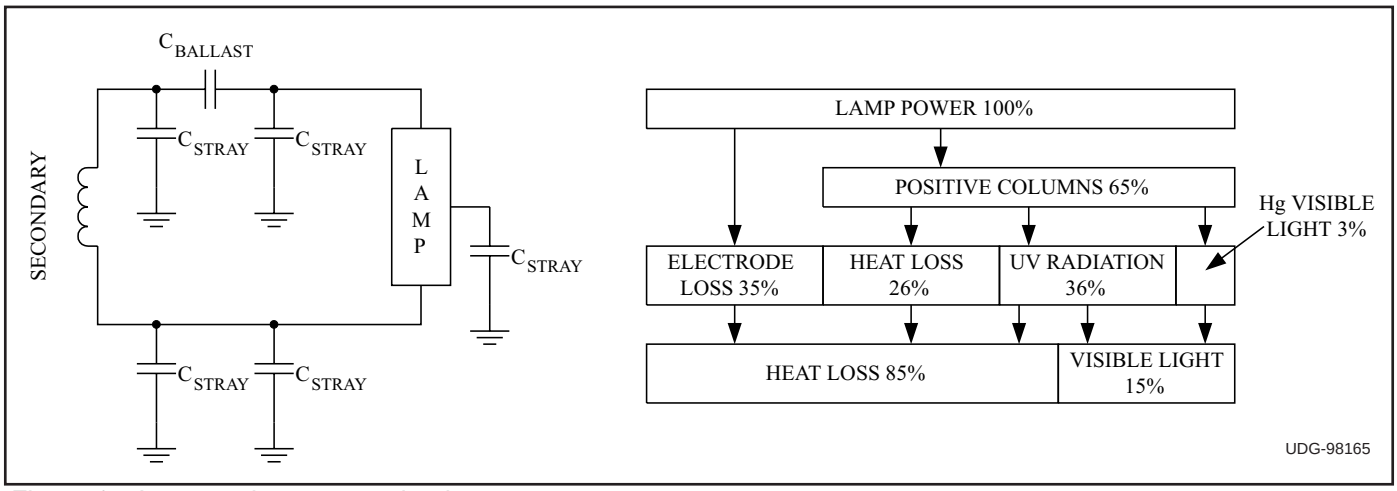


Figure 17. Lamp and stray capacitor losses.

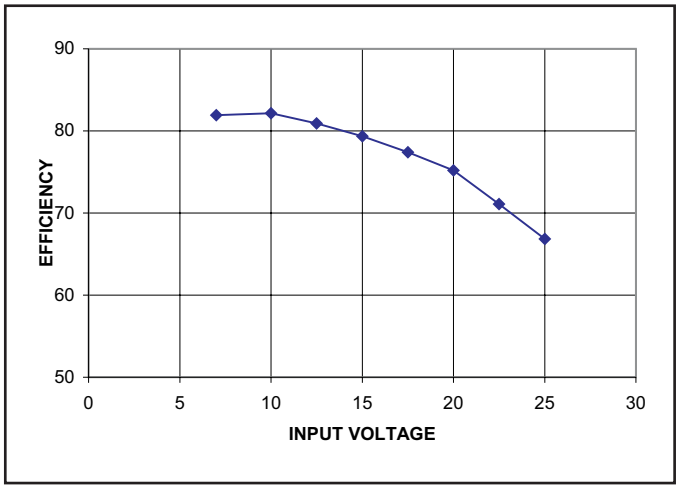


Figure 18. Design example efficiency vs. input voltage at 2W.

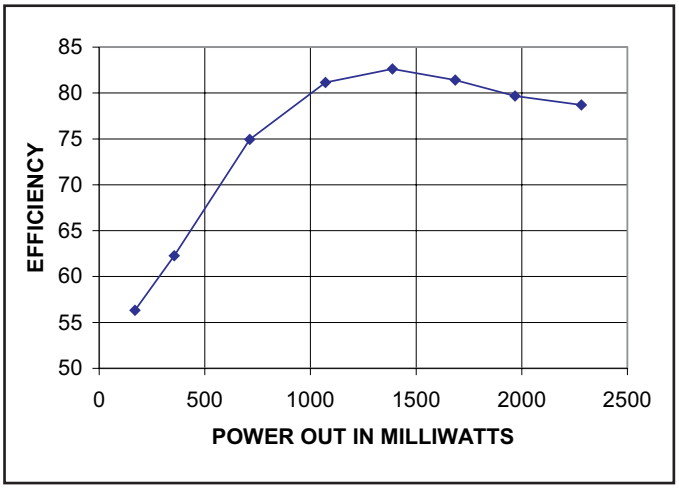


Figure 19. Design efficiency vs. output power.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2972PW	NRND	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2972	
UCC2973PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2973	Samples
UCC2973PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2973	Samples
UCC3972PW	NRND	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3972	
UCC3972PWG4	NRND	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3972	
UCC3972PWTR	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3972	
UCC3973PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3973	Samples
UCC3973PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3973	Samples
UCC3973PWTRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3973	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

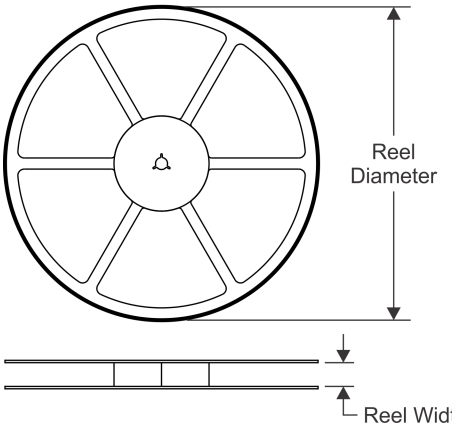
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

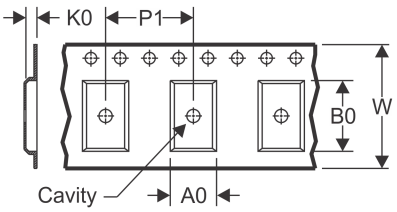
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

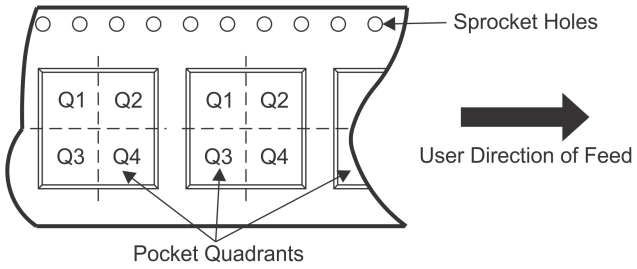


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

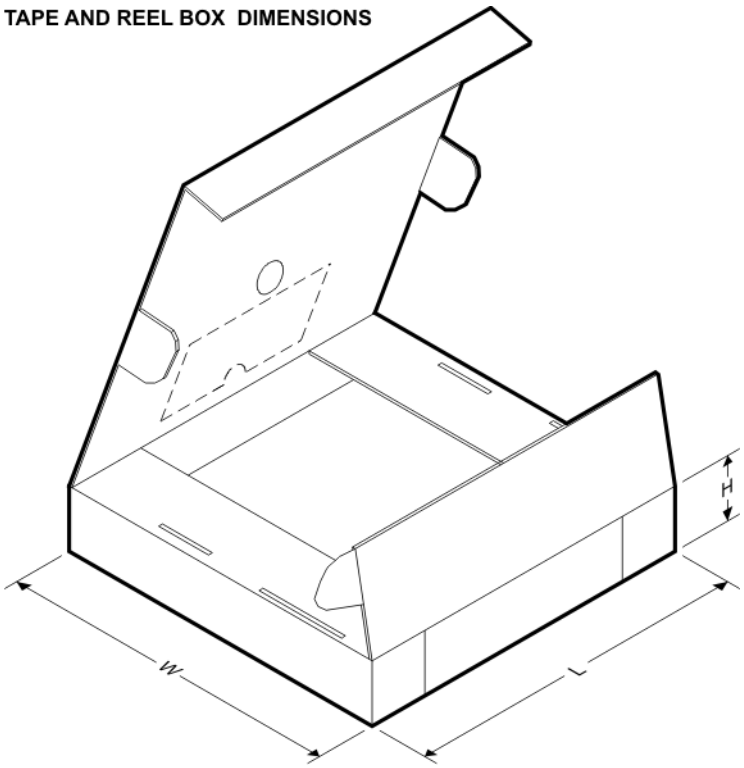
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2973PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3972PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3973PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

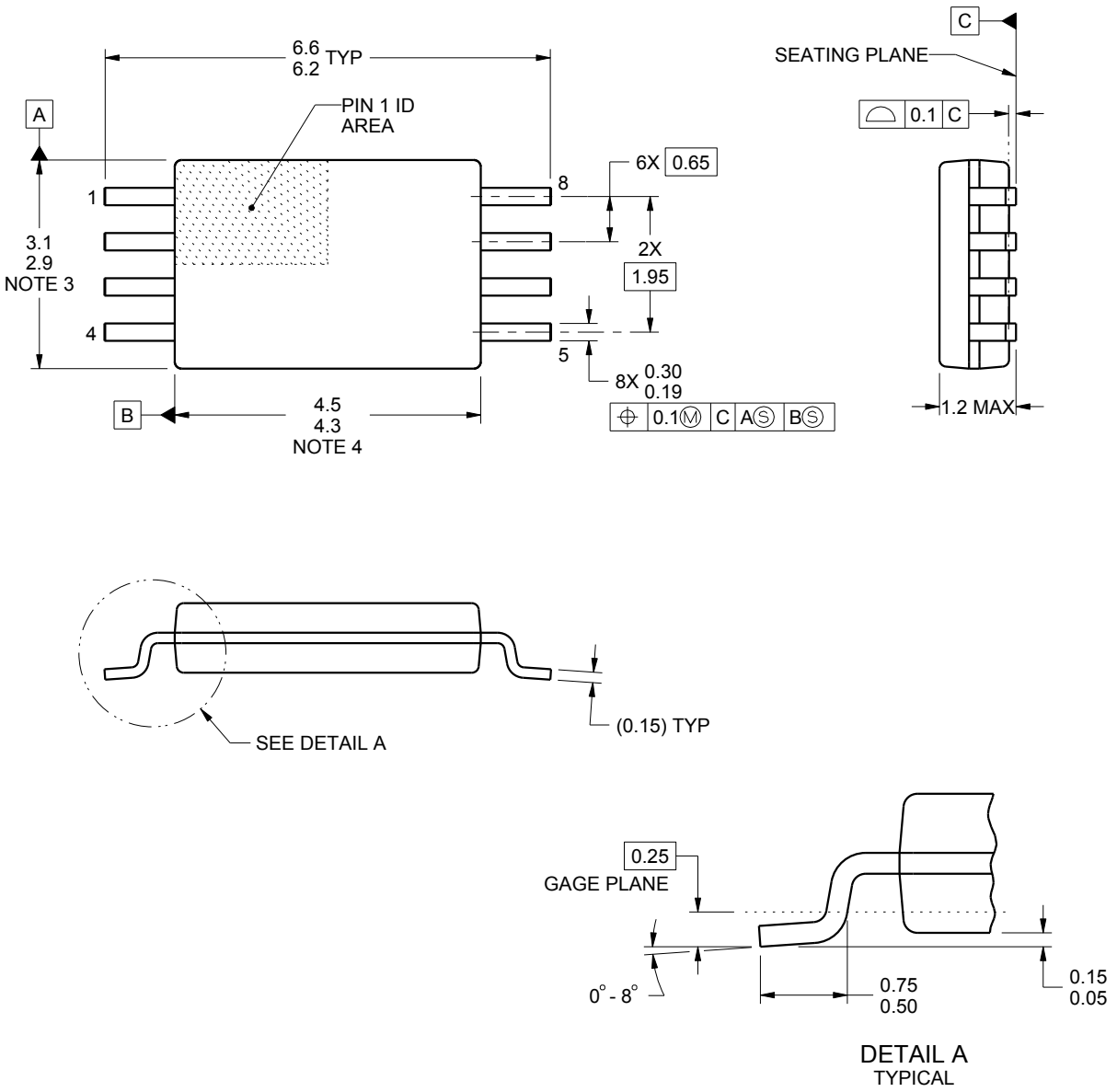
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2973PWTR	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC3972PWTR	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC3973PWTR	TSSOP	PW	8	2000	367.0	367.0	35.0

PACKAGE OUTLINE

PW0008A

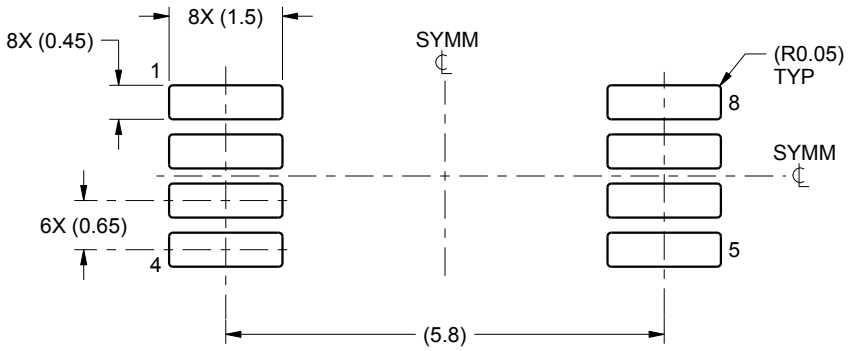
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

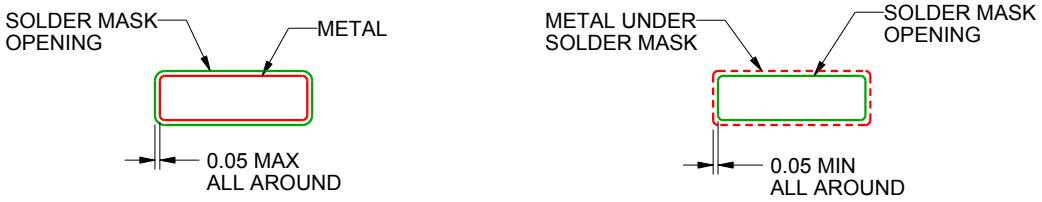


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

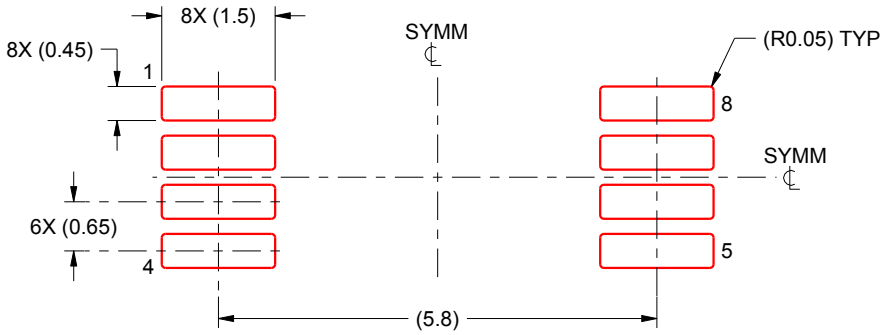


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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