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XIO3130
XIO3130

Data Manual

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XIO3130

Check for Samples: XIO3130

1 Features

- **PCI Express Base Specification, Revision 1.1**
- **PCI Express Card Electromechanical Specification, Revision 1.1**
- **PCI-to-PCI Bridge Architecture Specification, Revision 1.1**
- **PCI Bus Power Management Interface Specification, Revision 1.2**
- **PCI Express Fanout Switch With One ×1 Upstream Port and Three ×1 Downstream Ports**
- **Packet Transmission Starts While Reception Still in Progress (Cut-Through)**
- **256-Byte Maximum Data Payload Size**
- **Peer-to-Peer Support**
- **Wake Event and Beacon Support**
- **Support for D1, D2, D3hot, and D3cold**
- **Active State Power Management (ASPM) Using Both L0s and L1**
- **Low-Power PCI Express Transmitter Mode**
- **Integrated AUX Power Switch Drains VAUX Power Only When Main Power Is Off**
- **Integrated PCI Hot Plug Support**
- **Integrated REFCLK Buffers for Switch Downstream Ports**
- **3.3-V Multifunction I/O Pins for PCI Hot Plug Status and Control or General Purpose I/Os**
- **Optional Serial EEPROM for System-Specific Configuration Register Initialization**

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2 Introduction

The Texas Instruments XIO3130 switch is an integrated PCI Express fanout switch solution with one upstream x1 port and three downstream x1 ports. This high-performance integrated solution provides the latest in PCI Express switch technology including cut-through architecture, integrated reference clock buffers for downstream ports, integrated main power/V_{AUX} power switch, and downstream port PCI Hot Plug® support.

The reader is assumed to have prior knowledge of the PCI Express interface and associated terminology and of the PCI-SIG specifications.

2.1 Description

The Texas Instruments XIO3130 switch is a PCI Express ×1 3-port fanout switch. The XIO3130 provides a single x1 upstream port supporting full 250-MB/s packet throughput in each direction simultaneously. Three independently configurable ×1 downstream ports are provided that also support full 250-MB/s packet throughput in each direction simultaneously.

A cut-through architecture is implemented to reduce the latency associated with packets moving through the PCI Express fabric. As soon as the address or routing information is decoded within the header of a packet entering an ingress port, the packet is directed to the egress port for forwarding. Packet poisoning using the EDB framing signal is supported in circumstances where packet errors are detected after the transmission of the egress packet begins.

The downstream ports may be configured to support PCI Hot Plug slot implementations. In this scenario, the system designer may decide to use the integrated PCI Hot Plug-compliant controller. This feature is available through the classic PCI configuration space under the PCI Express Capability Structure. When enabled, the downstream ports provide the PCI Hot Plug standard mechanism to apply and remove power to the slot or socket.

Power-management features include Active State Power Management, PME mechanisms, the Beacon/Wake protocol, and all conventional PCI D-states. When ASPM is enabled, each link automatically saves power when idle using the L0s and L1 states. PME messages are supported along with the PME_Turn_Off/PME_TO_Ack protocol.

When enabled, the upstream port supports Beacon transmission as well as the $\overline{\text{WAKE}}$ side band signal to wake the system as the result of a PCI Hot Plug event. Furthermore, the downstream ports may be configured to detect Beacon from downstream devices and forward this upstream. The switch also supports the translation and forwarding of $\overline{\text{WAKE}}$ from a downstream device into Beacon on the upstream port for cabled implementations.

2.2 Related Documents

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2.3 Document Conventions

Throughout this data manual, several conventions are used to convey information. These conventions are listed below:

1. To identify a binary number or field, a lower case b follows the numbers. For example: 000b is a 3-bit binary field.
2. To identify a hexadecimal number or field, a lower case h follows the numbers. For example: 8AFh is a 12-bit hexadecimal field.
3. All other numbers that appear in this document that do not have either a b or h following the number are assumed to be decimal format.
4. If the signal or terminal name has a bar above the name (for example, $\overline{\text{GRST}}$), then this indicates the logical NOT function. When asserted, this signal is a logic low, 0, or 0b.
5. Differential signal names end with P, N, +, or – designators. The P or + designators signify the positive signal associated with the differential pair. The N or – designators signify the negative signal associated with the differential pair.
6. RSVD indicates that the referenced item is reserved.
7. In Sections 4 through 6, the configuration space for the bridge is defined. For each register bit, the software-access method is identified in an access column. The legend for this access column includes the following entries:
   - r – read access by software
   - u – updates by the bridge internal hardware
   - w – write access by software
   - c – clear an asserted bit with a write-back of 1b by software. Write of zero to the field has no effect
   - s – the field may be set by a write of one. Write of zero to the field has no effect.
   - na – not accessible or not applicable

2.4 Ordering Information

ORDERING NUMBER	TEMPERATURE	PACKAGE
XIO3130	0°C to 70°C	196-terminal ZHC
XIO3130I	–40°C to 85°C	

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2.5 Terminal Assignments

The XIO3130 is packaged in a 196-ball ZHC MicroStar™ BGA.

Table 2-1. XIO3130 Terminal Assignments

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	GPIO12	SCL	VDD15	GPIO4	VSSA (2)	DN2_ PERn	VSSA (2)	DN2_ Petn	DN2_ REFCKOn	DN2_ REFCKOp	VDD15	GPIO15	VDD15	VDD15
13	RSVD	GPIO13	VDD15	SDA	VDD15	DN2_ PERp	VDD15	DN2_ PETp	VSSA (2)	VSSA (2)	DN2_ DPSTRP	GPIO6	VDD15	GPIO7
12	GPIO2	RSVD	GPIO3	VDD33	VSS	VSSA (2)	VDDA15 (2)	VSSA (2)	VDDA15 (2)	VDD33	GPIO5	VDD15	GPIO14	GPIO16
11	VDD33	GPIO1	VDD15	VSS	VSS	VSSA (2)	VDDA15 (2)	VDDA15 (2)	VDDA15 (2)	VSS	VSS	VDD15	GPIO11	VDD33
10	VSSA (1)	VDD15	DN1_ DPSTRP	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	GPIO8	VDD15	VSSA (3)
9	DN1_ REFCK Op	DN1_ REFCK On	VSSA (1)	VDDA15 (1)	VSS	VSS	VSS	VSS	VSS	VSS	VSSA (3)	VSSA (3)	DN3_ PERp	DN3_ PERn
8	DN1_ PETp	DN1_ PETn	VSSA (1)	VDDA15 (1)	VSS	VSS	VSS	VSS	VSS	VSS	VDDA15 (3)	VDDA15 (3)	VDD15	VSSA (3)
7	VDDA15 (1)	VDD15	VSSA (1)	VDDA15 (1)	VSS	VSS	VSS	VSS	VSS	VSS	VDDA15 (3)	VSSA (3)	DN3_ PETp	DN3_ PETn
6	DN1_ PERp	DN1_ PERn	GPIO0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDA15 (3)	VDDA15 (3)	VSSA (3)	DN3_ REFCKOn
5	VSSA (1)	$\overline{\text{DN1_ PERST}}$	VDD15	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSSA (3)	DN3_ REFCKOp
4	VDD15	VDD33	RSVD	RSVD	VSSA REF	VDD COMB 33	VDDA15 (0)	VDDA15 (0)	VDDA15 (0)	VDD15	VSS	VDD33	DN3_ DPSTRP	VDD15
3	VDD33	VDD15	$\overline{\text{WAKE}}$	VDD COMBIO	REFR1	VDD15 REF	VSSA (0)	VDD15	VDDA33	VDDA15 (0)	GPIO18	GPIO17	GPIO9	VDD15
2	$\overline{\text{DN2_ PERST}}$	VDD15	$\overline{\text{GRST}}$	REFR0	VDD33 REF	VDD15	UP_ PETn	VDDA15 (0)	UP_ PERn	VSS	UP_ REFCKIn	VDD15	$\overline{\text{CLKREQ_UP}}$	GPIO10
1	$\overline{\text{DN3_ PERST}}$	$\overline{\text{UP_ PERST}}$	VDD COMB15	VSSD REF	VAUX33 REF	VDD15	UP_ PETp	VSSA (0)	UP_ PERp	VSSA (0)	UP_ REFCKIp	VDD15	VDD33	RSVD

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Table 2-2. XIO3130 Terminals Sorted Alphanumerically

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	$\overline{\text{DN3_PERST}}$	C13	VDD15	F11	VSSA(2)	J08	VSS	M06	VDDA15(3)
A02	$\overline{\text{DN2_PERST}}$	C14	VDD15	F12	VSSA(2)	J09	VSS	M07	VSSA(3)
A03	VDD33	D01	VSSDREF	F13	DN2_PERp	J10	VSS	M08	VDDA15(3)
A04	VDD15	D02	REFR0	F14	DN2_PERn	J11	VDDA15(2)	M09	VSSA(3)
A05	VSSA(1)	D03	VDDCOMBIO	G01	UP_PETp	J12	VDDA15(2)	M10	GPIO8
A06	DN1_PERp	D04	RSVD	G02	UP_PETn	J13	VSSA(2)	M11	VDD15
A07	VDDA15(1)	D05	VSS	G03	VSSA(0)	J14	DN2_REFCKOn	M12	VDD15
A08	DN1_PETp	D06	VSS	G04	VDDA15(0)	K01	VSSA(0)	M13	GPIO6
A09	DN1_REFCKOp	D07	VDDA15(1)	G05	VSS	K02	VSS	M14	GPIO15
A10	VSSA(1)	D08	VDDA15(1)	G06	VSS	K03	VDDA15(0)	N01	VDD33
A11	VDD33	D09	VDDA15(1)	G07	VSS	K04	VDD15	N02	$\overline{\text{CLKREQ_UP}}$
A12	GPIO2	D10	VSS	G08	VSS	K05	VSS	N03	GPIO9
A13	RSVD	D11	VSS	G09	VSS	K06	VSS	N04	DN3_DPSTRP
A14	GPIO12	D12	VDD33	G10	VSS	K07	VSS	N05	VSSA(3)
B01	$\overline{\text{UP_PERST}}$	D13	SDA	G11	VDDA15(2)	K08	VSS	N06	VSSA(3)
B02	VDD15	D14	GPIO4	G12	VDDA15(2)	K09	VSS	N07	DN3_PETp
B03	VDD15	E01	VAUX33REF	G13	VDD15	K10	VSS	N08	VDD15
B04	VDD33	E02	VDD33REF	G14	VSSA(2)	K11	VSS	N09	DN3_PERp
B05	$\overline{\text{DN1_PERST}}$	E03	REFR1	H01	VSSA(0)	K12	VDD33	N10	VDD15
B06	DN1_PERn	E04	VSSAREF	H02	VDDA15(0)	K13	VSSA(2)	N11	GPIO11
B07	VDD15	E05	VSS	H03	VDD15	K14	DN2_REFCKOp	N12	GPIO14
B08	DN1_PETn	E06	VSS	H04	VDDA15(0)	L01	UP_REFCKIp	N13	VDD15
B09	DN1_REFCKOn	E07	VSS	H05	VSS	L02	UP_REFCKIn	N14	VDD15
B10	VDD15	E08	VSS	H06	VSS	L03	GPIO18	P01	RSVD
B11	GPIO1	E09	VSS	H06	VSS	L04	VSS	P02	GPIO10
B12	RSVD	E10	VSS	H07	VSS	L05	VSS	P03	VDD15
B13	GPIO13	E11	VSS	H08	VSS	L06	VDDA15(3)	P04	VDD15
B14	SCL	E12	VSS	H09	VSS	L07	VDDA15(3)	P05	DN3_REFCKOp
C01	VDDCOMB15	E13	VDD15	H10	VSS	L08	VDDA15(3)	P06	DN3_REFCKOn
C02	$\overline{\text{GRST}}$	E14	VSSA(2)	H11	VDDA15(2)	L09	VSSA(3)	P07	DN3_PETn
C03	$\overline{\text{WAKE}}$	F01	VDD15	H12	VSSA(2)	L10	VSS	P08	VSSA(3)
C04	RSVD	F02	VDD15	H13	DN2_PETp	L11	VSS	P09	DN3_PERn
C05	VDD15	F03	VDD15REF	H14	DN2_PETn	L12	GPIO5	P10	VSSA(3)
C06	GPIO0	F04	VDDCOMB33	J01	UP_PERp	L13	DN2_DPSTRP	P11	VDD33
C07	VSSA(1)	F05	VSS	J02	UP_PERn	L14	VDD15	P12	GPIO16
C08	VSSA(1)	F06	VSS	J03	VDDA33	M01	VDD15	P13	GPIO7
C09	VSSA(1)	F07	VSS	J04	VDDA15(0)	M02	VDD15	P14	VDD15
C10	DN1_DPSTRP	F08	VSS	J05	VSS	M03	GPIO17		
C11	VDD15	F09	VSS	J06	VSS	M04	VDD33		
C12	GPIO3	F10	VSS	J07	VSS	M05	VSS		

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Table 2-3. XIO3130 Signal Names Sorted Alphabetically

Signal Name	Ball	Signal Name	Ball
$\overline{\text{CLKREQ_UP}}$	N02	GPIO5	L12
DN1_DPSTRP	C10	GPIO6	M13
DN1_PERn	B06	GPIO7	P13
DN1_PERp	A06	GPIO8	M10
$\overline{\text{DN1_PERST}}$	B05	GPIO9	N03
DN1_PETn	B08	$\overline{\text{GRST}}$	C02
DN1_PETp	A08 Suggested Program Value	REFR0	D02
DN1_REFCKOn	B09	REFR1	E03
DN1_REFCKOp	A09	RSVD	A13, B12, C04, D04, P01
DN2_DPSTRP	L13	SCL	B14
DN2_PERn	F14	SDA	D13
DN2_PERp	F13	UP_PERn	J02
$\overline{\text{DN2_PERST}}$	A02	UP_PERp	J01
DN2_PETn	H14	$\overline{\text{UP_PERST}}$	B01
DN2_PETp	H13	UP_PETn	G02
DN2_REFCKOn	J14	UP_PETp	G01
DN2_REFCKOp	K14	UP_REFCKIn	L02
DN3_DPSTRP	N04	UP_REFCKIp	L01
DN3_PERn	P09	VAUX33REF	E01
DN3_PERp	N09	VDD15	A04, B02, B03, B07, B10, C05, C11, C13, C14, E13, F01, F02, G13, H03, K04, L14, M01, M02, M11, M12, N08, N10, N13, N14, P03, P04, P14
$\overline{\text{DN3_PERST}}$	A01	VDDA15(0)	G04, H02, H04, J04, K03
DN3_PETn	P07	VDDA15(1)	A07, D07, D08, D09
DN3_PETp	N07	VDDA15(2)	G11, G12, H11, J11, J12
DN3_REFCKOn	P06	VDDA15(3)	L06, L07, L08, M06, M08
DN3_REFCKOp	P05	VDD15REF	F03
GPIO0	C06	VDD33	A03, A11, B04, D12, K12, M04, N01, P11
GPIO1	B11	VDD33REF	E02
GPIO10	P02	VDDA33	J03
GPIO11	N11	VDDCOMB15	C01
GPIO12	A14	VDDCOMB33	F04
GPIO13	B13	VDDCOMBIO	D03
GPIO14	N12	VSS	D05, D06, D10, D11, E05, E06, E07, E08, E09, E10, E11, E12, F05, F06, F07, F08, F09, F10, G05, G06, G07, G08, G09, G10, H05, H06, H07, H08, H09, H10, J05, J06, J07, J08, J09, J10, K02, K05, K06, K07, K08, K09, K10, K11, L04, L05, L10, L11, M05
GPIO15	M14	VSSA(0)	G03, H01, K01
GPIO16	P12	VSSA(1)	A05, A10, C07, C08, C09
GPIO17	M03	VSSA(2)	E14, F11, F12, G14, H12, J13, K13
GPIO18	L03	VSSA(3)	L09, M07, M09, N05, N06, P08, P10
GPIO2	A12	VSSAREF	E04
GPIO3	C12	VSSDREF	D01
GPIO4	D14	$\overline{\text{WAKE}}$	C03

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2.6 Terminal Descriptions

Table 2-4. Power Supply Terminals

Signal	Ball	I/O Type	External parts	Description
VDDA15(0)	G04, H02, H04, J04, K03	PWR	Filter	1.5-V analog power terminals for PCI-Express upstream port 0
VDDA15(1)	A07, D07, D08, D09	PWR	Filter	1.5-V analog power terminals for PCI-Express downstream port 1
VDDA15(2)	G11, G12, H11, J11, J12	PWR	Filter	1.5-V analog power terminals for PCI-Express downstream port 2
VDDA15(3)	L06, L07, L08, M06, M08	PWR	Filter	1.5-V analog power terminals for PCI-Express downstream port 3
VDD15	A04, B02, B03, B07, B10, C05, C11, C13, C14, E13, F01, F02, G13, H03, K04, L14, M01, M02, M11, M12, N08, N10, N13, N14, P03, P04, P14	PWR	Bypass capacitors	1.5-V digital core power terminals
VDD33	A03, A11, B04, D12, K12, M04, N01, P11	PWR	Bypass capacitors	3.3-V digital I/O power terminals
VDDA33	J03	PWR	Filter	3.3-V analog power terminal
VAUX33REF	E01	PWR	Bypass capacitors	3.3-V digital V_{AUX} power terminal
VDD15REF	F03	PWR	Filter	1.5-V PCI-Express reference power terminal
VDD33REF	E02	PWR	Filter	3.3-V PCI-Express reference power terminal

Table 2-5. Combined Power Terminals

Signal	Ball	I/O Type	External Parts	Description
VDDCOMBIO	D03	Passive	Bypass capacitors	Internally combined 3.3-V main and V_{AUX} power output for external bypass capacitor filtering. Supplies all internal 3.3-V input and output circuitry powered during D3 cold. **Caution: Do not use this terminal to supply external power to other devices.**
VDDCOMB33	F04	Passive	Bypass capacitors	Internally combined 3.3-V main and V_{AUX} power output for external bypass capacitor filtering. Supplies all internal 3.3-V circuitry powered during D3 cold. **Caution: Do not use this terminal to supply external power to other devices.**
VDDCOMB15	C01	Passive	Bypass capacitors	Internally combined 1.5-V main and V_{AUX} power output for external bypass capacitor filtering. Supplies all internal 1.5-V circuitry powered during D3 cold. **Caution: Do not use this terminal to supply external power to other devices.**

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Table 2-6. Ground Terminals

Signal	Ball	I/O Type	Description
VSS	D05, D06, D10, D11, E05, E06, E07, E08, E09, E10, E11, E12, F05, F06, F07, F08, F09, F10, G05, G06, G07, G08, G09, G10, H05, H06, H07, H08, H09, H10, J05, J06, J07, J08, J09, J10, K02, K05, K06, K07, K08, K09, K10, K11, L04, L05, L10, L11, M05	GND	Digital ground terminals
VSSA(0)	G03, H01, K01	GND	Analog ground terminals for upstream Port 0
VSSA(1)	A05, A10, C07, C08, C09	GND	Analog ground terminals for downstream Port 1
VSSA(2)	E14, F11, F12, G14, H12, J13, K13	GND	Analog ground terminals for downstream Port 2
VSSA(3)	L09, M07, M09, N05, N06, P08, P10	GND	Analog ground terminals for downstream Port 3
VSSAREF	E04	GND	1.5-V PCI-Express analog reference ground terminal
VSSDREF	D01	GND	1.5-V PCI-Express digital reference ground terminal

Table 2-7. PCI Express Reference Clock Terminals

Signal	Ball	I/O Type	External Parts	Description
UP_REFCKIp UP_REFCKIn	L01 L02	HS DIFF IN		Reference clock inputs. REFCKIp and REFCKIn comprise the differential input pair for the 100-MHz system reference clock.
DN1_REFCKOp DN1_REFCKOn	A09 B09	HS DIFF OUT		100 MHz differential reference clock outputs for downstream port 1
DN2_REFCKOp DN2_REFCKOn	K14 J14	HS DIFF OUT		100 MHz differential reference clock outputs for downstream port 2
DN3_REFCKOp DN3_REFCKOn	P05 P06	HS DIFF OUT		100 MHz differential reference clock outputs for downstream port 3

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Table 2-8. PCI Express Terminals

Signal	Ball	I/O Type	External Parts	Description
UP_PETp UP_PETn	G01 G02	HS DIFF OUT	Series capacitors	High-speed differential transmit pair for upstream port 0
DN1_PETp DN1_PETn	A08 B08	HS DIFF OUT	Series capacitors	High-speed differential transmit pair for downstream port 1
DN2_PETp DN2_PETn	H13 H14	HS DIFF OUT	Series capacitors	High-speed differential transmit pair for downstream port 2
DN3_PETp DN3_PETn	N07 P07	HS DIFF OUT	Series capacitors	High-speed differential transmit pair for downstream port 3
UP_PERp UP_PERn	J01 J02	HS DIFF IN		High-speed differential receiver pair for upstream port 0
DN1_PERp DN1_PERn	A06 B06	HS DIFF IN		High-speed differential receiver pair for downstream port 1
DN2_PERp DN2_PERn	F13 F14	HS DIFF IN		High-speed differential receiver pair for downstream port 2
DN3_PERp DN3_PERn	N09 P09	HS DIFF IN		High-speed differential receiver pair for downstream port 3
REFR0 REFR1	D02 E03	Passive	External bias resistor	External reference resistor terminals for setting TX driver current. An external resistor is connected between these terminals.
$\overline{\text{UP_PERST}}$	B01	LV CMOS IN	System-side pullup resistor	PCI-Express reset input. When logic high, the $\overline{\text{PERST}}$ signal identifies that the system power is stable. When logic low, the $\overline{\text{PERST}}$ signal generates an internal power-on reset. **Note:** The $\overline{\text{UP_PERST}}$ input buffer has hysteresis.
$\overline{\text{DN1_PERST}}$	B05	LV CMOS O	Pulldown resistor	PCI-Express reset output for downstream port 1.
$\overline{\text{DN2_PERST}}$	A02	LV CMOS O	Pulldown resistor	PCI-Express reset output for downstream port 2.
$\overline{\text{DN3_PERST}}$	A01	LV CMOS O	Pulldown resistor	PCI-Express reset output for downstream port 3.
$\overline{\text{WAKE}}$	C03	LV CMOS I/O	System-side pullup resistor	$\overline{\text{WAKE}}$ is an active low signal that is driven low to reactivate the PCI-Express link hierarchy's main power rails and reference clocks. **Note:** Since $\overline{\text{WAKE}}$ is an open-drain output buffer, a system-side pullup resistor is required.

Table 2-9. PCI Hot Plug Strapping Terminals

Signal	Ball	I/O Type	External Parts	Description
DN1_DPSTRP	C10	LV CMOS IN	Pullup or pulldown resistor	Downstream Port 1 Strap. This pin is pulled high at the de-assertion of reset. GPIO0, GPIO1, and GPIO2 are used as PCI Hot Plug terminals for downstream port 1 and are no longer available for use as GPIOs. The three terminals become $\overline{\text{PRESENT}}$, $\overline{\text{PWR_ON}}$, and PWR_GOOD respectively. These GPIOs are available for normal use if this terminal is pulled low at the de-assertion of reset.
DN2_DPSTRP	L13	LV CMOS IN	Pullup or pulldown resistor	Downstream Port 2 Strap. This pin is pulled high at the de-assertion of reset. GPIO4, GPIO5, and GPIO6 are used as PCI Hot Plug terminals for downstream port 2 and are no longer available for use as GPIOs. The three terminals become $\overline{\text{PRESENT}}$, $\overline{\text{PWR_ON}}$, and PWR_GOOD respectively. These GPIOs are available for normal use if this terminal is pulled low at the de-assertion of reset.
DN3_DPSTRP	N04	LV CMOS IN	Pullup or pulldown resistor	Downstream Port 3 Strap. This pin is pulled high at the de-assertion of reset. GPIO8, GPIO9, and GPIO10 are used as PCI Hot Plug terminals for downstream port 3 and are no longer available for use as GPIOs. The three terminals become $\overline{\text{PRESENT}}$, $\overline{\text{PWR_ON}}$, and PWR_GOOD respectively. These GPIOs are available for normal use if this terminal is pulled low at the de-assertion of reset.

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Table 2-10. GPIO Terminals

Signal	Ball	I/O Type	External Parts	Description
GPIO0	C06	LV CMOS I/O		GPIO 0. If the DN1_DPSTRP pin is pulled high at the de-assertion of reset, this pin functions as the PRSNT hotplug pin for downstream port 1. Otherwise this pin's function is programmed with the GPIO A Control register.
GPIO1	B11	LV CMOS I/O		GPIO 1. If the DN1_DPSTRP pin is pulled high at the de-assertion of reset, this pin functions as the POWERON hotplug pin for downstream port 1. Otherwise this pin's function is programmed with the GPIO A Control register.
GPIO2	A12	LV CMOS I/O		GPIO 2. If the DN1_DPSTRP pin is pulled high at the de-assertion of reset, this pin functions as the PWRGD hotplug pin for downstream port 1. Otherwise this pin's function is programmed with the GPIO A Control register
GPIO3	C12	LV CMOS I/O		GPIO 3. This pin's function is programmed with the GPIO A Control register.
GPIO4	D14	LV CMOS I/O		GPIO 4. If the DN2_DPSTRP pin is pulled high at the de-assertion of reset, this pin functions as the PRSNT hotplug pin for downstream port 2. Otherwise this pin's function is programmed with the GPIO A Control register.
GPIO5	L12	LV CMOS I/O		GPIO 5. If the DN2_DPSTRP pin is pulled high at the de-assertion of reset, this pin functions as the POWERON hotplug pin for downstream port 2. Otherwise this pin's function is programmed with the GPIO A Control register.
GPIO6	M13	LV CMOS I/O		GPIO 6. If the DN2_DPSTRP pin is pulled high at the de-assertion of reset, this pin functions as the PWRGD hotplug pin for downstream port 2. Otherwise this pin's function is programmed with the GPIO A Control register.
GPIO7	P13	LV CMOS I/O		GPIO 7. This pin's function is programmed with the GPIO A Control register.
GPIO8	M10	LV CMOS I/O		GPIO 8. If the DN3_DPSTRP pin is pulled high at the de-assertion of reset, this pin functions as the PRSNT hotplug pin for downstream port 3. Otherwise this pin's function is programmed with the GPIO B Control register.
GPIO9	N03	LV CMOS I/O		GPIO 9. If the DN3_DPSTRP pin is pulled high at the de-assertion of reset, this pin functions as the POWERON hotplug pin for downstream port 3. Otherwise this pin's function is programmed with the GPIO B Control register.
GPIO10	P02	LV CMOS I/O		GPIO 10. If the DN3_DPSTRP pin is pulled high at the de-assertion of reset, this pin functions as the PWRGD hotplug pin for downstream port 3. Otherwise this pin's function is programmed with the GPIO B Control register.
GPIO11	N11	LV CMOS I/O		GPIO 11. This pin's function is programmed with the GPIO B Control register.
GPIO12	A14	LV CMOS I/O		GPIO 12. This pin's function is programmed with the GPIO B Control register.
GPIO13	B13	LV CMOS I/O		GPIO 13. This pin's function is programmed with the GPIO B Control register.
GPIO14	N12	LV CMOS I/O		GPIO 14. This pin's function is programmed with the GPIO B Control register.
GPIO15	M14	LV CMOS I/O		GPIO 15. This pin's function is programmed with the GPIO B Control register.
GPIO16	P12	LV CMOS I/O		GPIO16. This pin's function is programmed with the GPIO C Control register.
GPIO17	M03	LV CMOS I/O		GPIO 17. This pin's function is programmed with the GPIO C Control register.
GPIO18	L03	LV CMOS I/O		GPIO 18. This pin's function is programmed with the GPIO C Control register.

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Table 2-11. Miscellaneous Terminals

Signal	Ball	I/O Type	External Parts	Description
$\overline{\text{GRST}}$	C02	LV CMOS IN	See description	Global power-on reset input. Note: a pullup to Vaux (if supported) or VDD3.3 (if not) is required unless this terminal is always driven by the upstream device.
SDA	D13	LV CMOS I/O		Serial Data. This pin is the serial data pin for the EEPROM interface.
SCL	B14	LV CMOS O		Serial Clock. This pin is the serial clock pin for the EEPROM interface.
$\overline{\text{CLKREQ_UP}}$	N02	LV CMOS O		Upstream Clock Request. When asserted low, requests upstream device restart clock in cases where upstream clock may be removed in L1
RSVD	A13, B12,			Reserved. These terminals must tied to VDD15.
RSVD	C04, P01			Reserved. This terminal must be tied to GND.
RSVD	D04		See description	Reserved. Pullup to Vaux (if supported) or VDD3.3 (if not)

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3 Description

Figure 3-1 is the block diagram of the XIO3130.

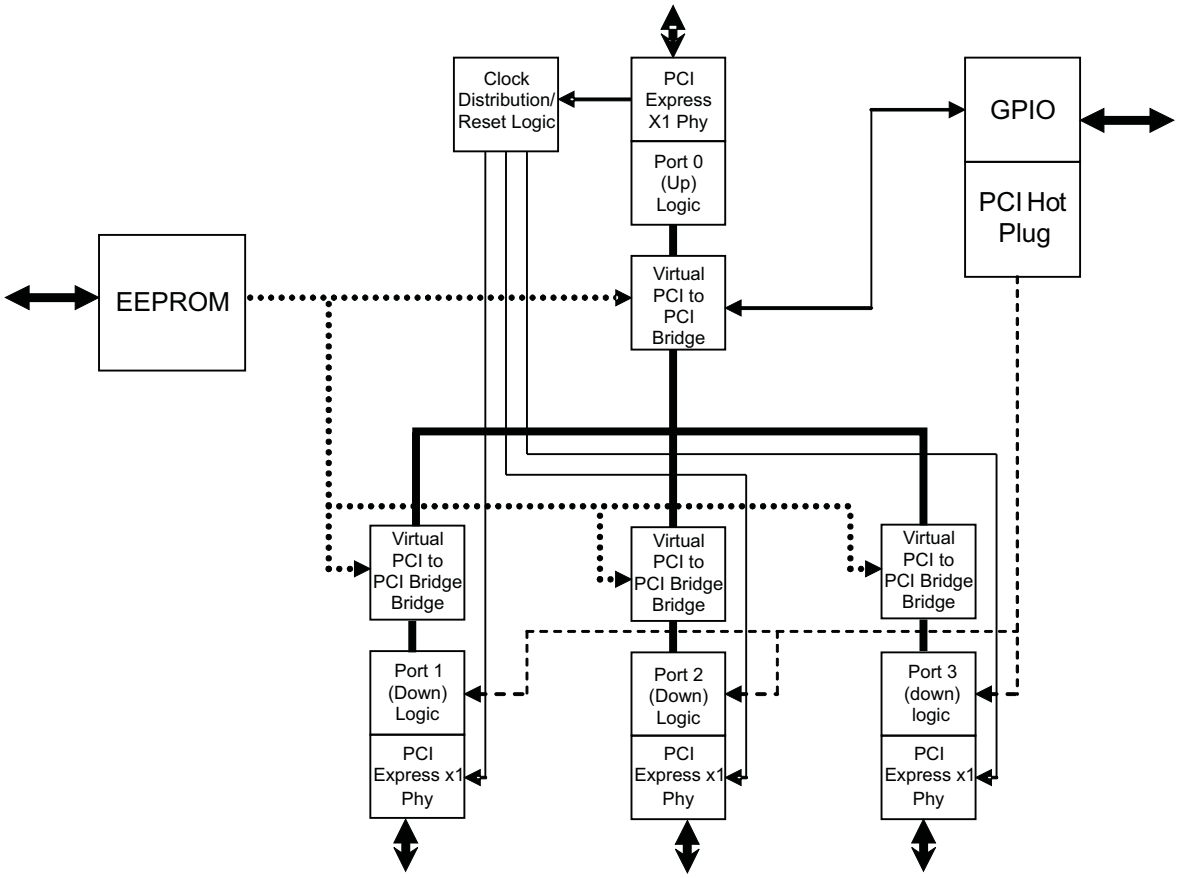

Figure 3-1. Block Diagram

3.1 Power-Up/Power-Down Sequencing

The following sections describe the procedures to power up and power down the XIO3130 switch.

3.1.1 Power-Up Sequence

1. Assert $\overline{\text{PERST}}$ to the device.
2. Apply 1.5-V and 3.3-V voltages in any order with any time relationship and with any ramp rate.
3. Apply a stable PCI Express reference clock.

To meet PCI Express specification requirements, $\overline{\text{PERST}}$ cannot be de-asserted until the following two delay requirements are satisfied:

- Wait a minimum of 100 μs after applying a stable PCI Express reference clock. The 100-μs limit satisfies the requirement for stable device clocks by the de-assertion of $\overline{\text{PERST}}$.
- Wait a minimum of 100 ms after applying power. The 100-ms limit satisfies the requirement for stable power by the de-assertion of $\overline{\text{PERST}}$.

See Figure 3-2, Power-Up Sequence Diagram.

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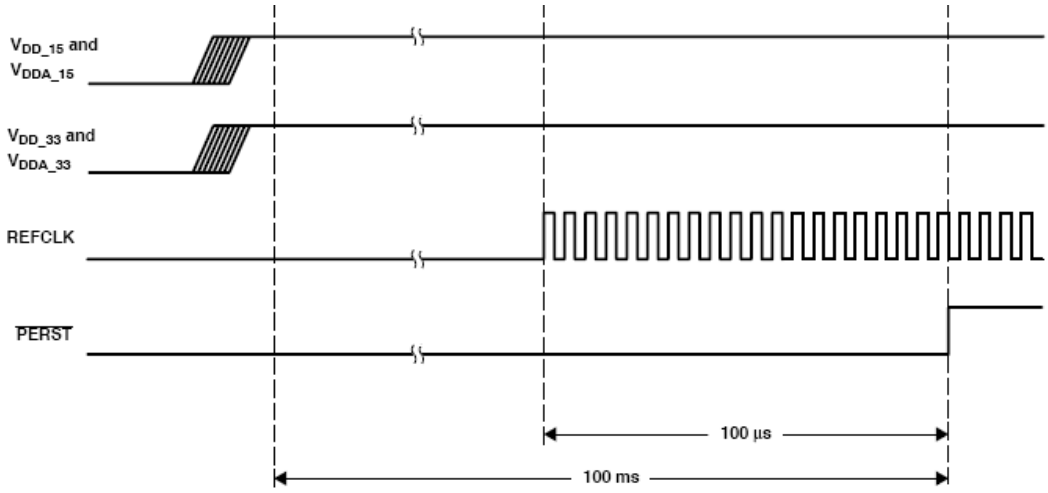

Figure 3-2. Power-Up Sequence Diagram

3.1.2 Power-Down Sequence

- Assert $\overline{\text{PERST}}$ to the device.
- Remove the reference clock.
- Remove 3.3-V and 1.5-V voltages.

See the power-down sequence diagram in Figure 3-3. If the VAUX33REF terminal is to remain powered after a system shutdown, the switch power-down sequence is exactly the same as shown in Figure 3-3.

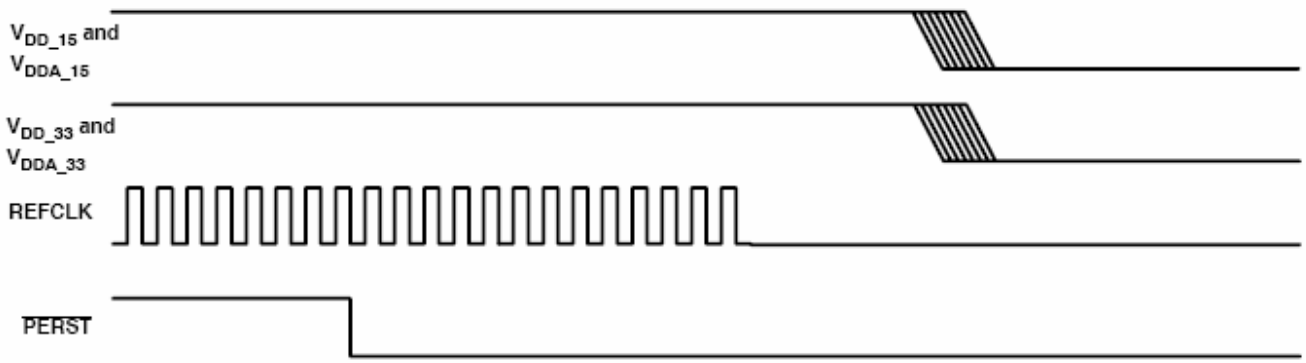

Figure 3-3. Power-Down Sequence Diagram

3.2 Express Interface

3.2.1 External Reference Clock

The Texas Instruments XIO3130 switch requires a differential 100 MHz common clock reference. The clock reference must meet all PCI Express electrical specification requirements for frequency tolerance, spread spectrum clocking, and signal electrical characteristics.

3.2.2 Clock Generator

The clock generator is responsible for generating all internal and external clocks from the PCI Express reference clock. This includes the PHY transmitter serial link clock, the three downstream reference clock outputs, the 60-kHz serial bus interface clock, and all internal clock domains.

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3.2.3 Beacon

The XIO3130 supports the PCI Express in-band beacon feature. Beacon is driven on the PCI Express link by the XIO3130 to request the re-application of main power when in the L2 link state. Once beacon is activated, the XIO3130 continues to send the beacon signal until main power is restored as indicated by $\overline{\text{PERST}}$ going inactive. At this time, the beacon signal is deactivated.

3.2.4 $\overline{\text{WAKE}}$

The XIO3130 supports the PCI Express sideband $\overline{\text{WAKE}}$ feature. $\overline{\text{WAKE}}$ is an active-low signal driven by the XIO3130 to request the re-application of main power when in the L2 link state. Since $\overline{\text{WAKE}}$ is an open-collector output, a system-side pullup resistor is required to prevent the signal from floating. If $\overline{\text{WAKE}}$ to Beacon translation is enabled (see section 3.2.60), the XIO3130 detects when $\overline{\text{WAKE}}$ is asserted and transmits beacon to alert the system. This enables support for devices that use the $\overline{\text{WAKE}}$ protocol in a system that does not support it.

3.2.5 Initial Flow Control Credits

The XIO3130 flow control credits are initialized using the rules defined in the PCI Express Base Specification. Table 3-1 identifies the initial flow control credit advertisement for the XIO3130. The initial advertisement is exactly the same for both upstream and downstream ports.

Table 3-1. Initial Flow Control Credit Advertisements

Credit Type	Initial Advertisement	
	Hex	Decimal
Posted Request Headers (PH)	10	16
Posted Request Data (PD)	80	128
Non-Posted Header (NPH)	10	16
Non-Posted Data (NPD)	10	16
Completion Header (CPLH)	10	16
Completion Data (CPLD)	80	128

3.2.6 PCI Express Message Transactions

PCI Express messages are initiated by, received by and passed through the XIO3130. Table 3-2 outlines message support within the switch.

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Table 3-2. Messages Supported by the XIO3130

Message	Supported	XIO3130 Action
Assert_INTx	Yes	Passed through upstream
Deassert_INTx	Yes	Passed through upstream
PM_Active_State_Nak	Yes	Received and processed
PM_PME	Yes	Passed through upstream Downstream PCI Hot Plug Event: Initiated upstream
PME_Turn_Off	Yes	Received and processed Passed through downstream
PME_TO_Ack	Yes	Downstream port: Received and processed Downstream ports: Initiated upstream
ERR_COR	Yes	Passed through upstream Initiated upstream
ERR_NONFATAL	Yes	Passed through upstream Initiated upstream
ERR_FATAL	Yes	Passed through upstream Initiated upstream
Unlock	Yes	Received and processed Passed through downstream
Set_Slot_Power_Limit	Yes	Upstream port: Received and processed Downstream port: Initiated downstream
Advanced Switching Messages	No	Discarded
Vendor Defined Type 0	Yes	Upstream port: Unsupported request Passed through downstream
Vendor Defined Type 1	Yes	Upstream port: Discarded Passed through downstream

All supported message transactions are processed according to the PCI Express Base Specification.

3.3 GPIO Terminals

Up to 19 general-purpose input/output (GPIO) terminals are provided for system customization. These GPIO terminals are 3.3-V tolerant.

The exact number of GPIO terminals available varies based on the implementation of various supported functions that share GPIO terminals. When any of the shared functions are enabled, the associated GPIO terminal is disabled. When pulled high, the DPSTRP terminals cause some GPIO terminals to be mapped to PCI Hot Plug functions for specific ports. Additional information can be found in the DPSTRP pin descriptions and in Chapter 4.

All GPIO terminals are individually configurable as either inputs or outputs by writing the corresponding bits in the GPIOA, GPIOB, GPIOC, or GPIOD Control Registers. The GPIO data register is used to monitor GPIO terminals defined as inputs or to set the state of GPIO terminals defined as outputs. For more information on GPIO terminals, see sections Section 4.2.61 through Section 4.2.65.

3.4 Serial EEPROM

The XIO3130 provides a two-wire serial-bus interface to load subsystem identification information and specific register defaults from an external EEPROM. This interface supports slow, fast, and high-speed EEPROM speed options.

3.4.1 Serial Bus Interface Implementation

To enable the serial bus interface, a pullup resistor must be implemented on the SCL signal. At the rising

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edge of $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$, whichever occurs last, the SCL terminal is checked for a pullup resistor. If one is detected, bit 3 (SBDETECT) in the serial bus control and status register (see Table 4-32) is set. Software may disable the serial bus interface at any time by writing a zero to the SBDETECT bit. If no external EEPROM is required, the serial bus interface is permanently disabled by attaching a pulldown resistor to the SCL signal.

The XIO3130 implements a two-terminal serial interface with one clock signal (SCL) and one data signal (SDA). The SCL signal is a unidirectional output from the XIO3130 and the SDA signal is bidirectional. Both are open-drain signals and require pullup resistors. The XIO3130 is a bus master device and drives SCL at approximately 60 kHz during data transfers and places SCL in a high-impedance state during bus idle states. The serial EEPROM is a bus slave device and must acknowledge a slave address equal to 1010_000X binary. Figure 3-4 illustrates a sample application implementing the two-wire serial bus.

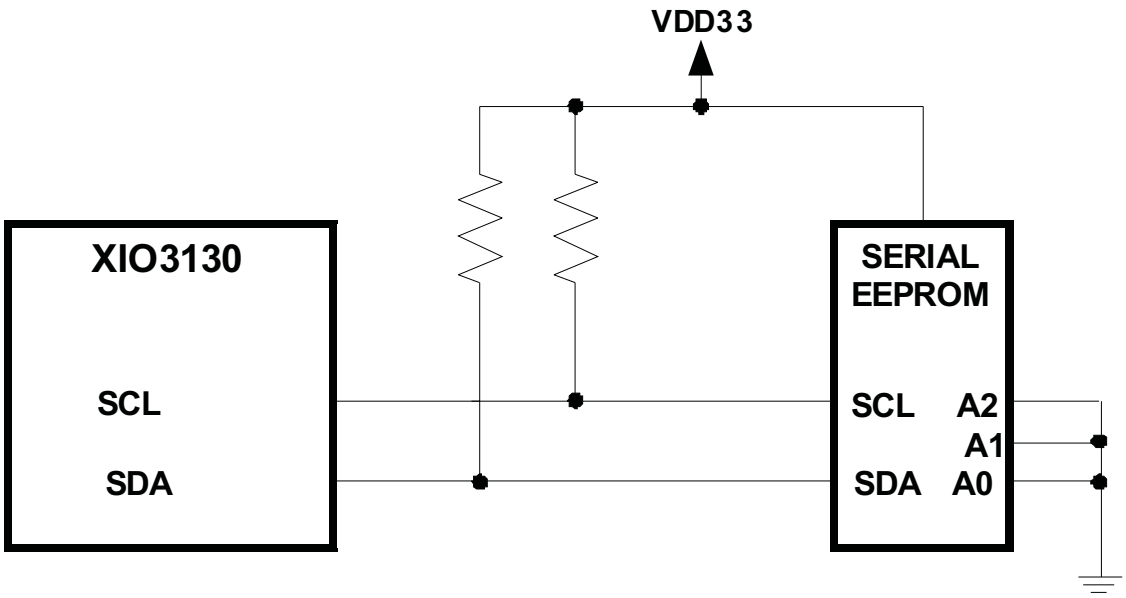

Figure 3-4. Serial EEPROM Applications

3.4.2 Serial Bus Interface Protocol

All data transfers are initiated by the serial bus master. The beginning of a data transfer is indicated by a start condition, which is signaled when the SDA line transitions to a low state while SCL is in the high state, as illustrated in Figure 3-5. The end of a requested data transfer is indicated by a stop condition, which is signaled by a low-to-high transition of SDA while SCL is in the high state, as shown in Figure 3-5. Data on SDA must remain stable during the high state of the SCL signal because changes on the SDA signal during the high state of SCL are interpreted as control signals (i.e., a start or a stop condition).

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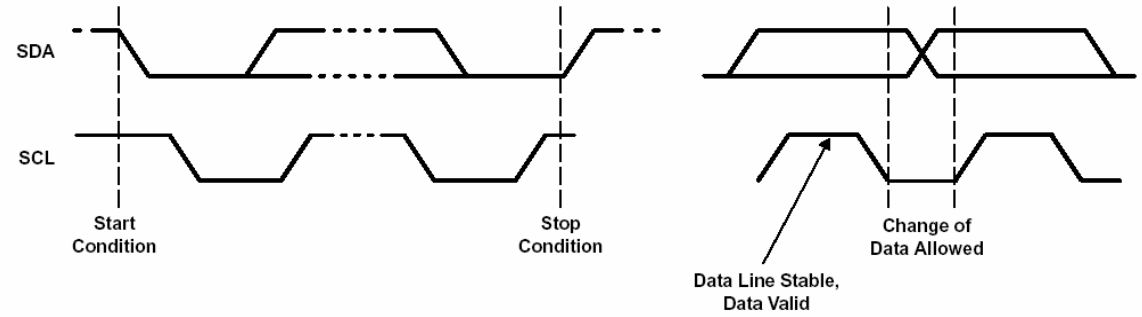

Figure 3-5. Serial-Bus Start/Stop Conditions and Bit Transfers

Data is transferred serially in 8-bit bytes. During a data transfer operation, an unlimited number of bytes are transmitted. However, each byte must be followed by an acknowledge bit to continue the data transfer operation. An acknowledge (ACK) is indicated by the data byte receiver pulling the SDA signal low, so that it remains low during the high state of the SCL signal. Figure 3-6 illustrates the acknowledge protocol.

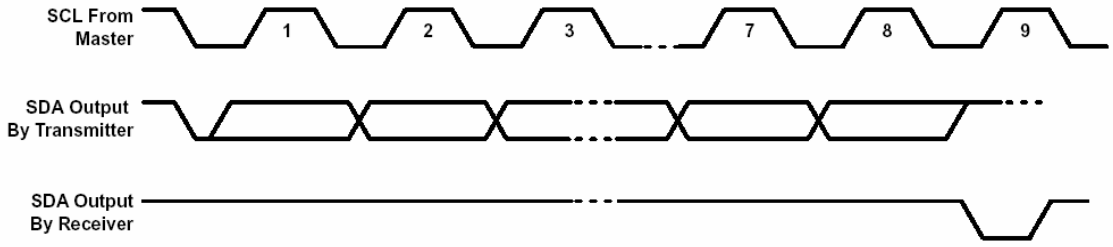

Figure 3-6. Serial-Bus Protocol Acknowledge

The XIO3130 performs three basic serial bus operations: single-byte reads, single-byte writes, and multiple-byte reads. The single-byte operations occur under software control. The multiple-byte read operations are performed by the serial EEPROM initialization circuitry immediately after a PCI Express Reset. For details on how the XIO3130 automatically loads the subsystem identification and other register defaults from the serial-bus EEPROM, see Section 3.4.3, *Serial Bus EEPROM Application*.

Figure 3-7 illustrates a single-byte write. The XIO3130 issues a start condition and sends the 7-bit slave device address and the R/W command bit equal to zero. A zero in the R/W command bit indicates that the data transfer is a write. The slave device acknowledges that it recognizes the slave address. If the XIO3130 receives no acknowledgment, the SB_ERR status bit is set in the serial-bus control and status register (PCI offset B3h; see Table 4-32). Next, the XIO3130 sends the EEPROM word address, and another slave acknowledgment is expected. Then the XIO3130 delivers the data byte (MSB first) and expects a final acknowledgment before issuing the stop condition.

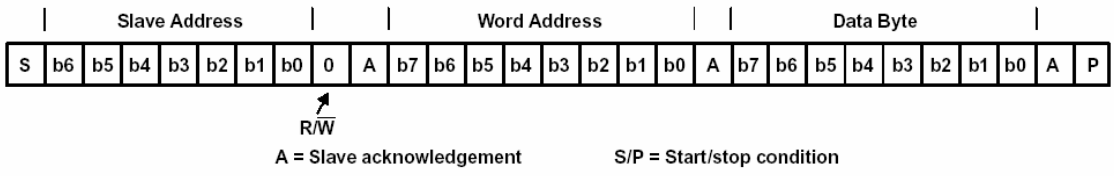

Figure 3-7. Serial-Bus Protocol – Byte Write

Figure 3-8 illustrates a single-byte read. The XIO3130 issues a start condition and sends the 7-bit slave device address and the R/W command bit equal to zero (write). The slave device acknowledges that it

recognizes the slave address. Next, the XIO3130 sends the EEPROM word address, and another slave acknowledgment is expected. Then, the XIO3130 issues a restart condition followed by the 7-bit slave address and the R/W command bit equal to one (read). Once again, the slave device responds with acknowledge. Next, the slave device sends the 8-bit data byte, MS bit first. Since this is a one-byte read, the XIO3130 responds with no acknowledge (logic high), indicating the last data byte. Finally, the XIO3130 issues a stop condition.

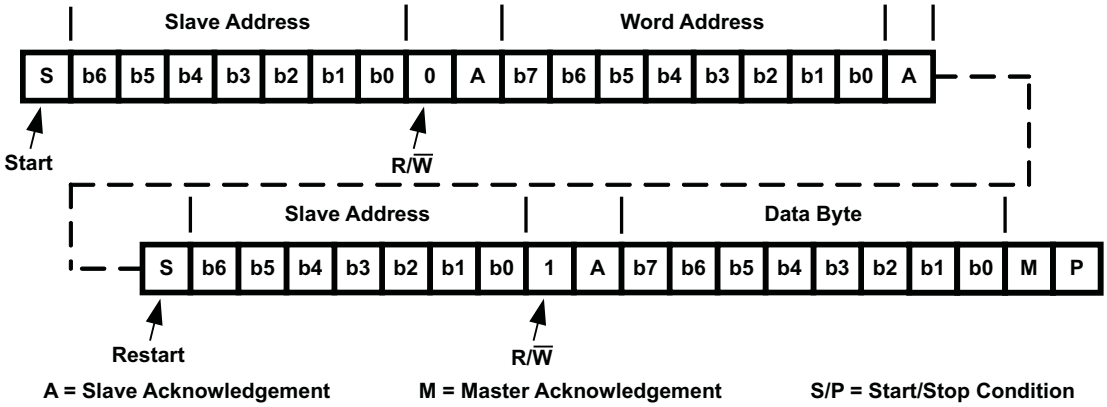

Figure 3-8. Serial-Bus Protocol – Byte Read

Figure 3-9 illustrates the serial interface protocol during a multiple-byte serial EEPROM download. The serial bus protocol starts exactly the same way as a one-byte read. The only difference is that multiple data bytes are transferred. The number of transferred data bytes is controlled by the XIO3130 master. After each data byte, if more data bytes are requested, the XIO3130 master issues acknowledge (logic low). The transfer ends after an XIO3130 master no acknowledge (logic high), followed by a stop condition.

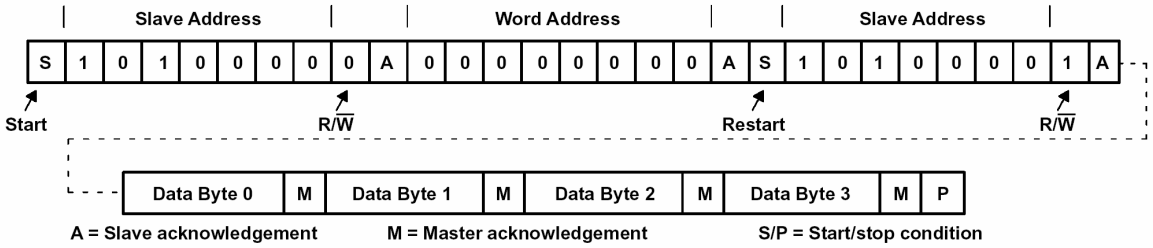

Figure 3-9. Serial-Bus Protocol – Multiple-Byte Read

The PROT_SEL bit (bit 7) in the Serial Bus Control and Status register changes the serial bus protocol. Each of the three previous serial-bus protocol figures illustrates the PROT_SEL bit default (logic low). When this control bit is asserted, the word address and corresponding acknowledge are removed from the serial bus protocol. This feature allows the system designer a second serial bus protocol option when selecting external EEPROM devices.

3.4.3 Serial Bus EEPROM Application

The registers and corresponding bits that are loaded through the EEPROM are provided in Table 3-3. Note the following:

- EEPROM bytes 00h through 1Dh affect the general control options for the XIO3130.
- EEPROM bytes 1Eh through 27h affect the operation of the upstream port (port 0).
- Bytes 00h through 27h are loaded into the configuration registers for the upstream virtual bridge or port 0 (see Figure 4-1).

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- EEPROM bytes 28h through 35h correspond to and are loaded into the configuration space for the first downstream virtual bridge or port 1 (see Figure 4-1).
- EEPROM bytes 36h through 43h correspond to and are loaded into the configuration space for the second downstream virtual bridge or port 2 (see Figure 4-1).
- EEPROM bytes 44h through 51h correspond to and are loaded into the configuration space for the third downstream virtual bridge or port 3 (see Figure 4-1).

Table 3-3. EEPROM Register Loading Map

EEPROM Byte Address (hex)	Suggested Programmed Value (hex)	CONFIG Register Address (hex)	Register Description
0	4C	NA	Global Switch/Upstream Port Function Indicator(1)
1	0	NA	TI Proprietary register(1)
2	24	0B4	Upstream Port Link PM Latency register
3	0	0B5	Upstream Port Link PM Latency register
4	0	0B8	Global Chip Control register
5	0	0B9	Global Chip Control register
6	0	0BA	Global Chip Control register
7	0	0BB	Global Chip Control register
8	0	0BC	GPIOA register
9	0	0BD	GPIOA register
0A	0	0BE	GPIOB register
0B	0	0BF	GPIOB register
0C	0	0C0	GPIOC register
0D	0	0C1	GPIOC register
0E	0	0C2	GPIOD register
0F	0	0C3	GPIOD register
10	0	0C4	GPIO Data register
11	0	0C5	GPIO Data register
12	0	0C6	GPIO Data register
13	0	0C7	GPIO Data register
14	01	0C8	TI Proprietary register(1)
15	0	0CC	TI Proprietary register(1)
16	0	0CD	TI Proprietary register(1)
17	0	0D0	TI Proprietary register(1)
18	0	0D1	TI Proprietary register(1)
19	14	0D2	TI Proprietary register(1)
1A	32	0D3	TI Proprietary register(1)
1B	2	0DC	TI Proprietary register(1)
1C	0	0DE	TI Proprietary register(1)
1D	0	0DF	TI Proprietary register(1)
1E	0	NA	Global Switch/Upstream Port 0 Function Indicator
1F	0	NA	Not used
20	XX	0E0	Subsystem Access Vendor ID register
21	XX	0E1	Subsystem Access Vendor ID register
22	XX	0E2	Subsystem Access Subsys ID register
23	XX	0E3	Subsystem Access Subsys ID register
24	0	0E4	General Control register
25	24	0E8	Downstream Port Link PM Latency register

(1) Required program value

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Table 3-3. EEPROM Register Loading Map (continued)

EEPROM Byte Address (hex)	Suggested Programmed Value (hex)	CONFIG Register Address (hex)	Register Description
26	3F	0E9	Downstream Port Link PM Latency register
27	4	0EA	Global Switch Control register
28	1	NA	Downstream Port 1 Function Indicator
29	0	NA	Not used
2A	01	0C8	TI Proprietary register(1)
2B	0	0CC	TI Proprietary register(1)
2C	0	0CD	TI Proprietary register(1)
2D	0	0D0	TI Proprietary register(1)
2E	0	0D1	TI Proprietary register(1)
2F	14	0D2	TI Proprietary register(1)
30	32	0D3	TI Proprietary register(1)
31	10	0D4	General Control register
32	60	0D5	General Control register
33	1A	0EC	L0s Timeout register
34	0	0EE	General Slot Info register
35	0	0EF	General Slot Info register
36	2	NA	Downstream Port 2 Function Indicator
37	0	NA	Not used
38	01	0C8	TI Proprietary register(1)
39	0	0CC	TI Proprietary register(1)
3A	0	0CD	TI Proprietary register(1)
3B	0	0D0	TI Proprietary register(1)
3C	0	0D1	TI Proprietary register(1)
3D	14	0D2	TI Proprietary register(1)
3E	32	0D3	TI Proprietary register(1)
3F	10	0D4	General Control register
40	60	0D5	General Control register
41	1A	0EC	L0s Timeout register
42	0	0EE	General Slot Info register
43	0	0EF	General Slot Info register
44	2	NA	Downstream Port 3 Function Indicator
45	0	NA	Not used
46	01	0C8	TI Proprietary register(1)
47	0	0CC	TI Proprietary register(1)
48	0	0CD	TI Proprietary register(1)
49	0	0D0	TI Proprietary register(1)
4A	0	0D1	TI Proprietary register(1)
4B	14	0D2	TI Proprietary register(1)
4C	32	0D3	TI Proprietary register(1)
4D	10	0D4	General Control register
4E	60	0D5	General Control register
4F	1A	0EC	L0s Timeout register
50	0	0EE	General Slot Info register
51	0	0EF	General Slot Info register

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This download table must be explicitly followed for the XIO3130 to correctly load initialization values from a serial EEPROM. All byte locations must be considered when programming the EEPROM.

The XIO3130 addresses the serial EEPROM using a default slave address of 1010_000X binary. For an EEPROM download operation that occurs immediately after $\overline{\text{PERST}}$, this address is fixed. The serial EEPROM in the sample application circuit (Figure 3-4) assumes the 1010b high-address nibble. The lower three address bits are terminal inputs to the chip, and the sample application shows these terminal inputs tied to VSS to match the least-significant three address bits.

During an EEPROM download operation, bit 4 (ROMBUSY) in the serial-bus control and status register is asserted. After the download is finished, bit 4 is negated. At that time, bit 0 (ROM_ERR) in the serial-bus control and status register may be monitored to verify a successful download.

3.4.4 Accessing Serial Bus Devices Through Software

The XIO3130 provides a programming mechanism to control serial bus devices through system software. The programming is accomplished through a doubleword of PCI configuration space at offset B0h. Table 3-4 lists the registers used to program a serial-bus device through software.

Table 3-4. Register for Programming Serial-Bus Devices

PCI Offset	Register Name	Description
B0h	Serial-bus data	This register contains the data byte to send on write commands or the received data byte on read commands.
B1h	Serial-bus word address	The content of this register is sent as the word address on byte writes or reads. This register is not used in the quick command protocol.
B2h	Serial-bus slave address	Write transactions to this register initiate a serial-bus transaction. The slave device address and the R/W command selector are programmed through this register.
B3h	Control and Status	Serial interface enable, busy, and error status are communicated through this register. In addition, the protocol-select bit and serial bus test bit are programmed through this register.

To access the serial EEPROM through the software interface, the software performs five steps:

1. Reads the Control and Status Byte to verify that the EEPROM interface is enabled (SBDETECT asserted) and not busy (REQBUSY and ROMBUSY negated).
2. Loads the Serial Bus word address. If the access is a write, the data byte is also loaded.
3. Writes the Serial Bus slave address and read/write command selector byte.
4. Monitors REQBUSY until this bit is negated.
5. Checks SB_ERR to verify that the serial bus operation completed without error. If the operation is a read, after REQBUSY is negated, the serial bus data byte is valid.

3.5 Switch Reset Features

Four XIO3130 reset options are available:

- Internally-generated power-on reset
- A global reset generated by asserting $\overline{\text{GRST}}$ input terminal
- A PCI Express reset generated by asserting $\overline{\text{PERST}}$ input terminal
- Software-initiated resets that are controlled by sending a PCI Express training control hot reset

Table 3-5 identifies these reset sources and describes how the XIO3130 responds to each reset.

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Table 3-5. Switch Reset Options

Reset Option	XIO3130 Feature	Reset Response
Internally-generated power-on reset	During a power-on cycle, the XIO3130 asserts an internal reset and monitors the VDDCOMB15 (C01) terminal. When this terminal reaches 90% of the nominal input voltage specification, power is considered stable. After stable power, the XIO3130 monitors the PCI Express reference clock (REFCLKI) and waits 10 μs after active clocks are detected. Then, internal power-on reset is de-asserted.	When the internal power-on reset is asserted, all control registers, state machines, sticky register bits, and power management state machines are initialized to their default state.
Global reset input $\overline{\text{GRST}}$ (C02)	When $\overline{\text{GRST}}$ is asserted low, an internal power-on reset occurs. This reset is asynchronous and functions during both normal power states and V_{AUX} power states.	When $\overline{\text{GRST}}$ is asserted low, all control registers, state machines, sticky register bits, and power management state machines are initialized to their default state. When the rising edge of $\overline{\text{GRST}}$ occurs, the switch samples the state of all static control inputs and latches the information internally. If an external serial EEPROM is detected, then a download cycle is initiated. Also, the process to configure and initialize the PCI Express link is started. The switch starts link training within 80 ms after $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is de-asserted.
PCI Express reset input $\overline{\text{PERST}}$ (B01)	This XIO3130 input terminal is used by an upstream PCI Express device to generate a PCI Express reset and to signal a system power good condition. When $\overline{\text{PERST}}$ is asserted low, all control register bits that are not sticky are reset. Also, all state machines that are not associated with sticky functionality or VAUX power management are reset. When the rising edge of $\overline{\text{PERST}}$ occurs, the switch samples the state of all static control inputs and latches the information internally. If an external serial EEPROM is detected, then a download cycle is initiated. Also, the process to configure and initialize the PCI Express link is started. The switch starts link training within 80 ms after $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is de-asserted. **Note:** The system must assert $\overline{\text{PERST}}$ before power is removed, before REFCLKI is removed, or before REFCLKI becomes unstable.	When $\overline{\text{PERST}}$ is asserted low, all control register bits that are not sticky are reset. Also, all state machines that are not associated with sticky functionality or V_{AUX} power management are reset. When the rising edge of $\overline{\text{PERST}}$ occurs, the switch samples the state of all static control inputs and latches the information internally. If an external serial EEPROM is detected, then a download cycle is initiated. Also, the process to configure and initialize the PCI Express link is started. The switch starts link training within 80 ms after $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$ is de-asserted.
PCI Express training control hot reset	The XIO3130 responds to a training control hot reset received on the PCI Express interface. After a training control hot reset, the PCI Express interface enters the DL_DOWN state.	In the DL_DOWN state, all remaining configuration register bits and state machines are reset. All remaining bits exclude sticky bits and EEPROM loadable bits. All remaining state machines exclude sticky functionality, EEPROM functionality, and V_{AUX} power management.

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4 XIO3130 Configuration Register Space

This chapter specifies the configuration registers that are used to enumerate the XIO3130 device within a PC system.

An overview of the configuration register space is provided along with a detailed description of the register bits associated with the upstream and downstream ports of the XIO3130.

4.1 PCI Configuration Register Space Overview

Each PCI Express port contains a set of PCI configuration registers. One of the upstream port registers, the Global Chip Control register, is used to control functions across the entire XIO3130.

For downstream ports, only one register set is specified, but this register set is duplicated for each downstream port. Figure 4-1 illustrates the enumeration topology.

The XIO3130 must appear as a hierarchy of PCI-to-PCI bridges in the manner outlined by the PCI Express base specification.

NOTE

This numbering scheme is typical but not ensured. Bus numbers are assigned within the Type 01h configuration header during the initial enumeration of the PCI bus by the system at power-up.

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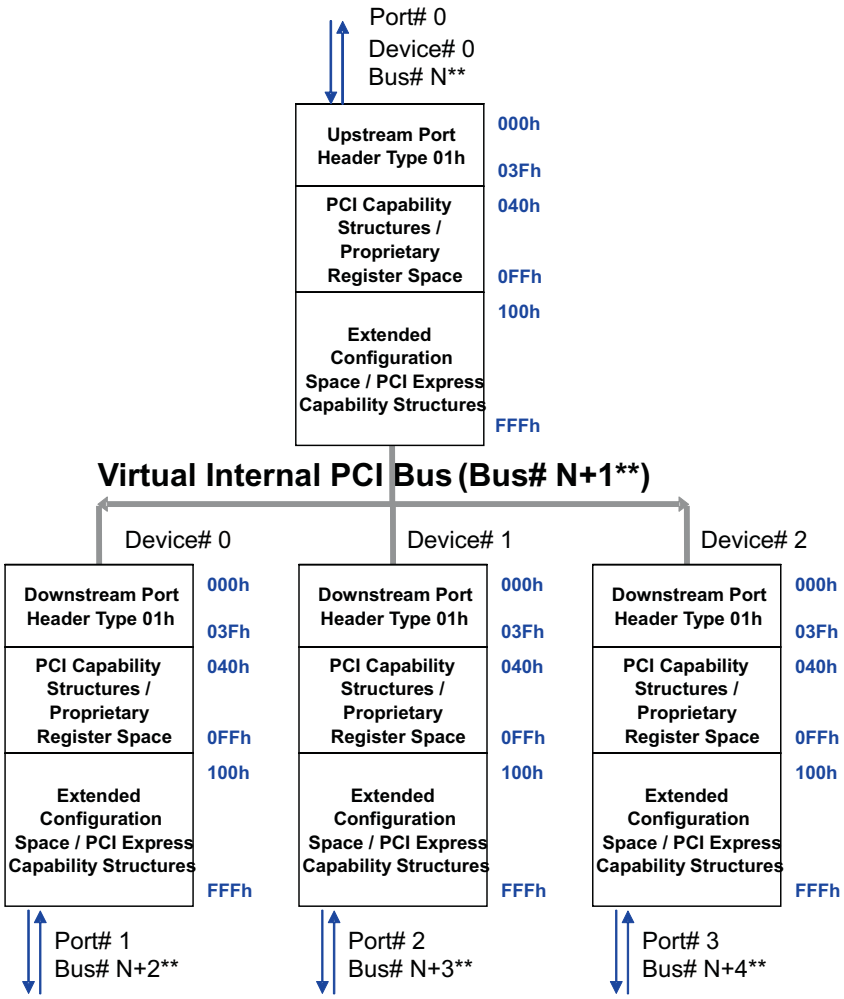

** Example values. Actual bus numbers may change based on system hierarchy.

Figure 4-1. XIO3130 Enumerations Topology

4.2 PCI Express Upstream Port Registers

The default reset domain for all upstream port registers is $\overline{\text{IPRST}}$. The internal $\overline{\text{IPRST}}$ reset signal is asserted when the internally-generated power-on reset is asserted, when $\overline{\text{GRST}}$ is asserted, when $\overline{\text{PERST}}$ is asserted, or when PCI Express training control hot reset is asserted. Some register fields are placed in a reset domain different from the default reset domain; all bit or field descriptions identify any unique reset domains. Generally, all sticky bits are placed in the $\overline{\text{GRST}}$ domain and all (non-sticky) EEPROM loadable bits are placed in the $\overline{\text{PERST}}$ domain.

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4.2.1 PCI Configuration Space (Upstream Port) Register Map

Table 4-1. PCI Express Upstream Port Configuration Register Map (Type 1)

Register Name				Offset
Device ID		Vendor ID		000h
Status		Command		004h
Class Code			Revision ID	008h
BIST	Header Type	Latency Timer	Cache Line Size	00Ch
Reserved				010h-014h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	018h
Secondary Status		I/O Limit	I/O Base	01Ch
Memory Limit		Memory Base		020h
Pre-fetchable Memory Limit		Pre-fetchable Memory Base		024h
Pre-fetchable Base Upper 32 Bits				028h
Pre-fetchable Limit Upper 32 Bits				02Ch
I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		030h
Reserved			Capabilities Pointer	034h
Reserved				038h
Bridge Control		Interrupt Pin	Interrupt Line	03Ch
Reserved				040h-04Ch
Power Management Capabilities		Next-item Pointer	PM CAP ID	050h
PM Data (RSVD)	PMCSR_BSE	Power Management CSR		054h
Reserved				058h-06Ch
MSI Message Control		Next-item Pointer	MSI CAP ID	070h
MSI Message Address				074h
MSI Upper Message Address				078h
Reserved		MSI Message Data		07Ch
Reserved		Next-item Pointer	SSID/SSVID CAP ID	080h
Subsystem ID		Subsystem Vendor ID		084h
Reserved				088h-08Ch
PCI Express Capabilities Register		Next-item Pointer	PCI Express Capability ID	090h
Device Capabilities				094h
Device Status		Device Control		098h
Link Capabilities				09Ch
Link Status		Link Control		0A0h
Reserved				0A4h-0ACh
SB Control and Status	Serial Bus Slave Address	Serial Bus Index	Serial Bus Data	0B0h
Upstream Port L1 Idle		Upstream Port Link PM Latency		0B4h
Global Chip Control				0B8h
GPIO B Control		GPIO A Control		0BCh
GPIO D Control		GPIO C Control		0C0h
GPIO Data				0C4h
TI Proprietary				0C8h-0DCh
Subsystem Access				0E0h
General Control				0E4h
Global Switch Control		Downstream Ports Link PM Latency		0E8h
Reserved				0ECh-0FCh

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Table 4-2. Extended Configuration Space (Upstream Port)

Register Name		Offset
Next Capability Offset / Capability Version	PCI Express Advanced Error Reporting Capabilities ID	100h
Uncorrectable Error Status Register		104h
Uncorrectable Error Mask Register		108h
Uncorrectable Error Severity Register		10Ch
Correctable Error Status Register		110h
Correctable Error Mask		114h
Advanced Error Capabilities and Control		118h
Header Log Register		11Ch
Header Log Register		120h
Header Log Register		124h
Header Log Register		128h
Reserved		12Ch-FFCh

4.2.2 Vendor ID Register

This 16-bit read-only register contains the value 104Ch, which is the vendor ID assigned to Texas Instruments.

PCI register offset: 00h
Register type: Read-only
Default value: 104Ch

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

4.2.3 Device ID Register

This 16-bit read-only register contains the value 8232h, which is the device ID assigned by TI to the XIO3130 upstream port function.

PCI register offset: 02h
Register type: Read-only
Default value: 8232Ch

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	1	0	0	0	1	1	0	0	1	0

4.2.4 Command Registers

PCI register offset: 04h
Register type: Read/Write; Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-3. Bit Descriptions – Command Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:11	RSVD	r	Reserved. When read, these bits return zeros.
10	INT_DISABLE	rw	$\overline{\text{INTx}}$ disable. This bit is used to enable device-specific interrupts. The XIO3130 upstream port does not generate any interrupts internally, so this bit is ignored. The XIO3130 does forward INTx messages from downstream ports to the upstream port.
9	FBB_ENB	r	Fast back-to-back enable. This bit does not apply to PCI-Express, and returns zero when read.
8	SERR_ENB	rw	$\overline{\text{SERR}}$ enable. When set, the XIO3130 can signal fatal and nonfatal errors on the upstream PCI Express interface. 0 – Disable the reporting of nonfatal errors and fatal errors. 1 – Enable the reporting of nonfatal errors and fatal errors.
7	STEP_ENB	r	Address/data stepping control. This bit does not apply to PCI-Express and is hardwired to 0.
6	PERR_ENB	rw	Parity error response enable. Mask bit for the DATAPAR bit in the Status Register. 0 – The upstream bridge must ignore any address or data parity errors that it detects and continue normal operation. 1 – The upstream bridge must detect address or data parity errors and report them by setting the DATAPAR bit in the Status Register.
5	VGA_ENB	r	VGA palette snoop enable. The XIO3130 does not support VGA palette snooping, thus this bit returns zero when read.
4	MWI_ENB	r	Memory write and invalidate enable. This bit does not apply to PCI-Express, and is hardwired to zero.
3	SPECIAL	r	Special cycle enable. This bit does not apply to PCI-Express and is hardwired to zero.
2	MASTER_ENB	rw	Bus master enable. When set, the XIO3130 is enabled to initiate cycles on the upstream PCI Express interface. 0 – Upstream PCI Express interface cannot initiate transactions. The bridge must disable response to memory and I/O transactions on the PCI interface. 1 – Upstream PCI Express interface can initiate transactions. The bridge can forward memory and I/O transactions from the secondary interface.
1	MEMORY_ENB	rw	Memory response enable. Setting this bit enables the XIO3130 to respond to memory transactions on the upstream PCI Express interface.
0	IO_ENB	rw	I/O space enable. Setting this bit enables the XIO3130 to respond to I/O transactions on the upstream PCI Express interface.

4.2.5 Status Register

The Status register provides information about the primary interface to the system.

PCI register offset: 06h
Register type: Read Only; Cleared by a Write of One; Hardware Update
Default value: 0010h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

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Table 4-4. Bit Descriptions – Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PAR_ERR	rcu	Detected parity error. This bit is set when the PCI Express interface receives a poisoned TLP on the upstream port. This bit is set regardless of the state of the Parity Error Response bit in the Command Register. 0 – No parity error detected. 1 – Parity Error detected.
14	SYS_ERR	rcu	Signaled system error. This bit is set when the XIO3130 sends an ERR_FATAL or ERR_NONFATAL message upstream, and the SERR Enable bit in the Command Register is set. 0 – No error signaled. 1 – ERR_FATAL or ERR_NONFATAL signaled.
13	MABORT	rcu	Received master abort. This bit is set when the upstream PCI Express interface of the XIO3130 receives a Completion with Unsupported Request Status 0 – Unsupported Request not received. 1 – Unsupported Request received on.
12	TABORT_REC	rcu	Received target abort. This bit is set when the upstream PCI Express interface of the XIO3130 receives a Completion with Completer Abort Status 0 – Completer Abort not received. 1 – Completer Abort received.
11	TABORT_SIG	rcu	Signaled target abort. This bit is set when the upstream PCI Express interface completes a Request with Completer Abort Status. 0 – Completer Abort not signaled. 1 – Completer Abort signaled.
10:9	PCI_SPEED	r	DEVSEL timing. These bits are read only zero because they do not apply to PCI Express.
8	DATAPAR	rcu	Master data parity error. This bit is set when the XIO3130 receives a poisoned completion or poisons a write request on the upstream PCI Express interface. This bit is never set if the parity error response enable bit in the Command register is clear.
7	FBB_CAP	r	Fast back-to-back capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to 0.
6	RSVD	r	Reserved. When read, this bit returns zero.
5	66MHZ	r	66 MHz capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to 0.
4	CAPLIST	r	Capabilities list. This bit returns 1 when read, indicating that the XIO3130 supports additional PCI capabilities.
3	INT_STATUS	r	Interrupt status. This bit reflects the interrupt status of the function. This bit is read-only zero since the XIO3130 upstream port does not generate any interrupts internally. The XIO3130 does forward INTx messages from downstream ports to the upstream port (see INTx Support section).
2:0	RSVD	r	Reserved. When read, these bits return zeros.

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4.2.6 Class Code and Revision ID Register

This read-only register categorizes the Base Class, Sub Class, and Programming Interface of the XIO3130. The Base Class is 06h, identifying the device as bridge device. The Sub Class is 04h, identifying the function as a PCI-to-PCI bridge, and the Programming Interface is 00h. Also, the TI chip revision is indicated in the lower byte (02h).

PCI register offset: 08h
Register type: Read only
Default value: 0604 0002h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Table 4-5. Bit Descriptions – Class Code and Revision ID Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	BASECLASS	r	Base Class. This field returns 06h when read, which classifies the function as a Bridge device.
23:16	SUBCLASS	r	Sub Class. This field returns 04h when read, which specifically classifies the function as a PCI-to-PCI bridge.
15:8	PGMIF	r	Programming Interface. This field returns 00h when read.
7:0	CHIPREV	r	Silicon Revision. This field returns the silicon revision.

4.2.7 Cache Line Size Register

The Cache Line Size Register is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

PCI register offset: 0Ch
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.2.8 Primary Latency Timer Register

This read-only register has no meaningful context for a PCI Express device and returns zeros when read.

PCI register offset: 0Dh
Register type: Read Only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

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4.2.9 Header Type Register

This read-only register indicates that this function has a type one PCI header. Bit seven of this register is a zero, indicating that the upstream port is a single device.

PCI register offset: 0Eh

Register type: Read Only

Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

4.2.10 BIST Register

Since the XIO3130 does not support a built-in self test (BIST), this read-only register returns the value of 00h when read.

PCI register offset: 0Fh

Register type: Read Only

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.2.11 Primary Bus Number

This read/write register specifies the bus number of the PCI bus segment to which the upstream PCI Express interface is connected.

PCI register offset: 18h

Register type: Read/Write

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.2.12 Secondary Bus Number

This read/write register specifies the bus number of the PCI bus segment for the XIO3130's internal PCI bus. The XIO3130 uses this register to determine how to respond to a Type 1 configuration transaction.

PCI register offset: 19h

Register type: Read/Write

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

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4.2.13 Subordinate Bus Number

This register specifies the bus number of the highest number PCI bus segment that is downstream of the XIO3130's upstream port. The XIO3130 uses this register to determine how to respond to a Type 1 configuration transaction.

PCI register offset: 1Ah
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.2.14 Secondary Latency Timer Register

This register does not apply to PCI-Express. It is hardwired to zero.

PCI register offset: 1Bh
Register type: Read Only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.2.15 I/O Base Register

This read/write register specifies the lower limit of the I/O addresses that the XIO3130 forwards downstream.

PCI register offset: 1Ch
Register type: Read/Write; Read Only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

Table 4-6. Bit Descriptions – I/O Base Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	IOBASE	rw	I/O base. These bits define the bottom address of the I/O address range that is used to determine when to forward I/O transactions from one interface to the other. These bits correspond to address bits [15:12] in the I/O address. The lower 12 I/O address bits are assumed to be 0. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O Base Upper 16 Bits register.
3:0	IOTYPE	r	I/O type. This field is read-only 01h, indicating that the XIO3130 supports 32-bit I/O addressing.

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4.2.16 I/O Limit Register

This read/write register specifies the upper limit of the I/O addresses that the XIO3130 forwards downstream.

PCI register offset: 1Dh

Register type: Read/Write; Read Only

Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

Table 4-7. Bit Descriptions – I/O Limit Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	IOLIMIT	rw	I/O limit. These bits define the top address of the I/O address range used to determine when to forward I/O transactions from one interface to the other. These bits correspond to address bits [15:12] in the I/O address. The lower 12 I/O address bits are assumed to be FFFh. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O Limit Upper 16 Bits register.
3:0	IOTYPE	r	I/O type. This field is read-only 01h, indicating that the XIO3130 supports 32-bit I/O addressing.

4.2.17 Secondary Status Register

The Secondary Status register provides information about the XIO3130's internal PCI bus between the upstream port and the downstream ports.

PCI register offset: 1Eh

Register type: Read only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-8. Bit Descriptions – Secondary Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PAR_ERR	r	Detected parity error. This bit is hardwired to zero. It is assumed that the relevant error checking is unnecessary for the XIO3130's internal PCI bus.
14	SYS_ERR	r	Received system error. This bit is hardwired to zero. It is assumed that the relevant error checking is unnecessary for the XIO3130's internal PCI bus.
13	MABORT	r	Received master abort. This bit is hardwired to zero. It is assumed that the relevant error checking is unnecessary for the XIO3130's internal PCI bus.
12	TABORT_REC	r	Received target abort. This bit is hardwired to zero. It is assumed that the relevant error checking is unnecessary for the XIO3130's internal PCI bus.
11	TABORT_SIG	r	Signaled target abort. This bit is hardwired to zero. It is assumed that the relevant error checking is unnecessary for the XIO3130's internal PCI bus.
10:9	PCI_SPEED	r	DEVSEL timing. These bits are hardwired to 00. These bits do not apply to PCI Express.
8	DATAPAR	r	Master data parity error. This bit is hardwired to zero. It is assumed that the relevant error checking is unnecessary for the XIO3130's internal PCI bus.
7	FBB_CAP	r	Fast back-to-back capable. This bit is hardwired to zero. This bit does not apply to PCI Express.
6	RSVD	r	Reserved. When read, this bit returns zero.
5	66MHZ	r	66 MHz capable. This bit is hardwired to zero. This bit does not apply to PCI Express.
4:0	RSVD	r	Reserved. When read, these bits return zeros.

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4.2.18 Memory Base Register

This read/write register specifies the lower limit of the memory addresses that the XIO3130 forwards downstream.

PCI register offset: 20h
Register type: Read/Write; Read Only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-9. Bit Descriptions – Memory Base Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MEMBASE	rw	Memory base. This field defines the bottom address of the memory address range used to determine when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 0.
3:0	RSVD	r	Reserved. When read, these bits return zeros.

4.2.19 Memory Limit Register

This read/write register specifies the upper limit of the memory addresses that the XIO3130 forwards downstream.

PCI register offset: 22h
Register type: Read/Write; Read Only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4-10. Bit Descriptions – Memory Limit Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MEMLIMIT	rw	Memory limit. This field defines the top address of the memory address range used to determine when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh.
3:0	RSVD	r	Reserved. When read, these bits return zeros.

4.2.20 Pre-fetchable Memory Base Register

This read/write register specifies the lower limit of the pre-fetchable memory addresses that the XIO3130 forwards downstream.

PCI register offset: 24h
Register type: Read/Write; Read Only
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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Table 4-11. Bit Descriptions – Pre-fetchable Memory Base Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	PREBASE	rw	Pre-fetchable memory base. This field defines the bottom address of the pre-fetchable memory address range that is used to determine when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 0. The Pre-fetchable Base Upper 32 Bits register is used to specify the bit [63:32] of the 64-bit pre-fetchable memory address.
3:0	64BIT	r	64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window.

4.2.21 Pre-Fetchable Memory Limit Register

This read/write register specifies the upper limit of the pre-fetchable memory addresses that the XIO3130 forwards downstream.

PCI register offset: 26h

Register type: Read/Write; Read Only

Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4-12. Bit Descriptions – Pre-fetchable Memory Limit Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	PRELIMIT	rw	Pre-fetchable memory limit. These bits define the top address of the pre-fetchable memory address range used to determine when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. The Pre-fetchable Limit Upper 32 Bits register is used to specify the bit [63:32] of the 64-bit pre-fetchable memory address.
3:0	64BIT	r	64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window.

4.2.22 Pre-Fetchable Base Upper 32 Bits Register

This read/write register specifies the upper 32 bits of the Pre-fetchable Memory Base register.

PCI register offset: 28h

Register type: Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-13. Bit Descriptions – Pre-fetchable Base Upper 32 Bits Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:0	PREBASE	rw	Pre-fetchable memory base upper 32 bits. This field defines the upper 32 bits of the bottom address of the pre-fetchable memory address range that is used to determine when to forward memory transactions downstream.

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4.2.23 Pre-fetchable Limit Upper 32 Bits Register

This read/write register specifies the upper 32 bits of the Pre-fetchable Memory Limit register.

PCI register offset: 2Ch
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-14. Bit Descriptions – Pre-fetchable Limit Upper 32 Bits Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:0	PRELIMIT	rw	Pre-fetchable memory limit upper 32 bits. This field defines the upper 32 bits of the top address of the pre-fetchable memory address range used to determine when to forward memory transactions downstream.

4.2.24 I/O Base Upper 16 Bits Register

This read/write register specifies the upper 16 bits of the I/O Base register.

PCI register offset: 30h
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-15. Bit Descriptions – I/O Base Upper 16 Bits Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:0	IOBASE	rw	I/O base upper 16 bits. This field defines the upper 16 bits of the bottom address of the I/O address range that is used to determine when to forward I/O transactions downstream.

4.2.25 I/O Limit Upper 16 Bits Register

This read/write register specifies the upper 16 bits of the I/O Limit register.

PCI register offset: 32h
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-16. Bit Descriptions – I/O Limit Upper 16 Bits Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:0	IOLIMIT	rw	I/O limit upper 16 bits. This field defines the upper 16 bits of the top address of the I/O address range used to determine when to forward I/O transactions downstream.

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4.2.26 Capabilities Pointer Register

This read-only register provides a pointer into the PCI configuration header where the PCI power management block resides. Since the PCI power management registers begin at 50h, this register is hardwired to 50h.

PCI register offset: 34h

Register type: Read only

Default value: 50h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	1	0	0	0	0

4.2.27 Interrupt Line Register

This read/write register, which is programmed by the system, indicates to the software which interrupt line the XIO3130 has assigned to it. The default value of this register is FFh, which indicates that an interrupt line has not yet been assigned to the function. Since the XIO3130 does not generate interrupts internally, this register is essentially a scratch-pad register; it has no effect on the XIO3130 itself.

PCI register offset: 3Ch

Register type: Read/Write

Default value: FFh

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	1	1	1	1	1	1	1

4.2.28 Interrupt Pin Register

The Interrupt Pin register is read-only 00h, which indicates that the XIO3130 upstream port does not generate interrupts. The value of this register has no effect on forwarding interrupts from the downstream ports to the upstream port.

PCI register offset: 3Dh

Register type: Read Only

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.2.29 Bridge Control Register

The Bridge Control register provides extensions to the Command register that are specific to a bridge.

PCI register offset: 3Eh

Register type: Read/Write; Read Only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-17. Bit Descriptions – Bridge Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:12	RSVD	r	Reserved. When read, these bits return zeros.
11	DTSERR	r	Discard timer $\overline{\text{SERR}}$ enable. This bit is hardwired to zero. This bit does not apply to PCI Express.
10	DTSTATUS	r	Discard timer status. This bit is hardwired to zero. This bit does not apply to PCI Express.
9	SEC_DT	r	Secondary discard timer. This bit is hardwired to zero. This bit does not apply to PCI Express.
8	PRI_DEC	r	Primary discard timer. This bit is hardwired to zero. This bit does not apply to PCI Express.
7	FBB_EN	r	Fast back-to-back enable. This bit is hardwired to zero. This bit does not apply to PCI Express.
6	SRST	rw	Secondary bus reset. This bit is set when software wishes to reset all devices downstream of the XIO3130. Setting this bit causes all of the downstream ports to be reset, and all of the downstream ports to send a reset via a training sequence. 0 – Downstream ports not in Reset state. 1 – Downstream ports in Reset state.
5	MAM	r	Master abort mode. This bit is hardwired to zero. This bit does not apply to PCI Express.
4	VGA16	rw	VGA 16-bit decode. This bit enables the XIO3130 to provide full 16-bit decoding for VGA I/O addresses. This bit only has meaning if the VGA enable bit is set. 0 – Ignore address bits [15:10] when decoding VGA I/O addresses. 1 – Decode address bits [15:10] when decoding VGA I/O addresses.
3	VGA	rw	VGA enable. This bit modifies the response by the XIO3130 to VGA-compatible addresses. If this bit is set, the XIO3130 positively decodes and forwards the following accesses on the primary interface to the secondary interface (and, conversely, blocks the forwarding of these addresses from the secondary to primary interface): • Memory accesses in the range 000A 0000h to 000BFFFFh • I/O addresses in the first 64 KB of the I/O address space (Address bits [31:16] are 0000h) and where address bits [9:0] is in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – Address bits [15:10] may possess any value and is not used in the decoding). If the VGA Enable bit is set, forwarding of VGA addresses is independent of the value of the ISA Enable bit (located in the Bridge Control register), the I/O address range and memory address ranges defined by the I/O Base and Limit registers, the Memory Base and Limit registers, and the Pre-fetchable Memory Base and Limit registers of the bridge. The forwarding of VGA addresses is qualified by the I/O Enable and Memory Enable bits in the Command register. 0 – Do not forward VGA-compatible memory and I/O addresses from the primary to secondary interface (addresses defined above) unless they are enabled for forwarding by the defined I/O and memory address ranges. 1 – Forward VGA-compatible memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (if the I/O Enable and Memory Enable bits are set) independent of the I/O and memory address ranges and independent of the ISA Enable bit.
2	ISA	rw	ISA enable. This bit modifies the response by the XIO3130 to ISA I/O addresses. This bit applies only to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, the bridge blocks any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1 KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1K block. 0 – Forward downstream all I/O addresses in the address range defined by the I/O Base and I/O Limit registers. 1 – Forward upstream ISA I/O addresses in the address range defined by the I/O Base and I/O Limit registers that are in the first 64 KB of PCI I/O address space (top 768 bytes of each 1 KB block).
1	SERR_EN	rw	SERR enable. This bit controls forwarding of system error events upstream from the secondary interface to the primary interface. The XIO3130 forwards system error events when: • This bit is set. • The $\overline{\text{SERR}}$ enable bit in the upstream port command register is set. • $\overline{\text{SERR}}$ is asserted on the secondary interface. 0 – Disable the forwarding of system error events. 1 – Enable the forwarding of system error events.

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Table 4-17. Bit Descriptions – Bridge Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
0	PERR_EN	rw	Parity error response enable. It is assumed that the relevant error checking is unnecessary for the XIO3130's internal PCI bus; therefore, setting this bit has no effect.

4.2.30 Capability ID Register

This read-only register identifies the linked list item as the register for PCI power management. The register returns 01h when read.

PCI register offset: 50h
Register type: Read only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

4.2.31 Next-Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the XIO3130. This register reads 70h, which points to the MSI Capabilities registers.

PCI register offset: 51h
Register type: Read only
Default value: 70h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	1	1	0	0	0	0

4.2.32 Power Management Capabilities Register

This register indicates the capabilities of the XIO3130 related to PCI power management.

PCI register offset: 52h
Register type: Read only
Default value: XX03h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	y	1	1	x	1	1	x	0	0	0	0	0	0	0	1	1

Table 4-18. Bit Descriptions – Power Management Capabilities Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:11	PME_SUPPORT	r	$\overline{\text{PME}}$ support. This five-bit field indicates the power states from which the (upstream) port may assert $\overline{\text{PME}}$. These five bits return a value of 5'by11x1, indicating that the XIO3130 can assert $\overline{\text{PME}}$ from D0, D2, D3hot, maybe D3cold (i.e., depending on y), and maybe D1 (i.e., depending on x). The bit defining this for D3cold (i.e., y) is controlled by the AUX_PRSNT bit in the Global Chip Control register. The bit defining this for D1 (i.e., x) is controlled by the D1_SUPPORT bit in the Global Switch Control register.
10	D2_SUPPORT	r	D2 device power state support. This bit returns a 1 when read, which indicates that the function supports the D2 device power state.
9	D1_SUPPORT	r	D1 device power state support. This bit indicates whether the function supports the D1 device power state. This bit is controlled by the D1_SUPPORT bit in the Global Switch Control register. The default value x refers to whatever the default value is for the D1_SUPPORT bit in the Global Switch Control register.

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Table 4-18. Bit Descriptions – Power Management Capabilities Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
8:6	AUX_CURRENT	r	3.3-V_{AUX} auxiliary current requirements. This field is hardwired to 3'b000. See *PCI Power Management Specification Revision 1.2*, Section 3.2.3, Page 26, for mapping this field to specific current consumption values.
5	DSI	r	Device-specific initialization. This bit returns 0 when read, which indicates that the XIO3130 does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it.
4	RSVD	r	Reserved. When read, this bit returns zero.
3	PME_CLK	r	$\overline{\text{PME}}$ clock. This bit returns zero, which indicates that the PCI clock is not needed to generate $\overline{\text{PME}}$.
2:0	PM_VERSION	r	Power management version. This field returns 3'b011, which indicates Revision 1.2 compatibility.

4.2.33 Power Management Control/Status Register

This register determines and changes the current power state of the XIO3130.

PCI register offset: 54h
Register type: Read/Write; Read Only
Default value: 0008h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Table 4-19. Bit Descriptions – Power Management Control/Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PME_STAT	r	$\overline{\text{PME}}$ status. This bit is hardwired to 0b since the XIO3130's upstream port does not generate $\overline{\text{PME}}$ regardless of PME_SUPPORT field setting.
14:13	DATA_SCALE	r	Data scale. This 2-bit field returns 0's when read since the XIO3130 does not use the Data Register.
12:9	DATA_SEL	r	Data select. This 4-bit field returns 0's when read since the XIO3130 does not use the Data Register
8	PME_EN	r	$\overline{\text{PME}}$ enable. This bit enables $\overline{\text{PME}}$ signaling. This bit is hardwired to 0b since the XIO3130's upstream port does not generate $\overline{\text{PME}}$.
7:4	RSVD	r	Reserved. When read, these bits return zeros.
3	NO_SOFT_RST	r	No soft reset. This bit controls whether the transition from D3hot to D0 resets the state according to the *PCI Power Management Specification Revision 1.2*. This bit is hardwired to 1'b1. 0 – D3hot to D0 transition causes reset. 1 – D3hot to D0 transition does not cause reset.
2	RSVD	r	Reserved. When read, this bit returns zero.
1:0	PWR_STATE	rw	Power state. This 2-bit field is used both to determine the current power state of the function and to set the function into a new power state. This field is encoded as follows: 00 = D0 01 = D1 10 = D2 11 = $D3_{hot}$ See the Power Management section of this document for information about what the XIO3130 does in these different power states.

4.2.34 Power Management Bridge Support Extension Register

This read-only register is used to indicate to host software the state of the secondary bus when the XIO3130 is placed in D3.

PCI register offset: 56h

Register type: Read only

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-20. Bit Descriptions – PM Bridge Support Extension Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	BPCC	r	Bus power/Clock control enable. This bit is read-only zero. This bit does not apply to PCI Express.
6	BSTATE	r	B2/B3 support. This bit is read-only zero. This bit does not apply to PCI Express.
5:0	RSVD	r	Reserved. When read, these bits return zeros.

4.2.35 Power Management Data Register

This read-only register is not applicable to the XIO3130 and returns 00h when read.

PCI register offset: 57h

Register type: Read only

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.2.36 MSI Capability ID Register

This read-only register identifies the linked list item as the register for Message Signaled Interrupts (MSI) Capabilities. The register returns 05h when read.

PCI register offset: 70h

Register type: Read only

Default value: 05h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	1

4.2.37 Next-Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the XIO3130. This register reads 80h, which points to the Subsystem ID and Subsystem Vendor ID Capabilities registers.

PCI register offset: 71h

Register type: Read only

Default value: 80h

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BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	0	0

4.2.38 MSI Message Control Register

This register is used to control the sending of MSI messages.

PCI register offset: 72h
Register type: Read/Write; Read Only
Default value: 0080h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Table 4-21. Bit Descriptions – MSI Message Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	r	Reserved. When read, these bits return zeros.
7	64CAP	r	64-bit message capability. This bit is read-only 1, which indicates that the XIO3130 supports 64-bit MSI message addressing.
6:4	MM_EN	rw	Multiple message enable. This bit indicates the number of distinct messages that the XIO3130 is allowed to generate. 000 – 1 Message 001 – 2 Messages 010 – 4 Messages 011 – 8 Messages 100 – 16 Messages 101 – 32 Messages 110 – Reserved 111 – Reserved
3:1	MM_CAP	r	Multiple message capabilities. This field indicates the number of distinct messages that the XIO3130 is capable of generating. This field is read-only 000, which indicates that the XIO3130 can signal one interrupt.
0	MSI_EN	rw	MSI enable. This bit is used to enable MSI interrupt signaling. MSI signaling must be enabled by software for the XIO3130 to send MSI messages. 0 – MSI signaling is prohibited. 1 – MSI signaling is enabled.

4.2.39 MSI Message Address Register

This register contains the lower 32 bits of the address that a MSI message shall be written to when an interrupt is to be signaled.

PCI register offset: 74h
Register type: Read/Write; Read Only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-22. Bit Descriptions – MSI Message Address Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:2	ADDRESS	rw	System Specified Message Address.
1:0	RSVD	r	Reserved. When read, these bits return zeros.

4.2.40 MSI Message Upper Address Register

This register contains the upper 32 bits of the address that a MSI message shall be written to when an interrupt is to be signaled. If this register is 0000 0000h, 32-bit addressing is used; otherwise, 64-bit addressing is used.

PCI register offset: 78h

Register type: Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCI register offset: 56h

Register type: Read only

Default value: 00h

4.2.41 MSI Message Data Register

This register contains the data that software programmed the device to send when it sends a MSI message.

PCI register offset: 7Ch

Register type: Read/Write

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-23. Bit Descriptions – MSI Data Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MSG	rw	System-specific message. This field contains the portion of the message that the XIO3130 can never modify.
3:0	MSG_NUM	rw	Message number. This portion of the message field may be modified to contain the message number if multiple messages are enabled. Since the XIO3130 only generates one MSI type, these bits are not modified by XIO3130 hardware.

4.2.42 Capability ID Register

This read-only register identifies the linked list item as the register for Subsystem ID and Subsystem Vendor ID Capabilities. The register returns 0Dh when read.

PCI register offset: 80h

Register type: Read only

Default value: 0Dh

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BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	1	1	0	1

4.2.43 Next-Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the XIO3130. This register reads 90h, which points to the PCI Express Capabilities registers.

PCI register offset: 81h
Register type: Read only
Default value: 90h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	1	0	0	0	0

4.2.44 Subsystem Vendor ID Register

This register, which is used for system and option card identification purposes, may be required for certain operating systems. This read-only register is a direct reflection of the Subsystem Access register, which is read/write and is initialized through the EEPROM (if present).

PCI register offset: 84h
Register type: Read only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.2.45 Subsystem ID Register

This register, which is used for system and option card identification purposes, may be required for certain operating systems. This read-only register is a direct reflection of the Subsystem Access register, which is read/write and is initialized through the EEPROM (if present).

PCI register offset: 86h
Register type: Read only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.2.46 PCI Express Capability ID Register

This read-only register identifies the linked list item as the register for PCI Express Capabilities. The register returns 10h when read.

PCI register offset: 90h
Register type: Read only
Default value: 10h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0

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4.2.47 Next-Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the XIO3130. This register reads 00h, which indicates that no additional capabilities are supported.

PCI register offset: 91h
Register type: Read only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.2.48 PCI Express Capabilities Register

This register indicates the capabilities of the upstream port of the XIO3130 related to PCI Express.

PCI register offset: 92h
Register type: Read only
Default value: 0051h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1

Table 4-24. Bit Descriptions – PCI Express Capabilities Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:14	RSVD	r	Reserved. When read, these bits return zeros.
13:9	INT_NUM	r	Interrupt message number. This field is used for MSI support and is implemented as read-only zero in the XIO3130.
8	SLOT	r	Slot implemented. This bit is invalid for the upstream port on the XIO3130 and is read-only zero.
7:4	DEV_TYPE	r	Device/Port type. This read-only field returns 0101b, which indicates that the device is an upstream port of a PCI Express XIO3130.
3:0	VERSION	r	Capability version. This field returns 0001b, which indicates revision 1 of the PCI Express capability.

4.2.49 Device Capabilities Register

The Device Capabilities register indicates the device-specific capabilities of the XIO3130.

PCI register offset: 94h
Register type: Read Only; Hardware Update
Default value: 0000 8001h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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Table 4-25. Bit Descriptions – Device Capabilities Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:28	RSVD	r	Reserved. When read, these bits return zeros.
27:26	CSPLS	ru	Captured slot power limit scale. The value in this register is programmed by the host by issuing a Set_Slot_Power_Limit Message. When a Set_Slot_Power_Limit Message is received, bits 9:8 are written to this field. The value in this register specifies the scale used for the Slot Power Limit. 00 – 1.0x 01 – 0.1x 10 – 0.01x 11 – 0.001x
25:18	CSPLV	ru	Captured slot power limit value. The value in this register is programmed by the host by issuing a Set_Slot_Power_Limit Message. When a Set_Slot_Power_Limit Message is received, bits 7:0 are written to this field. The value in this register, in combination with the Slot power limit scale value, specifies the upper limit of power supplied to the slot. The power limit is calculated by multiplying the value in this field by the value in the Slot power limit scale field.
17:16	RSVD	r	Reserved. When read, these bits return zeros.
15	RBER	r	Role-based error reporting. This field is set to 1b to indicate support for role-based error reporting.
14:6	RSVD	r	Reserved. When read, these bits return zeros.
5	ETFS	r	Extended tag field supported. This field indicates the size of the tag field supported. This bit is hardwired to zero, indicating support for 5-bit tag fields.
4:3	PFS	r	Phantom functions supported. This field is read-only 00b, indicating that function numbers are not used for phantom functions.
2:0	MPSS	r	Max payload size supported. This field indicates the maximum payload size that the device can support for TLPs. This field is encoded as 001b, which indicates that the maximum payload size for a TLP is 256 bytes.

4.2.50 Device Control Register

The Device Control register controls PCI Express device-specific parameters.

PCI register offset: 98h
Register type: Read/Write; Read Only
Default value: 2000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-26. Bit Descriptions – Device Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	RSVD	r	Reserved. When read, this bit returns zero.
14:12	MRRS	rw	Max read request size. This field is programmed by the host software to set the maximum size of a read request that the XIO3130 can generate. The XIO3130 uses this field in conjunction with the cache line size register to determine how much data to fetch on a read request. This field is encoded as: 000 – 128B 001 – 256B 010 – 512B 011 – 1024B 100 – 2048B 101 – 4096B 110 – Reserved 111 – Reserved

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Table 4-26. Bit Descriptions – Device Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
11	ENS	r	Enable no snoop. Since the XIO3130 does not initiate such transactions, this bit is read-only zero.
10	APPE	r	Auxiliary power PM enable. This bit is read-only zero, since the XIO3130 requires a minimal amount of AUX power when PME is disabled.
9	PFE	r	Phantom function enable. Since the XIO3130 part does not support phantom functions, this bit is read-only zero.
8	ETFE	r	Extended tag field enable. Since the XIO3130 part does not support extended tags, this bit is read-only zero.
7:5	MPS	rw	Max payload size. This field is programmed by the host software to set the maximum size of posted writes or read completions that the XIO3130 can initiate. This field is encoded as: 000 – 128B 001 – 256B 010 – 512B 011 – 1024B 100 – 2048B 101 – 4096B 110 – Reserved 111 – Reserved
4	ERO	r	Enable relaxed ordering. Since the XIO3130 part does not support relaxed ordering, this bit is read-only zero.
3	URRE	rw	Unsupported request reporting enable. If this bit is set, the XIO3130 is enabled to send ERR_NONFATAL messages to the root complex when an unsupported request is received by the upstream port. 0 – Do not report unsupported requests to the root complex. 1 – Report unsupported requests to the root complex.
2	FERE	rw	Fatal error reporting enable. If this bit is set, the XIO3130 is enabled to send ERR_FATAL messages to the root complex when a system error event occurs. 0 – Do not report fatal errors to the root complex. 1 – Report fatal errors to the root complex.
1	NFERE	rw	Nonfatal error reporting enable. If this bit is set, the XIO3130 is enabled to send ERR_NONFATAL messages to the root complex when a system error event occurs. 0 – Do not report nonfatal errors to the root complex. 1 – Report nonfatal errors to the root complex.
0	CERE	rw	Correctable error reporting enable. If this bit is set, the XIO3130 is enabled to send ERR_CORR messages to the root complex when a system error event occurs. 0 – Do not report correctable errors to the root complex. 1 – Report correctable errors to the root complex.

4.2.51 Device Status Register

The Device Status register controls PCI Express device-specific parameters.

PCI register offset: 9Ah

Register type: Read Only; Clear by a Write of One; Hardware Update

Default value: 00X0h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	x	0	0	0	0

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Table 4-27. Bit Descriptions – Device Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:6	RSVD	r	Reserved. When read, these bits return zeros.
5	PEND	ru	Transaction PENDING. This bit is set when the XIO3130 has issued a non-posted transaction that has not been completed yet.
4	APD	ru	AUX power detected. This bit indicates that AUX power is present. This bit is a direct reflection of the AUX_PRSNT bit in the Global Chip Control register and has the same default value. 0 – No AUX power detected. 1 – AUX power detected.
3	URD	rcu	Unsupported request detected. This bit is asserted when a request is received that results in sending a completion with an Unsupported Request status). Errors are logged in this bit regardless of whether error reporting is enabled in the Device Control register.
2	FED	rcu	Fatal error detected. This bit is set by the XIO3130 when a fatal error is detected. Errors are logged in this bit regardless of whether error reporting is enabled in the Device Control register.
1	NFED	rcu	Nonfatal error detected. This bit is set by the XIO3130 when a nonfatal error is detected. Errors are logged in this bit regardless of whether error reporting is enabled in the Device Control register.
0	CED	rcu	Correctable error detected. This bit is set by the XIO3130 when a correctable error is detected. Errors are logged in this bit regardless of whether error reporting is enabled in the Device Control register.

4.2.52 Link Capabilities Register

The Link Capabilities register indicates the link-specific capabilities of the device.

PCI register offset: 9Ch
Register type: Read only
Default value: 000X XX11h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	y	y

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	y	z	z	z	x	1	0	0	0	0	0	1	0	0	0	1

Table 4-28. Bit Descriptions – Link Capabilities Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	PORT_NUM	r	Port number. This field indicates the port number for the PCI Express link. This field is read-only zero.
23:19	RSVD	r	Reserved. When read, these bits return zeros.
18	CLK_PM	r	Clock power management. This field is read-only 1b, which indicates that $\overline{\text{CLKREQ}}$ is supported on the upstream port.
17:15	L1_LATENCY	r	L1 exit latency. This field indicates the time that it takes to transition from the L1 state to the L0 state. This field is a direct reflection of the Upstream Port Link PM Latency register L1_EXIT_LAT field, which is a read/write field that is loaded from EEPROM (if present). The default value of this field, yyy, is the same as the default value of the Link PM Latency register L1_EXIT_LAT field.
14:12	L0S_LATENCY	r	L0s exit latency. This field indicates the time that required to transition from the L0s state to the L0 state. This field is a direct reflection of the Upstream Port Link PM Latency register L0S_EXIT_LAT field, which is a read/write field that is loaded from EEPROM (if present). The default value of this field, zzz, is the same as the default value of the Link PM Latency register L0S_EXIT_LAT field.
11:10	ASLPMS	r	Active state link PM support. This field reads either 01b or 11b, which indicates that the device supports L0s and may or may not support ASPM-based L1 for Active State Link PM. ASPM-based L1 support is controlled by the ASPM_L1_EN field in the Global Chip Control register.

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Table 4-28. Bit Descriptions – Link Capabilities Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
9:4	MLW	r	Maximum link width. This field is encoded 000001b to indicate that the device only supports an x1 PCI Express link.
3:0	MLS	r	Maximum link speed. This field is encoded 0001b to indicate that the device supports a maximum link speed of 2.5 Gb/s.

4.2.53 Link Control Register

The Link Control register is used to control link-specific behavior.

PCI register offset: A0h

Register type: Read/Write; Read Only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-29. Bit Descriptions – Link Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:9	RSVD	r	Reserved. When read, these bits return zeros.
8	CPM_EN	rw	Clock power management enable. When $\overline{\text{CLKREQ}}$ support is enabled, the EP_LI_LAT field in the Upstream Ports Link PM Latency register increases due to link PLL locking requirements. 0 – Disable $\overline{\text{CLKREQ}}$ on upstream port 1 – Enable $\overline{\text{CLKREQ}}$ on upstream port
7	ES	rw	Extended synch. This bit is used to force the device to extend the transmission of FTS ordered sets and an extra TS2 when exiting from L1 before entering to L0. 0 – Normal synch 1 – Extended synch
6	CCC	rw	Common clock configuration. This bit is set when a common clock is provided to both ends of the PCI Express link. This bit can be used to change the L0s and L1 exit latencies. 0 – Reference clock is asynchronous. 1 – Reference clock is synchronous.
5	RL	r	Retrain link. This bit has no function for upstream ports and is read-only zero.
4	LD	r	Link disable. This bit has no function for upstream ports and is read-only zero.
3	RCB	r	Read completion boundary. This bit specifies the minimum size read completion packet that the XIO3130 can send when breaking a read request into multiple completion packets. This field is not applicable to XIO3130 switches; i.e., the XIO3130 does not break up completion packets and is hardwired to zero. 0 – 64 bytes 1 – 128 bytes
2	RSVD	r	Reserved. When read, this bit returns zero.
1:0	ASLPMC	rw	Active state link PM control. This field is used to enable and disable active state PM. 00 – Active state PM disabled 01 – L0s entry enabled 10 – Reserved 11 – L0s and L1 entry enable

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4.2.54 Link Status Register

The Link Status register indicates the current state of the PCI Express Link.

PCI register offset: A2h
Register type: Read only
Default value: 1X11h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	x	0	0	0	0	0	1	0	0	0	1

Table 4-30. Bit Descriptions – Link Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:13	RSVD	r	Reserved. When read, these bits return zeros.
12	SCC	r	Slot clock configuration. This bit reflects the reference clock configurations and is read-only 1, indicating that a 100 MHz common clock reference is used.
11	LT	r	Link training in progress. This bit has no function for upstream ports and is read-only zero.
10	UNDEF	r	Undefined. The value read from this bit is undefined.
9:4	NLW	r	Negotiated link width. This field is read-only 000001b, which indicates that the lane width is x1.
3:0	LS	r	Link speed. This field is read-only 0001b, which indicates that the link speed is 2.5Gb/s.

4.2.55 Serial Bus Data Register

The Serial Bus Data register is used to read and write data on the serial bus interface, e.g., for use with a serial EEPROM. When writing data to the serial bus, this register must be written before writing to the Serial Bus Address register to initiate the cycle. When reading data from the serial bus, this register contains the data read after the REQBUSY (bit 5 Serial Bus Control register) bit is cleared. This register is reset with $\overline{\text{PERST}}$.

PCI register offset: B0h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.2.56 Serial Bus Index Register

The value written to the Serial Bus Index register represents the byte address of the byte being read or written from the serial bus device. The Serial Bus Index register must be written before initiating a serial bus cycle by writing to the Serial Bus Slave Address register. This register is reset with $\overline{\text{PERST}}$.

PCI register offset: B1h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

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4.2.57 Serial Bus Slave Address Register

The Serial Bus Slave Address register is used to indicate the address of the device being targeted by the serial bus cycle. This register also indicates whether the cycle will be a read or a write cycle. Writing to this register initiates the cycle on the serial interface. This register is reset with PERST. The default value corresponds to a serial EEPROM slave address of 7'b101_0000.

PCI register offset: B2h

Register type: Read/Write

Default value: A0h

BIT NUM BER	7	6	5	4	3	2	1	0
RESET STATE	1	0	1	0	0	0	0	0

Table 4-31. Bit Descriptions – Serial Bus Slave Address Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1	SLAVE_ADDR	rw	Serial bus slave address. This bit field represents the slave address for a read/write transaction on the serial interface. This field is reset with PERST.
0	RW_CMD	rw	Read/Write command. This bit is used to determine whether the serial bus cycle is a read or a write cycle. 0 – A single byte write is requested. 1 – A single byte read is requested. This field is reset with PERST.

4.2.58 Serial Bus Control and Status Register

The Serial Bus Control and Status register is used to control the behavior of the serial bus interface. This register also provides status information about the state of the serial bus.

PCI register offset: B3h

Register type: Read/Write; Read Only; Clear by a Write of One; Hardware Update

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-32. Bit Descriptions – Serial Bus Control and Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	PROT_SEL	rw	Protocol select. This bit is used to select the serial bus address mode used. 0 – Slave address and byte address are sent on the serial bus. 1 – Only the slave address is sent on the serial bus. This field is reset with PERST.
6	RSVD	r	Reserved. When read, this bit returns zero.
5	REQBUSY	ru	Requested serial bus access busy. This bit is set when a serial bus cycle is in progress. 0 – No serial bus cycle 1 – Serial bus cycle in progress This field is reset with PERST.

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Table 4-32. Bit Descriptions – Serial Bus Control and Status Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
4	ROMBUSY	ru	Serial EEPROM access busy. This bit is set when the serial EEPROM circuitry in the XIO3130 device is downloading register defaults from a serial EEPROM. 0 – No EEPROM activity 1 – EEPROM download in progress This field is reset with $\overline{\text{PERST}}$.
3	SBDETECT	rwu	Serial EEPROM detected. This bit is automatically set when a serial EEPROM is detected via the strapping option. For more information on strapping options, see section 1.9.1. The value of this bit is used to enable the serial bus interface and to control whether the EEPROM load occurs. Note that a serial EEPROM is only detected once following $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$. 0 – No EEPROM present, EEPROM load process does not occur. 1 – EEPROM present, EEPROM load process occurs. Note that even if a serial EERPOM is not detected following $\overline{\text{PERST}}$, system software can still set this bit to enable the serial bus interface. For more information on system software setting the bit, see section 1.9.4. This field is reset with $\overline{\text{PERST}}$.
2	RSVD	r	Reserved. When read, this bit returns zero.
1	SB_ERR	rc	Serial bus error. This bit is set when an error occurs during a software-initiated serial bus cycle. 0 – No error 1 – Serial bus error This field is reset with $\overline{\text{PERST}}$.
0	ROM_ERR	rc	Serial EEPROM load error. This bit is set when an error occurs while downloading registers from a serial EEPROM. 0 – No error 1 – EEPROM load error This field is reset with $\overline{\text{PERST}}$.

4.2.59 Upstream Port Link PM Latency Register

This read/write register is used to program L0s and L1 exit latencies for the upstream port.

PCI register offset: B4h
Register type: Read/Write; Read Only; Clear by a Write of One; Hardware Update
Default value: 0024h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

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Table 4-33. Bit Descriptions – Upstream Port Link PM Latency Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:14	RSVD	r	Reserved. When read, these bits return zeros.
13:11	EP_L0S_LAT	rw	Endpoint L0s acceptable latency. This field is used to program the maximum acceptable latency when exiting the L0s state. This field is used to set the L0s Acceptable Latency field in the Device Capabilities register. 000 – Less than 64 ns (default) 001 – 64 ns up to less than 128 ns 010 – 128 ns up to less than 256 ns 011 – 256 ns up to less than 512 ns 100 – 512 ns up to less than 1 μs 101 – 1 μs up to less than 2 μs 110 – 2 μs to 4 μs 111 – More than 4 μs This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$.
10:8	EP_L1_LAT	rw	Endpoint L1 acceptable latency. This field is used to program the maximum acceptable latency when exiting the L1 state. This field is used to set the L1 Acceptable Latency field in the Device Capabilities register. 000 – Less than 1 μs (default) 001 – 1 μs up to less than 2 μs 010 – 2 μs up to less than 4 μs 011 – 4 μs up to less than 8 μs 100 – 8 μs up to less than 16 μs 101 – 16 μs up to less than 32 μs 110 – 32 μs to 64 μs 111 – More than 64 μs This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$.
7:6	RSVD	r	Reserved. When read, these bits return zeros.
5:3	L0S_EXIT_LAT	rw	L0s exit latency. This field is used to program the maximum latency for the PHY to exit the L0s state. This field is used to set the L0s Exit Latency field in the Link Capabilities register. 000 – Less than 64 ns 001 – 64 ns up to less than 128 ns 010 – 128 ns up to less than 256 ns 011 – 256 ns up to less than 512 ns 100 – 512 ns up to less than 1 μs (default) 101 – 1 μs up to less than 2 μs 110 – 2 μs to 4 μs 111 – More than 4 μs Define writtenBySW to default to false, be set to true whenever the software or serial EEPROM writes this field to a value that is different from its current state, and can only be subsequently set to false as a result of a reset. When writtenBySW is false, this field is set to 011b when the CCC bit in the Link Control register is asserted (i.e., common clock mode) and set to 100b when the CCC bit is de-asserted (i.e., non-common clock mode). When writtenBySW is true, this field is the value that was last written by the software. This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$. This field may be programmed differently depending on the values programmed in the DEFER_L_EXIT and SMART_L_EXIT fields in the Global Switch Control register.

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Table 4-33. Bit Descriptions – Upstream Port Link PM Latency Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
2:0	L1_EXIT_LAT	rw	L1 exit latency. This field is used to program the maximum latency for the PHY to exit the L1 state. This field is used to set the L1 Exit Latency field in the Link Capabilities register. 000 – Less than 1 μs 001 – 1 μs up to less than 2 μs 010 – 2 μs up to less than 4 μs 011 – 4 μs up to less than 8 μs 100 – 8 μs up to less than 16 μs (default) 101 – 16 μs up to less than 32 μs 110 – 32 μs to 64 μs 111 – More than 64 μs Define writtenBySW to default to false, be set to true when the software or serial EEPROM writes this field to a value that is different from its current state, and can only be subsequently set to false as a result of a reset. When writtenBySW is false, this field is set to 100b. When writtenBySW is true, this field is the value last written by the software. This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$. This field may be programmed differently depending on the values programmed in the DEFER_L_EXIT and SMART_L_EXIT fields in the Global Switch Control register.

4.2.60 Global Chip Control Register

This read/write register is used to control various functionalities across the entire device.

PCI register offset: B8h
Register type: Read/Write; Read Only; Hardware Update; Sticky
Default value: 0000 000Xh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

Table 4-34. Bit Descriptions – Global Chip Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31	RSVD	r	Reserved. When read, this bit returns zero.
30	ASPM_L1_PLL_DIS	rw	ASPM-based L1 PLL disable. This bit enables or disables PLL during ASPM-based L1 for all PHYs on the XIO3130. This setting does not affect D-state-based L1, for which PLLs must be shut off during L1. 0 – Enable PLL during ASPM-based L1. 1 – Disable PLL during ASPM-based L1. This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$.
29	ASPM_L1_EN	rw	ASPM-based L1 enable. This bit enables ASPM-based L1 on the PCI Express chip-level upstream port. This field controls whether the ASPM Support field in the Link Capabilities register reports support for ASPM-based L1 for all functions in a multifunction device. 0 – Disable ASPM based L1. 1 – Enable ASPM based L1. This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$.
28	RSVD	rw	This bit is a reserved diagnostic bit and must be set to 0 for proper operation. If an EEPROM is used, the corresponding bit in the EEPROM must be set to 0.
27:22	RSVD	r	Reserved. When read, these bits return zeros.

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Table 4-34. Bit Descriptions – Global Chip Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
21:20	MIN_POWER_SCALE	rw	Minimum power scale. This value is programmed to indicate the scale of the Minimum Power Value field. 00 – 1.0x 01 – 0.1x 10 – 0.01x 11 – 0.001x This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$.
19:12	MIN_POWER_VALUE	rw	Minimum power value. This value is programmed to indicate the minimum power requirements for all circuitry powered by a slot, and is not applicable for motherboard down applications (i.e., must be programmed to zero in that case). This value is multiplied by the Minimum Power Scale field. When the value is non-zero, the resultant power figure is compared against information conveyed in Set_Slot_Power_Limit Messages received on the upstream port. When the value is zero, the comparison is ignored as if there is no power limit. This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$.
11:10	PWR_OVRD	rw	Power override. This field is used to determine how the device responds when the slot power limit (via Set_Slot_Power_Limit Message received) is greater than the amount of power programmed in the MIN_SLOT_POWER field of this register. This power comparison is disabled when the MIN_SLOT_POWER field of the register is zero. 00 – Ignore slot power limit. 01 – Assert the $\overline{\text{PWR_OVER}}$ pin. 10 – Assert the $\overline{\text{PWR_OVER}}$ pin and respond with Unsupported request to all transactions except configuration transactions (Type 0 or Type 1) and Set_Slot_Power_Limit Messages. 11 – Reserved This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$.
9:3	RSVD	r	Reserved. When read, these bits return zeros.
2	WAKE_OR_BCN	rwh	Wake or beacon. This bit controls whether wake events are signaled using the $\overline{\text{WAKE}}$ pin or a beacon transmission. 0 – Beacon mode. 1 – $\overline{\text{WAKE}}$ mode. This field is reset with $\overline{\text{GRST}}$ and is loaded from EEPROM (when present).
1	WAKE2BCN	rwh	Wake to beacon enable. This bit enables externally generated wake events detected on the $\overline{\text{WAKE}}$ pin to cause a beacon to be transmitted. This field is ignored if WAKE_OR_BCN is set to $\overline{\text{WAKE}}$ mode. 0 – $\overline{\text{WAKE}}$ input to beacon translation disabled. 1 – $\overline{\text{WAKE}}$ input to beacon translation enabled. This field is reset with $\overline{\text{GRST}}$ and is loaded from EEPROM (when present).
0	AUX_PRSNT	ru	AUX power present. This bit reflects the state of a 3.3-VAUX presence detection circuit output in the PCI Express reference macro. This bit controls the AUX Power Detected bit in the Device Status register (i.e., whether AUX power is present) for all ports. 0 – AUX power is not present. 1 – AUX power is present.

4.2.61 GPIO A Control Register

This register is used to control the function of the PCIE_GPIO 0 – 4 pins.

PCI register offset: BCh

Register type: Read/Write; Read Only; Hardware Update; Sticky

Default value: 0000h

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BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-35. Bit Descriptions – GPIO A Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	RSVD	r	Reserved. Reads back zero.
14:12	PCIE_GPIO4_CTL	rw	GPIO 4 Control. This field controls the GPIO4 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 1 ACT_$\overline{\text{BTN0}}$ 011 – Port 3 ACT_$\overline{\text{BTN2}}$ 100 – Port 1 $\overline{\text{PWRFLT0}}$ 101 – Port 3 $\overline{\text{PWRFLT2}}$ 110 – Port 1 EMIL_ENG0 111 – Port 3 EMIL_ENG2 See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If the DN2_DPSTRP terminal is pulled high at the de-assertion of reset, the GPIO4 terminal is directly mapped as the $\overline{\text{PRESENT}}$ PCI Hot Plug terminal for port 3 and is no longer available for use as a GPIO. In this situation these bits have no meaning and should be left at their default value.
11:9	PCIE_GPIO3_CTL	rw	GPIO 3 Control. This field controls the GPIO3 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 1 $\overline{\text{CLKREQ0}}$ 011 – Port 1 MRLS_$\overline{\text{DET0}}$ 100 – Port 2 $\overline{\text{PWRFLT1}}$ 101 – Port 3 $\overline{\text{PWRFLT2}}$ 110 – Port 2 MRLS_$\overline{\text{DET1}}$ 111 – Port 3 MRLS_$\overline{\text{DET2}}$, See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
8:6	PCIE_GPIO2_CTL	rw	GPIO 2 Control. This field controls the GPIO2 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 2 ACT_$\overline{\text{BTN1}}$ 011 – Port 3 ACT_BTN2 100 – Port 2 $\overline{\text{PWRFLT1}}$ 101 – Port 3 $\overline{\text{PWRFLT2}}$ 110 – Port 2 MRLS_$\overline{\text{DET1}}$ 111 – Port 3 MRLS_$\overline{\text{DET2}}$ See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If the DN1_DPSTRP terminal is pulled high at the de-assertion of reset, the GPIO2 terminal is directly mapped as the PWR_GOOD PCI Hot Plug terminal for port 2 and is no longer available for use as a GPIO. In this situation these bits have no meaning and should be left at their default value.

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Table 4-35. Bit Descriptions – GPIO A Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
5:3	PCIE_GPIO1_CTL	rw	GPIO 1 Control. This field controls the GPIO1 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 2 EMIL_CTL1 011 – Port 3 EMIL_CTL2 100 – Port 2 ATN_$\overline{\text{LED1}}$ 101 – Port 3 ATN_$\overline{\text{LED2}}$ 110 – Port 2 PWR_$\overline{\text{LED1}}$ 111 – Port 3 PWR_$\overline{\text{LED2}}$ See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If the DN1_DPSTRP terminal is pulled high at the de-assertion of reset, the GPIO1 terminal is directly mapped as the PWR_$\overline{\text{ON}}$ PCI Hot Plug terminal for port 2 and is no longer available for use as a GPIO. In this situation these bits have no meaning and should be left at their default value.
2:0	PCIE_GPIO0_CTL	rw	GPIO 0 Control. This field controls the GPIO0 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 2 ACT_$\overline{\text{BTN1}}$ 011 – Port 3 ACT_$\overline{\text{BTN2}}$ 100 – Port 2 $\overline{\text{PWRFLT1}}$ 101 – Port 3 $\overline{\text{PWRFLT2}}$ 110 – Port 2 EMIL_ENG1 111 – Port 3 EMIL_ENG2 See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If the DN1_DPSTRP terminal is pulled high at the de-assertion of reset, the GPIO1 terminal is directly mapped as the $\overline{\text{PWR_ON}}$ PCI Hot Plug terminal for port 2 and is no longer available for use as a GPIO. In this situation these bits have no meaning and should be left at their default value.

4.2.62 GPIO B Control Register

This register is used to control the function of the PCIE_GPIO 5 – 9 pins.

PCI register offset: BEh
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-36. Bit Descriptions – GPIO B Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	RSVD	r	Reserved, reads back zero
14:12	PCIE_GPIO9_CTL	rw	GPIO 9 Control. This field controls the GPIO9 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 1 EMIL_CTL0 011 – Port 2 EMIL_CTL2 100 – Port 1 ATN_$\overline{\text{LED0}}$ 101 – Port 2 ATN_$\overline{\text{LED1}}$ 110 – Port 1 PWR_$\overline{\text{LED0}}$ 111 – Port 2 PWR_$\overline{\text{LED1}}$ See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If the DN3_DPSTRP terminal is pulled high at the de-assertion of reset, the GPIO9 terminal is directly mapped as the PWR_$\overline{\text{ON}}$ PCI Hot Plug terminal for port 3 and is no longer available for use as a GPIO. In this situation these bits have no meaning and should be left at their default value.
11:9	PCIE_GPIO8_CTL	rw	GPIO 8 Control. This field controls the GPIO8 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 1 ACT_$\overline{\text{BTN0}}$ 011 – Port 2 ACT_$\overline{\text{BTN1}}$ 100 – Port 1 $\overline{\text{PWRFLT0}}$ 101 – Port 2 $\overline{\text{PWRFLT1}}$ 110 – Port 1 EMIL_ENG0 111 – Port 2 EMIL_ENG1 See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If the DN3_DPSTRP terminal is pulled high at the de-assertion of reset, the GPIO8 terminal is directly mapped as the $\overline{\text{PRESENT}}$ PCI Hot Plug terminal for port 3 and is no longer available for use as a GPIO. In this situation these bits have no meaning and should be left at their default value.
8:6	PCIE_GPIO7_CTL	rw	GPIO 7 Control. This field controls the GPIO7 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 2 $\overline{\text{CLKREQ1}}$ 011 – Port 2 MRLS_$\overline{\text{DET1}}$ 100 – Port 1 $\overline{\text{PWRFLT0}}$ 101 – Port 3 $\overline{\text{PWRFLT2}}$ 110 – Port 1 MRLS_$\overline{\text{DET0}}$ 111 – Port 3 MRLS_$\overline{\text{DET2}}$, See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.

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Table 4-36. Bit Descriptions – GPIO B Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
5:3	PCIE_GPIO6_CTL	rw	GPIO 6 Control. This field controls the GPIO6 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 1 ACT_$\overline{\text{BTN0}}$ 011 – Port 3 ACT_$\overline{\text{BTN2}}$ 100 – Port 1 $\overline{\text{PWRFLT0}}$ 101 – Port 3 $\overline{\text{PWRFLT2}}$ 110 – Port 1 MRLS_$\overline{\text{DET0}}$ 111 – Port 3 MRLS_$\overline{\text{DET2}}$ See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If DPSTRP[1] == 1, this bit field is read only and reads back zero. If the DN2_DPSTRP terminal is pulled high at the de-assertion of reset, the GPIO6 terminal is directly mapped as the PWR_GOOD PCI Hot Plug terminal for port 3 and is no longer available for use as a GPIO. In this situation these bits have no meaning and should be left at their default value.
2:0	PCIE_GPIO5_CTL	rw	GPIO 5 Control. This field controls the GPIO5 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 1 EMIL_CTL0 011 – Port 3 EMIL_CTL2 100 – Port 1 ATN_$\overline{\text{LED0}}$ 101 – Port 3 ATN_$\overline{\text{LED2}}$ 110 – Port 1 PWR_$\overline{\text{LED0}}$ 111 – Port 3 PWR_$\overline{\text{LED2}}$ See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If DPSTRP[1] == 1, this bit field is read only and reads back zero. If the DN2_DPSTRP terminal is pulled high at the de-assertion of reset, the GPIO5 terminal is directly mapped as the PWR_$\overline{\text{ON}}$ PCI Hot Plug terminal for port 3 and is no longer available for use as a GPIO. In this situation these bits have no meaning and should be left at their default value.

4.2.63 GPIO C Control Register

This register is used to control the function of the PCIE_GPIO 10 – 13 pins.

PCI register offset: C0h

Register type: Read/Write; Sticky

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-37. Bit Descriptions – GPIO C Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	RSVD	r	Reserved. Reads back zero.
14:12	PCIE_GPIO14_CTL	rw	GPIO 14 Control. This field controls the GPIO14 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 1 $\overline{\text{ACT_LED0}}$ 011 – Port 2 $\overline{\text{ACT_LED1}}$ 100 – Port 3 $\overline{\text{ACT_LED2}}$ 101 – Port 1 $\overline{\text{PWR_LED0}}$ 110 – Port 2 $\overline{\text{PWR_LED1}}$ 111 – Port 3 $\overline{\text{PWRFLT2}}$ See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
11:9	PCIE_GPIO13_CTL	rw	GPIO 12 Control. This field controls the GPIO12 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 1 $\overline{\text{ACT_LED0}}$ 011 – Port 2 $\overline{\text{ACT_LED1}}$ 100 – Port 3 $\overline{\text{ACT_LED2}}$ 101 – Port 1 $\overline{\text{ATN_LED0}}$ 110 – Port 2 $\overline{\text{PWR_LED1}}$ 111 – Port 3 $\overline{\text{PWR_LED2}}$ See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
8:6	PCIE_GPIO12_CTL	rw	GPIO 12 Control. This field controls the GPIO12 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 1 $\overline{\text{ACT_LED0}}$ 011 – Port 2 $\overline{\text{ACT_LED1}}$ 100 – Port 3 $\overline{\text{ACT_LED2}}$ 101 – Port 1 $\overline{\text{PWR_LED0}}$ 110 – Port 2 $\overline{\text{ATN_LED1}}$ 111 – Port 3 $\overline{\text{ATN_LED2}}$ See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
5:3	PCIE_GPIO11_CTL	rw	GPIO 11 Control. This field controls the GPIO11 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 3 $\overline{\text{CLKREQ2}}$ 011 – Port 3 $\overline{\text{MRLS_DET2}}$ 100 – Port 1 $\overline{\text{PWRFLT0}}$ 101 – Port 2 $\overline{\text{PWRFLT1}}$ 110 – Port 1 $\overline{\text{MRLS_DET0}}$ 111 – Port 2 $\overline{\text{MRLS_DET1}}$, See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.

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Table 4-37. Bit Descriptions – GPIO C Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
2:0	PCIE_GPIO10_CTL	rw	GPIO 10 Control. This field controls the GPIO10 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 1 $\overline{\text{ACT_BTN0}}$ 011 – Port 2 $\overline{\text{ACT_BTN1}}$ 100 – Port 1 $\overline{\text{PWRFLT0}}$ 101 – Port 2 $\overline{\text{PWRFLT1}}$ 110 – Port 1 $\overline{\text{MRLS_DET0}}$ 111 – Port 2 $\overline{\text{MRLS_DET1}}$ See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If the DN3_DPSTRP terminal is pulled high at the de-assertion of reset, the GPIO10 terminal is directly mapped as the PWR_GOOD PCI Hot Plug terminal for port 3 and is no longer available for use as a GPIO. In this situation these bits have no meaning and should be left at their default value.

4.2.64 GPIO D Control Register

This register is used to control the function of the PCIE_GPIO 15–19 pins.

PCI register offset: C2h

Register type: Read/Write; Read Only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-38. Bit Descriptions – GPIO D Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:10	RSVD	r	Reserved. When read, these bits return zeros.
9:8	PCIE_GPIO18_CTL	rw	GPIO 18 Control. This field controls the GPIO18 pin as follows: 00 – General Purpose Input (default) 01 – General Purpose Output 10 – $\overline{\text{HP_INTX}}$, PCI Hot Plug Interrupt Output 11 – $\overline{\text{PD_CHG}}$, Presence Detect Changed Output See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
7:6	PCIE_GPIO17_CTL	rw	GPIO 17 Control. This field controls the GPIO19 pin as follows: 00 – General Purpose Input (default) 01 – General Purpose Output 10 – General Purpose Input 11 – $\overline{\text{PWR_OVER}}$, Power Limits exceeded See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
5:3	PCIE_GPIO16_CTL	rw	GPIO 16 Control. This field controls the GPIO16 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 1 $\overline{\text{ATN_LED0}}$ 011 – Port 2 $\overline{\text{ATN_LED1}}$ 100 – Port 3 $\overline{\text{ATN_LED2}}$ 101 – Port 1 $\overline{\text{PWRFLT0}}$ 110 – Port 2 $\overline{\text{PWRFLT1}}$ 111 – Port 3 $\overline{\text{PWRFLT2}}$ See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
2:0	PCIE_GPIO15_CTL	rw	GPIO 15 Control. This field controls the GPIO15 pin as follows: 000 – General Purpose Input (default) 001 – General Purpose Output 010 – Port 1 $\overline{\text{ATN_LED0}}$ 011 – Port 2 $\overline{\text{ATN_LED1}}$ 100 – Port 3 $\overline{\text{PWR_LED2}}$ 101 – Port 1 $\overline{\text{PWRFLT0}}$ 110 – Port 2 $\overline{\text{PWRFLT1}}$ 111 – Port 3 $\overline{\text{PWRFLT2}}$. See GPIO Data register for a detailed description of this field. This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.

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4.2.65 GPIO Data Register

This register is used to read the state of the GPIO pins and to change the state of GPIO pins that are in output mode. Reads to this register return the state of the GPIO pins, regardless of PCI Hot Plug strapping or GPIO configuration. Writes to this register only affect pins that are configured as a general purpose output.

PCI register offset: C4h

Register type: Read/Write; Read Only

Default value: 00000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-39. Bit Descriptions – GPIO Data Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:19	RSVD	r	
18	PCIE_GPIO18_DATA	rw	GPIO 18 data. $\overline{\text{HP_INTX}}$ / $\overline{\text{PD_CHG}}$ / GPIO 18 data. $\overline{\text{HP_INTX}}$ output mode: Reads indicate current state of pin Writes have no affect $\overline{\text{PD_CHG}}$ output mode: Reads indicate current state of pin Writes have no affect $\overline{\text{PD_CHG}}$ is asserted whenever all of the following are true for any given slot: PDC[n] bit is asserted in the Slot Status register for switch downstream port n, and PDC_EN[n] bit is asserted in Slot Control Register for switch downstream port n GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
17	PCIE_GPIO17_DATA	rw	$\overline{\text{PWR_OVER}}$ / GPIO 17 data. $\overline{\text{PWR_OVER}}$ mode: reads state of pin; writes have no affect $\overline{\text{PWR_OVER}}$ pin is asserted whenever any of the following conditions are true: $\overline{\text{PERST}}$ is asserted Conditions are met for exceeding slot power limit (see PWR_OVRD field in Global Chip Control Register) GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
16	PCIE_GPIO16_DATA	rw	GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
15	PCIE_GPIO15_DATA	rw	GPIO 15 data. GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.

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Table 4-39. Bit Descriptions – GPIO Data Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
14	PCIE_GPIO14_DATA	rw	GPIO 14 data. GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin This field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
13	PCIE_GPIO13_DATA	rw	GPIO 13 data. LED driver (see GPIO C Controls) GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin This bit field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
12	PCIE_GPIO12_DATA	rw	GPIO 12 data. LED driver (see GPIO C Controls) GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin This bit field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
11	PCIE_GPIO11_DATA	rw	GPIO 11 data. GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin Program-selectable HP input or output pin This bit field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
10	PCIE_GPIO10_DATA	rw	GPIO 10 data. GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin Program-selectable HP input pin This field is valid only if DN3_DPSTRP == 0. If this bit field is valid then it is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If this field is invalid, it is a read-only bit field.
9	PCIE_GPIO9_DATA	rw	GPIO 9 data. GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin Program-selectable HP input pin This field is valid only if DN3_DPSTRP == 0. If this bit field is valid then it is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If this field is invalid, it is a read-only bit field.
8	PCIE_GPIO8_DATA	rw	GPIO 8 data. GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin Program-selectable HP output pin This field is valid only if DN3_DPSTRP == 0. If this bit field is valid then it is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If this field is invalid, it is a read-only bit field.
7	PCIE_GPIO7_DATA	rw	GPIO 7 data. GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin GP Output mode: reads and also controls state of pin This bit field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.

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Table 4-39. Bit Descriptions – GPIO Data Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
6	PCIE_GPIO6_DATA	rw	GPIO 6 data. GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin Program-selectable HP input pin This field is valid only if DN2_DPSTRP == 0. If this bit field is valid then it is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If this field is invalid, it is a read-only bit field.
5	PCIE_GPIO5_DATA	rw	GPIO 5 data. GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin Program-selectable HP input pin This field is valid only if DN2_DPSTRP == 0. If this bit field is valid then it is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If this field is invalid, it is a read-only bit field.
4	PCIE_GPIO4_DATA	rw	GPIO 4 data. GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin Program-selectable HP output pin This field is valid only if DN2_DPSTRP == 0. If this bit field is valid then it is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If this field is invalid, it is a read-only bit field.
3	PCIE_GPIO3_DATA	rw	GPIO 3 data. GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin Program-selectable HP Input or Output pin This bit field is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$.
2	PCIE_GPIO2_DATA	rw	GPIO 2 data. GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin Program-selectable HP input pin This field is valid only if DN1_DPSTRP == 0. If this bit field is valid then it is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If this field is invalid, it is a read-only bit field.
1	PCIE_GPIO1_DATA	rw	GPIO 1 data. GP Input mode: reads state of pin; writes have no affect GP Output mode: reads and also controls state of pin Program-selectable HP input pin This field is valid only if DN1_DPSTRP == 0. If this bit field is valid then it is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If this field is invalid, it is a read-only bit field.
0	PCIE_GPIO0_DATA	rw	GPIO 0 data. GP Input mode: reads state of pin; writes have no effect GP Output mode: reads and also controls state of pin Program-selectable HP output pin This field is valid only if DN1_DPSTRP == 0. If this bit field is valid then it is loaded from EEPROM (if present), and reset with $\overline{\text{FRST}}$. If this field is invalid, it is a read-only bit field.

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4.2.66 TI Proprietary Register

This read/write TI proprietary register is located at offset C8h and controls TI proprietary functions. This register must not be changed from the specified default state. If the default value is changed in error, a PCI Express Reset (PERST) returns this register to a default state.

If an EEPROM is used to load configuration registers, the value loaded for this register must be 00000001h.

PCI register offset: C8h

Register type: Read/Write

Default value: xxxx 0001h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

4.2.67 TI Proprietary Register

This read/write TI proprietary register is located at offset CCh and controls TI proprietary functions. This register must not be changed from the specified default state. If the default value is changed in error, a PCI Express Reset (PERST) returns this register to a default state.

If an EEPROM is used to load configuration registers, the value loaded for this register must be 00000000h.

PCI register offset: CCh

Register type: Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.2.68 TI Proprietary Register

This read/write TI proprietary register is located at offset D0h and controls TI proprietary functions. This register must not be changed from the specified default state. If the default value is changed in error, a PCI Express Reset (PERST) returns this register to a default state.

If an EEPROM is used to load configuration registers, the value loaded for this register must be 32140000h.

PCI register offset: D0h

Register type: Read/Write

Default value: 3214 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	1	1	0	0	1	0	0	0	0	1	0	1	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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4.2.69 TI Proprietary Register

This read/write TI proprietary register is located at offset D4h and controls TI proprietary functions. This register must not be changed from the specified default state. If the default value is changed in error, a PCI Express Reset (PERST) returns this register to a default state.

If an EEPROM is used to load configuration registers, the value loaded for register D5h must be 10h.

PCI register offset: D4h

Register type: Read/Write

Default value: 0000 0010

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

4.2.70 TI Proprietary Register

This read/write TI proprietary register is located at offset D8h and controls TI proprietary functions. This register must not be changed from the specified default state. If the default value is changed in error, a PCI Express Reset (PERST) returns this register to a default state.

PCI register offset: D8h

Register type: Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.2.71 TI Proprietary Register

This read/write TI proprietary register is located at offset DCh and controls TI proprietary functions. This register must not be changed from the specified default state. If the default value is changed in error, a PCI Express Reset (PERST) returns this register to a default state.

PCI register offset: DCh

Register type: Read/Write

Default value: 0000 0002h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

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4.2.72 Subsystem Access Register

This register is a read/write register. The contents of this register are aliased to the Subsystem Vendor ID and Subsystem ID registers at PCI Offsets 84h and 86h for all PCI Express ports.

PCI register offset: E0h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-40. Bit Descriptions – Subsystem Access Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:16	SubsystemID	rw	Subsystem ID. The value written to this field is aliased to the Subsystem ID register at PCI Offset 66h. This field is loaded from EEPROM (when present) and reset with PERST.
15:0	SubsystemVendorID	rw	Subsystem Vendor ID. The value written to this field is aliased to the Subsystem Vendor ID register at PCI Offset 64h. This field is loaded from EEPROM (when present) and reset with PERST.

4.2.73 General Control Register

This register is a read/write register that is used to control various functions of the XIO3130.

PCI register offset: E4h
Register type: Read/Write; Read Only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-41. Bit Descriptions – General Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:3	RSVD	r	Reserved. When read, these bits return zeros.
2	TI_PROPRIETARY	rw	TI proprietary. This bit must not be changed from the specified default value.
1	L1_DISABLE	rw	L1 disable. This bit may be used to disable software-directed L1 entry when in lower D-states (D1-D3). The value of L1_DISABLE is 0 (the default). Link power states are managed in accordance with the PCI Express base specification. When L1_DISABLE is 1, the upstream port of the XIO3130 does not enter L1 even when directed to do so through software.
0	RSVD	r	Reserved. When read, this bit returns zero.

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4.2.74 Downstream Ports Link PM Latency Register

This read/write register is used to program L0s and L1 exit latencies for all XIO3130 downstream ports. Similar information is provided in a separate register for the upstream port.

PCI register offset: E8h

Register type: Read/Write; Read Only

Default value: 3F24h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-42. Bit Descriptions – Downstream Ports Link PM Latency Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:14	RSVD	r	Reserved. When read, these bits return zeros.
13:11	EP_L0S_LAT	rw	Endpoint L0s acceptable latency. This field is used to program the maximum acceptable latency when exiting the L0s state. This field is used to set the L0s Acceptable Latency field in the Device Capabilities register. 000 – Less than 64 ns 001 – 64 ns up to less than 128 ns 010 – 128 ns up to less than 256 ns 011 – 256 ns up to less than 512 ns 100 – 512 ns up to less than 1 μs 101 – 1 μs up to less than 2 μs 110 – 2 μs to 4 μs 111 – More than 4 μs (default) This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$.
10:8	EP_L1_LAT	rw	Endpoint L1 acceptable latency. This field is used to program the maximum acceptable latency when exiting the L1 state. This field is used to set the L1 Acceptable Latency field in the Device Capabilities register. 000 – Less than 1 μs 001 – 1 μs up to less than 2 μs 010 – 2 μs up to less than 4 μs 011 – 4 μs up to less than 8 μs 100 – 8 μs up to less than 16 μs 101 – 16 μs up to less than 32 μs 110 – 32 μs to 64 μs 111 – More than 64 μs (default) This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$.
7:6	RSVD	r	Reserved. When read, these bits return zeros.
5:3	L0S_EXIT_LAT	rw	L0s exit latency. This field is used to program the maximum latency for the PHY to exit the L0s state. This is used to set the L0s Exit Latency field in the Link Capabilities register. 000 – Less than 64 ns 001 – 64 ns up to less than 128 ns 010 – 128 ns up to less than 256 ns 011 – 256 ns up to less than 512 ns 100 – 512 ns up to less than 1 μs (default) 101 – 1 μs up to less than 2 μs 110 – 2 μs to 4 μs 111 – More than 4 μs

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Table 4-42. Bit Descriptions – Downstream Ports Link PM Latency Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
2:0	L1_EXIT_LAT	rw	L1 exit latency. This field is used to program the maximum latency for the PHY to exit the L1 state. This is used to set the L1 Exit Latency field in the Link Capabilities register. 000 – Less than 1 μs 001 – 1 μs up to less than 2 μs 010 – 2 μs up to less than 4 μs 011 – 4 μs up to less than 8 μs 100 – 8 μs up to less than 16 μs (default) 101 – 16 μs up to less than 32 μs 110 – 32 μs to 64 μs 111 – More than 64 μs

4.2.75 Global Switch Control Register

This read/write register is used to control various functions across the entire XIO3130.

PCI register offset: EAh

Register type: Read/Write; Read Only; Clear by a Write of One; Sticky

Default value: 0004h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-43. Bit Descriptions – Global Switch Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:7	RSVD	r	Reserved. When read, these bits return zeros.
6	DP_L0S_IND	rw	Downstream ports L0s independence 0 – Downstream ports (all) Tx L0s entry dependent on whether upstream Rx is in L0s according to *PCI Express Base Specification*, section 5.4.1.1.1. 1 – Downstream ports Tx L0s entry not dependent on whether upstream Rx is in L0s.
5	RSVD	r	Reserved. When read, this bit returns zero.
4	DEFER_L_EXIT	rw	Defer L0s, L1 exit. This bit configures logic to not automatically power up all downstream ports when the upstream port receives a downstream flowing packet. This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$.
3	RSVD	r	Reserved. When read, this bit returns zero.
2	D1_SUPPORT	rw	D1 support. This bit enables whether all PCI Express XIO3130 functions are capable of D1 support. The field controls (1) the D1_SUPPORT bit in the Power Management Capabilities register for all XIO3130 ports, and (2) bit 1 in the 5-bit PME_SUPPORT field in the Power Management Capabilities register for all XIO3130 ports. 0 – D1 not supported 1 – D1 supported This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$.
1	HP_PME_MSG_EN	rw	PCI Hot Plug PME message enable. This bit enables PME_Turn_Off/PME_TO_Ack messages when power is shut off to a slot using the PC_CTL bit in the Slot Control register for downstream ports. 0 – Disable PME_Turn_Off / PME_TO_Ack messages for slot power control 1 – Enable PME_Turn_Off / PME_TO_Ack messages for slot power control This field is loaded from EEPROM (when present) and reset with $\overline{\text{PERST}}$.

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Table 4-43. Bit Descriptions – Global Switch Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
0	BCN_DET_DIS	rwh	Beacon detect disable. This bit disables beacon detection on all downstream ports and allows the reference macro to be placed in low power state during D3cold. 0 – Beacon detection enabled 1 – Beacon detection disabled This field is loaded from EEPROM (when present) and reset with $\overline{\text{GRST}}$.

4.2.76 Advanced Error Reporting Capability ID Register

This read-only register identifies the linked list item as the register for PCI Express Advanced Error Reporting Capabilities. The register returns 0001h when read.

PCI register offset: 100h

Register type: Read only

Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

4.2.77 Next Capability Offset/Capability Version Register

This read-only register returns the value 0000h to indicate that this extended capability block represents the end of the linked list of extended capability structures. The least significant four bits identify the revision of the current capability block as 1h.

PCI register offset: 102h

Register type: Read only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.2.78 Uncorrectable Error Status Register

This register reports the status of individual errors as they occur. Software may clear these bits only by writing a 1 to the desired location.

PCI register offset: 104h

Register type: Read Only, Cleared by a Write of one

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-44. Uncorrectable Error Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	r	Reserved. Return zeros when read.
20	UR_ERROR	rcuh	Unsupported Request error. This bit is asserted when an Unsupported Request error is detected (i.e., when a request is received that results in the sending of a completion with an Unsupported Request status).
19	ECRC_ERROR	rcuh	Extended CRC error. This bit is asserted when an Extended CRC error is detected.
18	MAL_TLP	rcuh	Malformed TLP. This bit is asserted when a malformed TLP is detected.
17	RX_OVERFLOW	rcuh	Receiver overflow. This bit is asserted when the flow control logic detects that the transmitting device has illegally exceeded the number of credits that were issued.
16	UNXP_CPL	rcuh	Unexpected completion. This bit is asserted when a completion packet is received that does not correspond to an issued request.
15	CPL_ABORT	rcuh	Completer abort. This bit is asserted when the completion to a pending request arrives with Completer Abort status.
14	CPL_TIMEOUT	rcuh	Completion timeout. This bit is asserted when no completion has been received for an issued request before the timeout period.
13	FC_ERROR	rcuh	Flow control error. This bit is asserted when a flow control protocol error is detected either during initialization or during normal operation.
12	PSN_TLP	rcuh	Poisoned TLP. This bit is asserted when an outgoing packet (request or completion) has been poisoned by setting the poison bit and has inverted the extended CRC attached to the end of the packet.
11:6	RSVD	r	Reserved. Return zeros when read.
5	SD_ERROR	rcuh	Surprise down error. See Surprise Down ECN for a description of this error condition.
4	DLL_ERROR	rcuh	Data link protocol error. This bit is asserted if a data link layer protocol error is detected.
3:1	RSVD	r	Reserved. Return zeros when read.
0	Undefined	r	The value read from this bit is undefined.

4.2.79 Uncorrectable Error Mask Register

The Uncorrectable Error Mask register controls the reporting of individual errors as they occur. When a bit is set to one, the error status bits are still affected, but the error is not logged and no error reporting message is sent upstream.

PCI register offset: 108h
Register type: Read Only, Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-45. Uncorrectable Error Mask Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	r	Reserved. Return zeros when read.
20	UR_ERROR_MASK	rwh	Unsupported Request error mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
19	ECRC_ERROR_MASK	rwh	Extended CRC error mask. 0 - Error condition is unmasked. 1 - Error condition is masked.

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Table 4-45. Uncorrectable Error Mask Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
18	MAL_TLP_MASK	rwh	Malformed TLP mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
17	RX_OVERFLOW_MASK	rwh	Receiver Overflow mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
16	UNXP_CPL_MASK	rwh	Unexpected Completion mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
15	CPL_ABORT_MASK	rwh	Completer Abort mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
14	CPL_TIMEOUT_MASK	rwh	Completion Timeout mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
13	FC_ERROR_MASK	rwh	Flow Control error mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
12	PSN_TLP_MASK	rwh	Poisoned TLP mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
11:6	RSVD	r	Reserved. Return zeros when read.
5	SD_MASK	rwh	Surprise Down error mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
4	DLL_ERROR_MASK	rwh	Data Link Protocol error mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
3:1	RSVD	r	Reserved. Return zeros when read.
0	Undefined	r	The value read from this bit is undefined.

4.2.80 Uncorrectable Error Severity Register

The Uncorrectable Error Severity register controls the reporting of individual errors as ERR_FATAL or ERR_NONFATAL. When a bit is set, the corresponding error condition is identified as fatal. When a bit is clear, the corresponding error condition is identified as nonfatal.

PCI register offset: 10Ch

Register type: Read Only, Read/Write

Default value: 0003 2030h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0

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Table 4-46. Uncorrectable Error Severity Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	r	Reserved. Return zeros when read.
20	UR_ERROR_SEVR	rwh	Unsupported Request error severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
19	ECRC_ERROR_SEVR	rwh	Extended CRC error severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
18	MAL_TLP_SEVR	rwh	Malformed TLP severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
17	RX_OVERFLOW_SEVR	rwh	Receiver Overflow severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
16	UNXP_CPL_SEVR	rwh	Unexpected Completion severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
15	CPL_ABORT_SEVR	rwh	Completer Abort severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
14	CPL_TIMEOUT_SEVR	rwh	Completion Timeout severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
13	FC_ERROR_SEVR	rwh	Flow Control error severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
12	PSN_TLP_SEVR	rwh	Poisoned TLP severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
11:6	RSVD	r	Reserved. Return zeros when read.
5	SD_ERROR_SEVR	rwh	Surprise Down error severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
4	DLL_ERROR_SEVR	rwh	Data Link Protocol error severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
3:1	RSVD	r	Reserved. Return zeros when read.
0	Undefined	r	The value read from this bit is undefined.

4.2.81 Correctable Error Status Register

The Correctable Error Status register reports the status of individual errors as they occur. Software may clear these bits only by writing a 1 to the desired location.

PCI register offset: 110h
Register type: Read Only, Cleared by a Write of one
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-47. Correctable Error Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	r	Reserved. Return zeroes when read.
13	ANFES	rcuh	Advisory nonfatal error status.
12	REPLAY_TMOUT	rcuh	Replay timer timeout. This bit is asserted when the replay timer expires for a pending request or completion that has not been acknowledged.
11:9	RSVD	r	Reserved. Return zeroes when read.
8	REPLAY_ROLL	rcuh	REPLAY_NUM rollover. This bit is asserted when the replay counter rolls over when a pending request of completion has not been acknowledged.
7	BAD_DLLP	rcuh	Bad DLLP error. This bit is asserted when an 8b/10n error is detected by the PHY during reception of a DLLP.
6	BAD_TLP	rcuh	Bad TLP error. This bit is asserted when an 8b/10b error is detected by the PHY during reception of a TLP.
5:1	RSVD	r	Reserved. Return zeros when read.
0	RX_ERROR	rcuh	Receiver error. This bit is asserted when an 8b/10b error is detected by the PHY at any time.

4.2.82 Correctable Error Mask Register

The Correctable Error Mask register controls the reporting of individual errors as they occur. When a bit is set to one, error status bits are still affected, but the error is not logged and no error reporting message is sent upstream.

PCI register offset: 114h

Register type: Read Only, Read/Write

Default value: 0000 2000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-48. Correctable Error Mask Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	r	Reserved. Return zeros when read.
13	ANFEM	rwh	Advisory nonfatal error mask. This bit is set by default to enable compatibility with software that does not comprehend role-based error reporting. 0 – Error condition is unmasked 1 – Error condition is masked
12	REPLAY_TMOUT_MASK	rwh	Replay timer timeout mask. 0 – Error condition is unmasked 1 – Error condition is masked
11:9	RSVD	r	Reserved. Return zeros when read.

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Table 4-48. Correctable Error Mask Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
8	REPLAY_ROLL_MASK	rwh	REPLAY_NUM rollover mask. 0 – Error condition is unmasked 1 – Error condition is masked
7	BAD_DLLP_MASK	rwh	Bad DLLP error mask. 0 – Error condition is unmasked 1 – Error condition is masked
6	BAD_TLP_MASK	rwh	Bad TLP error mask. 0 – Error condition is unmasked 1 – Error condition is masked
5:1	RSVD	r	Reserved. Return zeros when read.
0	RX_ERROR_MASK	rwh	Receiver error mask. 0 – Error condition is unmasked 1 – Error condition is masked

4.2.83 Advanced Error Capabilities and Control Register

The Advanced Error Capabilities and Control register allows the system to monitor and control the advanced error reporting capabilities.

PCI register offset: 118h
Register type: Read Only, Read/Write
Default value: 0000 00A0h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Table 4-49. Advanced Error Capabilities and Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:9	RSVD	r	Reserved. Return zeros when read.
8	ECRC_CHK_EN	rwh	Extended CRC check enable. 0 – Extended CRC checking is disabled 1 – Extended CRC checking is enabled
7	ECRC_CHK_CAPABLE	r	Extended CRC check capable. This read-only bit returns a value of ‘1’ indicating that the bridge is capable of checking extended CRC information.
6	ECRC_GEN_EN	rwh	Extended CRC generation enable. 0 – Extended CRC generation is disabled 1 – Extended CRC generation is enabled
5	ECRC_GEN_CAPABLE	r	Extended CRC generation capable. This read-only bit returns a value of ‘1’ indicating that the bridge is capable of generating extended CRC information.
4:0	FIRST_ERR	rh	First error pointer. This five-bit value reflects the bit position within the Uncorrectable Error Status register corresponding to the class of the first error condition that was detected.

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4.2.84 Header Log Register

The Header Log register stores the TLP header for the packet that lead to the most recently detected error condition. Offset 11Ch contains the first DWORD. Offset 128h contains the last DWORD (in the case of a 4DW TLP header).

PCI register offset: 11Ch – 128h

Register type: Read only

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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4.3 PCI Express Downstream Port Registers

The default reset domain for all downstream port registers is SBRST. Some register fields are placed in a different reset domain from the default reset domain; all bit and field descriptions identify any unique reset domains. Generally, all sticky bits are placed in the GRST domain and all (non-sticky) EEPROM loadable bits are placed in the PERST domain.

4.3.1 PCI Configuration Space (Downstream Port) Register Map

Table 4-50. PCI Express Downstream Port Configuration Register Map (Type 1)

Register Name				Offset
Device ID		Vendor ID		000h
Status		Command		004h
Class Code			Revision ID	008h
BIST	Header Type	Latency Timer	Cache Line Size	00Ch
Reserved				010h-014h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	018h
Secondary Status		I/O Limit	I/O Base	01Ch
Memory Limit		Memory Base		020h
Pre-fetchable Memory Limit		Pre-fetchable Memory Base		024h
Pre-fetchable Base Upper 32 Bits				028h
Pre-fetchable Limit Upper 32 Bits				02Ch
I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		030h
Reserved			Capabilities Pointer	034h
Reserved				038h
Bridge Control		Interrupt Pin	Interrupt Line	03Ch
Reserved				040h-04Ch
Power Management Capabilities		Next-item Pointer	PM CAP ID	050h
PM Data (RSVD)	PMCSR_BSE	Power Management CSR		054h
Reserved				058h-06Ch
MSI Message Control		Next-item Pointer	MSI CAP ID	070h
MSI Message Address				074h
MSI Upper Message Address				078h
Reserved		MSI Message Data		07Ch
Reserved		Next-item Pointer	SSID/SSVID CAP ID	080h
Subsystem ID		Subsystem Vendor ID		084h
Reserved				088h-08Ch
PCI Express Capabilities Register		Next-item Pointer	PCI Express Capability ID	090h
Device Capabilities				094h
Device Status		Device Control		098h
Link Capabilities				09Ch
Link Status		Link Control		0A0h
Slot Capabilities				A4h
Slot Status		Slot Control		A8h
Reserved				0ACh-0C4h
TI Proprietary				0C8h-0D0h
General Control				0D4h
Reserved				0D8h-0E8h
General Slot Info		Reserved	LOs Idle Timeout	0ECh
Reserved				0F0h-0FCh

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Table 4-51. Extended Configuration Space (Downstream Port)

Register Name		Offset
Next Capability Offset / Capability Version	PCI Express Advanced Error Reporting Capabilities ID	100h
Uncorrectable Error Status Register		104h
Uncorrectable Error Mask Register		108h
Uncorrectable Error Severity Register		10Ch
Correctable Error Status Register		110h
Correctable Error Mask		114h
Advanced Error Capabilities and Control		118h
Header Log Register		11Ch
Header Log Register		120h
Header Log Register		124h
Header Log Register		128h
Reserved		12Ch-FFCh

4.3.2 Vendor ID Register

This 16-bit read-only register contains the value 104Ch, which is the vendor ID assigned to Texas Instruments.

PCI register offset: 00h

Register type: Read only

Default value: 104Ch

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

4.3.3 Device ID Register

This 16-bit read-only register contains the device ID assigned by TI to the XIO3130. The value in this register is the same for all downstream ports, as defined in the following table.

PCI register offset: 02h

Register type: Read only

Default value: 8233h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	1	0	0	0	1	1	0	0	1	1

4.3.4 Command Register

The Command register controls the way the downstream port bridge behaves on its primary interface; i.e., the internal PCI bus between the upstream and downstream ports.

PCI register offset: 04h

Register type: Read/Write; Read Only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-52. Bit Descriptions – Command Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:11	RSVD	r	Reserved. When read, these bits return zeros.
10	INT_DISABLE	rw	$\overline{\text{INTx}}$ disable. This bit is used to enable device-specific INTx interrupts. The XIO3130 downstream ports can generate INTx interrupts due to PCI Hot Plug events. The XIO3130 forwards INTx messages from downstream ports to the upstream port (see INTx Support section) regardless of this bit.
9	FBB_ENB	r	Fast back-to-back enable. This bit does not apply to PCI-Express, so it returns zero when read.
8	SERR_ENB	rw	$\overline{\text{SERR}}$ enable. The relevant error checking is unnecessary for the XIO3130 internal PCI bus. When set, this bit enables the transmission by the primary interface of ERR_NONFATAL and ERR_FATAL messages forwarded from the secondary interface. This bit does not affect transmission of ERR_COR messages.
7	STEP_ENB	r	Address/data stepping control. This bit does not apply to PCI-Express and is hardwired to 0.
6	PERR_ENB	rw	Parity error response enable. This bit has no impact on hardware behavior. It is assumed that the relevant error checking is unnecessary for the XIO3130 internal PCI bus.
5	VGA_ENB	r	VGA palette snoop enable. The XIO3130 does not support VGA palette snooping, so this bit returns zero when read.
4	MWI_ENB	r	Memory write and invalidate enable. This bit does not apply to PCI-Express, so it is hardwired to zero.
3	SPECIAL	r	Special cycle enable. This bit does not apply to PCI-Express and is hardwired to zero.
2	MASTER_ENB	rw	Bus master enable. When set, the XIO3130 is enabled to initiate cycles on the downstream PCI Express interface. 0 – Downstream PCI Express interface cannot initiate transactions. The XIO3130 must disable response to memory and I/O transactions on the downstream interface. 1 – Downstream PCI Express interface can initiate transactions. The bridge can forward memory and I/O transactions.
1	MEMORY_ENB	rw	Memory response enable. Setting this bit enables the downstream port to respond to memory transactions.
0	IO_ENB	rw	I/O space enable. Setting this bit enables the downstream port to respond to I/O transactions.

4.3.5 Status Register

The Status register provides information about the downstream port's primary interface, i.e., the internal PCI bus between the upstream and downstream ports.

PCI register offset: 06h

Register type: Read Only; Clear by a Write of One; Hardware Update

Default value: 0010h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-53. Bit Descriptions – Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PAR_ERR	rcu	Detected parity error. This bit is set when the virtual internal PCI interface receives a poisoned TLP. This bit is set regardless of the state of the Parity Error Response bit in the Command register. 0 – No parity error detected. 1 – Parity error detected.
14	SYS_ERR	rcu	Signaled system error. This bit is set when the XIO3130 sends an ERR_FATAL or ERR_NONFATAL message upstream and the SERR Enable bit in the Command register is set. 0 – No error signaled. 1 – ERR_FATAL or ERR_NONFATAL signaled.

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Table 4-53. Bit Descriptions – Status Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
13	MABORT	r	Received master abort. This bit is hardwired to zero. It is assumed that the relevant error checking is unnecessary for the XIO3130 internal PCI bus.
12	TABORT_REC	r	Received target abort. This bit is hardwired to zero. It is assumed that the relevant error checking is unnecessary for the XIO3130 internal PCI bus.
11	TABORT_SIG	r	Signaled target abort. This bit is hardwired to zero. It is assumed that the relevant error checking is unnecessary for the XIO3130 internal PCI bus.
10:9	PCI_SPEED	r	DEVSEL timing. These bits are read only zero because they do not apply to PCI Express.
8	DATAPAR	rcu	Master data parity error. This bit is set when the downstream port receives a poisoned completion or poisons a write request on the internal virtual PCI bus. This bit is never set if the parity error response enable bit in the Command register is clear.
7	FBB_CAP	r	Fast back-to-back capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to zero.
6	RSVD	r	Reserved. When read, this bit returns zero.
5	66MHZ	r	66-MHz capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to zero.
4	CAPLIST	r	Capabilities list. This bit returns 1 when read, indicating that the XIO3130 supports additional PCI capabilities.
3	INT_STATUS	r	Interrupt status. This bit reflects the INTx interrupt status of the function. The XIO3130 forwards INTx messages from downstream ports to the upstream port.
2:0	RSVD	r	Reserved. When read, these bits return zeros.

4.3.6 Class Code and Revision ID Register

This read-only register categorizes the Base Class, Sub Class, and Programming Interface of the XIO3130. The Base Class is 06h, which identifies the device as a bridge device. The Sub Class is 04h, which identifies the function as a PCI-to-PCI bridge. The Programming Interface is 00h. In addition, the TI chip revision is indicated in the lower byte (01h).

PCI register offset: 08h

Register type: Read only

Default value: 0604 0001h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4-54. Bit Descriptions – Class Code and Revision ID Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	BASECLASS	r	Base class. This field returns 06h when read, which classifies the function as a bridge device.
23:16	SUBCLASS	r	Subclass. This field returns 04h when read, which specifically classifies the function as a PCI-to-PCI bridge.
15:8	PGMIF	r	Programming interface. This field returns 00h when read.
7:0	CHIPREV	r	Silicon revision. This field returns the silicon revision.

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4.3.7 Cache Line Size Register

The Cache Line Size register is implemented by PCI Express devices as a read-write field for legacy compatibility, but has no impact on any PCI Express device functionality.

PCI register offset: 0Ch
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.3.8 Primary Latency Timer Register

This read-only register has no meaningful context for a PCI Express device, so it returns zeros when read.

PCI register offset: 0Dh
Register type: Read only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.3.9 Header Type Register

This read-only register indicates that this function has a Type 1 PCI header. Bit seven of this register is zero, indicating that the XIO3130 downstream port PCI-to-PCI bridge is not a multifunction device.

PCI register offset: 0Eh
Register type: Read only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

4.3.10 BIST Register

Since the XIO3130 does not support a built-in self test (BIST), this read-only register returns the value 00h when read.

PCI register offset: 0Fh
Register type: Read only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

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4.3.11 Primary Bus Number

This register specifies the bus number of the PCI bus segment for the downstream port primary interface (i.e., the internal PCI bus).

PCI register offset: 18h

Register type: Read/Write

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.3.12 Secondary Bus Number

This register specifies the bus number of the PCI bus segment for the downstream port secondary interface (i.e., the PCI Express interface). The XIO3130 uses this register to determine how to respond to a Type 1 configuration transaction.

PCI register offset: 19h

Register type: Read/Write

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.3.13 Subordinate Bus Number

This register specifies the bus number of the highest number PCI bus segment that is downstream of the XIO3130 downstream port. The XIO3130 uses this register to determine how to respond to a Type 1 configuration transaction.

PCI register offset: 1Ah

Register type: Read/Write

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.3.14 Secondary Latency Timer Register

This register does not apply to PCI-Express, so it is hardwired to zero.

PCI register offset: 1Bh

Register type: Read only

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

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4.3.15 I/O Base Register

This read/write register specifies the lower limit of the I/O addresses that the XIO3130 downstream port forwards downstream.

PCI register offset: 1Ch
Register type: Read/Write; Read Only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

Table 4-55. Bit Descriptions – I/O Base Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	IOBASE	rw	I/O base. This field defines the bottom address of the I/O address range that is used to determine when to forward I/O transactions from one interface to the other. These bits correspond to address bits [15:12] in the I/O address. The lower 12 bits are assumed to be 0. The 16 bits that correspond to address bits [31:16] of the I/O address are defined in the I/O Base Upper 16 Bits register.
3:0	IOTYPE	r	I/O type. This field is read-only 01h, which indicates 32 bit I/O addressing support.

4.3.16 I/O Limit Register

This read/write register specifies the upper limit of the I/O addresses that the XIO3130 downstream port forwards downstream.

PCI register offset: 1Dh
Register type: Read/Write; Read Only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

Table 4-56. Bit Descriptions – I/O Limit Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	IOLIMIT	rw	I/O limit. This field defines the top address of the I/O address range that is used to determine when to forward I/O transactions from one interface to the other. These bits correspond to address bits [15:12] in the I/O address. The lower 12 bits are assumed to be FFFh. The 16 bits that correspond to address bits [31:16] of the I/O address are defined in the I/O Limit Upper 16 Bits register.
3:0	IOTYPE	r	I/O type. This field is read-only 01h, which indicates 32-bit I/O addressing support.

4.3.17 Secondary Status Register

The Secondary Status register provides information about the downstream port PCI Express interface.

PCI register offset: 1Eh
Register type: Read Only; Clear by a Write of One; Hardware Update
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-57. Bit Descriptions – Secondary Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PAR_ERR	rcu	Detected parity error. This bit is set when the PCI Express interface receives a poisoned TLP on the downstream port. This bit is set regardless of the state of the Parity Error Response bit in the Bridge Control register. 0 – No parity error detected. 1 – Parity error detected.
14	SYS_ERR	rcu	Received System Error. This bit is set when the XIO3130 sends an ERR_FATAL or ERR_NONFATAL message upstream and the SERR Enable bit in the Command register is set. 0 – No error signaled. 1 – ERR_FATAL or ERR_NONFATAL signaled.
13	MABORT	rcu	Received master abort. This bit is set when the downstream PCI Express interface of the XIO3130 receives a completion with Unsupported Request Status. 0 – Unsupported Request not received. 1 – Unsupported Request received on.
12	TABORT_REC	rcu	Received target abort. This bit is set when the downstream PCI Express interface of the XIO3130 receives a completion with Completer Abort Status. 0 – Completer Abort not received. 1 - Completer Abort received.
11	TABORT_SIG	rcu	Signaled target abort. This bit is set when the downstream PCI Express interface completes a Request with Completer Abort Status. 0 – Completer Abort not signaled. 1 – Completer Abort signaled.
10:9	PCI_SPEED	r	DEVSEL timing. These bits are hardwired to 00. These bits do not apply to PCI Express.
8	DATAPAR	rcu	Master data parity error. This bit is set when the XIO3130 receives a poisoned completion or poisons a write request on the downstream PCI Express interface. This bit is never set if the parity error response enable bit in the Bridge Control register is clear.
7	FBB_CAP	r	Fast back-to-back capable. This bit is hardwired to zero. This bit does not apply to PCI Express.
6	RSVD	r	Reserved. When read, this bit returns zero.
5	66MHZ	r	66-MHz capable. This bit is hardwired to zero. This bit does not apply to PCI Express.
4:0	RSVD	r	Reserved. When read, these bits return zeros.

4.3.18 Memory Base Register

This read/write register specifies the lower limit of the memory addresses that the downstream port forwards downstream.

PCI register offset: 20h

Register type: Read/Write; Read Only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-58. IBit Descriptions – Memory Base Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MEMBASE	rw	Memory base. This field defines the bottom address of the memory address range that is used to determine when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be zero.
3:0	RSVD	r	Reserved. When read, these bits return zeros.

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4.3.19 Memory Limit Register

This read/write register specifies the upper limit of the memory addresses that the downstream port forwards downstream.

PCI register offset: 22h
Register type: Read/Write; Read Only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-59. Bit Descriptions – Memory Limit Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MEMLIMIT	rw	Memory limit. This field defines the top address of the memory address range that is used to determine when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh.
3:0	RSVD	r	Reserved. When read, these bits return zeros.

4.3.20 Pre-fetchable Memory Base Register

This read/write register specifies the lower limit of the pre-fetchable memory addresses that the downstream port forwards downstream.

PCI register offset: 24h
Register type: Read/Write; Read Only
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4-60. Descriptions – Pre-fetchable Memory Base Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	PREBASE	rw	Pre-fetchable memory base. This field defines the bottom address of the pre-fetchable memory address range that is used to determine when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be zero. The Pre-fetchable Base Upper 32 Bits register is used to specify the bit [63:32] of the 64-bit pre-fetchable memory address.
3:0	64BIT	r	64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window.

4.3.21 Pre-fetchable Memory Limit Register

This read/write register specifies the upper limit of the memory addresses that the downstream port forwards downstream.

PCI register offset: 26h
Register type: Read/Write; Read Only
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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Table 4-61. Bit Descriptions – Pre-fetchable Memory Limit Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	PRELIMIT	rw	Pre-fetchable memory limit. This field defines the top address of the pre-fetchable memory address range that is used to determine when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. The Pre-fetchable Limit Upper 32 Bits register is used to specify the bit [63:32] of the 64-bit pre-fetchable memory address.
3:0	64BIT	r	64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window.

4.3.22 Pre-fetchable Base Upper 32 Bits Register

This read/write register specifies the upper 32 bits of the Pre-fetchable Memory Base register.

PCI register offset: 28h

Register type: Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-62. Bit Descriptions – Pre-fetchable Base Upper 32 Bits Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:0	PREBASE	rw	Pre-fetchable memory base upper 32 bits. This field defines the upper 32 bits of the bottom address of the pre-fetchable memory address range that is used to determine when to forward memory transactions downstream.

4.3.23 Pre-fetchable Limit Upper 32 Bits Register

This read/write register specifies the upper 32 bits of the Pre-fetchable Memory Limit register.

PCI register offset: 2Ch

Register type: Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-63. Descriptions – Pre-fetchable Limit Upper 32 Bits Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:0	PRELIMIT	rw	Pre-fetchable memory limit upper 32 bits. This field defines the upper 32 bits of the top address of the pre-fetchable memory address range that is used to determine when to forward memory transactions downstream.

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4.3.24 I/O Base Upper 16 Bits Register

This read/write register specifies the upper 16 bits of the I/O Base register.

PCI register offset: 30h
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-64. Bit Descriptions – I/O Base Upper 16 Bits Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:0	IOBASE	rw	I/O base upper 16 bits. This field defines the upper 16 bits of the bottom address of the I/O address range that is used to determine when to forward I/O transactions downstream.

4.3.25 I/O Limit Upper 16 Bits Register

This read/write register specifies the upper 16 bits of the I/O Limit register.

PCI register offset: 32h
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-65. Bit Descriptions – I/O Limit Upper 16 Bits Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:0	IOLIMIT	rw	I/O limit upper 16 bits. This field defines the upper 16 bits of the top address of the I/O address range that is used to determine when to forward I/O transactions downstream.

4.3.26 Capabilities Pointer Register

This read-only register provides a pointer into the PCI configuration header, which is where the PCI power management block resides. Since the PCI power management registers begin at 50h, this register is hardwired to 50h.

PCI register offset: 34h
Register type: Read only
Default value: 50h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	1	0	0	0	0

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4.3.27 Interrupt Line Register

This read/write register, which the system programs, indicates to the software which interrupt line that the XIO3130 downstream port has assigned to it. The default value of this register is FFh, which indicates that an interrupt line has not yet been assigned to the function. This register is essentially a scratch-pad register; it has no effect on the XIO3130 itself.

PCI register offset: 3Ch

Register type: Read/Write

Default value: FFh

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	1	1	1	1	1	1	1

4.3.28 Interrupt Pin Register

The Interrupt Pin register is read-only, which indicates that the XIO3130 downstream ports generate INTx interrupts as follows:

- Downstream port 0 on PCI Interrupt pin $\overline{\text{INTA}}$ (register value of 01h)
- Downstream port 1 on PCI Interrupt pin $\overline{\text{INTA}}$ (register value of 01h)
- Downstream port 2 on PCI Interrupt pin $\overline{\text{INTA}}$ (register value of 01h)

Interrupts originated by XIO3130 downstream ports are associated with the primary side of the downstream port PCI-to-PCI bridge, and as a result are only passed through the upstream port PCI-to-PCI bridge as described in *PCI Express Base Specification Revision 1.1*, Page 69, Table 2-13.

PCI register offset: 3Dh

Register type: Read only

Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

4.3.29 Bridge Control Register

The Bridge Control register provides extensions to the Command register that are specific to a bridge.

PCI register offset: 3Eh

Register type: Read/Write; Read Only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-66. Bit Descriptions – Bridge Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:12	RSVD	r	Reserved. When read, these bits return zeros.
11	DTSERR	r	Discard timer $\overline{\text{SERR}}$ enable. This bit is hardwired to zero. This bit does not apply to PCI Express.
10	DTSTATUS	r	Discard timer status. This bit is hardwired to zero. This bit does not apply to PCI Express.
9	SEC_DT	r	Secondary discard timer. This bit is hardwired to zero. This bit does not apply to PCI Express.
8	PRI_DEC	r	Primary discard timer. This bit is hardwired to zero. This bit does not apply to PCI Express.
7	FBB_EN	r	Fast back-to-back enable. This bit is hardwired to zero. This bit does not apply to PCI Express.

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Table 4-66. Bit Descriptions – Bridge Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
6	SRST	rw	Secondary bus reset. This bit is set when the software resets all devices downstream of the XIO3130 downstream port. Setting this bit causes the downstream port to send a reset downstream via a training sequence. 0 – Downstream port not in Reset state 1 – Downstream port in Reset state
5	MAM	r	Master abort mode. This bit is hardwired to zero. This bit does not apply to PCI Express.
4	VGA16	rw	VGA 16-bit decode. This bit enables the XIO3130 downstream port to provide full 16-bit decoding for VGA I/O addresses. This bit only has meaning if the VGA enable bit is set. 0 – Ignore address bits [15:10] when decoding VGA I/O addresses. 1 – Decode address bits [15:10] when decoding VGA I/O addresses.
3	VGA	rw	VGA enable. This bit modifies the response by the XIO3130 downstream port to VGA-compatible addresses. If this bit is set, the XIO3130 downstream port positively decodes and forwards the following accesses on the primary interface to the secondary interface (and, conversely, blocks the forwarding of these addresses from the secondary to primary interface): • = Memory accesses in the range 000A 0000h to 000BFFFFh • = I/O addresses in the first 64KB of the I/O address space (address bits [31:16] are 0000h.) and where address bits [9:0] are in the range 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases; address bits [15:10] may possess any value and are not used in the decoding). If the VGA Enable bit is set, forwarding of VGA addresses is independent of the value of the ISA Enable bit (located in the Bridge Control register), the I/O address range and memory address ranges defined by the I/O Base and Limit registers, the Memory Base and Limit registers, and the Pre-fetchable Memory Base and Limit registers of the bridge. Forwarding of VGA addresses is qualified by the I/O Enable and Memory Enable bits in the Command register. 0 – Do not forward VGA-compatible memory and I/O addresses from the primary to secondary interface unless they are enabled for forwarding by the defined I/O and memory address ranges. 1 – Forward VGA-compatible memory and I/O addresses from the primary interface to the secondary interface (if the I/O Enable and Memory Enable bits are set) independent of the I/O and memory address ranges and independent of the ISA Enable bit.
2	ISA	rw	ISA enable. This bit modifies the response by the XIO3130 downstream port to ISA I/O addresses. This bit applies only to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, the bridge blocks any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1 KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1K block. 0 – Forward downstream all I/O addresses in the address range defined by the I/O Base and I/O Limit registers. 1 – Forward upstream ISA I/O addresses in the address range defined by the I/O Base and I/O Limit registers that are in the first 64 KB of PCI I/O address space (top 768 bytes of each 1 KB block).
1	SERR_EN	rw	SERR enable. This bit controls the forwarding of system error events upstream from the secondary interface to the primary interface. The XIO3130's downstream port forwards system error events upstream when: • = This bit is set. • = The $\overline{\text{SERR}}$ enable bit in the downstream port command register is set. • = A nonfatal or fatal error condition is detected on the secondary interface (i.e., the PCI Express interface). 0 – Disable the reporting of nonfatal errors and fatal errors. 1 – Enable the reporting of nonfatal errors and fatal errors.
0	PERR_EN	rw	Parity error response enable. For PCI Express, this bit controls responses to poisoned TLPs received on the downstream port. 0 – Disable responses to poisoned TLPs. 1 – Enable responses to poisoned TLPs.

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4.3.30 Capability ID Register

This read-only register identifies the linked list item as the register for PCI power management. It returns 01h when read.

PCI register offset: 50h

Register type: Read only

Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

4.3.31 Next-Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the XIO3130 downstream port. This register reads 70h, which points to the MSI Capabilities registers.

PCI register offset: 51h

Register type: Read only

Default value: 70h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	1	1	0	0	0	0

4.3.32 Power Management Capabilities Register

This register indicates the capabilities of the XIO3130 downstream port related to PCI power management.

PCI register offset: 52h

Register type: Read only

Default value: XXX3h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	y	1	1	x	1	1	x	0	0	y	0	0	0	0	1	1

Table 4-67. Bit Descriptions – Power Management Capabilities Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:11	PME_SUPPORT	r	$\overline{\text{PME}}$ support. This 5-bit field indicates the power states from which the downstream port may assert $\overline{\text{PME}}$. These five bits return a value of 5'by11x1, which indicates that the XIO3130 can assert $\overline{\text{PME}}$ from D0, D2, D3hot, maybe D3cold (i.e., depending on y), and maybe D1 (i.e., depending on x). The bit that defines this power state for D3cold (i.e., y) is controlled by the AUX_PRESENT bit in the Global Chip Control register. The bit defining this power state for D1 (i.e., x) is controlled by the D1_SUPPORT bit in the Global Switch Control register.
10	D2_SUPPORT	r	This bit returns a 1 when read, which indicates that the function supports the D2 device power state.
9	D1_SUPPORT	r	This bit indicates whether the function supports the D1 device power state. This bit is controlled by the D1_SUPPORT bit in the Global Switch Control register. The default value x is controlled by the default value for the D1_SUPPORT bit in the Global Switch Control register.
8:6	AUX_CURRENT	r	3.3-V_{AUX} auxiliary current requirements. This field reads 3'b00y, i.e., either 3'b001 or 3'b000, depending on the AUX_PRESENT bit in the Global Chip Control register. 3'b001 indicates 55 mA maximum current in D3cold when $\overline{\text{PME}}$ is enabled, according to *PCI Power Management Specification Revision 1.2*, Section 3.2.3, page 26.

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Table 4-67. Bit Descriptions – Power Management Capabilities Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
5	DSI	r	Device-specific initialization. This bit returns 0 when read, which indicates that the XIO3130 does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it.
4	RSVD	r	Reserved. When read, this bit returns zero.
3	PME_CLK	r	$\overline{\text{PME}}$ clock. This bit returns zero, which indicates that the PCI clock is not needed to generate $\overline{\text{PME}}$.
2:0	PM_VERSION	r	Power management version. This field returns 3'b011, which indicates Revision 1.2 compatibility.

4.3.33 Power Management Control/Status Register

This register determines and changes the current power state of the downstream port.

PCI register offset: 54h

Register type: Read/Write; Read Only; Clear by a Write of One; Hardware Update; Sticky

Default value: 0008h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Table 4-68. Bit Descriptions – Power Management Control/Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PME_STAT	rcuh	$\overline{\text{PME}}$ status. PME events are generated due to PCI Hot Plug events. This bit reflects the PME status regardless of the state of PME_EN. 0 – No PME event pending 1 – PME event pending This bit is reset with $\overline{\text{GRST}}$.
14:13	DATA_SCALE	r	Data scale. This 2-bit field returns 0s when read since the XIO3130 does not use the Data register.
12:9	DATA_SEL	r	Data select. This 4-bit field returns 0s when read since the XIO3130 does not use the Data register.
8	PME_EN	rwh	$\overline{\text{PME}}$ enable. This bit enables $\overline{\text{PME}}$/$\overline{\text{WAKE}}$ signaling, even though the XIO3130 never generates $\overline{\text{WAKE}}$. 0 – Disable PME signaling. 1 – Enable PME signaling. This bit is reset with $\overline{\text{GRST}}$.
7:4	RSVD	r	Reserved. When read, these bits return zeros.
3	NO_SOFT_RST	r	No Soft Reset. This bit controls whether the transition from D3hot to D0 resets the state according to PCI Power Management Specification Revision 1.2. This bit is hardwired to 1'b1. 0 – D3hot to D0 transition causes reset. 1 – D3hot to D0 transition does not cause reset.
2	RSVD	r	Reserved. When read, this bit returns zero.
1:0	PWR_STATE	rw	Power state. This 2-bit field is used to determine the current power state of the function and to set the function into a new power state. This field is encoded as follows: 00 = D0 01 = D1 10 = D2 11 = D3hot

4.3.34 Power Management Bridge Support Extension Register

This read-only register is used to indicate to the host software what the state of the downstream port's secondary bus will be when the downstream port is placed in D3.

PCI register offset: 56h

Register type: Read only

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-69. Bit Descriptions – PM Bridge Support Extension Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	BPCC	r	Bus power/Clock control enable. This bit is read-only zero. This bit does not apply to PCI Express.
6	BSTATE	r	B2/B3 support. This bit is read-only zero. This bit does not apply to PCI Express.
5:0	RSVD	r	Reserved. When read, these bits return zeros.

4.3.35 Power Management Data Register

The read-only register is not applicable to the XIO3130 and returns 00h when read.

PCI register offset: 57h

Register type: Read only

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.3.36 MSI Capability ID Register

This read-only register identifies the linked list item as the register for Message Signaled Interrupts Capabilities. The register returns 05h when read.

PCI register offset: 70h

Register type: Read only

Default value: 05h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	1

4.3.37 Next-Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the XIO3130. This register reads 80h, which points to the Subsystem ID and Subsystem Vendor ID Capabilities registers.

PCI register offset: 71h

Register type: Read only

Default value: 80h

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BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	0	0

4.3.38 MSI Message Control Register

This register is used to control the sending of MSI messages.

PCI register offset: 72h
Register type: Read/Write; Read Only
Default value: 0080h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Table 4-70. Bit Descriptions – MSI Message Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	r	Reserved. When read, these bits return zeros.
7	64CAP	r	64-bit message capability. This bit is read-only 1, which indicates that the XIO3130 downstream port supports 64-bit MSI message addressing.
6:4	MM_EN	rw	Multiple message enable. This field indicates the number of distinct messages that the XIO3130 downstream port is allowed to generate. 000 – 1 message 001 – 2 messages 010 – 4 messages 011 – 8 messages 100 – 16 messages 101 – 32 messages 110 – Reserved 111 – Reserved
3:1	MM_CAP	r	Multiple message capabilities. This field indicates the number of distinct messages that the XIO3130 downstream port can generate. This field is read-only 000, which indicates that the downstream port can signal one interrupt.
0	MSI_EN	rw	MSI Enable. This bit is used to enable MSI interrupt signaling. The software must enable MSI signaling for the XIO3130 downstream port to send MSI messages. 0 – MSI signaling is prohibited 1 – MSI signaling is enabled

4.3.39 MSI Message Address Register

This register contains the lower 32 bits of the address that an MSI message shall be written to when an interrupt is to be signaled.

PCI register offset: 74h
Register type: Read/Write; Read Only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-71. Bit Descriptions – MSI Message Address Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:2	ADDRESS	rw	System-specified message address.
1:0	RSVD	r	Reserved. When read, these bits return zeros.

4.3.40 MSI Message Upper Address Register

This read/write register contains the upper 32 bits of the address that a MSI message shall be written to when an interrupt is to be signaled. If this register is 0000 0000h, 32-bit addressing is used in the MSI Message packet. Otherwise, 64-bit addressing is used.

PCI register offset: 78h

Register type: Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.3.41 MSI Message Data Register

This register contains the data that the software programmed the device to send when it sends an MSI message.

PCI register offset: 7Ch

Register type: Read/Write

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-72. Bit Descriptions – MSI Data Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MSG	rw	System-specific message. This field contains the portion of the message that the XIO3130 can never modify.
3:0	MSG_NUM	rw	Message number. This portion of the message field may be modified to contain the message number if multiple messages are enabled. Since the XIO3130 downstream port only generates one MSI type, the XIO3130 hardware does not modify these bits.

4.3.42 Capability ID Register

This read-only register identifies the linked list item as the register for Subsystem ID and Subsystem Vendor ID Capabilities. This register returns 0Dh when read.

PCI register offset: 80h

Register type: Read only

Default value: 0Dh

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BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	1	1	0	1

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4.3.43 Next-Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the XIO3130 downstream port. This register reads 90h, which points to the PCI Express Capabilities registers.

PCI register offset: 81h

Register type: Read only

Default value: 90h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	1	0	0	0	0

4.3.44 Subsystem Vendor ID Register

This register is used for system and option card identification and may be required for certain operating systems. This read-only register is a direct reflection of the upstream port's Subsystem Access register, which is read/write and is initialized through the EEPROM (if present).

PCI register offset: 84h

Register type: Read only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.3.45 Subsystem ID Register

This register is used for system and option card identification and may be required for certain operating systems. This read-only register is a direct reflection of the upstream port's Subsystem Access register, which is read/write and is initialized through the EEPROM (if present).

PCI register offset: 86h

Register type: Read only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.3.46 PCI Express Capability ID Register

This read-only register identifies the linked list item as the register for PCI Express Capabilities. When read, this register returns 10h.

PCI register offset: 90h

Register type: Read only

Default value: 10h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0

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4.3.47 Next-Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the XIO3130 downstream port. This register reads 00h, which indicates that no additional capabilities are supported.

PCI register offset: 91h
Register type: Read only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.3.48 PCI Express Capabilities Register

This register indicates the capabilities of the downstream port of the XIO3130 related to PCI Express.

PCI register offset: 92h
Register type: Read only
Default value: 0061h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1

Table 4-73. Bit Descriptions – PCI Express Capabilities Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:14	RSVD	r	Reserved. When read, these bits return zeros.
13:9	INT_NUM	r	Interrupt message number. This field is used for MSI support and is implemented as read-only zero.
8	SLOT	r	Slot implemented. This bit indicates whether the port is connected to a slot connector (e.g., for PCI Express, ExpressCard™ or other add-in cards). This field can be programmed by writing to the General Control register. 0 – Port not connected to a slot 1 – Port connected to a slot
7:4	DEV_TYPE	r	Device/Port type. This read-only field returns 0110b, which indicates that the device is a downstream port of a PCI Express XIO3130.
3:0	VERSION	r	Capability version. This field returns 0001b, which indicates revision 1 of the PCI Express capability.

4.3.49 Device Capabilities Register

The Device Capabilities register indicates the device-specific capabilities of the XIO3130 downstream port.

PCI register offset: 94h
Register type: Read Only; Hardware Update
Default value: 0000 8XX1h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	u	u	u	v	v	v	0	0	0	0	0	1

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Table 4-74. Bit Descriptions – Device Capabilities Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:28	RSVD	r	Reserved. When read, these bits return zeros.
27:26	CSPLS	ru	Captured slot power limit scale. This field is only applicable to upstream ports and is hardwired to zero.
25:18	CSPLV	ru	Captured slot power limit value. This field is only applicable to upstream ports and is hardwired to zero.
17:16	RSVD	r	Reserved. When read, these bits return zeros.
15	RBER	r	Role-based error reporting. This bit is set to 1b to indicate support for role-based error reporting.
14	PIP	r	Power indicator present. This bit indicates whether the XIO3130 has a power indicator. This bit is hardwired to zero.
13	AIP	r	Attention indicator present. This bit indicates whether the XIO3130 has an attention indicator. This bit is hardwired to zero.
12	ABP	r	Attention button present. This bit indicates whether the XIO3130 has a power button. This bit is hardwired to zero.
11:6	RSVD	r	Reserved. When read, these bits return zeros.
5	ETFS	r	Extended tag field supported. This bit indicates the size of the tag field supported. This bit is hardwired to 0, which indicates support for 5-bit tag fields.
4:3	PFS	r	Phantom functions supported. This field is read-only 00b, which indicates that function numbers are not used for phantom functions.
2:0	MPSS	r	Max payload size supported. This field indicates the maximum payload size that the device can support for TLPs. This field is encoded as 001b, which indicates that the maximum payload size for a TLP is 256 bytes.

4.3.50 Device Control Register

The Device Control register controls PCI Express device-specific parameters.

PCI register offset: 98h

Register type: Read/Write; Read Only

Default value: 2000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-75. Bit Descriptions – Device Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	RSVD	r	Reserved. When read, this bit returns zero.
14:12	MRRS	rw	Max read request size. This field is programmed by the host software to set the maximum size of a read request that the XIO3130 can generate. The XIO3130 uses this field in conjunction with the Cache Line Size register to determine how much data to fetch on a read request. This field is encoded as: 000 – 128B 001 – 256B 010 – 512B (default) 011 – 1024B 100 – 2048B 101 – 4096B 110 – Reserved 111 – Reserved
11	ENS	r	Enable no snoop. Since the XIO3130 does not support setting the no-snoop attribute, this bit is read-only zero.

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Table 4-75. Bit Descriptions – Device Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
10	APPE	r	Auxiliary power PM enable. This bit is read-only zero, since the XIO3130 requires a minimal amount of AUX power when PME is disabled.
9	PFE	r	Phantom function enable. Since the XIO3130 part does not support phantom functions, this bit is read-only zero.
8	ETFE	r	Extended tag field enable. Since the XIO3130 part does not support extended tags, this bit is read-only zero.
7:5	MPS	rw	Max payload size. This field is programmed by the host software to set the maximum size of posted writes or read completions that the XIO3130 can initiate. This field is encoded as: 000 – 128B (default) 001 – 256B 010 – 512B 011 – 1024B 100 – 2048B 101 – 4096B 110 – Reserved 111 – Reserved
4	ERO	r	Enable relaxed ordering. Since the XIO3130 part does not support relaxed ordering, this bit is read-only zero.
3	URRE	rw	Unsupported request reporting enable. If this bit is set, the XIO3130 is enabled to send ERR_NONFATAL messages to the root complex when an unsupported request is received by the downstream port. 0 – Do not report unsupported requests to the root complex. 1 – Report unsupported requests to the root complex.
2	FERE	rw	Fatal error reporting enable. If this bit is set, the XIO3130 is enabled to send ERR_FATAL messages to the root complex when a system error event occurs. 0 – Do not report fatal errors to the root complex. 1 – Report fatal errors to the root complex.
1	NFERE	rw	Nonfatal error reporting enable. If this bit is set, the XIO3130 is enabled to send ERR_NONFATAL messages to the root complex when a system error event occurs. 0 – Do not report nonfatal errors to the root complex. 1 – Report nonfatal errors to the root complex.
0	CERE	rw	Correctable error reporting enable. If this bit is set, the XIO3130 is enabled to send ERR_CORR messages to the root complex when a system error event occurs. 0 – Do not report correctable errors to the root complex. 1 – Report correctable errors to the root complex.

4.3.51 Device Status Register

The Device Status register controls PCI Express device-specific parameters.

PCI register offset: 9Ah
Register type: Read Only; Clear by a Write of One; Hardware Update
Default value: 00X0h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	x	0	0	0	0

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Table 4-76. Bit Descriptions – Device Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:6	RSVD	r	Reserved. When read, these bits return zeros.
5	PEND	ru	Transaction pending. This bit is set when the XIO3130 downstream port has issued a non-posted transaction that has not been completed yet.
4	APD	ru	AUX power detected. This bit indicates that AUX power is present. This bit is a direct reflection of the AUX_PRSNT bit in the Global Chip Control register, and it has the same default value. 0 – No AUX power detected. 1 – AUX power detected.
3	URD	rcu	Unsupported Request detected. This bit is asserted when an Unsupported Request error is detected (i.e., when a request is received that results in sending a completion with an Unsupported Request status). Errors are logged in this bit regardless of whether error reporting is enabled in the Device Control register.
2	FED	rcu	Fatal error detected. This bit is set by the XIO3130 when a fatal error is detected. Errors are logged in this bit regardless of whether error reporting is enabled in the Device Control register.
1	NFED	rcu	Nonfatal error detected. This bit is set by the XIO3130 when a nonfatal error is detected. Errors are logged in this bit regardless of whether error reporting is enabled in the Device Control register.
0	CED	rcu	Correctable error detected. This bit is set by the XIO3130 when a correctable error is detected. Errors are logged in this bit regardless of whether error reporting is enabled in the Device Control register.

4.3.52 Link Capabilities Register

The Link Capabilities register indicates the link-specific capabilities of the XIO3130 downstream port.

PCI register offset: 9Ch

Register type: Read only

Default value: 0XXX XC11h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	x	x	0	0	0	w	w	1	y	y

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	y	z	z	z	1	1	0	0	0	0	0	1	0	0	0	1

Table 4-77. Bit Descriptions – Link Capabilities Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	PORT_NUM	r	Port number. This field indicates the port number for the PCI Express link. This field is set to 8'h01 for downstream port 0, 8'h02 for downstream port 1, and 8'h03 for downstream port 2.
23:21	RSVD	r	Reserved. When read, these bits return zeros.
20	DLL_LARC	r	Data link layer link active reporting capable. This bit indicates whether this slot is capable of reporting whether the link is active. This field can be programmed by writing to the General Control register. The default state w is that of the LINK_ACT_RPT_CAP field in the General Control register. 0 – Incapable of link active reporting 1 – Capable of link active reporting
19	SDERC	r	Surprise down error reporting capable. This bit indicates whether this slot is capable of detecting and reporting a surprise down error condition. This field can be programmed by writing to the LINK_ACT_RPT_CAP field in the General Control register. The default state w is that of the LINK_ACT_RPT_CAP field in the General Control register. 0 – Incapable of detecting and reporting a surprise down error condition 1 – Capable of detecting and reporting a surprise down error condition
18	CPM	r	Clock power management. This bit is 1b, which indicates support for $\overline{\text{CLKREQ}}$.

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Table 4-77. Bit Descriptions – Link Capabilities Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
17:15	L1_LATENCY	r	L1 exit latency. This field indicates the time required to transition from the L1 state to the L0 state. This field is a direct reflection of the Downstream Ports Link PM Latency register L1_EXIT_LAT field, which is a read/write field that is loaded from EEPROM (if present). The default value of this field is yyy, which is the same as the default value of the Link PM Latency register L1_EXIT_LAT field.
14:12	L0S_LATENCY	r	L0s exit latency. This field indicates the time required to transition from the L0s state to the L0 state. This field is a direct reflection of the Downstream Ports Link PM Latency register L0S_EXIT_LAT field, which is a read/write field that is loaded from EEPROM (if present). The default value of this field is zzz, which is the same as the default value of the Link PM Latency register L0S_EXIT_LAT field.
11:10	ASLPMS	r	Active State Link PM support. This field reads 11b, which indicates that the XIO3130 supports both L0s and L1 for Active State Link PM.
9:4	MLW	r	Maximum link width. This field is encoded 000001b to indicate that the XIO3130 downstream port supports only an x1 PCI Express link.
3:0	MLS	r	Maximum link speed. This field is encoded 0001b to indicate that the XIO3130 downstream port supports a maximum link speed of 2.5 Gb/s.

4.3.53 Link Control Register

The Link Control register is used to control link-specific behavior.

PCI register offset: A0h

Register type: Read/Write; Read Only

Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-78. Bit Descriptions – Link Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:9	RSVD	r	Reserved. When read, these bits return zeros.
8	CPM_EN	rw	Clock power management enable. When $\overline{\text{CLKREQ}}$ support is enabled, the EP_LI_LAT field in the Downstream Ports Link PM Latency register increases due to link PLL locking requirements. 0 – Disables $\overline{\text{CLKREQ}}$ support on downstream port 1 – Enables $\overline{\text{CLKREQ}}$ support on downstream port
7	ES	rw	Extended synch. This bit is used to force the XIO3130 downstream port to extend the transmission of FTS ordered sets and an extra TS2 when exiting from L1 before entering to L0. 0 – Normal synch 1 – Extended synch
6	CCC	rw	Common clock configuration. This bit is set when a common clock is provided to both ends of the downstream port's PCI Express link. This bit can be used to change the L0s and L1 exit latencies. 0 – Reference clock is asynchronous 1 – Reference clock is synchronous
5	RL	rw	Retrain link. This bit initiates link retraining on the downstream port. This bit always returns 0b when read. 0 – Do not initiate link retraining 1 – Initiate link retraining
4	LD	rw	Link disable. This bit disables the link. Writes to this bit are immediately reflected in the value read from the bit, regardless of the actual link state. 0 – Link enabled 1 – Link disabled

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Table 4-78. Bit Descriptions – Link Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
3	RCB	r	Read completion boundary. This bit specifies the minimum size read completion packet that the XIO3130 can send when breaking a read request into multiple completion packets. This field is not applicable to XIO3130; i.e., the XIO3130 does not break up completion packets and is hardwired to zero. 0 – 64 bytes 1 – 128 bytes
2	RSVD	r	Reserved. When read, this bit returns zero.
1:0	ASLPMC	rw	Active State Link PM Control. This field is used to enable and disable active state PM. 00 – Active State PM disabled 01 – L0s entry enabled 10 – Reserved 11 – L0s and L1 entry enabled

4.3.54 Link Status Register

The Link Status register indicates the current state of the PCI Express Link.

PCI register offset: A2h

Register type: Read Only; Hardware Update

Default value: XX11h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	x	0	0	0	0	0	1	0	0	0	1

Table 4-79. Bit Descriptions – Link Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:14	RSVD	r	Reserved. When read, these bits return zeros.
13	DLL_ACTV	r	Data link layer active. When the DLL_LARC field in the Link Capabilities register is asserted, this field returns the value of the following comparison: (Link_State == DL_Active). This field returns zero when the DLL_LARC field in the Link Capabilities register is de-asserted.
12	SCC	r	Slot clock configuration. This bit reflects the reference clock configurations and is read-only 1, indicating that a 100 MHz common clock reference is used.
11	LT	ru	Link training in progress. The hardware automatically clears this bit when the LTSSM exits the Configuration/Recovery state.
10	UNDEF	r	Undefined. The value read from this bit is undefined.
9:4	NLW	r	Negotiated link width. This field is read-only 000001b, which indicates that the lane width is x1.
3:0	LS	r	Link speed. This field is read-only 0001b, which indicates that the link speed is 2.5 Gb/s.

4.3.55 Slot Capabilities Register

The Slot Capabilities register indicates the slot-specific capabilities of the downstream port.

PCI register offset: A4h

Register type: Read/Write; Read Only; Hardware Update

Default value: 0000 0060h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0

Table 4-80. Bit Descriptions – Slot Capabilities Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:19	SLOT_NUM	r	Physical slot number. This field indicates a system-dependent physical slot number that is unique to each slot in the system. This field can be programmed by writing to the General Slot Info register.
18	EMILP	ru	Electromechanical interlock present. This bit indicates whether an electromechanical interlock is implemented on the chassis for this slot. This bit can be programmed by writing to the General Control register. 0 – Electromechanical interlock not present. 1 – Electromechanical interlock present.
17	NCCS	ru	No command completed support. This bit is hardwired to zero, which indicates that command completed software notification (i.e., interrupt generation) is always supported. 0 – Command completed support is provided. 1 – Command completed support is not provided.
16:15	SPLS	rw	Slot power limit scale. This field Indicates the scale that is used for the slow power limit value. This field may be written only once after any given PERST; the effect when written is to cause the port to send the Set_Slot_Power_Limit message. 00 – 1.0x 01 – 0.1x 10 – 0.01x 11 – 0.001x This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$.
14:7	SPLV	rw	Slot power limit value. When multiplied by the SPLS field (see previous row in this table), this field indicates the maximum power in watts that can be consumed by a card plugged into a slot attached to this port,. This field may be written only once after any given PERST; the effect when written is to cause the port to send the Set_Slot_Power_Limit message. This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$.
6	HP_CAPABLE	r	PCI Hot Plug capable. This bit indicates whether this slot is capable of supporting PCI Hot Plug operations. The default setting of this register is defined by the DPSTRP[2,0] strapping. This bit can be programmed by writing to the General Control register bit 14, which is SLOT_HPC. For more information on the General Control register, see section 3.3.61. 0 – Incapable of supporting PCI Hot Plug operations 1 – Capable of supporting PCI Hot Plug operations
5	HP_SURPRISE	r	PCI Hot Plug surprise. This bit indicates whether a device present in this slot can be removed from the system without any prior notification. This bit can be programmed by writing to the General Control register bit 13, which is SLOT_HPS. For more information on the General Control register, see section 3.3.61. 0 – No device present that can be removed by surprise 1 – Device present that can be removed by surprise
4	PIP	r	Power indicator present. This bit indicates whether a power indicator is implemented on the chassis for this slot. This bit can be programmed by writing to the General Control register bit 12, which is SLOT_PIP. For more information on the General Control register, see section 3.3.61. 0 – Power indicator not present 1 – Power indicator present
3	AIP	r	Attention indicator present. This bit indicates whether an attention indicator is implemented on the chassis for this slot. This bit can be programmed by writing to the General Control register bit 11, which is SLOT_AIP. For more information on the General Control register, see section 3.3.61. 0 – Attention indicator not present 1 – Attention indicator present

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Table 4-80. Bit Descriptions – Slot Capabilities Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
2	MRLSP	r	Manual retention latch sensor present. This bit indicates whether a manual retention latch (MRL) sensor is implemented on the chassis for this slot. This bit can be programmed by writing to the General Control register bit 10, which is SLOT_MRLSP. For more information on the General Control register, see section 3.3.61. 0 – MRL sensor not present 1 – MRL sensor present
1	PCP	r	Power controller present. This bit indicates whether a power controller is implemented for this slot. The default setting of this register is defined by the DPSTRP[2,0] strapping. This bit can be programmed by writing to the General Control register bit 9, which is SLOT_PCP. For more information on the General Control Register, see section 3.3.61. If this bit is zero, then the PWRON_EC output signal, which may go to a pin, is forced asserted; there is no such effect on the PWRON output signal. 0 – Power controller not present 1 – Power controller present
0	ABP	r	Attention button present. This bit indicates whether an attention button is implemented on the chassis for this slot. This bit can be programmed by writing to the General Control register bit 8, which is SLOT_ABP. For more information on the General Control register, see section 3.3.61. 0 – Attention button not present 1 – Attention button present

4.3.56 Slot Control Register

The Slot Control register controls slot-specific parameters.

PCI register offset: A8h

Register type: Read/Write; Read Only

Default value: 07C0h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0

Table 4-81. Bit Descriptions – Slot Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:13	RSVD	r	Reserved. When read, these bits return zeros.
12	DLLSC_EN	rw	Data link layer state changed enable. This bit enables software notification (i.e., interrupts) due to an assertion of the DLLSC field in the Slot Status register. 0 – DLLSC interrupts disabled 1 – DLLSC interrupts enabled
11	EMIL_CTL	rw	Electromechanical interlock control. When read, this bit returns zero. A write of 1'b0 has no effect. If the EMILP field in the Slot Capabilities register is asserted, then a write of 1'b1 causes a 100 ms high-going pulse on the EMIL_CTL output pin; otherwise, the write has no effect.
10	PC_CTL	rw	Power controller control. When read, this bit indicates the current state of power applied to the slot. Writes set the power state of the slot and control the PWR_ON pin. When this bit transitions from power on to power off, and the HP_PME_MSG_EN bit in the Global Switch Control register is asserted, a PME_Turn_Off message is sent and the PWRON output pin gets de-asserted only after a PME_TO_Ack is received or after a 100 ms timeout. 0 – Power on 1 – Power off

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Table 4-81. Bit Descriptions – Slot Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
9:8	PI_CTL	rw	Power indicator control. When read, this field indicates the current state of the power indicator. Writes set the power indicator state. When writes cause this field to change, the appropriate POWER_INDICATOR_* messages are sent. This bit controls the PWR_LED output pin. 00b – Reserved 01b – On 10b – Blinking 11b – Off
7:6	AI_CTL	rw	Attention indicator control. When read, this field indicates the current state of the attention indicator. Writes set the attention indicator state. When writes cause this field to change, the appropriate ATTENTION_INDICATOR_* messages are sent. This bit controls the ATN_LED output pin. 00b – Reserved 01b – On 10b – Blinking 11b – Off
5	HPI_EN	rw	PCI Hot Plug interrupt enable. This bit enables generation of PCI Hot Plug interrupts on enabled PCI Hot Plug events. 0 – PCI Hot Plug interrupts disabled 1 – PCI Hot Plug interrupts enabled
4	CCI_EN	rw	Command-completed interrupt enable. This bit enables generation of an interrupt upon completion of a command by the PCI Hot Plug Controller. HPI_EN, and MSI_EN (see MSI Message Control register) must also be enabled for interrupt generation. A Hot Plug Controller Command is defined as a state change in any of the *_CTL bits in this register (i.e., software writes). 0 – Command-completed interrupts disabled 1 – Command-completed interrupts enabled
3	PDC_EN	rw	Presence detect changed enable. This bit enables generation of a • = = = = = = = = = PCI Hot Plug interrupt • = = = = = = = = = PME when the PDC bit in the Slot Status register is asserted. 0 – Disabled 1 – Enabled HPI_EN and MSI_EN (see MSI Message Control register) must also be enabled for interrupt generation. PME_EN must also be enabled for PME signaling during D1, D2, or D3hot. For more information, see section 6.7.7 in *PCI Express Base Specification Revision 1.0a*.
2	MRLSC_EN	rw	Manual retention latch sensor changed enable. This bit enables generation of a • = = = = = = = = = PCI Hot Plug interrupt • = = = = = = = = = PME when the MRLSC bit in the Slot Status register is asserted. 0 – Disabled 1 – Enabled HPI_EN and MSI_EN (see MSI Message Control register) must also be enabled for interrupt generation. PME_EN must also be enabled for PME signaling during D1, D2, or D3hot. For more information, see section 6.7.7 in *PCI Express Base Specification Revision 1.0a.*
1	PFD_EN	rw	Power fault detected enable. This bit enables generation of a • = = = = = = = = = PCI Hot Plug interrupt • = = = = = = = = = PME when the PFD bit in the Slot Status register is asserted. 0 – Disabled 1 – Enabled HPI_EN and MSI_EN (see MSI Message Control register) must also be enabled for interrupt generation. PME_EN must also be enabled for PME signaling during D1, D2, or D3hot. For more information, see section 6.7.7 in *PCI Express Base Specification Revision 1.0a.*

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Table 4-81. Bit Descriptions – Slot Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
0	ABP_EN	rw	Attention button pressed enable. This bit enables generation of a • = = = = = = = = = = PCI Hot Plug interrupt • = = = = = = = = = = PME when the ABP bit in the Slot Status register is asserted. 0 – Disabled 1 – Enabled HPI_EN and MSI_EN (see Table 3i21) must also be enabled for interrupt generation. PME_EN must also be enabled for PME signaling during D1, D2, or D3hot. For more information, see section 6.7.7 in *PCI Express Base Specification Revision 1.0a.*

4.3.57 Slot Status Register

The Slot Status register provides information about slot-specific parameters.

PCI register offset: AAh

Register type: Read Only; Clear by a Write of One; Hardware Update

Default value: 0010h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Table 4-82. Bit Descriptions – Slot Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:9	RSVD	r	Reserved. When read, these bits return zeros.
8	DLLSC	ruc	Data link layer state changed. This bit is set when the DLL_ACTV field in the Link Status register changes state. A write of 1'b1 clears this field. A write of 1'b0 has no effect.
7	EMIL_STAT	r	Electromechanical interlock status. If an electromechanical interlock is implemented for the slot, this field indicates the current status of the electromechanical interlock. 0 – Electromechanical interlock disengaged 1 – Electromechanical interlock engaged
6	PDS	ru	Presence detect state. This bit indicates whether a card is present in a slot. If the SLOT_PRSNT bit in the General Control register is de-asserted, this bit always reads back asserted. If the SLOT_PRSNT bit is asserted, this bit indicates the state of a de-bounced derivative of the $\overline{\text{PRSNT}}$ input pin. 0 – Card presence detection output de-asserted (i.e., slot empty) 1 – Card presence detection output asserted (i.e., card present in slot)
5	MRLSS	ru	Manual retention latch sensor state. This bit indicates the state of a de-bounced derivative of the $\overline{\text{MRLS_DET}}$ input pin. 0 – $\overline{\text{MRLS_DET}}$ pin asserted (i.e., MRL closed) 1 – $\overline{\text{MRLS_DET}}$ pin de-asserted (i.e., MRL open)
4	CC	ruc	Command completed. This bit is set when the PCI Hot Plug Controller is ready to accept another command; it does not ensure that the previous command is completely finished. A Hot Plug controller command is defined as a state change in any of the *_CTL bits in the Slot Control register (i.e., software writes). 0 – PCI Hot Plug controller is not ready to accept a new command. 1 – PCI Hot Plug controller is ready to accept a new command.
3	PDC	ruc	Presence detect changed. This bit indicates whether the state of the PDS bit has changed. 0 – PDS bit has not changed. 1 – PDS bit has changed.

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Table 4-82. Bit Descriptions – Slot Status Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
2	MRLSC	ruc	MRL sensor changed. This bit indicates whether the state of the MRLSS bit has changed. 0 – MRLSS bit has not changed. 1 – MRLSS bit has changed.
1	PFD	ruc	Power fault detected. This bit indicates the state of the PWRFLT pin. 0 – PWRFLT pin de-asserted (no power fault at slot). 1 – PWRFLT pin asserted (power fault at slot).
0	ABP	ruc	Attention button pressed. This bit indicates a de-asserted-to-asserted transition on a de-bounced derivative of the ATN_BTN pin. 0 – Attention button not pressed 1 – Attention button pressed

4.3.58 TI Proprietary Register

This read/write TI proprietary register is located at offset C8h and controls TI proprietary functions. This register must not be changed from the specified default state. If the default value is changed in error, a PCI Express Reset (PERST) returns this register to a default state.

If an EEPROM is used to load configuration registers, the value loaded for this register must be 0000 0001h.

PCI register offset: C8h
Register type: Read/Write
Default value: xxxx 0001

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

4.3.59 TI Proprietary Register

This read/write TI proprietary register is located at offset CCh and controls TI proprietary functions. This register must not be changed from the specified default state. If the default value is changed in error, a PCI Express Reset (PERST) returns this register to a default state.

If an EEPROM is used to load configuration registers, the value loaded for this register must be 0000 0000h.

PCI register offset: CCh
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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4.3.60 TI Proprietary Register

This read/write TI proprietary register is located at offset D0h and controls TI proprietary functions. This register must not be changed from the specified default state. If the default value is changed in error, a PCI Express Reset (PERST) returns this register to a default state.

If an EEPROM is used to load configuration registers, the value loaded for this register must be 3214 0000h.

PCI register offset: D0h

Register type: Read/Write

Default value: 3214 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	1	1	0	0	1	0	0	0	0	1	0	1	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.3.61 General Control Register

This read/write register is used to control various functions of the XIO3130 downstream port.

PCI register offset: D4h

Register type: Read/Write; Read Only

Default value: 0000 x0xx

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	x	x	0	0	0	0	0	x	0	0	1	0	0	0	x

Table 4-83. Bit Descriptions – General Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:17	RSVD	r	Reserved. When read, these bits return zeros.
16	TI_PROPRIETARY	rw	TI proprietary. This bit must not be changed from the specified default state.
15	RC_PF_CTL	rw	REFCK power fault control. This bit controls whether REFCK output should be disabled when PWR_FAULT is asserted. 0 – REFCK output enable is not a function of PWR_FAULT. 1 – REFCK output enable is a function of PWR_FAULT. This field is loaded from EEPROM (if present) and reset with PERST.
14	SLOT_HPC	rw	PCI Hot Plug capable. This bit indicates whether this slot is capable of PCI Hot Plug operations. This bit is used to control the PCI Hot Plug capable (HPC) field in the Slot Capabilities register. 0 – Slot is not PCI Hot Plug capable. 1 – Slot is PCI Hot Plug capable. This field is loaded from EEPROM (if present) and reset with PERST. The default value for this bit is that of the DNn_DPSTRP pin for the associated port.

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Table 4-83. Bit Descriptions – General Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
13	SLOT_HPS	rw	PCI Hot Plug surprise. This bit indicates whether a device present in this slot can be removed from the system without prior notification. This bit is used to control the PCI Hot Plug surprise (HPS) field in the Slot Capabilities register. 0 – No device present that can be removed without prior notification 1 – Device present that can be removed without prior notification. This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$. The default value for this bit is that of the DNn_DPSTRP pin for the associated port.
12	SLOT_PIP	rw	Power indicator present. This bit indicates whether a power indicator is implemented on the chassis for this slot. This bit is used to control the PIP field in the Slot Capabilities register. 0 – Power indicator not implemented 1 – Power indicator implemented This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$.
11	SLOT_AIP	rw	Attention indicator present. This bit indicates whether an attention indicator is implemented on the chassis for this slot. This bit is used to control the AIP field in the Slot Capabilities register. 0 – Attention indicator not implemented 1 – Attention indicator implemented This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$.
10	SLOT_MRLSP	rw	Manual retention latch sensor present. This bit indicates whether an MRL sensor is implemented on the chassis for this slot. This bit is used to control the MRLSP field in the Slot Capabilities register. 0 – MRL sensor not implemented 1 – MRL sensor implemented This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$.
9	SLOT_PCP	rw	Power controller present. This bit indicates whether a power controller is implemented for this slot to control power. This bit is used to control the power controller present (PCP) field in the Slot Capabilities register. 0 – Power controller not implemented 1 – Power controller implemented This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$.
8	SLOT_ABP	rw	Attention button present. This bit indicates whether an attention button is implemented on the chassis for this slot. This bit is used to control the attention button present (ABP) field in the Slot Capabilities register. 0 – Attention button not implemented 1 – Attention button implemented This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$.
7	SLOT_PRSNT	rw	Slot implemented. This bit indicates that the downstream port is connected to an add-in card slot (e.g., PCI Express, ExpressCard, etc.). This bit is used to control the SLOT bit in the PCI Express Capabilities register. 0 – Port not connected to slot 1 – Port connected to slot This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$. The default value for this bit is that of the DNn_DPSTRP pin for the associated port.
6	SLOT_PFIP	rw	Power fault input present. This bit indicates whether an input pin is used as a power fault detection input for this slot. This bit is used to control whether the power fault input pin is used, e.g., for disabling the REFCLK output buffer. 0 – Power fault input not implemented 1 – Power fault input implemented This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$.

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Table 4-83. Bit Descriptions – General Control Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
5	SLOT_EMILP	rw	Electromechanical interlock present. This bit indicates whether an electromechanical interlock is implemented on the chassis for this slot. This bit is used to control the EMILP field in the Slot Capabilities register. 0 – Electromechanical interlock not implemented 1 – Electromechanical interlock implemented This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$.
4	LINK_ACT_RPT_CAP	rw	Link active reporting capable. This bit indicates whether this slot is capable of reporting whether the link is active. This bit is used to control the DLL_LARC field in the Link Capabilities register. This field is used to control the SDERC field in the Link Capabilities register. 0 – Slot is not link active reporting capable 1 – Slot is link active reporting capable This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$.
3	RSVD	rw	This bit is a reserved diagnostic bit that must be set to 0 for proper operation. If an EEPROM is used, the corresponding bit in the EEPROM must be set to 0.
2	RSVD	r	Reserved. When read, this bit returns zero.
1	REFCK_DIS	rw	Reference clock disable. This bit is used to disable the REFCK output. 0 – REFCK enabled 1 – REFCK disabled This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$.
0	RCVR_PRSNT_EN	rw	Receiver presence detect enable. This bit selects whether the $\overline{\text{PRSNT}}$ pin or receiver detect us used to determine whether the slot is present. 0 – $\overline{\text{PRSNT}}$ pin is used to determine whether slot is present 1 – Receiver detect is used to determine whether slot is present. It is recommended to only use this option when $\overline{\text{PRSNT}}$ is not available and the card is removable. This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$. The default value for this bit is the inverse of the DNn_DPSTRP pin for the associated port.

4.3.62 L0s Idle Timeout Register

This read/write register controls the idle timeout for initiating L0s entry on the Tx path. The value is in units of 256 ns. The default value is set for just under 7 = s. The minimum timeout is 256 ns. This register is loaded from serial EEPROM and is reset with $\overline{\text{PERST}}$.

PCI register offset: ECh
Register type: Read/Write
Default value: 1Ah

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	1	0	1	0

4.3.63 General Slot Info Register

This read/write register contains information that is used in the slot capabilities and control registers for the downstream port.

PCI register offset: EEh
Register type: Read/Write; Read Only
Default value: 0000h

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BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-84. Bit Descriptions – General Slot Info Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:3	SLOT_NUM	rw	Slot number. This field is used to program the Physical Slot Number field in the Slot Capabilities register. This field is loaded from EEPROM (if present) and reset with $\overline{\text{PERST}}$.
2:0	RSVD	r	Reserved. When read, these bits return zeros.

4.3.64 Advanced Error Reporting Capabilities ID Register

This read-only register identifies the linked list item as the register for PCI Express Advanced Error Reporting Capabilities. The register returns 0001h when read.

PCI register offset: 100h
Register type: Read only
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

4.3.65 Next Capability Offset/Capability Version Register

This read-only register returns the value 0000h to indicate that this extended capability block represents the end of the linked list of extended capability structures. The least significant four bits identify the revision of the current capability block as 1h.

PCI register offset: 102h
Register type: Read only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.3.66 Uncorrectable Error Status Register

This register reports the status of individual errors as they occur. Software may clear these bits only by writing a 1 to the desired location.

PCI register offset: 104h
Register type: Read Only, Cleared by a Write of one
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-85. Uncorrectable Error Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	r	Reserved. Return zeros when read.
20	UR_ERROR	rcuh	Unsupported Request error. This bit is asserted when an Unsupported Request error is detected (i.e., when a request is received that results in the sending of a completion with an Unsupported Request status).
19	ECRC_ERROR	rcuh	Extended CRC error. This bit is asserted when an Extended CRC error is detected.
18	MAL_TLP	rcuh	Malformed TLP. This bit is asserted when a malformed TLP is detected.
17	RX_OVERFLOW	rcuh	Receiver Overflow. This bit is asserted when the flow control logic detects that the transmitting device has illegally exceeded the number of credits that were issued.
16	UNXP_CPL	rcuh	Unexpected Completion. This bit is asserted when a completion packet is received that does not correspond to an issued request.
15	CPL_ABORT	rcuh	Completer Abort. This bit is asserted when the completion to a pending request arrives with Completer Abort status.
14	CPL_TIMEOUT	rcuh	Completion Timeout. This bit is asserted when no completion has been received for an issued request before the timeout period.
13	FC_ERROR	rcuh	Flow Control error. This bit is asserted when a flow control protocol error is detected either during initialization or during normal operation.
12	PSN_TLP	rcuh	Poisoned TLP. This bit is asserted when an outgoing packet (request or completion) has been poisoned by setting the poison bit and has inverted the extended CRC attached to the end of the packet.
11:6	RSVD	r	Reserved. Return zeros when read.
5	SD_ERROR	rcuh	Surprise Down error. See Surprise Down ECN for a description of this error condition.
4	DLL_ERROR	rcuh	Data Link Protocol error. This bit is asserted if a data link layer protocol error is detected.
3:1	RSVD	r	Reserved. Return zeros when read.
0	Undefined	r	This value read from this bit is undefined.

4.3.67 Uncorrectable Error Mask Register

The Uncorrectable Error Mask register controls the reporting of individual errors as they occur. When a bit is set to one, the error status bits are still affected, but the error is not logged and no error reporting message is sent upstream.

PCI register offset: 108h

Register type: Read Only, Read/Write

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-86. Uncorrectable Error Mask Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	r	Reserved. Return zeros when read.
20	UR_ERROR_MASK	rwh	Unsupported Request error mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
19	ECRC_ERROR_MASK	rwh	Extended CRC error mask. 0 - Error condition is unmasked. 1 - Error condition is masked.

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Table 4-86. Uncorrectable Error Mask Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
18	MAL_TLP_MASK	rwh	Malformed TLP mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
17	RX_OVERFLOW_MASK	rwh	Receiver Overflow mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
16	UNXP_CPL_MASK	rwh	Unexpected Completion mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
15	CPL_ABORT_MASK	rwh	Completer Abort mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
14	CPL_TIMEOUT_MASK	rwh	Completion Timeout mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
13	FC_ERROR_MASK	rwh	Flow Control error mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
12	PSN_TLP_MASK	rwh	Poisoned TLP mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
11:6	RSVD	r	Reserved. Return zeros when read.
5	SD_MASK	rwh	Surprise Down error mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
4	DLL_ERROR_MASK	rwh	Data Link Protocol error mask. 0 - Error condition is unmasked. 1 - Error condition is masked.
3:1	RSVD	r	Reserved. Return zeros when read.
0	Undefined	r	This value read from this bit is undefined.

4.3.68 Uncorrectable Error Severity Register

The Uncorrectable Error Severity register controls the reporting of individual errors as ERR_FATAL or ERR_NONFATAL. When a bit is set, the corresponding error condition is identified as fatal. When a bit is clear, the corresponding error condition is identified as nonfatal.

PCI register offset: 10Ch
Register type: Read Only, Read/Write
Default value: 0003 2030h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0

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Table 4-87. Uncorrectable Error Severity Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	r	Reserved. Return zeros when read.
20	UR_ERROR_SEVR	rwh	Unsupported Request error severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
19	ECRC_ERROR_SEVR	rwh	Extended CRC error severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
18	MAL_TLP_SEVR	rwh	Malformed TLP severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
17	RX_OVERFLOW_SEVR	rwh	Receiver Overflow severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
16	UNXP_CPL_SEVR	rwh	Unexpected Completion severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
15	CPL_ABORT_SEVR	rwh	Completer Abort severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
14	CPL_TIMEOUT_SEVR	rwh	Completion Timeout severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
13	FC_ERROR_SEVR	rwh	Flow Control error severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
12	PSN_TLP_SEVR	rwh	Poisoned TLP severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
11:6	RSVD	r	Reserved. Return zeros when read.
5	SD_ERROR_SEVR	rwh	Surprise Down error severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
4	DLL_ERROR_SEVR	rwh	Data Link Protocol error severity. 0 - Error condition is signaled using ERR_NONFATAL. 1 - Error condition is signaled using ERR_FATAL.
3:1	RSVD	r	Reserved. Return zeros when read.
0	Undefined	r	This value read from this bit is undefined.

4.3.69 Correctable Error Status Register

The Correctable Error Status register reports the status of individual errors as they occur. Software may clear these bits only by writing a 1 to the desired location.

PCI register offset: 110h

Register type: Read Only, Cleared by a Write of one

Default value: 0000 0000h

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BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-88. Correctable Error Status Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	r	Reserved. Return zeroes when read.
13	ANFES	rcuh	Advisory nonfatal error status.
12	REPLAY_TMOUT	rcuh	Replay timer timeout. This bit is asserted when the replay timer expires for a pending request or completion that has not been acknowledged.
11:9	RSVD	r	Reserved. Return zeroes when read.
8	REPLAY_ROLL	rcuh	REPLAY_NUM rollover. This bit is asserted when the replay counter rolls over when a pending request of completion has not been acknowledged.
7	BAD_DLLP	rcuh	Bad DLLP error. This bit is asserted when an 8b/10n error is detected by the PHY during reception of a DLLP.
6	BAD_TLP	rcuh	Bad TLP error. This bit is asserted when an 8b/10b error is detected by the PHY during reception of a TLP.
5:1	RSVD	r	Reserved. Return zeros when read.
0	RX_ERROR	rcuh	Receiver error. This bit is asserted when an 8b/10b error is detected by the PHY at any time.

4.3.70 Correctable Error Mask Register

The Correctable Error Mask register controls the reporting of individual errors as they occur. When a bit is set to one, error status bits are still affected, but the error is not logged and no error reporting message is sent upstream.

PCI register offset: 114h
Register type: Read Only, Read/Write
Default value: 0000 2000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-89. Correctable Error Mask Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	r	Reserved. Return zeros when read.
13	ANFEM	rwh	Advisory nonfatal error mask. This bit is set by default to enable compatibility with software that does not comprehend role-based error reporting.
12	REPLAY_TMOUT_MASK	rwh	Replay timer timeout mask. 0 – Error condition is unmasked 1 – Error condition is masked
11:9	RSVD	r	Reserved. Return zeros when read.
8	REPLAY_ROLL_MASK	rwh	REPLAY_NUM rollover mask. 0 – Error condition is unmasked 1 – Error condition is masked

Table 4-89. Correctable Error Mask Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	BAD_DLLP_MASK	rwh	Bad DLLP error mask. 0 – Error condition is unmasked 1 – Error condition is masked
6	BAD_TLP_MASK	rwh	Bad TLP error mask. 0 – Error condition is unmasked 1 – Error condition is masked
5:1	RSVD	r	Reserved. Return zeros when read.
0	RX_ERROR_MASK	rwh	Receiver error mask. 0 – Error condition is unmasked 1 – Error condition is masked

4.3.71 Advanced Error Capabilities and Control Register

The Advanced Error Capabilities and Control register allows the system to monitor and control the advanced error reporting capabilities.

PCI register offset: 118h

Register type: Read Only, Read/Write

Default value: 0000 00A0h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0

Table 4-90. Advanced Error Capabilities and Control Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:9	RSVD	r	Reserved. Return zeros when read.
8	ECRC_CHK_EN	rwh	Extended CRC check enable. 0 – Extended CRC checking is disabled 1 – Extended CRC checking is enabled
7	ECRC_CHK_CAPABLE	r	Extended CRC check capable. This read-only bit returns a value of ‘1’ indicating that the bridge is capable of checking extended CRC information.
6	ECRC_GEN_EN	rwh	Extended CRC generation enable. 0 – Extended CRC generation is disabled 1 – Extended CRC generation is enabled
5	ECRC_GEN_CAPABLE	r	Extended CRC generation capable. This read-only bit returns a value of ‘1’ indicating that the bridge is capable of generating extended CRC information.
4:0	FIRST_ERR	rh	First error pointer. This five-bit value reflects the bit position within the Uncorrectable Error Status register corresponding to the class of the first error condition that was detected.

4.3.72 Header Log Register

The Header Log register stores the TLP header for the packet that lead to the most recently detected error condition. Offset 11Ch contains the first DWORD. Offset 128h contains the last DWORD (in the case of a 4DW TLP header).

PCI register offset: 11Ch – 128h

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Register type: Read only

Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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5 PCI Hot Plug Implementation Overview

5.1 PCI Hot Plug Architecture Overview

The PCI Express architecture is designed to natively support both hot-add and hot-removal (collectively Hot-Plug) of adapters. The architecture also provides a 'toolbox' of mechanisms that allow different user/operator models to be supported using a self-consistent infrastructure. PCI Express defines the registers necessary to support the integration of a PCI Hot Plug controller within individual root and switch ports. Under PCI Hot-Plug software control, the PCI Hot-Plug controllers and the associated port interface within the root or switch port must control the card interface signals to ensure orderly power-down and power-up as cards are removed and replaced.

Table 5-1. GPIO Matrix

GPIO[#]	0	1	2	3		4	5	6	7		8	9	10	11		12	13	14	15	16
$\overline{\text{PRSNT1}}$	**S**																			
$\overline{\text{PWRON1}}$		**S**																		
PWRGD1			**S**																	
$\overline{\text{CLKREQ1}}$				2																
$\overline{\text{MRLSDET1}}$				3				6	6				6	6						
$\overline{\text{ACTLED1}}$																2	2	2		
$\overline{\text{PWRLED1}}$							6					6				5		5		
$\overline{\text{ATNLED1}}$							4					4					5		2	2
$\overline{\text{ATNBTN1}}$						2		2			2		2							
$\overline{\text{PWRFLT1}}$						4		4	4		4		4	4					5	5
EMILCTL1							2					2								
EMILENG1						6					6									
$\overline{\text{PRSNT2}}$						**S**														
$\overline{\text{PWRON2}}$							**S**													
PWRGD2								**S**												
$\overline{\text{CLKREQ2}}$									2											
$\overline{\text{MRLSDET2}}$			6	6					3				7	7						
$\overline{\text{ACTLED2}}$																3	3	3		
$\overline{\text{PWRLED2}}$		6										7					6	6		
$\overline{\text{ATNLED2}}$		4										5				6			3	3
$\overline{\text{ATNBTN2}}$	2		2								3		3							
$\overline{\text{PWRFLT2}}$	4		4	4							5		5	5					6	6
EMILCTL2		2										3								
EMILENG2	6										7									
$\overline{\text{PRSNT3}}$											**S**									
$\overline{\text{PWRON3}}$												**S**								
PWRGD3													**S**							
$\overline{\text{CLKREQ3}}$														2						
$\overline{\text{MRLSDET3}}$			7	7				7	7					3						
$\overline{\text{ACTLED3}}$																4	4	4		
$\overline{\text{PWRLED3}}$		7					7										7		4	
$\overline{\text{ATNLED3}}$		5					5									7				4
$\overline{\text{ATNBTN3}}$	3		3			3		3												
$\overline{\text{PWRFLT3}}$	5		5	5		5		5	5									7	7	7
EMILCTL3		3					3													

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Table 5-1. GPIO Matrix (continued)

GPIO[#]	0	1	2	3		4	5	6	7		8	9	10	11		12	13	14	15	16
EMILENG3	7					7														

In Table 2-11, **S** indicates a strapping option. If the appropriate DNn_DPSTRP pin is pulled high, the GPIO is mapped to this value and is no longer mapped by the GPIO Control register.

Each downstream port of the XIO3130 is assigned one dedicated sideband pin, $\overline{\text{DNn_PERST}}$. Three additional sideband pins may be dedicated to each port for PCI Hot Plug support. The DNn_DPSTRP pins are set for the corresponding ports to indicate support for PCI Hot Plug. When the DNn_DPSTRP pin strapping defines a GPIO pin as a PCI Hot Plug support pin, that pin is associated with the Slot Capability, Slot Status, and Slot Control registers of the corresponding downstream port. These registers are defined in sections Section 4.3.55, Section 4.3.56, and Section 4.3.57, respectively. When the DPSTRP[2:0] pin strapping defines a GPIO pin as a GPIO pin, that pin is mapped to a bit field in the GPIO Configuration registers and Data register. These registers are defined in section Section 4.2.61 through Section 4.2.65.

Table 5-2. PCI Hot Plug Sideband Signals

Signal	I/O	Function
$\overline{\text{Dn_PERST}}$	O	Port n PE Reset. The PCI Hot Plug card or device is held in a reset state when this signal is low.
$\overline{\text{PRSNTn}}$	I	Port n Present. A PCI Hot Plug card or device is attached to a port when this signal is low. This signal is reported in the PDC bit of the Slot Status register. When this signal is in a de-asserted high state, the $\overline{\text{DNn_PERST}}$ pin is asserted low, REFCLK is disabled, and $\overline{\text{PWRONn}}$ is de-asserted high.
$\overline{\text{PWRONn}}$	O	Port n Power On. Power is applied to the PCI Hot Plug card or device attached to the port when this signal is low.
PWRGDn	I	Port n Power Good: The power to the PCI Hot Plug card or device is adequate and it is alright to enable REFCLK to the card or device and de-assert $\overline{\text{DNn_PERST}}$. When this signal transitions to a low state, the XIO3130 switch asserts $\overline{\text{DNn_PERST}}$ low and turns off REFCLK.

Additional GPIO pins may be allocated to PCI Hot Plug support via programming by assigning the pins to PCI Hot Plug pin functionality in the GPIO Control registers defined in sections Section 4.2.62 through Section 4.2.65.

Table 5-3. Pins Assigned to GPIO Control Registers

Signal	I/O	Function
$\overline{\text{CLKREQn}}$	I	Port n CLK REQ. This signal is used to disable the clock during normal operation. If $\overline{\text{PWRONn}}$ is high or $\overline{\text{PRSNTn}}$ is high or PWRGDn is low, this signal is ignored by the XIO3130.
$\overline{\text{ACT_LEDn}}$	O	Port n Activity. This pin toggles at anytime activity is detected on the port interface. Otherwise, this pin is high.
$\overline{\text{PWR_LEDn}}$	O	Port n Power Indicator: See PI_CTL bit field in Slot Control register (section Section 4.3.56).
$\overline{\text{ATN_LEDn}}$	O	Port n Attention Indicator: See AI_CTL bit field in Slot Control register (section Section 4.3.56).
$\overline{\text{ATN_BTNn}}$	I	Port n Attention Push button: See ABP bit field in Slot Status register (section Section 4.3.57).
$\overline{\text{MRLS_DETn}}$	I	Port n Manually-Operated Retention Latch (MRL): See MRLSS bit field in Slot Status register (section Section 4.3.57).
EMIL_CTLn	O	Port n Electromechanical Interlock: See EMIL_CTL bit field in Slot Control register (section Section 4.3.56).
EMIL_ENGn	I	Port n Electromechanical Interlock status: See EMIL_STAT bit field in Slot Status register (section Section 4.3.57).

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5.2 PCI Hot Plug Timing

5.2.1 Power-Up Cycle

The XIO3130 switch can be powered up numerous ways depending on the way the DPSTRP[2:0] strapping defines the port. The different power-up cycles are: nonPCI Hot Plug power-up cycle, PCI Hot Plug power-up cycle with PWRGDn feedback, and PCI Hot Plug power-up cycle without PWRGDn feedback.

5.2.1.1 NonPCI Hot Plug Power-Up Cycle

For nonPCI Hot Plug power-up cycles, there are no $\overline{\text{PWRONn}}$, PWRGDn, or $\overline{\text{PRSNTn}}$ signals, and the Slot Control register is not used to power the port up. As soon as the REFCLKn output is stable on the port, the $\overline{\text{PERSTn}}$ signal is de-asserted high. If no device is detected on the port before Link Training times out, the $\overline{\text{PERSTn}}$ signal is asserted low and REFCLKn is disabled.

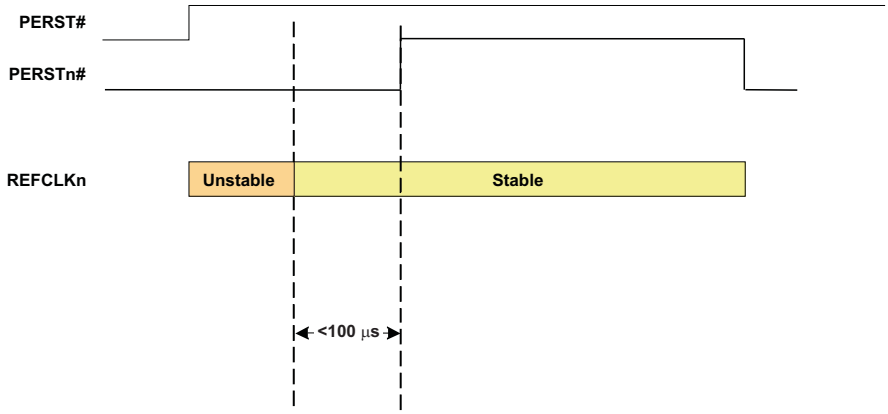

Figure 5-1. NonPCI Hot Plug Power-Up Cycle

5.2.1.2 PCI Hot Plug Power-Up Cycle With PWRGDn Feedback

For PCI Hot Plug power up cycles with PWRGDn feedback, the $\overline{\text{PWRONn}}$ signal going low gates the power-up cycle. The XIO3130 switch asserts $\overline{\text{PWRONn}}$ and waits for the PWRGDn signal to transition high, indicating that power to the slot is now stable. When PWRGDn goes high, REFCLKn is enabled and a 100 ms time-out starts. After the 100 ms time-out completes, $\overline{\text{PERSTn}}$ is de-asserted. If the port has been programmed (see GPIO Control Registers in sections Section 4.2.61 through Section 4.2.64) to have a $\overline{\text{CLKREQn}}$ input when $\overline{\text{PERSTn}}$ de-asserts high, REFCLKn is disabled when $\overline{\text{CLKREQn}}$ is not low.

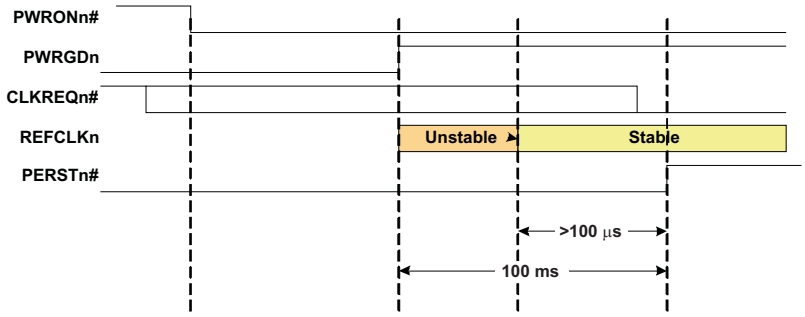

Figure 5-2. PCI Hot Plug Power-Up Cycle With PWFRDn Feedback

5.2.1.3 PCI Hot Plug Power-Up Cycle With No PWRGDn Feedback

This application requires the PWRGDn signal to be tied high. The $\overline{\text{PWRONn}}$ signal going low gates the

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power-up cycle. The XIO3130 switch asserts PWRONn and because the PWRGDn signal is tied high, the power-up cycle starts as soon as PWRONn is asserted. After 100 ms, REFCLKn is enabled, and a 100 ms time-out starts. After the 100 ms time-out completes, PERSTn is de-asserted. If the port has been programmed (see GPIO Control registers in sections Section 4.2.61 through Section 4.2.64) to have a CLKREQn input when PERSTn de-asserts high, REFCLKn is disabled when CLKREQn is not low.

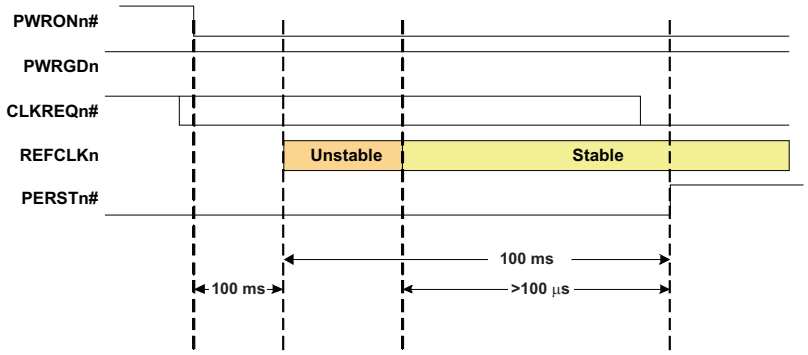

Figure 5-3. PCI Hot Plug Power-Up Cycle With No PWGRDn Feedback

5.2.2 Power-Down Cycles

Various conditions cause the assertion of PERSTn, which also cause REFCLKn to stop a short time later.

5.2.2.1 Normal Power-Down

For PCI Hot Plug ports, other conditions may also power-down the port. Software can power the port down by de-asserting the PC_CTL bit in the Slot Control register. This invokes a normal power-down cycle, which is the same power-down cycle invoked by the upstream PERST being asserted.

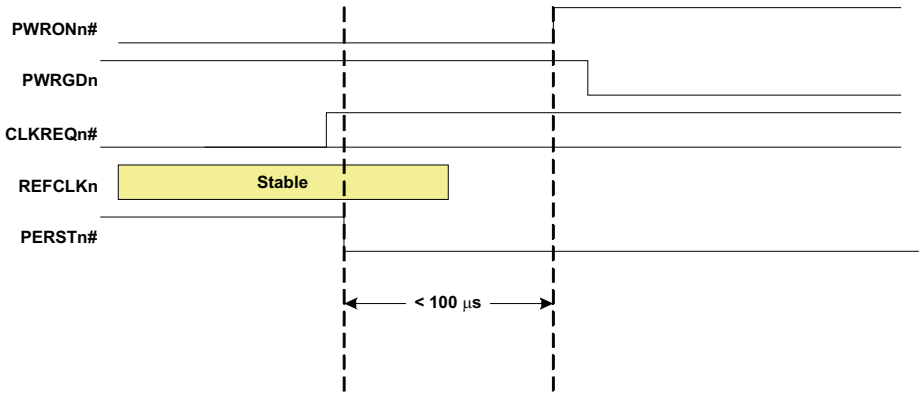

Figure 5-4. Normal Power-Down

5.2.2.2 Surprise Removal

Another PCI Hot Plug Port power-down condition occurs when the PRSNTn pin is de-asserted, indicating that the card or device has been removed without warning (i.e., surprise removal).

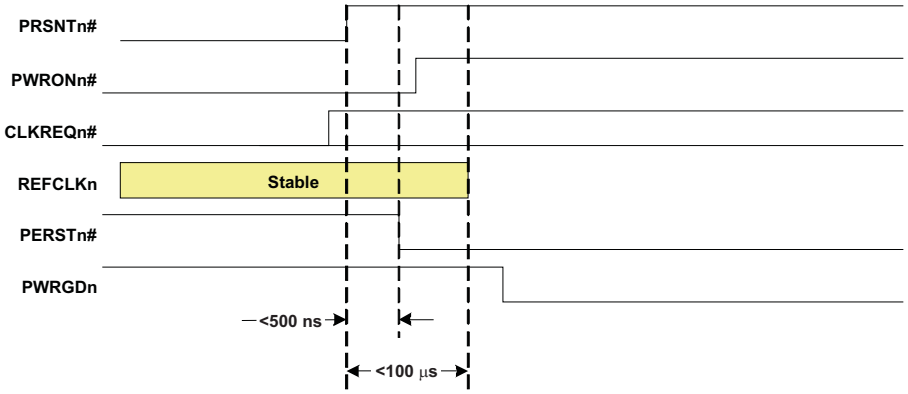

Figure 5-5. Surprise Removal

In the case of surprise removal, the XIO3130 switch de-asserts $\overline{\text{PERST}}$ within 500 ns after a de-bounced $\overline{\text{PRSNTn}}$ de-asserted state exists. Then REFCLKn is disabled, and the $\overline{\text{PWRONn}}$ signal is de-asserted within 100 µs.

5.2.2.3 PWRGDn De-Assertion

Another situation that forces a PCI Hot Plug port to power-down is the de-assertion of $\overline{\text{PWRGDn}}$. If $\overline{\text{PWRGDn}}$ is de-asserted, the XIO3130 switch disables REFCLKn but does not de-assert $\overline{\text{PWRONn}}$.

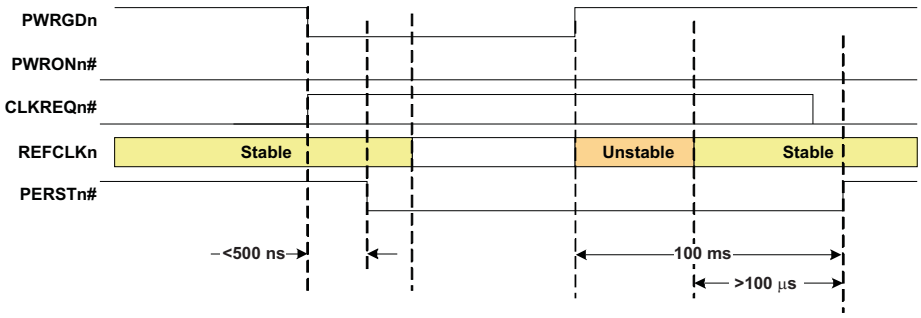

Figure 5-6. Effect When PWFRGn Goes Low

Note that once $\overline{\text{PERSTn}}$ goes low, it must remain low for at least 100 ms.

5.2.3 PMI_Turn_Off and PME_To_Ack Messages

For information on the PME_Turn_Off and PME_To_Ack messages, see section Section 3.2.6.

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5.2.4 Debounce Circuits

Integrated de-bounce circuits are provided for the following input pins:

- $\overline{\text{PRSNT}}$[2:0] present detects for each downstream port; used with PCI Express or ExpressCard (formerly NEWCARD) slots.
- $\overline{\text{ATN_BTN}}$[2:0], which are attention button inputs, are MUXed onto GPIO pins; de-bounce is only needed when the relevant GPIO pins are programmed to this mode.
- $\overline{\text{MRLS_DET}}$[2:0], which are manual retention latch detection inputs, are MUXed onto GPIO pins; de-bounce is only needed when the relevant GPIO pins are programmed to this mode.

A timeout of approximately 10 ms is used.

5.2.5 $\overline{\text{HP_INTX}}$ Pin

The $\overline{\text{HP_INTX}}$ output signal is asserted when a PCI Hot Plug interrupt occurs within the switch, but only asserted due to PCI Hot Plug events. This signal is typically be connected on system boards to an SCI (System Control Interrupt) input, which invokes an interrupt service routine included in the system BIOS; other system implementations may connect $\overline{\text{HP_INTX}}$ to a PCI bus interrupt pin.

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6 Electrical Characteristics

This chapter describes the electrical characteristics of the XIO3130.

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
VDDRC, VAUX33REF, VDD33REF	Supply voltage range		–0.5 to 3.6	V
VDDAREF, VDDA, VDDD, VDD15			–0.5 to 1.65	V
V_I	Input voltage range	PCI Express (PER)	–0.6 to 0.6	V
		PCI Express REFCKI (differential)	–0.5 to V_{DD_15}	V
		Miscellaneous 3.3 – V_{IO}	–0.5 to V_{DD_33}	V
V_O	Output voltage range	PCI Express (PET)	–0.5 to V_{DD_15}	V
		PCI Express REFCKO	–0.5 to V_{DD_15}	V
		Miscellaneous 3.3 – V_{IO}	–0.5 to V_{DD_33}	V
	Input clamp current, (V_I < 0 or V_I > V_{DD})(2)		±20	mA
	Output clamp current, (V_O < 0 or V_O > V_{DD})(3)		±20	mA
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) Applies to external input. V_I < 0 or V_I > V_{DD}.
(3) Applies to external output. V_O < 0 or V_O > V_{DD}.

6.2 Recommended Operating Conditions

			OPERATION	MIN	NOM	MAX	UNIT
VDDD	Supply voltage		1.5 V	1.35	1.5	1.65	V
VDD15							
VDDAREF							
VDDA							
VDDRC	Supply voltage		3.3 V	3	3.3	3.6	V
VDD33							
VAUX33REF							
VDD33REF							
T_A	Operating ambient temperature range	XIO3130		0	25	70	°C
		XIO3130I		–40		85	
T_J	Virtual junction temperature(1)	XIO3130		0	25	105	°C
		XIO3130I		–40		105	

(1) The junction temperature reflects simulated conditions. The customer is responsible for verifying junction temperature.

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6.3 PCI Express Differential Transmitter Output Ranges

PARAMETER	TERMINALS	MIN	NOM	MAX	UNIT	COMMENTS
UI Unit interval	PETP, PETN	399.88	400	400.12	ps	Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations.See (1)
$V_{TX-DIFFp-p}$ Differential peak-to-peak output voltage	PETP, PETN	0.8		1.2	V	$V_{TX-DIFFp-p} = 2*\|V_{TXP} – V_{TXN}\|$. See (2)
$V_{TX-DE-RATIO}$ De-emphasized differential output voltage (ratio)	PETP, PETN	–3	–3.5	–4.0	dB	This value is the ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See (2)
T_{TX-EYE} Minimum TX eye width	PETP, PETN	0.75			UI	The maximum transmitter jitter can be derived as $T_{TXMAX-JITTER} = 1 – T_{TX-EYE} = 0.25$ UI. See (2) (3)
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ Maximum time between the jitter median and maximum deviation from the median	PETP, PETN			0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to recovered TX UI. A recovered TX UI is calculated over 3500 consecutive UIs of sample data. Jitter is measured using all edges of the 250 consecutive UIs in the center of the 3500 UIs that are used for calculating the TX UI. See (2) (3)
$T_{TX-RISE}$, $T_{TX-FALL}$ Differential TX output rise/fall time	PETP, PETN	0.125			UI	See (2) (4)
$V_{TX-CM-ACp}$ RMS ac peak common mode output voltage	PETP, PETN			20	mV	$V_{TX-CM-ACp} = RMS(\|V_{TXP} + V_{TXN}\|/2 – V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TXP} + V_{TXN}\|/2$ See (2)
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$ Absolute delta of DC common mode voltage during L0 and electrical idle.	PETP, PETN	0		100	mV	$\|V_{TX-CM-DC} – V_{TX-CM-IDLE-DC}\| \le 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TXP} + V_{TXN}\|/2$ [during L0] $V_{TX-CM-IDLE-DC} = DC_{(avg)}$ of $\|V_{TXP} + V_{TXN}\|/2$ [during electrical idle] See (2)
$V_{TX-CM-DC-LINE-DELTA}$ Absolute delta of DC common mode voltage between P and N	PETP, PETN	0		25	mV	$\|V_{TXP-CM-DC} – V_{TXN-CM-DC}\| \le 25$ mV when $V_{TXP-CM-DC} = DC_{(avg)}$ of $\|V_{TXP}\|$ $V_{TXN-CM-DC} = DC_{(avg)}$ of $\|V_{TXN}\|$ See (2)
$V_{TX-IDLE-DIFFp}$ Electrical idle differential peak output voltage	PETP, PETN	0		20	mV	$V_{TX-IDLE-DIFFp} = \|V_{TXP-IDLE} – V_{TXN-IDLE}\| \le 20$ mV See (2)
$V_{TX-RCV-DETECT}$ The amount of voltage change allowed during receiver detection	PETP, PETN			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present.
$V_{TX-DC-CM}$ The TX DC common mode voltage	PETP, PETN	0		3.6	V	The allowed DC common mode voltage under any condition
$I_{TX-SHORT}$ TX short circuit current limit	PETP, PETN			90	mA	The total current that the transmitter can provide when shorted to its ground.
$T_{TX-IDLE-MIN}$ Minimum time spent in electrical idle	PETP, PETN	50			UI	Minimum time that a transmitter must be in electrical Idle. The receiver uses this value to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set.
$T_{TX-IDLE-SET-to-IDLE}$ Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	PETP, PETN			20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a de-bounce time for the transmitter to meet electrical idle after transitioning from L0.

(1) No test load is necessarily associated with this value.
(2) Specified at the measurement point into a timing and voltage compliance test load and measured over any 250 consecutive TX UIs.
(3) A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
(4) Measured between 20% and 80% at transmitter package terminals into a test load for both VTX-D+ and VTX-D–.

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PCI Express Differential Transmitter Output Ranges *(continued)*

PARAMETER	TERMINALS	MIN	NOM	MAX	UNIT	COMMENTS
$T_{TX-IDLE-to-DIFF-DATA}$ Maximum time to transition to valid TX specifications after leaving an electrical idle condition	PETP, PETN			20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This value is considered a de-bounce time for the TX to meet all TX specifications after leaving electrical idle.
$RL_{TX-DIFF}$ Differential return loss	PETP, PETN	10			dB	Measured over 50 MHz to 1.25 GHz. See (5)
RL_{TX-CM} Common mode return loss	PETP, PETN	6			dB	Measured over 50 MHz to 1.25 GHz. See (5)
$Z_{TX-DIFF-DC}$ DC differential TX impedance	PETP, PETN	80	100	120	Ω	TX DC differential mode low impedance
Z_{TX-DC} Transmitter DC impedance	PETP, PETN	40			Ω	Required TX-D+ as well as TX-D– DC impedance during all states
C_{TX} AC coupling capacitor	PETP, PETN	75		200	nF	All transmitters are AC-coupled and capacitors are required on the PWB.

(5) The transmitter input impedance results in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the P and N lines. Note that the series capacitors CTX is optional for the return loss measurement.

6.4 PCI Express Differential Receiver Input Ranges

PARAMETER	TERMINALS	MIN	NOM	MAX	UNIT	COMMENTS
$V_{RX-DIFFp-p}$ Differential input peak-to-peak voltage	PERP, PERN	0.175		1.2	V	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} – V_{RX-D–}\|$ See (1)
T_{RX-EYE} Minimum receiver eye width	PERP, PERN	0.4			UI	The maximum interconnect media and transmitter jitter that can be tolerated by the Receiver is derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = .6$ UI See (1) (2) (3)
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ Maximum time between the jitter median and maximum deviation from the median.	PERP, PERN			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See (1) (2)
$V_{RX-CM-ACp}$ AC peak common mode input voltage	PERP, PERN			150	mV	$V_{RX-CM-ACp}$ = RMS($\|V_{RX-D+} + V_{RX-D–}\| / 2 – V_{RX-CM-DC}$) $V_{RX-CM-DC} = DC_{(avg)}$ of $\|V_{RX-D+} + V_{RX-D-}\| / 2$ See (1)

(1) Specified at the measurement point and measured using the clock recovery function specified in *PCI Express™ Base Specification Revision 1.1*, Section 4.3.3.2. The test load in Figure 4-25 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 4-26 of the specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as a reference for the eye diagram.

(2) The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.64. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. The RX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as the reference for the eye diagram. This parameter is measured with the equivalent of a zero jitter reference clock. The T_{RX-EYE} measurement is to be met at the target bit error rate. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification is to be met using the compliance pattern at a sample size of 1,000,000 UI.

(3) See the PCI Express Jitter and BER white paper for more details on the Rx-Eye measurement.

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PCI Express Differential Receiver Input Ranges *(continued)*

PARAMETER	TERMINALS	MIN	NOM	MAX	UNIT	COMMENTS
$RL_{RX-DIFF}$ Differential return loss	PERP, PERN	10			dB	Measured over 50 MHz to 1.25 GHz with the P and N lines biased at +300 mV and –300 mV, respectively. See (4)
RL_{RX-CM} Common mode return loss	PERP, PERN	6			dB	Measured over 50 MHz to 1.25 GHz with the P and N lines biased at +300 mV and –300 mV, respectively. See (4).
$Z_{RX-DIFF-DC}$ DC differential input impedance	PERP, PERN	80	100	120	Ω	RX DC differential mode impedance. See (5).
Z_{RX-DC} DC input impedance	PERP, PERN	40	50	60	Ω	Required RX-D+ as well as RX-D– DC impedance (50 Ω ±20% tolerance). See (1) and (5).
$Z_{RX-HIGH-IMP-DC}$ Powered-down DC input impedance	PERP, PERN	200K			Ω	Required RX-D+ as well as RX-D– DC impedance when the receiver terminations do not have power. See (6).
$V_{RX-IDLE-DET-DIFFp-p}$ Electrical idle detect threshold	PERP, PERN	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 * \lvert V_{RX-D+} - V_{RX-D-} \rvert$ measured at the receiver package pins
$T_{RX-IDLE-DET-DIFF-ENTER-TIME}$ Unexpected electrical idle enter detect threshold integration time	PERP, PERN			10	ms	An unexpected electrical idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTER-TIME}$ to signal an unexpected idle condition.

(4) The Receiver input impedance shall result in a differential return loss greater than or equal to 10 dB with a differential test input signal of no less than 200 mV (peak value, 400 mV differential peak to peak) swing around ground applied to D+ and D– lines and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (i.e., as measured by a Vector Network Analyzer with 50 Ω probes; see Figure 4-25 in the specification). Note that the series capacitors CTX is optional for the return loss measurement.

(5) Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

(6) The RX DC common mode impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 200 mV above the RX ground.

6.5 PCI Express Differential Reference Clock Input Ranges(1)

PARAMETER	TERMINALS	MIN	NOM	MAX	UNIT	COMMENTS
$f_{IN-DIFF}$ Differential input frequency	REFCKIp REFCKIn		100		MHz	The input frequency is 100 MHz +300 ppm and –2800 = ppm including SSC-dictated variations.
$V_{RX-DIFFp-p}$ Differential input peak-to-peak voltage	REFCKIp REFCKIn	0.175		1.2	V	$V_{RX-DIFFp-p} = 2*\lvert V_{REFCKp} - V_{REFCKn} \rvert$
$V_{RX-CM-ACp}$ AC peak common mode input voltage	REFCKIp REFCKIn			140	mV	$V_{RX-CM-ACp} = RMS(\lvert V_{REFCKp} + V_{REFCKn} \rvert/2 - V_{RX-CM-DC})$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{REFCKp} + V_{REFCKn} \rvert/2$
Duty cycle	REFCKIp REFCKIn	40%		60%		Differential waveform input duty cycle
$Z_{RX-DIFF-DC}$ DC differential input impedance	REFCKIp REFCKIn		20		kΩ	REFCKIp/ REFCKIn DC differential mode impedance

(1) The XIO3130 is compliant with the defined system jitter models for a PCI Express reference clock and associated TX/RX link. These system jitter models are described in the *PCI Express Jitter Modeling, Revision 1.0RD* document. Any usage of the XIO3130 in a system configuration that does not conform to the defined system jitter models requires the system designer to validate the system jitter budgets.

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6.6 PCI Express Reference Clock Output Requirements

SYMBOL	PARAMETER	100-MHz INPUT		UNIT	NOTES
		MIN	MAX		
Rise Edge Rate	Rising edge rate	0.6	4	V/ns	See (1) and (2).
Fall Edge Rate	Falling edge rate	0.6	4	V/ns	See (1) and (2).
V_{IH}	Differential input high voltage	150		mV	See (1).
V_{IL}	Differential input low voltage		–150	mV	See (1).
V_{CROSS}	Absolute crossing point voltage	250	550	mV	See Notes (3), (4), and (5).
$R_{CROSS\ DELTA}$	Variation of V_{CROSS} over all rising clock edges		140	mV	See Notes (3), (4), and (6).
V_{RB}	Ring-back voltage margin	–100	100	mV	See (1) and (7).
T_{STABLE}	Time before V_{RB} is allowed	500		ps	See (1) and (7).
$T_{PERIOD\ AVG}$	Average clock period accuracy	–300	2800	ppm	See Notes (1), (8), and (9).
$T_{PERIOD\ ABS}$	Absolute period (including jitter and spread spectrum)	9.847	10.203	ns	See (1) and (10).
$T_{CCJITTER}$	Cycle-to-cycle jitter		150	ps	See (1).
V_{MAX}	Absolute maximum input voltage		1.15	V	See (3) and (11).
V_{MIN}	Absolute minimum input voltage		–0.3	V	See (3) and (12).
Duty Cycle	Duty cycle	40	60	%	See (1).
Rise-Fall Matching	Rising edge rate (REFCKOp) to falling edge rate (REFCKOn) matching		20	%	See (3) and (13).
Z_{C-DC}	Clock source DC impedance	40	60	Ω	See (3) and (14).

(1) Measurement taken from differential waveform.
(2) Measured from –150 mV to +150 mV on the differential waveform (derived from REFCKOp minus REFCKOn). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
(3) Measurement taken from single-ended waveform.
(4) Measured at crossing point where the instantaneous voltage value of the rising edge of REFCKOp equals the falling edge of REFCKOn.
(5) Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
(6) Defined as the total variation of all crossing voltages of rising REFCKOp and falling REFCKOn. This is the maximum allowed variance in VCROSS for any particular system.
(7) TSTABLE is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100 mV differential range.
(8) Refer to Section 4.3.2.1 of the *PCI Express Base Specification, Revision 1.1* for information regarding PPM considerations.
(9) PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For 300 PPM then we have a error budget of 100 Hz/PPM * 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 PPM applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500 PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800 PPM.
(10) Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative PPM tolerance, and spread spectrum modulation.
(11) Defined as the maximum instantaneous voltage including overshoot.
(12) Defined as the minimum instantaneous voltage including undershoot.
(13) Matching applies to rising edge rate for REFCKOp and falling edge rate for REFCKOn. It is measured using a ±75 mV window centered on the median cross point where REFCKOp rising meets REFCKOn falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCKOp should be compared to the Fall Edge Rate of REFCKOn, the maximum allowed difference should not exceed 20% of the slowest edge rate.
(14) System board compliance measurements must use the recommended test load card. REFCKOp and REFCKOn are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL = 2 pF.

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6.7 3.3-V I/O Electrical Characteristics(1)

PARAMETER		OPERATIONS	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage(2)	V_{DD33}		0.7 V_{DD33}	V_{DD33}	V
V_{IL}	Low-level input voltage(2)	V_{DD33}		0	0.3 V_{DD33}	V
V_I	Input voltage			0	V_{DD33}	V
V_O	Output voltage(3)			0	V_{DD33}	V
t_π	Input transition time (trise and tfall)			0	25	ns
V_{hys}	Input hysteresis(4)				0.13 V_{DD33}	V
V_{OH}	High-level output voltage	V_{DD33}	I_{OH} = –4 mA	0.8 V_{DD33}		V
V_{OL}	Low-level output voltage	V_{DD33}	I_{OL} = 4 mA		0.22 V_{DD33}	V
I_{OZ}	High-impedance, output current (3)	V_{DD33}	V_I = 0 to VDD33		±20	µA
I_{OZP}	High-impedance, output current with internal pullup or pulldown resistor (5)	V_{DD33}	V_I = 0 to VDD33		±175	µA
I_I	Input current (6)	V_{DD33}	V_I = 0 to VDD33		±1	µA

(1) This table applies to $\overline{\text{PERST}}$, $\overline{\text{WAKE}}$, REFCLK_SEL, $\overline{\text{GRST}}$, and GPIO18:0.
(2) Applies to external inputs and bidirectional buffers.
(3) Applies to external outputs and bidirectional buffers.
(4) Applies to $\overline{\text{PERST}}$ and $\overline{\text{GRST}}$.
(5) Applies to $\overline{\text{GRST}}$ (pullup resistor) and most GPIO (pullup resistor).
(6) Applies to external input buffers.

6.8 POWER CONSUMPTION(1)

PARAMETER	MIN	NOM(2)	MAX(3)	UNIT
$I_{3.3V}$		11.21	20.61	mA
$I_{1.5V}$		578.7	725.8	mA
$P_{3.3V}$		36.99	68.01	mW
$P_{1.5V}$		868.05	1088.7	mW
I_{AUX} (4)		5.28		mA

(1) Measurements taken at 25°C with nominal power supply, 3.3 V and 1.5 V.
(2) Nominal conditions are defined as switch only power, no devices downstream, and downstream clocks not running.
(3) Maximum power conditions are defined as three downstream devices constantly running traffic and downstream clocks running.
(4) Measurement performed with three devices downstream, system in S5.

6.9 THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS(1)		TYP	UNIT
θ_{JA}	Junction-to-free-air thermal resistance	Low K JEDEC test board, 1s (single-signal layer), no air flow		51.2	°C/W
		High K JEDEC test board, 2s2p (double-signal layer, double buried power plane)	No air flow	30.5	
			400 LFM	17.7	
			200 LFM	14.7	
θ_{JC}	Junction-to-case thermal resistance	Cu cold plate measurement process		7	°C/W
θ_{JB}	Junction-to-board thermal resistance	EIA/JESD 51-8		13.9	°C/W
Ψ_{JT}	Junction-to-top of package	EIA/JESD 51-2		0.5	°C/W
Ψ_{JB}	Junction-to-board	EIA/JESD 51-6		12	°C/W

(1) For more details, refer to TI application report *IC Package Thermal Metrics* (literature number SPRA953).

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XIO3130IZHC	ACTIVE	BGA MICROSTAR	ZHC	196	126	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	XIO3130I	Samples
XIO3130ZHC	ACTIVE	BGA MICROSTAR	ZHC	196	126	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 70	XIO3130	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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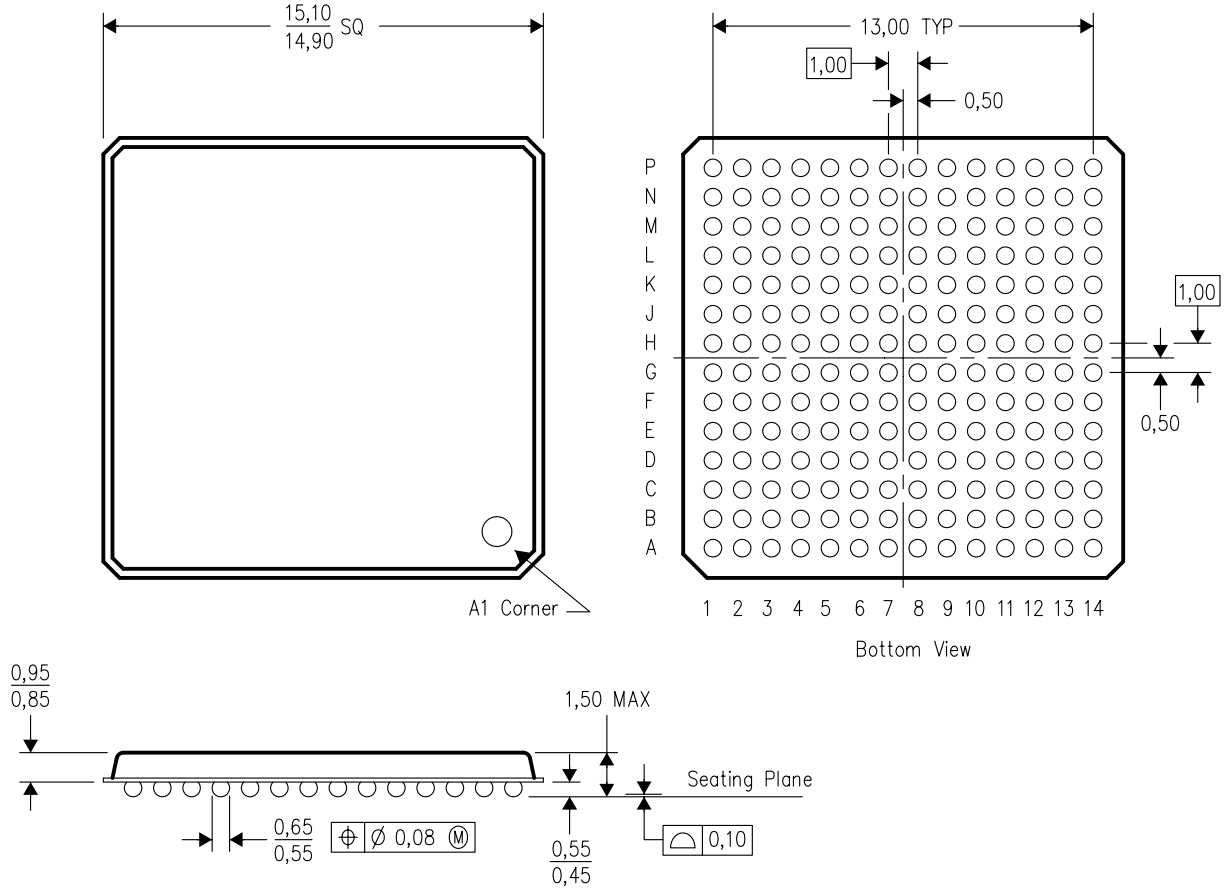
ZHC (S–PBGA–N196) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Micro Star BGA configuration
D. This is a lead–free solder ball design.

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