



**THE DATASHEET OF
74LVTH16543DGGRE4**

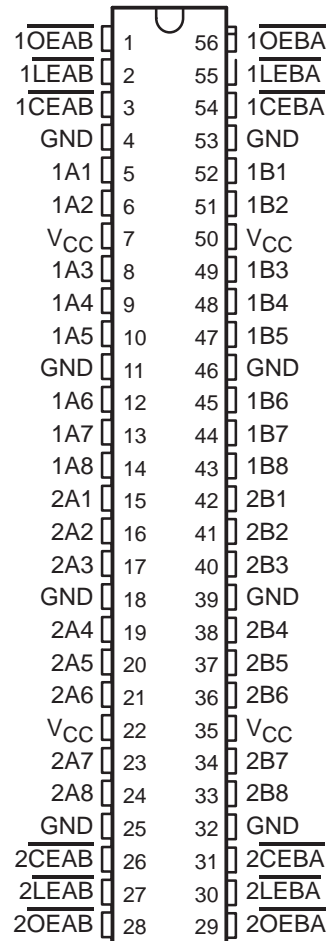


SN54LVTH16543, SN74LVTH16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS699D – JULY 1997 – REVISED APRIL 1999

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16543 . . . WD PACKAGE
SN74LVTH16543 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The LVTH16543 devices are 16-bit registered transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (\overline{CEAB}) input must be low to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.



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 **TEXAS
INSTRUMENTS**

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SN54LVTH16543, SN74LVTH16543

3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS

WITH 3-STATE OUTPUTS

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description (continued)

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH16543 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16543 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†
(each 8-bit section)

| INPUTS | | | | OUTPUT |
|-------------------|-------------------|-------------------|---|------------------|
| \overline{CEAB} | \overline{LEAB} | \overline{OEAB} | A | B |
| H | X | X | X | Z |
| X | X | H | X | Z |
| L | H | L | X | B_0^{\ddagger} |
| L | L | L | L | L |
| L | L | L | H | H |

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .

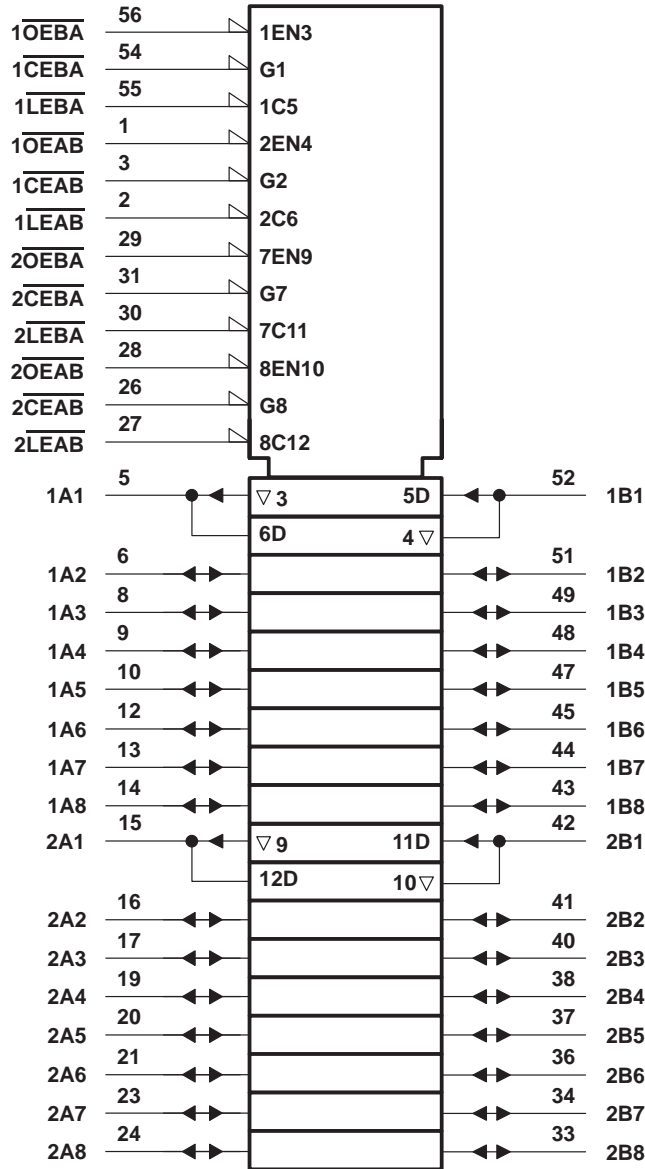
‡ Output level before the indicated steady-state input conditions were established



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logic symbol†



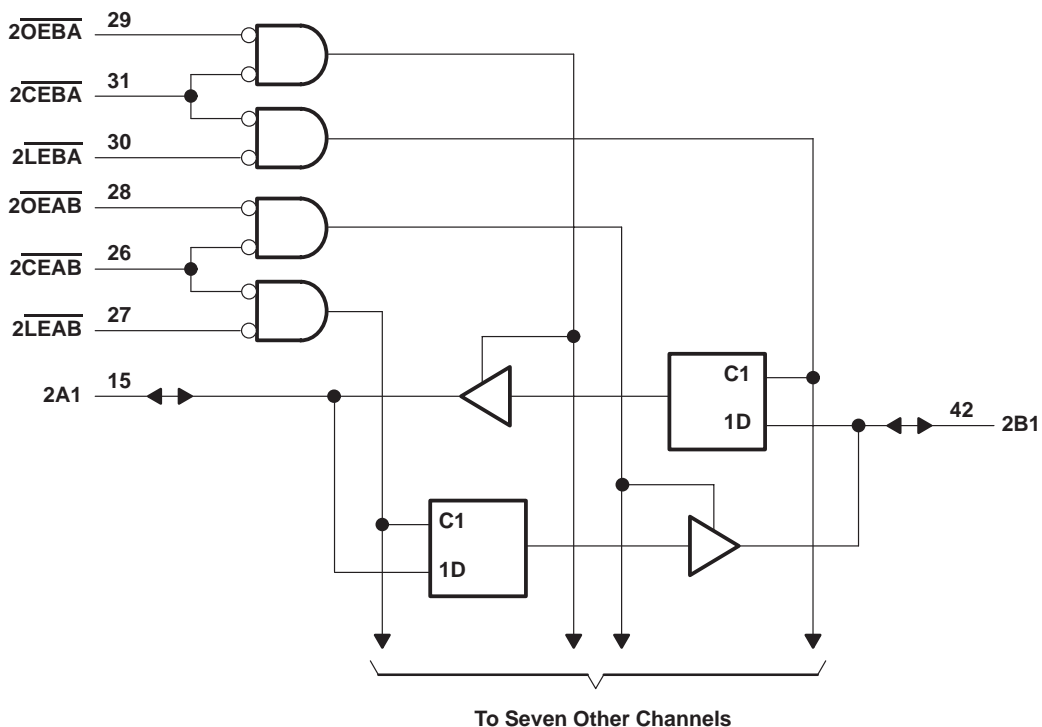
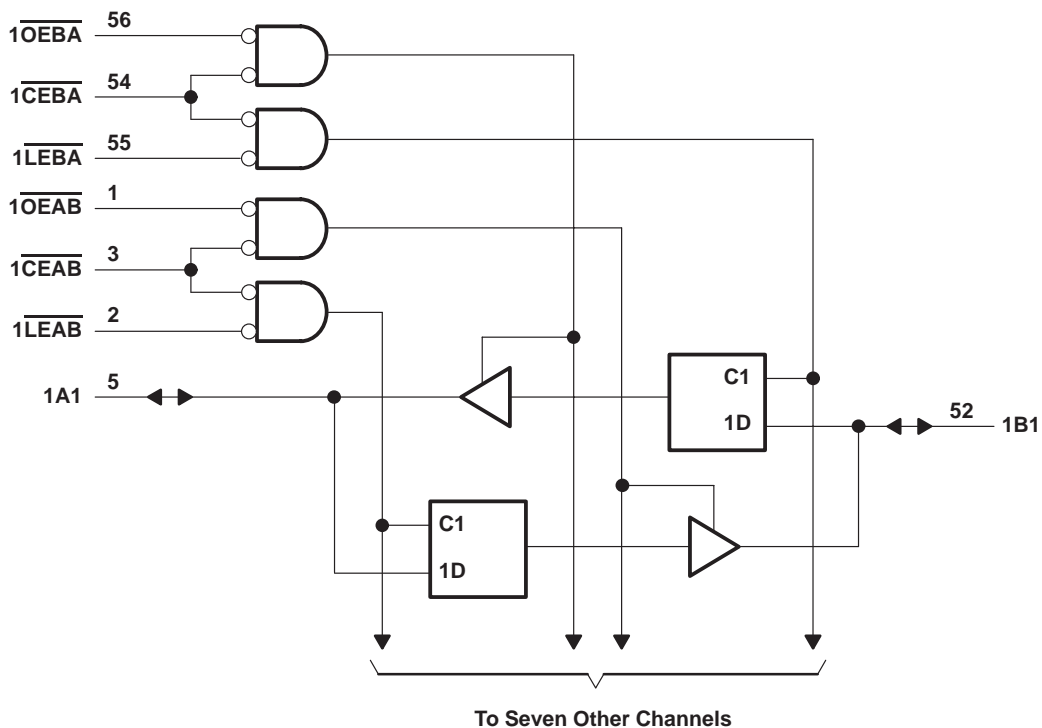
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVTH16543, SN74LVTH16543

3.3-V ABT 16-BIT REGISTERED TRANSCIEVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



SN54LVTH16543, SN74LVTH16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high state, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_O : SN54LVTH16543 | 96 mA |
| SN74LVTH16543 | 128 mA |
| Current into any output in the high state, I_O (see Note 2): SN54LVTH16543 | 48 mA |
| SN74LVTH16543 | 64 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): DGG package | 81°C/W |
| DL package | 74°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

| | | SN54LVTH16543 | | SN74LVTH16543 | | UNIT |
|--------------------------|------------------------------------|-----------------|-----|---------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 2.7 | 3.6 | 2.7 | 3.6 | V |
| V_{IH} | High-level input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I | Input voltage | | 5.5 | | 5.5 | V |
| I_{OH} | High-level output current | | –24 | | –32 | mA |
| I_{OL} | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 200 | | 200 | | μs/V |
| T_A | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SN54LVTH16543 | | | SN74LVTH16543 | | | UNIT |
|-----------------------|--|--|--|-------|------|----------------------|------|------|------|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V _{IK} | | V _{CC} = 2.7 V, I _I = -18 mA | -1.2 | | | -1.2 | | | V |
| V _{OH} | | V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA | V _{CC} -0.2 | | | V _{CC} -0.2 | | | V |
| | | V _{CC} = 2.7 V, I _{OH} = -8 mA | 2.4 | | | 2.4 | | | |
| | | V _{CC} = 3 V | 2 | | | 2 | | | |
| V _{OL} | | V _{CC} = 2.7 V | I _{OL} = 100 μA | | 0.2 | | 0.2 | | V |
| | | | I _{OL} = 24 mA | | 0.5 | | 0.5 | | |
| | | V _{CC} = 3 V | I _{OL} = 16 mA | | 0.4 | | 0.4 | | |
| | | | I _{OL} = 32 mA | | 0.5 | | 0.5 | | |
| | | | I _{OL} = 48 mA | | 0.55 | | 0.55 | | |
| | | | I _{OL} = 64 mA | | | | 0.55 | | |
| I _I | | Control inputs | V _{CC} = 3.6 V, V _I = V _{CC} or GND | | ±1 | | ±1 | | μA |
| | | | V _{CC} = 0 or 3.6 V, V _I = 5.5 V | | 10 | | 10 | | |
| | | A or B ports‡ | V _{CC} = 3.6 V, V _I = 5.5 V | | 20 | | 20 | | |
| | | | V _{CC} = 3.6 V, V _I = V _{CC} | | 1 | | 1 | | |
| | | V _{CC} = 3.6 V, V _I = 0 | | -5 | | -5 | | | |
| I _{off} | | V _{CC} = 0, V _I or V _O = 0 to 4.5 V | | | | ±100 | | μA | |
| I _I (hold) | | V _{CC} = 3 V | V _I = 0.8 V | | 75 | | 75 | | μA |
| | | | V _I = 2 V | | -75 | | -75 | | |
| | | V _{CC} = 3.6 V§, V _I = 0 to 3.6 V | | | | | | ±500 | |
| I _{OZPU} | | V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care | | ±100* | | ±100 | | μA | |
| I _{OZPD} | | V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care | | ±100* | | ±100 | | μA | |
| I _{CC} | | V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND | Outputs high | | 0.19 | | 0.19 | | mA |
| | | | Outputs low | | 5 | | 5 | | |
| | | | Outputs disabled | | 0.19 | | 0.19 | | |
| ΔI _{CC} ¶ | | V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | | 0.2 | | 0.2 | | mA | |
| C _i | | V _I = 3 V or 0 | | 4 | | 4 | | pF | |
| C _{io} | | V _O = 3 V or 0 | | 10 | | 10 | | pF | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ Unused pins at V_{CC} or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | | SN54LVTH16543 | | | | SN74LVTH16543 | | | | UNIT | |
|----------|--|--|--|-----|-------------------------|-----|--|-----|-------------------------|-----|------|----|
| | | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| t_w | Pulse duration, \overline{LEAB} or \overline{LEBA} low | | 3.3 | | 3.3 | | 3.3 | | 3.3 | | ns | |
| t_{su} | Setup time | A or B before $\overline{LEAB}\uparrow$ or $\overline{LEBA}\uparrow$ | Data high | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| | | | Data low | 0.8 | | 1.3 | | 0.8 | | 1.3 | | |
| | | A or B before $\overline{CEAB}\uparrow$ or $\overline{CEBA}\uparrow$ | Data high | 0 | | 0 | | 0 | | 0 | | |
| | | | Data low | 0.6 | | 1.1 | | 0.6 | | 1.1 | | |
| t_h | Hold time | A or B after $\overline{LEAB}\uparrow$ or $\overline{LEBA}\uparrow$ | Data high | 1.5 | | 0.7 | | 1.5 | | 0.7 | | ns |
| | | | Data low | 1.2 | | 1.3 | | 1.2 | | 1.3 | | |
| | | A or B after $\overline{CEAB}\uparrow$ or $\overline{CEBA}\uparrow$ | Data high | 1.7 | | 0.9 | | 1.7 | | 0.9 | | |
| | | | Data low | 1.6 | | 1.8 | | 1.6 | | 1.8 | | |

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH16543 | | | | SN74LVTH16543 | | | | UNIT | |
|-----------|-----------------|-------------|--|-----|-------------------------|-----|--|------|-----|-------------------------|------|-----|
| | | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | | $V_{CC} = 2.7\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | TYP† | MAX | MIN | | MAX |
| t_{PLH} | A or B | B or A | 1.1 | 3.4 | | 3.9 | 1.2 | 2.3 | 3.2 | | 3.7 | ns |
| t_{PHL} | | | 1.1 | 3.4 | | 3.9 | 1.2 | 2.1 | 3.2 | | 3.7 | |
| t_{PLH} | \overline{LE} | A or B | 1.2 | 4.1 | | 5.1 | 1.3 | 2.5 | 3.9 | | 4.9 | ns |
| t_{PHL} | | | 1.2 | 4.1 | | 5.1 | 1.3 | 2.3 | 3.9 | | 4.9 | |
| t_{PZH} | \overline{OE} | A or B | 1.2 | 4.5 | | 5.6 | 1.3 | 2.8 | 4.3 | | 5.4 | ns |
| t_{PZL} | | | 1.2 | 4.5 | | 5.6 | 1.3 | 2.8 | 4.3 | | 5.4 | |
| t_{PHZ} | \overline{OE} | A or B | 1.9 | 4.9 | | 5.4 | 2 | 3.5 | 4.7 | | 5.2 | ns |
| t_{PLZ} | | | 1.9 | 4.6 | | 4.7 | 2 | 3.3 | 4.4 | | 4.5 | |
| t_{PZH} | \overline{CE} | A or B | 1.2 | 4.7 | | 5.8 | 1.3 | 3 | 4.5 | | 5.6 | ns |
| t_{PZL} | | | 1.2 | 4.7 | | 5.8 | 1.3 | 3 | 4.5 | | 5.6 | |
| t_{PHZ} | \overline{CE} | A or B | 1.9 | 5.1 | | 5.6 | 2 | 3.6 | 4.9 | | 5.4 | ns |
| t_{PLZ} | | | 1.9 | 4.9 | | 5.1 | 2 | 3.5 | 4.7 | | 4.9 | |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

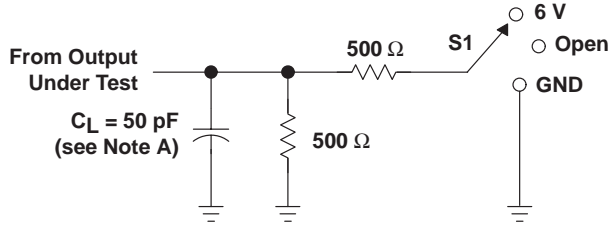
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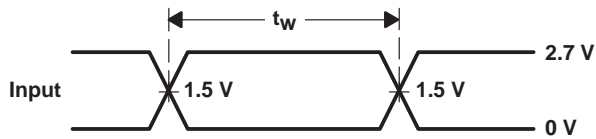
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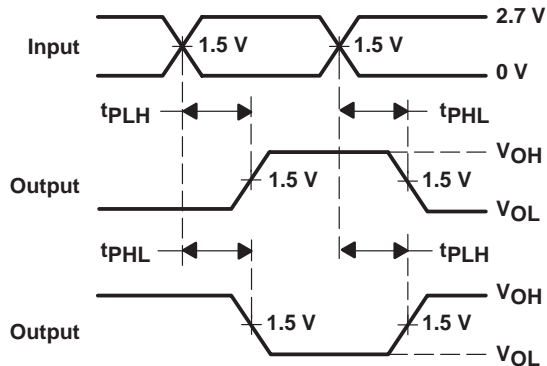
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

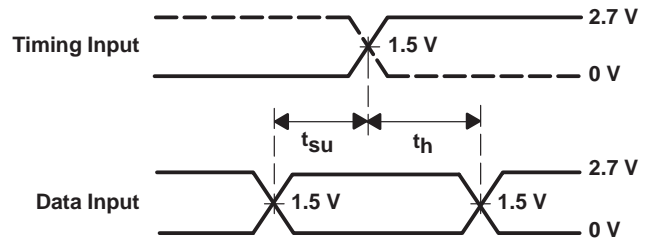


VOLTAGE WAVEFORMS
PULSE DURATION

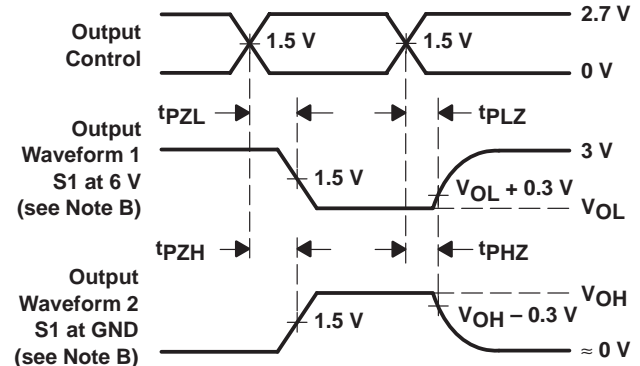


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 74LVTH16543DGGRE4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74LVTH16543DGGRG4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74LVTH16543DLRG4 | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH16543DGGR | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH16543DL | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH16543DLG4 | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH16543DLR | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVTH16543 :

- Enhanced Product: [SN74LVTH16543-EP](#)

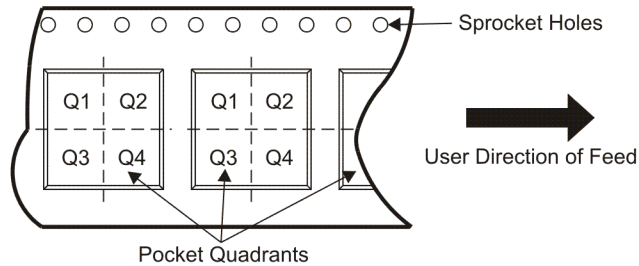
NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVTH16543DGGR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74LVTH16543DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVTH16543DGGR | TSSOP | DGG | 56 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LVTH16543DLR | SSOP | DL | 56 | 1000 | 346.0 | 346.0 | 49.0 |

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

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