



THE DATASHEET OF SG3503DM



SN74LV125AT Quadruple Bus Buffer Gates With 3-State Outputs

1 Features

- Inputs Are TTL-Voltage Compatible
- 4.5-V to 5.5-V V_{CC} Operation
- Typical t_{pd} of 3.8 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Description

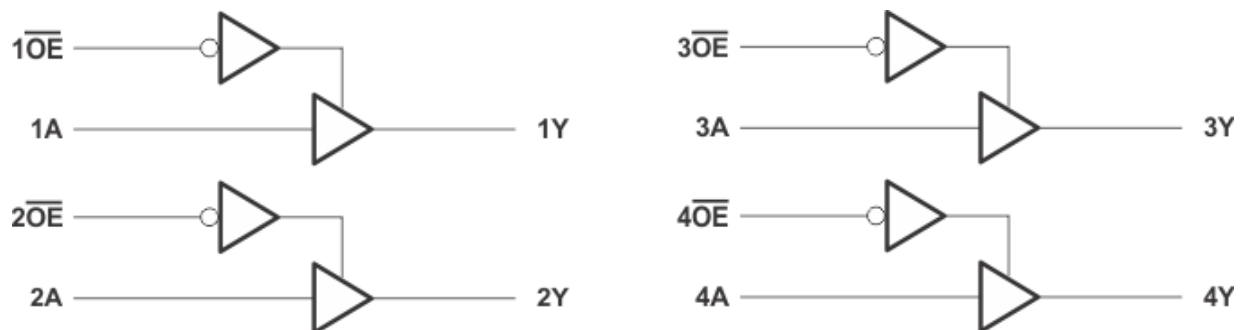
The SN74LV125AT is a quadruple bus buffer gate. This device features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

Package Information

PART NUMBER	PACKAGE ¹	PACKAGE SIZE ²
SN74LV125AT	RGY (VQFN, 14)	3.50 mm x 3.50 mm
	D (SOIC, 14)	8.65 mm x 6 mm
	NS (SO, 14)	10.20 mm x 7.8 mm
	DB (SSOP, 14)	6.20 mm x 7.8 mm
	PW (TSSOP, 14)	5.00 mm x 6.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The package size (length x width) is a nominal value and includes pins, where applicable.



Simplified Schematic

Table of Contents

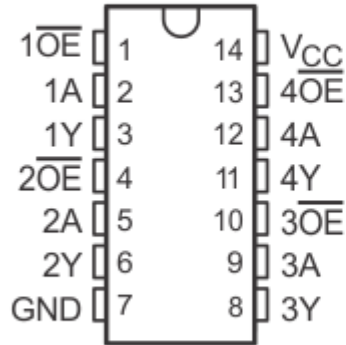
1 Features	1	6 Parameter Measurement Information	8
2 Description	1	7 Detailed Description	9
3 Revision History	2	7.1 Overview.....	9
4 Pin Configuration and Functions	3	7.2 Functional Block Diagram.....	9
5 Specifications	4	7.3 Device Functional Modes.....	9
5.1 Absolute Maximum Ratings.....	4	8 Device and Documentation Support	10
5.2 ESD Ratings.....	4	8.1 Documentation Support.....	10
5.3 Recommended Operating Conditions.....	5	8.2 Receiving Notification of Documentation Updates....	10
5.4 Thermal Information.....	5	8.3 Support Resources.....	10
5.5 Electrical Characteristics.....	6	8.4 Trademarks.....	10
5.6 Switching Characteristics.....	6	8.5 Electrostatic Discharge Caution.....	10
5.7 Noise Characteristics.....	6	8.6 Glossary.....	10
5.8 Operating Characteristics.....	7	9 Mechanical, Packaging, and Orderable Information..	10

3 Revision History

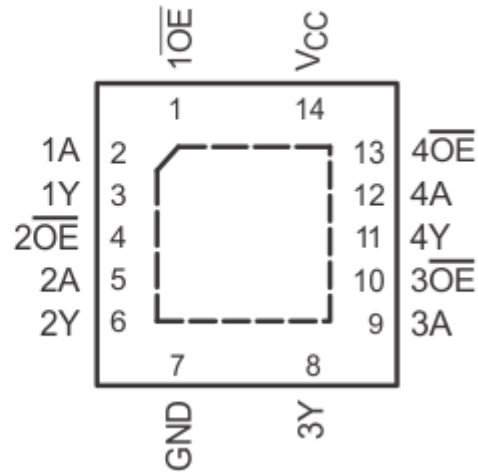
Changes from Revision A (May 2023) to Revision B (July 2023)	Page
• Added <i>Package Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

4 Pin Configuration and Functions

SN74LV125A . . . D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LV125A . . . RGY PACKAGE
(TOP VIEW)



NO.	PIN		TYPE ⁽¹⁾	DESCRIPTION
		NAME		
1		1 \overline{OE}	I	Output Enable 1, Active Low
2		1A	I	1A Input
3		1Y	O	1Y Output
4		2 \overline{OE}	I	Output Enable 2, Active Low
5		2A	I	2A Input
6		2Y	O	2Y Output
7		GND	—	Ground Pin
8		3Y	O	3Y Output
9		3A	I	3A Input
10		3 \overline{OE}	I	Output Enable 3, Active Low
11		4Y	O	4Y Output
12		4A	I	4A Input
13		4 \overline{OE}	I	Output Enable 4, Active Low
14		V _{CC}	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	7	V
V _I	Input voltage range ⁽²⁾	-0.5	7	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	7	V
V _O	Output voltage range ^{(2) (3)}	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-20 mA
I _{OK}	Output clamp current	V _O < 0		±50 mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±35 mA
	Continuous current through V _{CC} or GND			±70 mA
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

5.2 ESD Ratings

		MAX	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN74LV125AT		UNIT
		MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V		V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V		V
V _I	Input voltage	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}
		3-state	0	5.5
I _{OH}	High-level output current	V _{CC} = 4.5 V to 5.5 V		–16 mA
I _{OL}	Low-level output current	V _{CC} = 4.5 V to 5.5 V		16 mA
Δt/Δv	Input transition rise or fall rate	V _{CC} = 4.5 V to 5.5 V		20 ns/V
T _A	Operating free-air temperature	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LV125AT					UNIT	
	D	DB	NS	PW	RGY		
	14 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	86	96	76	113	47	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	High-level output voltage I _{OH} = –50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
		4.5 V	3.8		3.8		3.8			
V _{OL}	Low-level output voltage I _{OL} = 50 μA	4.5 V		0	0.1		0.1		V	
		4.5 V			0.55		0.55			0.55
I _I	Input leakage current V _I = 5.5 V or GND	0 to 5.5 V			±1		±1		μA	
I _{oz}	Off-State (High-Impedance State) Output Current V _O = V _{CC} or GND	5.5 V			±0.25		±2.5		μA	
I _{CC}	Static supply current V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20		μA	
ΔI _{CC} ⁽¹⁾	Additional static supply current One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5		1.5	
I _{off}	Input/Output Power-Off Leakage Current V _I or V _O = 0 to 5.5 V	0			0.5		5		5	
C _i	Input capacitance V _I = V _{CC} or GND				2				pF	

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit And Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	C _L = 15 pF	1.9	3.8	5.5	1	6.5	1	8.5	ns
t _{en}	\overline{OE}	Y		2	3.6	5.1	1	6	1	7.5	
t _{dis}	\overline{OE}	Y		1.5	3.2	6.8	1	8	1	10	
t _{pd}	A	Y	C _L = 50 pF	2.9	5.3	7.5	1	8.5	1	10.5	ns
t _{en}	\overline{OE}	Y		2.8	5.1	7.1	1	8	1	9.5	
t _{dis}	\overline{OE}	Y		2.8	6.1	8.8	1	10	1	10	
t _{sk(o)}						1		1		1	

5.7 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER ⁽¹⁾	SN74LV125AT			UNIT
	MIN	TYP	MAX	
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}			V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}			V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}			V
V _{IH(D)}	High-level dynamic input voltage			V
V _{IL(D)}	Low-level dynamic input voltage			V

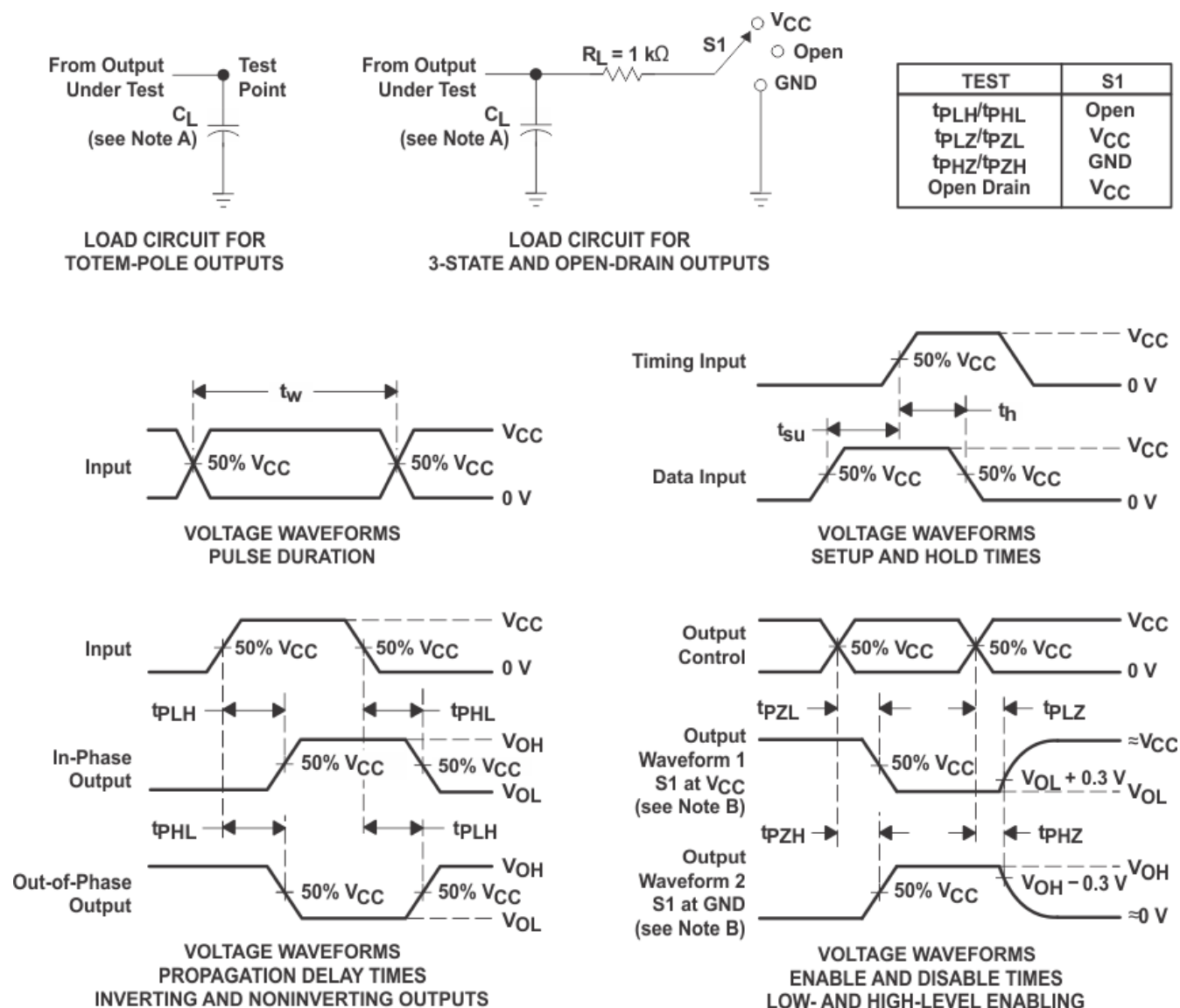
(1) Characteristics are for surface-mount packages only.

5.8 Operating Characteristics

 $V_{CC} = 5\text{ V}, T_A = -25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled $C_L = 50\text{ pF}, f = 10\text{ MHz}$	16	pF

6 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time, with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit And Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LV125AT is a quadruple bus buffer gate. This device features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

7.2 Functional Block Diagram

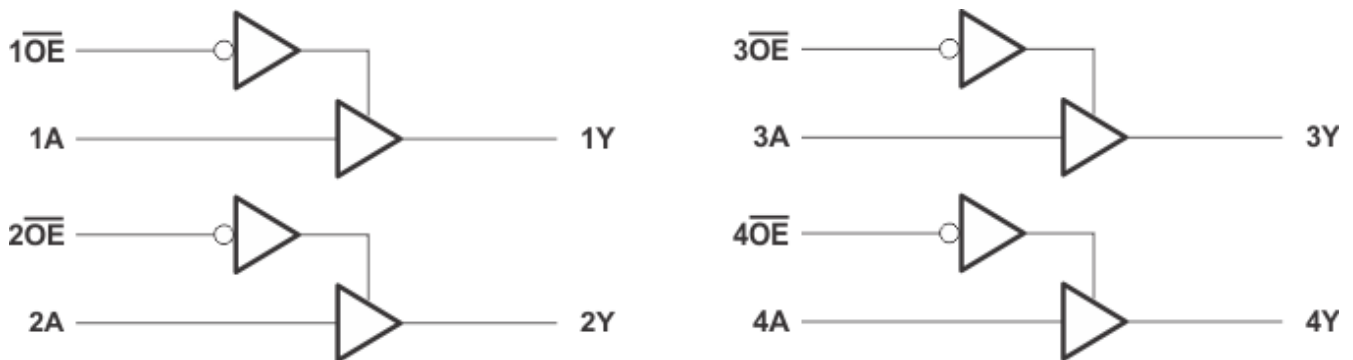


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

Table 7-1. Function Table
(Each Buffer)

INPUTS ⁽¹⁾		OUTPUT ⁽²⁾
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
 (2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV125AT	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV125ATDBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV125AT	Samples
SN74LV125ATDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LV125AT	Samples
SN74LV125ATNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV125AT	Samples
SN74LV125ATPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV125AT	Samples
SN74LV125ATRGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VV125	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV125ATDBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV125ATDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV125ATDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV125ATDR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74LV125ATNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV125ATPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV125ATRGR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

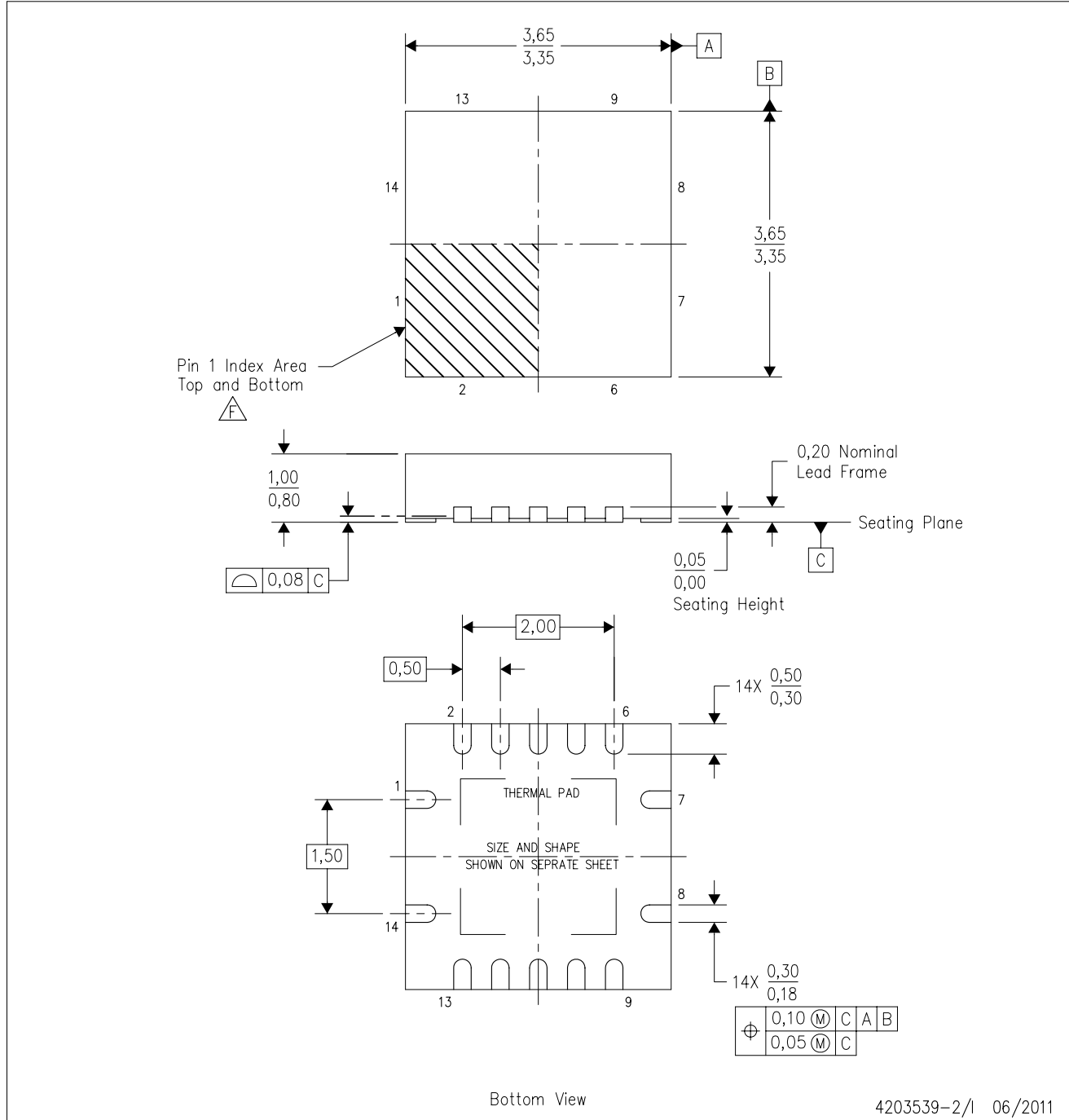


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV125ATDBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV125ATDR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV125ATDR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV125ATDR	SOIC	D	14	2500	366.0	364.0	50.0
SN74LV125ATNSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LV125ATPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV125ATRGYR	VQFN	RGY	14	3000	360.0	360.0	36.0

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G**)

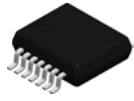
PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View SG3503DM on WIN SOURCE](#)

 [Microchip Technology](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management