



**THE DATASHEET OF
DG441AK**



Quad SPST CMOS Analog Switches

FEATURES

- Low On-Resistance: 50 Ω
- Low Leakage: 80 pA
- Low Power Consumption: 0.2 mW
- Fast Switching Action— t_{ON} : 150 ns
- Low Charge Injection— Q : -1 pC
- DG201A/DG202 Upgrades
- TTL/CMOS-Compatible Logic
- Single Supply Capability

BENEFITS

- Less Signal Errors and Distortion
- Reduced Power Supply Requirements
- Faster Throughput
- Improved Reliability
- Reduced Pedestal Errors
- Simplifies Retrofit
- Simple Interfacing

APPLICATIONS

- Audio Switching
- Battery Powered Systems
- Data Acquisition
- Hi-Rel Systems
- Sample-and-Hold Circuits
- Communication Systems
- Automatic Test Equipment
- Medical Instruments

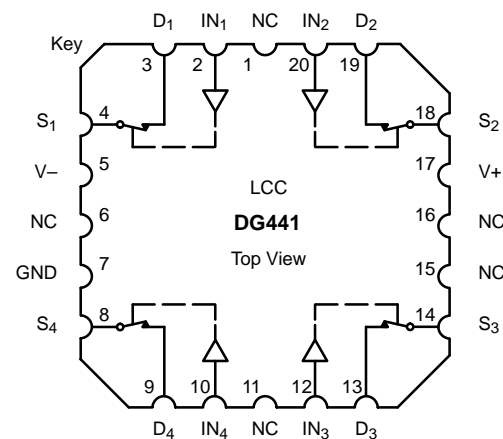
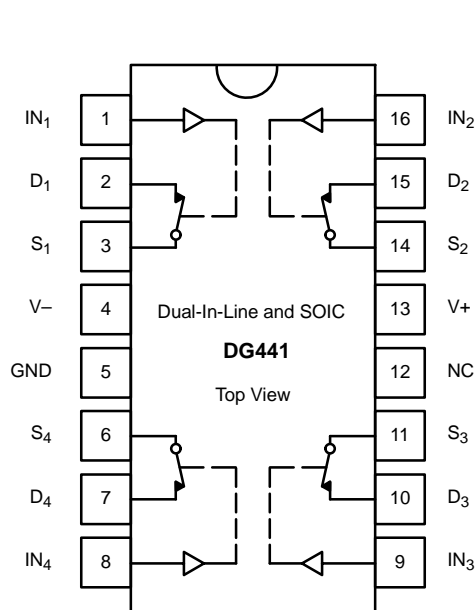
DESCRIPTION

The DG441/442 monolithic quad analog switches are designed to provide high speed, low error switching of analog and audio signals. The DG441 has a normally closed function. The DG442 has a normally open function. Combining low on-resistance (50 Ω , typ.) with high speed (t_{ON} 150 ns, typ.), the DG441/442 are ideally suited for upgrading DG201A/202 sockets. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

To achieve high voltage ratings and superior switching performance, the DG441/442 are built on Vishay Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages to the supply levels when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	DG441	DG442
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG441DJ
		DG442DJ
	16-Pin Narrow SOIC	DG441DY
		DG442DY
-55 to 125°C	16-Pin CerDIP	DG441AK
		DG441AK/883
		5962-9204101MEA
		DG442AK
		DG442AK/883
		5962-9204102MEA
	LCC-20	5962-9204101M2A
		5962-9204102M2A

ABSOLUTE MAXIMUM RATINGS

V+ to V-	44 V
GND to V-	25 V
Digital Inputs ^a V _S , V _D	(V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
Continuous Current (Any Terminal)	30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle)	100 mA
Storage Temperature (AK Suffix)	-65 to 150°C
(DJ, DY Suffix)	-65 to 125°C

Power Dissipation (Package) ^b	
16-Pin Plastic DIP ^c	450 mW
16-Pin CerDIP ^d	900 mW
16-Pin Narrow Body SOIC ^d	900 mW
LCC-20 ^d	1200 mW

- Notes:
- Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
 - All leads welded or soldered to PC Board.
 - Derate 6 mW/°C above 75°C
 - Derate 12 mW/°C above 25°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

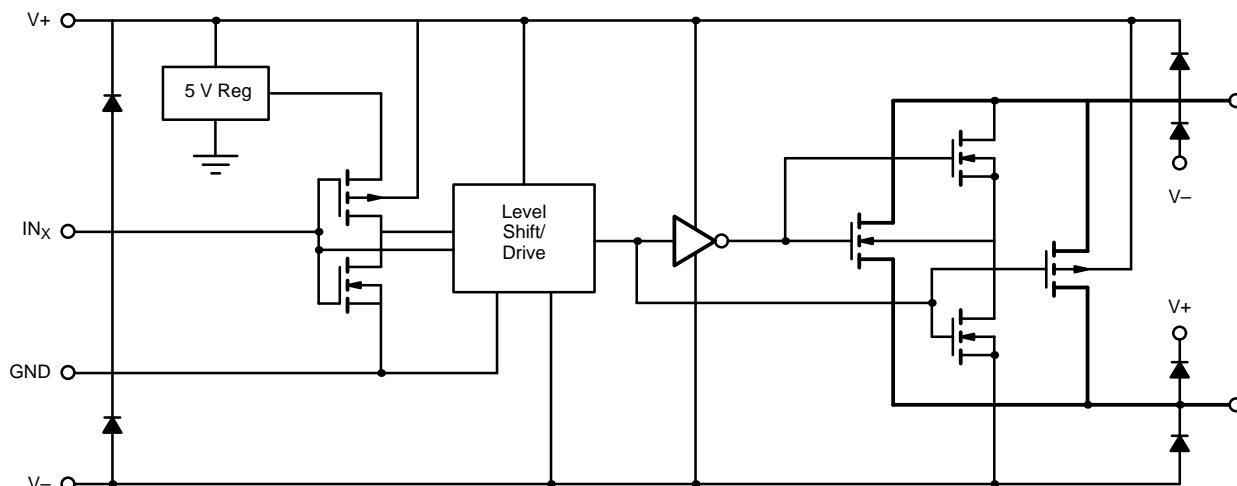


FIGURE 1.



SPECIFICATIONS ^a FOR DUAL SUPPLIES										
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp ^b	Typ ^c	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit	
					Min ^d	Max ^d	Min ^d	Max ^d		
Analog Switch										
Analog Signal Range ^e	V_{ANALOG}		Full		-15	15	-15	15	V	
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = \pm 8.5\text{ V}$ $V_+ = 13.5\text{ V}, V_- = -13.5\text{ V}$	Room Full	50		85 100		85 100	Ω	
On-Resistance Match Between Channels ^e	$\Delta r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = \pm 10\text{ V}$ $V_+ = 15\text{ V}, V_- = -15\text{ V}$	Room Full			4 5		4 5		
Switch Off Leakage Current	$I_{S(off)}$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}, V_S = \mp 15.5\text{ V}$	Room Full	± 0.01	-0.5 -20	0.5 20	-0.5 -5	0.5 5	nA	
	$I_{D(off)}$		Room Full	± 0.01	-0.5 -20	0.5 20	-0.5 -5	0.5 5		
Channel On Leakage Current	$I_{D(on)}$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_S = V_D = \pm 15.5\text{ V}$	Room Full	± 0.08	-0.5 -40	0.5 40	-0.5 -10	0.5 10		
Digital Control										
Input Current V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V, All Other = 2.4 V	Full	-0.01	-500	500	-500	500	nA	
Input Current V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V, All Other = 0.8 V	Full	0.01	-500	500	-500	500		
Dynamic Characteristics										
Turn-On Time	t_{ON}	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}, \text{ See Figure 2}$	Room	150		250		250	ns	
Turn-Off Time	DG441		Room	90		120		120		
	DG442		Room	110		210		210		
Charge Injection ^e	Q	$C_L = 1\text{ nF}, V_S = 0\text{ V}$ $V_{gen} = 0\text{ V}, R_{gen} = 0\text{ }\Omega$	Room	-1					pC	
Off Isolation ^e	OIRR	$R_L = 50\text{ }\Omega, C_L = 5\text{ pF}$ $f = 1\text{ MHz}$	Room	60					dB	
Crosstalk (Channel-to-Channel)	X_{TALK}		Room	100						
Source Off Capacitance ^e	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	4					pF	
Drain Off Capacitance ^e	$C_{D(off)}$		Room	4						
Channel On Capacitance ^e	$C_{D(on)}$	$V_{ANALOG} = 0\text{ V}$	Room	16						
Power Supplies										
Positive Supply Current	I_+	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Full	15		100		100	μA	
Negative Supply Current	I_-		Room Full	-0.000 1	-1 -5		-1 -5			
Ground Current	I_{GND}		Full	-15	-100		-100			

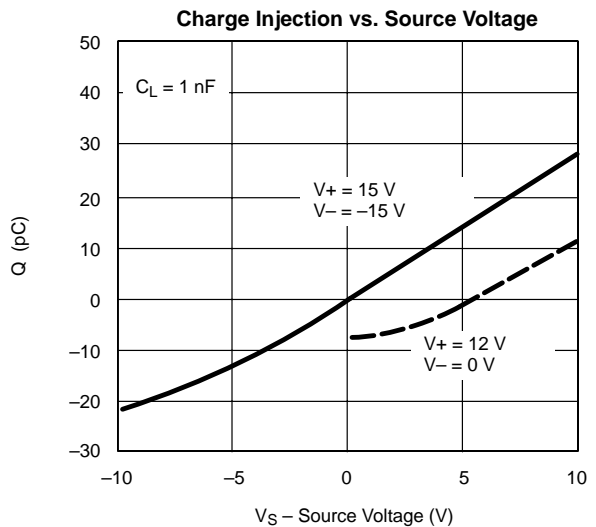
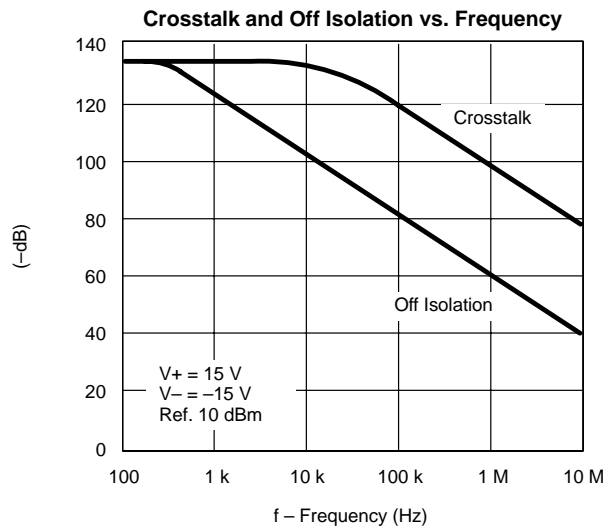
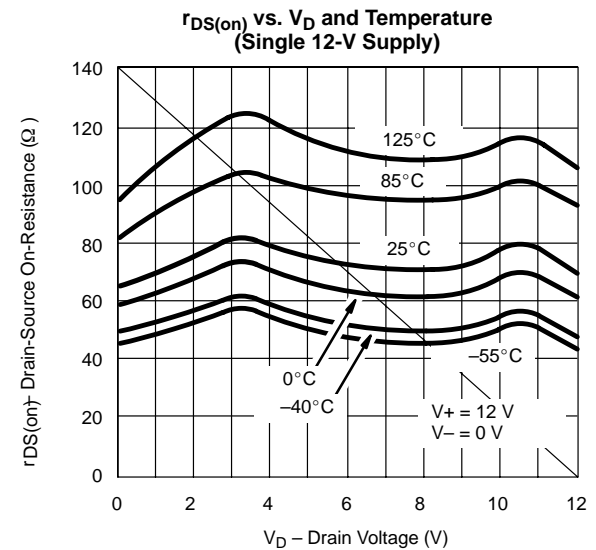
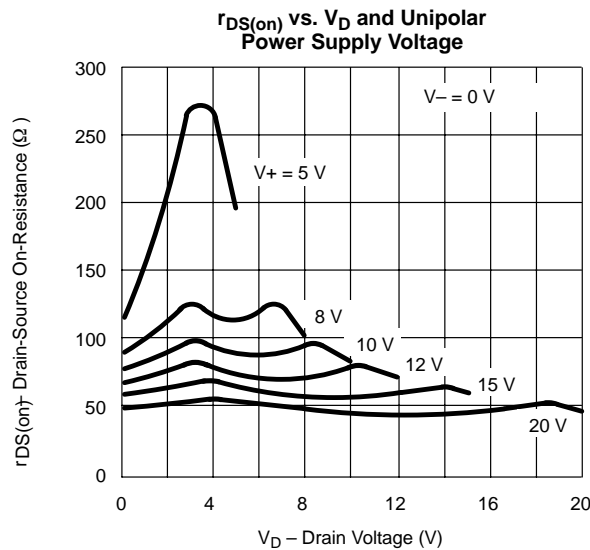
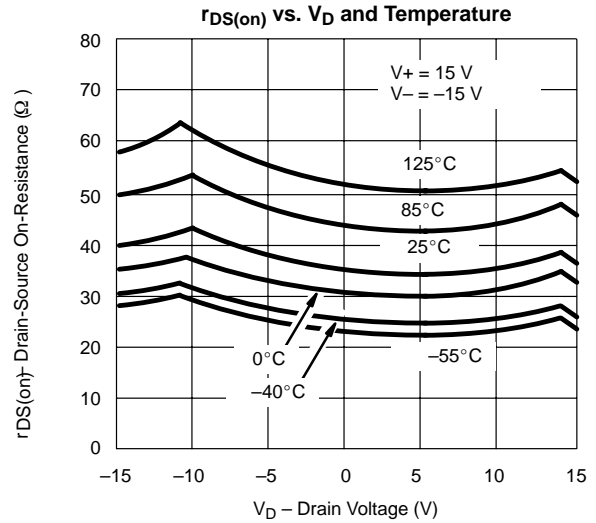
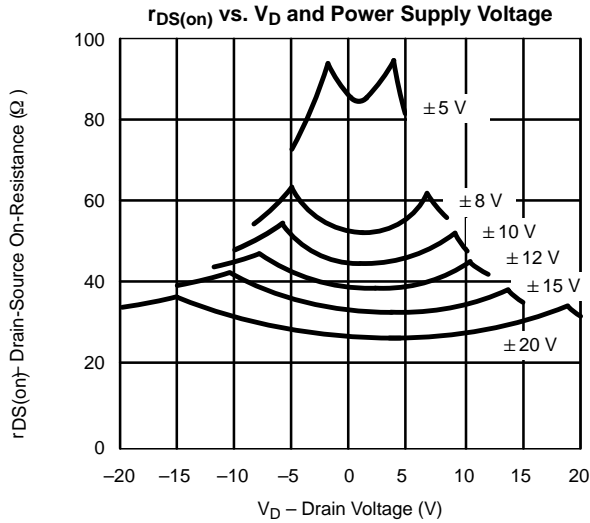


SPECIFICATIONS ^a FOR SINGLE SUPPLY									
Parameter	Symbol	Test Conditions Otherwise Unless Specified $V_+ = 12\text{ V}$, $V_- = 0\text{ V}$, $V_{IN} = 2.4\text{ V}$, 0.8 V^f	Temp ^b	Typ ^c	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}$, $V_D = 3\text{ V}$, 8 V $V_+ = 10.8\text{ V}$	Room Full	100		160 200		160 200	Ω
Dynamic Characteristics									
Turn-On Time	t_{ON}	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$, See Figure 2	Room	300		450		450	ns
Turn-Off Time	t_{OFF}		Room	60		200		200	
Charge Injection	Q	$C_L = 1\text{ nF}$, $V_{gen} = 6\text{ V}$, $R_{gen} = 0\ \Omega$	Room	2					pC
Power Supplies									
Positive Supply Current	I+	$V_+ = 13.2\text{ V}$, $V_- = 0\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Full	15		100		100	μA
Negative Supply Current	I-		Room Full	-0.0001	-1 -100		-1 -100		
Ground Current	I_{GND}		Full	-15	-100		-100		

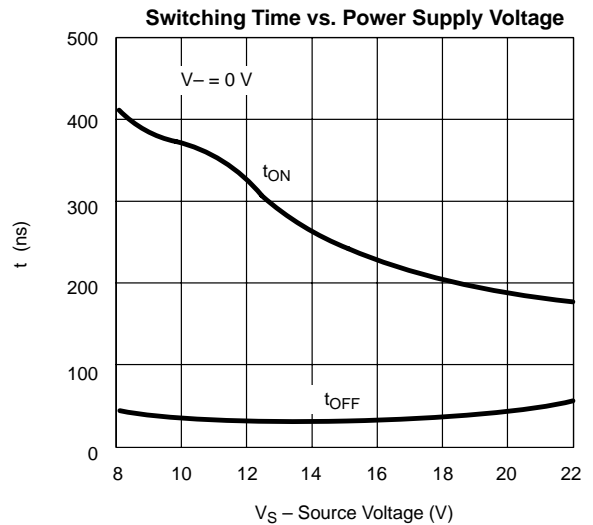
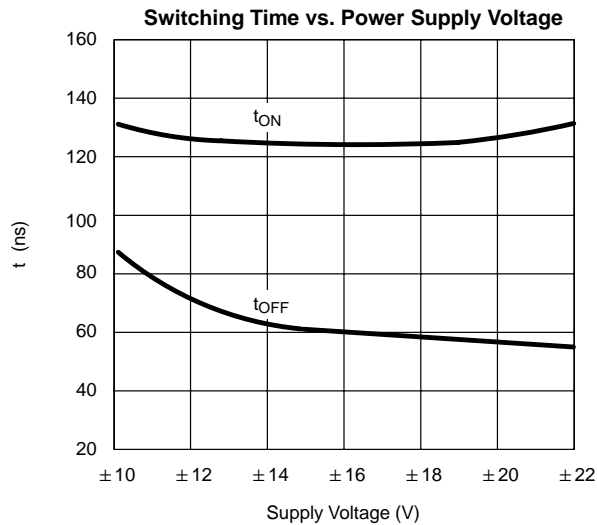
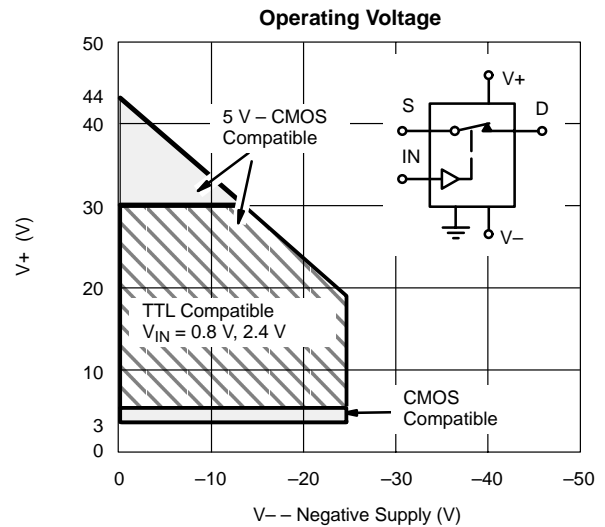
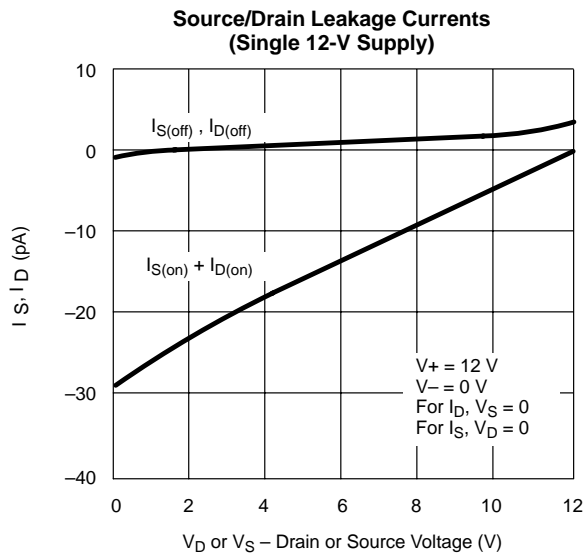
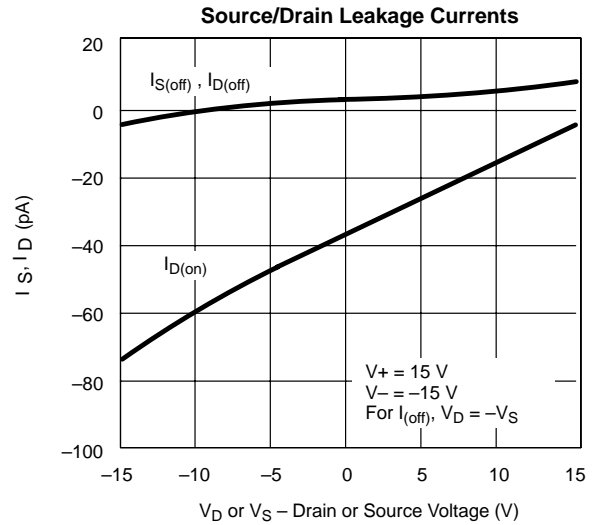
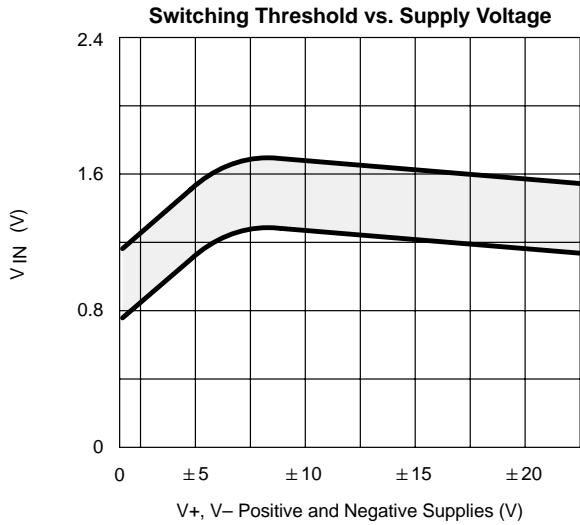
Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

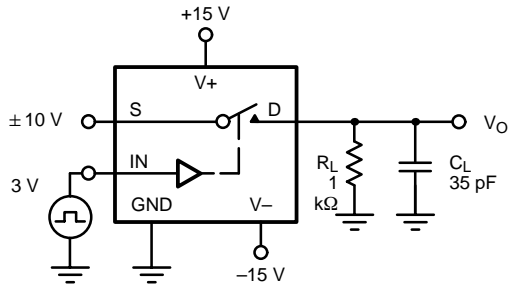
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



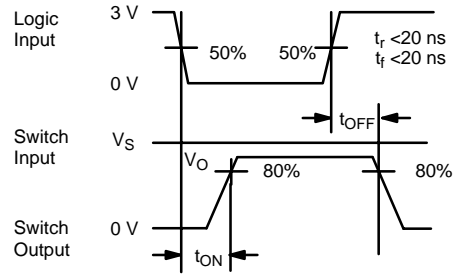
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TEST CIRCUITS



C_L (includes fixture and stray capacitance)



Note: Logic input waveform is inverted for DG442.

FIGURE 2. Switching Time

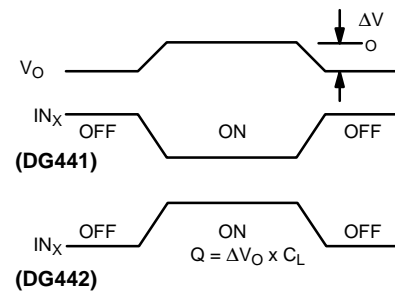
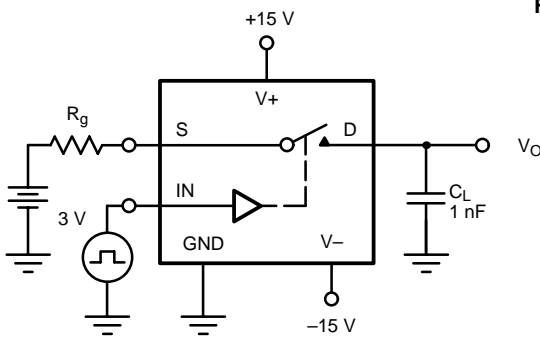
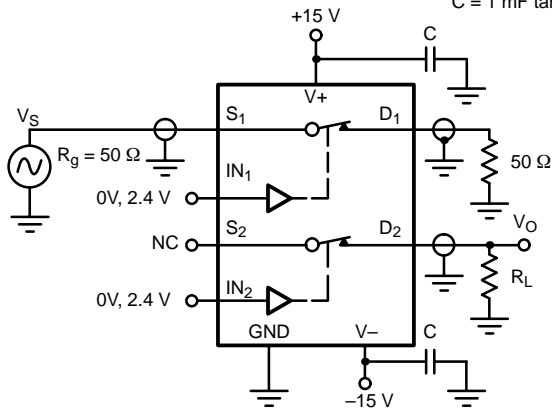


FIGURE 3. Charge Injection

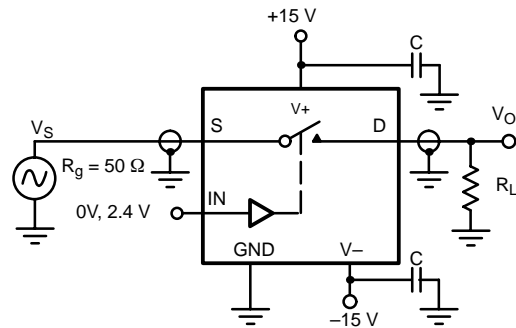
$C = 1 \text{ mF}$ tantalum in parallel with 0.01 mF ceramic



$$X_{\text{TALK Isolation}} = 20 \log \left| \frac{V_S}{V_O} \right|$$

$C = \text{RF bypass}$

FIGURE 4. Crosstalk



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

FIGURE 5. Off Isolation

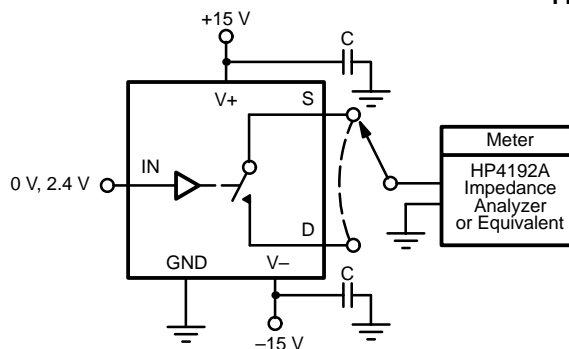


FIGURE 6. Source/Drain Capacitances

APPLICATIONS

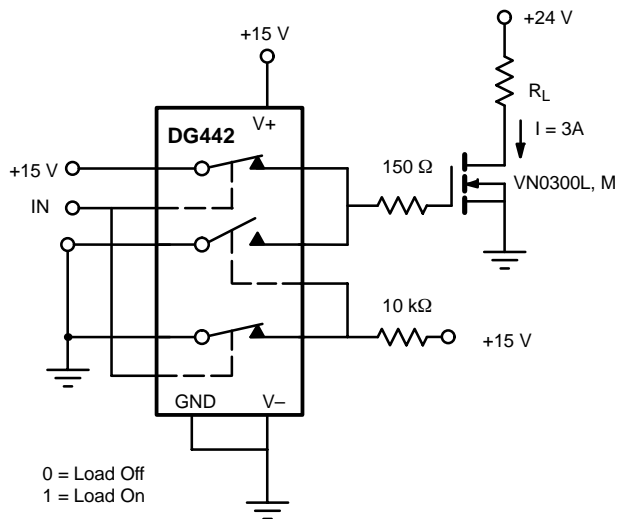


FIGURE 7. Power MOSFET Driver

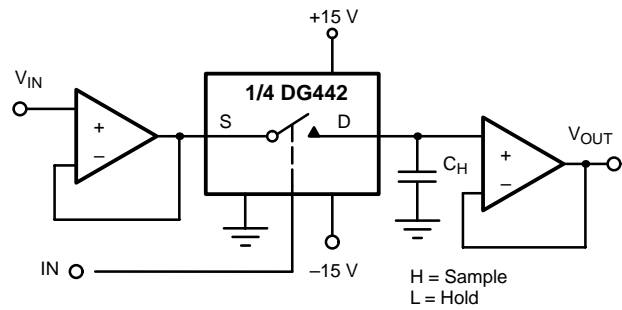
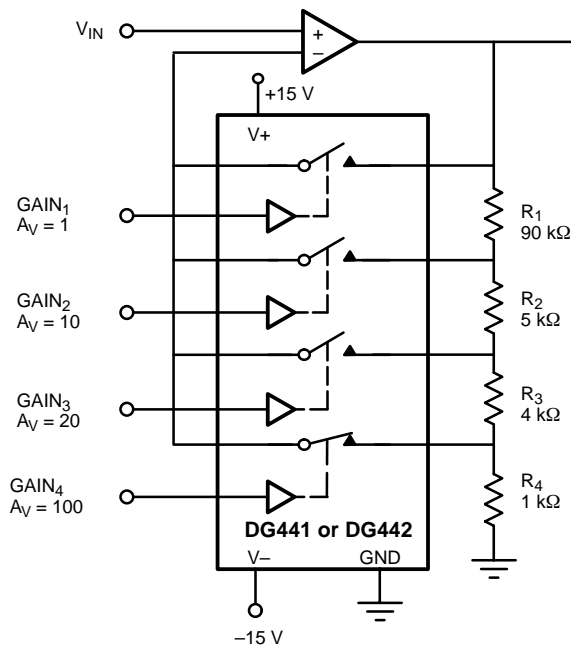


FIGURE 8. Open Loop Sample-and-Hold



Gain error is determined only by the resistor tolerance. Op amp offset and CMRR will limit accuracy of circuit.

With SW₄ Closed

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

FIGURE 9. Precision-Weighted Resistor Programmable-Gain Amplifier

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