



**THE DATASHEET OF  
SN74LVCC3245ADWG4**



# SN74LVCC3245A Octal Bus Transceiver With Adjustable Output Voltage and 3-State Outputs

## 1 Features

- Bidirectional Voltage Translator
- 2.3 V to 3.6 V on A Port and 3 V to 5.5 V on B Port
- Control Inputs  $V_{IH}$  and  $V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- Level translation
- USB
- Interfacing
- Analog and Digital Applications

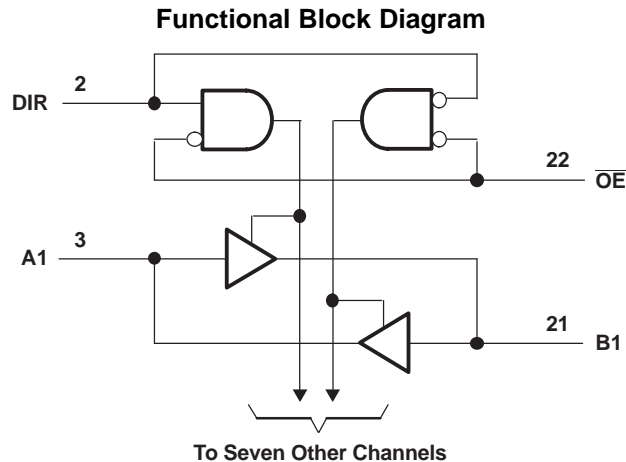
## 3 Description

The SN74LVCC3245A device is 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track  $V_{CCB}$ , which accepts voltages from 3 V to 5.5 V, and the A port is designed to track  $V_{CCA}$ , which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, from a 2.5-V to a 3.3-V system environment and vice versa.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVCC3245ADBQ	SSOP (24)	8.65 mm × 3.90 mm
SN74LVCC3245ADW	SOIC (24)	15.40 mm × 7.50 mm
SN74LVCC3245ADB	SSOP (24)	8.20 mm × 5.30 mm
SN74LVCC3245ANS	SO (24)	15.00 mm × 5.30 mm
SN74LVCC3245APW	TSSOP (24)	7.80 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

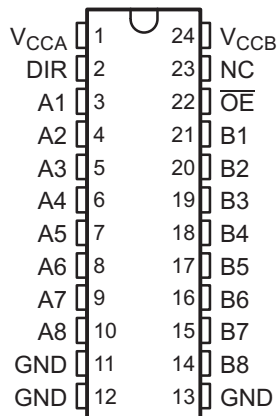
### Changes from Revision O (March 2005) to Revision P

Page

- Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. .... 1
- Removed *Ordering Information* table. .... 1

## 5 Pin Configuration and Functions

DB, DBQ, DW, NS, or PW Package  
24-Pin SSOP, SOIC, SO, or TSSOP  
Top View



NC – No internal connection

See [Mechanical, Packaging, and Orderable Information](#) for dimensions.

### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A1	3	I/O	A1 port
A2	4	I/O	A2 port
A3	5	I/O	A3 port
A4	6	I/O	A4 port
A5	7	I/O	A5 port
A6	8	I/O	A6 port
A7	9	I/O	A7 port
A8	10	I/O	A8 port
B1	21	I/O	B1 port
B2	20	I/O	B2 port
B3	19	I/O	B3 port
B4	18	I/O	B4 port
B5	17	I/O	B5 port
B6	16	I/O	B6 port
B7	15	I/O	B7 port
B8	14	I/O	B8 port
DIR	2	I	Dir input
GND	11	--	Ground
	12		
	13		
NC	23	--	Unconnected
$\overline{OE}$	22	I	Output Enable active low
V <sub>CCA</sub>	1	--	A port power
V <sub>CCB</sub>	24	--	B port power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CCA}$ $V_{CCB}$	Supply voltage	-0.5	6	V
$V_I$	Input voltage	All A ports <sup>(2)</sup>	$V_{CCA} + 0.5$	V
		All B ports <sup>(3)</sup>	$V_{CCB} + 0.5$	
		Except I/O ports <sup>(2)</sup>	$V_{CCA} + 0.5$	
$V_O$	Output voltage <sup>(3)</sup>	All A ports	$V_{CCA} + 0.5$	V
		All B ports	$V_{CCB} + 0.5$	
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		±50	mA
	Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND		±100	mA
$T_J$	Junction temperature		150	°C
$T_{stg}$	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) This value is limited to 4.6 V maximum.

(3) This value is limited to 6 V maximum.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(1)</sup>

		$V_{CCA}$	$V_{CCB}$	MIN	NOM	MAX	UNIT
$V_{CCA}$	Supply voltage			2.3	3.3	3.6	V
$V_{CCB}$	Supply voltage			3	5	5.5	V
$V_{IHA}$	High-level input voltage	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
$V_{IHB}$	High-level input voltage	2.3 V	3 V	2			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	3.85			
$V_{ILA}$	Low-level input voltage	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	

(1) All unused inputs of the device must be held at the associated  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

**Recommended Operating Conditions<sup>(1)</sup> (continued)**

		V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	NOM	MAX	UNIT
V <sub>ILB</sub>	Low-level input voltage	2.3 V	3 V			0.8	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			1.65	
V <sub>IH</sub>	High-level input voltage (control terminals) (referenced to V <sub>CCA</sub> )	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
V <sub>IL</sub>	Low-level input voltage (control terminals) (referenced to V <sub>CCA</sub> )	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
V <sub>IA</sub>	Input voltage			0		V <sub>CCA</sub>	V
V <sub>IB</sub>	Input voltage			0		V <sub>CCB</sub>	V
V <sub>OA</sub>	Output voltage			0		V <sub>CCA</sub>	V
V <sub>OB</sub>	Output voltage			0		V <sub>CCB</sub>	V
I <sub>OHA</sub>	High-level output current	2.3 V	3 V			-8	mA
		2.7 V	3 V			-12	
		3 V	3 V			-24	
		2.7 V	4.5 V			-24	
I <sub>OHB</sub>	High-level output current	2.3 V	3 V			-12	mA
		2.7 V	3 V			-12	
		3 V	3 V			-24	
		2.7 V	4.5 V			-24	
I <sub>OLA</sub>	Low-level output current	2.3 V	3 V			8	mA
		2.7 V	3 V			12	
		3 V	3 V			24	
		2.7 V	4.5 V			24	
I <sub>OLB</sub>	Low-level output current	2.3 V	3 V			12	mA
		2.7 V	3 V			12	
		3 V	3 V			24	
		2.7 V	4.5 V			24	
Δt/Δv	Input transition rise or fall rate					10	ns/V
T <sub>A</sub>	Operating free-air temperature			-40		85	°C

**6.4 Thermal Information**

THERMAL METRIC <sup>(1)(2)</sup>	SN74LVCC3245A					UNIT	
	DB (SSOP)	DBQ (SSOP)	DW (SOIC)	NS (SO)	PW (TSSOP)		
	24 PINS	24 PINS	24 PINS	24 PINS	24 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	63	61	46	65	88	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	UNIT
V <sub>OHA</sub>		I <sub>OH</sub> = –100 μA	3 V	3 V	2.9	3		V
		I <sub>OH</sub> = –8 mA	2.3 V	3 V	2			
		I <sub>OH</sub> = –12 mA	2.7 V	3 V	2.2	2.5		
			3 V	3 V	2.4	2.8		
		I <sub>OH</sub> = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	2	2.3		
V <sub>OHB</sub>		I <sub>OH</sub> = –100 μA	3 V	3 V	2.9	3		V
		I <sub>OH</sub> = –12 mA	2.3 V	3 V	2.4			
			2.7 V	3 V	2.4	2.8		
		I <sub>OH</sub> = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	3.2	4.2		
V <sub>OLA</sub>		I <sub>OL</sub> = 100 μA	3 V	3 V			0.1	V
		I <sub>OL</sub> = 8 mA	2.3 V	3 V			0.6	
		I <sub>OL</sub> = 12 mA	2.7 V	3 V		0.1	0.5	
			3 V	3 V		0.2	0.5	
		I <sub>OL</sub> = 24 mA	2.7 V	4.5 V		0.2	0.5	
V <sub>OLB</sub>		I <sub>OL</sub> = 100 μA	3 V	3 V			0.1	V
		I <sub>OL</sub> = 12 mA	2.3 V	3 V			0.4	
			3 V	3 V		0.2	0.5	
		I <sub>OL</sub> = 24 mA	2.7 V	4.5 V		0.2	0.5	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	3.6 V	3.6 V		±0.1	±1	μA
				5.5 V		±0.1	±1	
I <sub>OZ</sub> <sup>(1)</sup>	A or B ports	V <sub>O</sub> = V <sub>CCA/B</sub> or GND, V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	3.6 V	3.6 V		±0.5	±5	μA
I <sub>CCA</sub>	B to A	A port = V <sub>CCA</sub> or GND, I <sub>O</sub> = 0	3.6 V	Open		5	50	μA
		B port = V <sub>CCB</sub> or GND, I <sub>O</sub> = 0	3.6 V	3.6 V		5	50	
				5.5 V		5	50	
I <sub>CCB</sub>	A to B	A port = V <sub>CCA</sub> or GND, I <sub>O</sub> = 0	3.6 V	3.6 V		5	50	μA
				5.5 V		8	80	
ΔI <sub>CCA</sub> <sup>(2)</sup>	A port	V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V, Other inputs at V <sub>CCA</sub> or GND, OE at GND and DIR at V <sub>CCA</sub>	3.6 V	3.6 V		0.35	0.5	mA
	OE	V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V, Other inputs at V <sub>CCA</sub> or GND, DIR at V <sub>CCA</sub>	3.6 V	3.6 V		0.35	0.5	
	DIR	V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V, Other inputs at V <sub>CCA</sub> or GND, OE at GND	3.6 V	3.6 V		0.35	0.5	
ΔI <sub>CCB</sub> <sup>(2)</sup>	B port	V <sub>I</sub> = V <sub>CCB</sub> – 2.1 V, Other inputs at V <sub>CCB</sub> or GND, OE at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	Open	Open		4		pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CCA/B</sub> or GND	3.3 V	5 V		18.5		pF

 (1) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

 (2) This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0 V or the associated V<sub>CC</sub>.

## 6.6 Switching Characteristics

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#) through [Figure 5](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA}, V_{CCB}$	MIN	MAX	UNIT
$t_{PHL}$	A	B	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	9.4	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	6	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	7.1	
$t_{PLH}$	A	B	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	9.1	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	5.3	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	7.2	
$t_{PHL}$	B	A	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	11.2	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	5.8	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	6.4	
$t_{PLH}$	B	A	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	9.9	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	7	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	7.6	
$t_{PZL}$	$\overline{OE}$	A	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	14.5	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	9.2	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	9.7	
$t_{PZH}$	$\overline{OE}$	A	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	12.9	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	9.5	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	9.5	
$t_{PZL}$	$\overline{OE}$	B	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	13	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	8.1	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	9.2	
$t_{PZH}$	$\overline{OE}$	B	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	12.8	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	8.4	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	9.9	
$t_{PLZ}$	$\overline{OE}$	A	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	7.1	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	7	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	6.6	

## Switching Characteristics (continued)

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#) through [Figure 5](#))

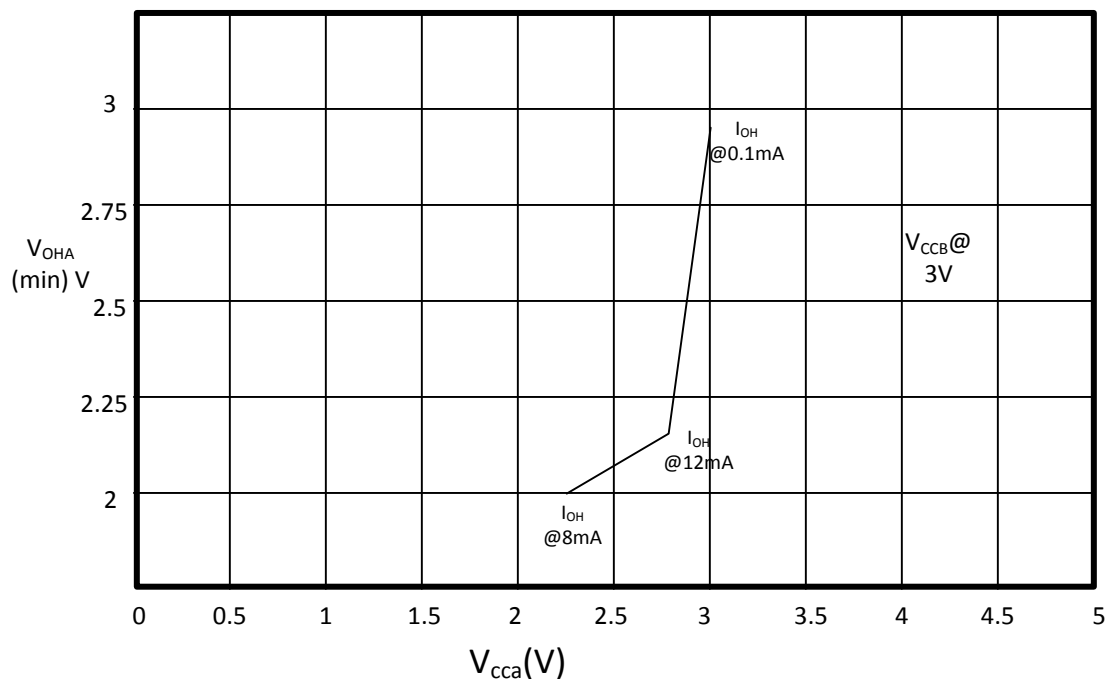
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA}, V_{CCB}$	MIN	MAX	UNIT
$t_{PHZ}$	$\overline{OE}$	A	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	6.9	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	7.8	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	6.9	
$t_{PLZ}$	$\overline{OE}$	B	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	8.8	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	7.3	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	7.5	
$t_{PHZ}$	$\overline{OE}$	B	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	8.9	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	7	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	7.9	

## 6.7 Operating Characteristics

 $V_{CCA} = 3.3\text{ V}, V_{CCB} = 5\text{ V}, T_A = 25^\circ\text{C}$ 

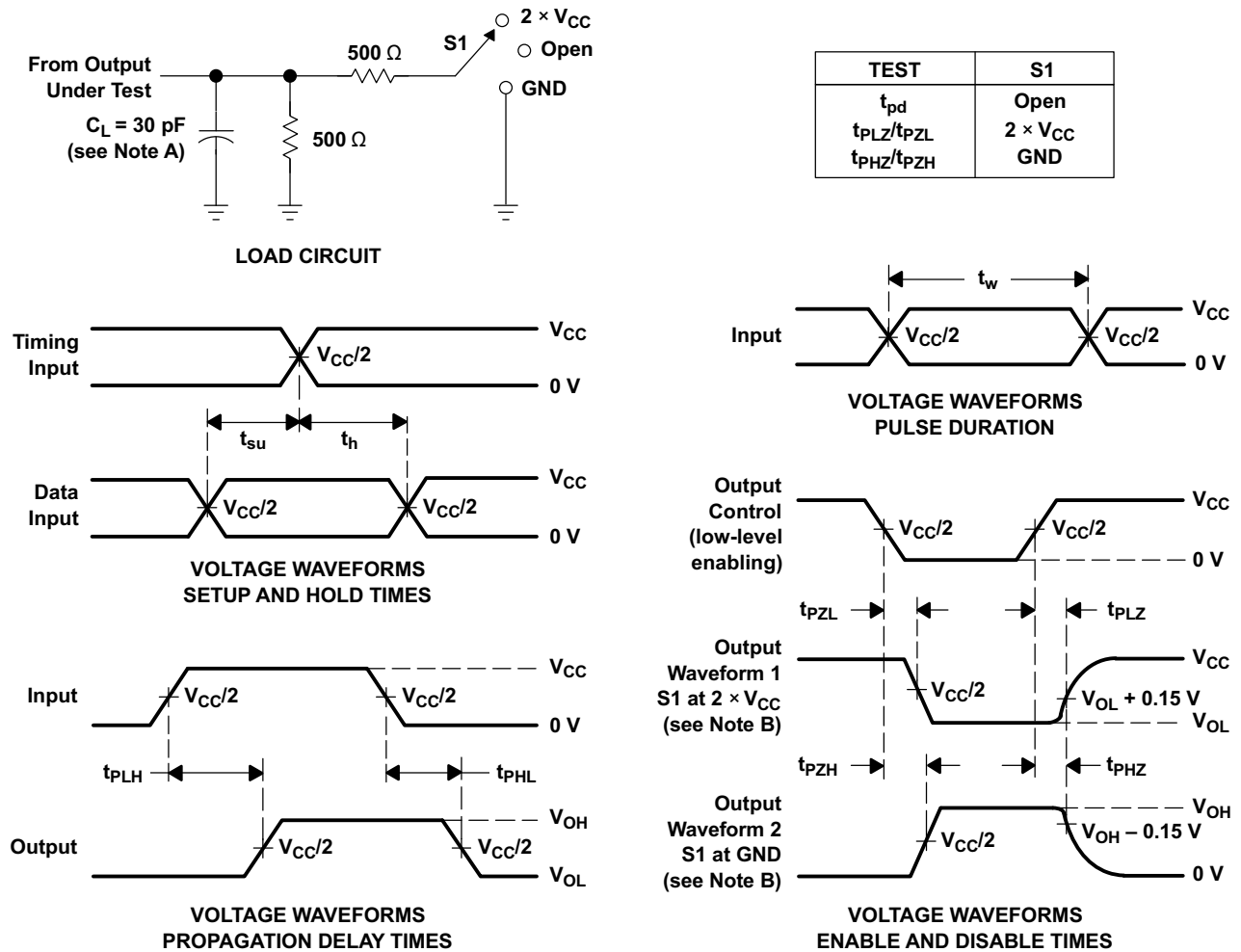
PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs enabled	38	pF
		Outputs disabled	4.5	

## 6.8 Typical Characteristics


**Figure 1.  $V_{OHA(\min)}$  VS  $V_{CCA}$**

## 7 Parameter Measurement Information

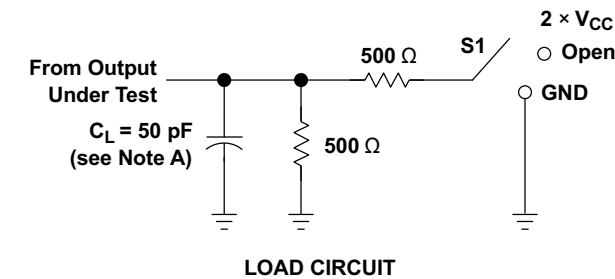
### 7.1 A Port ( $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ and $V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$ )



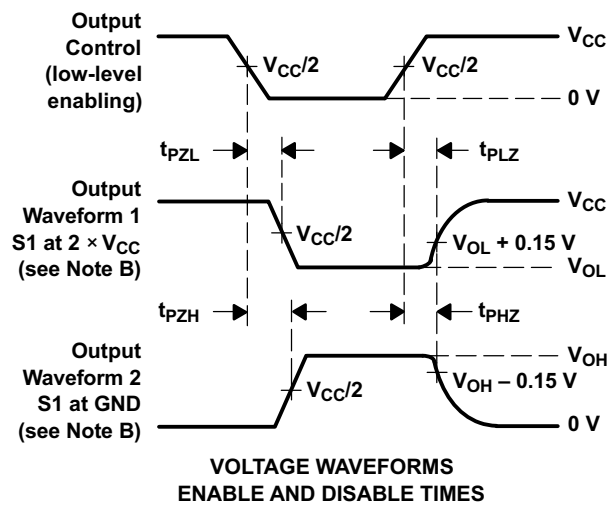
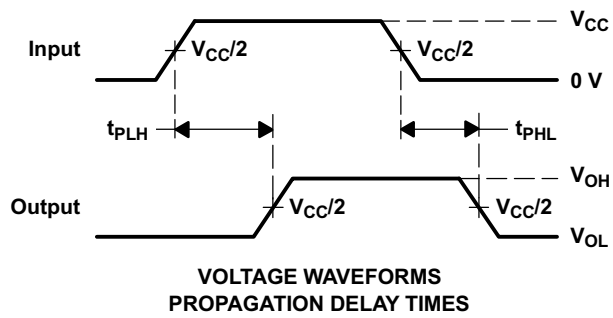
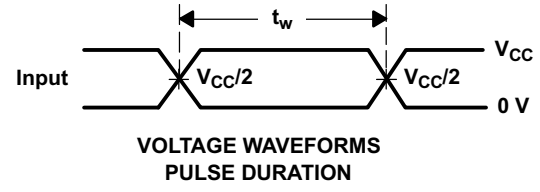
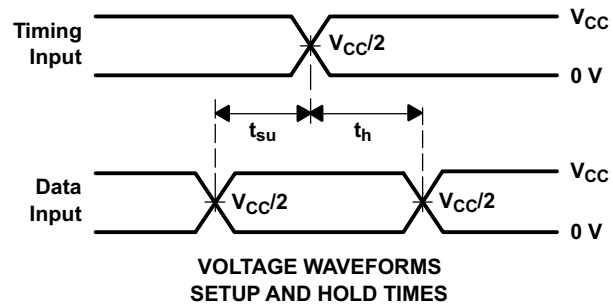
- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

7.2 B Port ( $V_{CCA} = 2.5 V \pm 0.2 V$  and  $V_{CCB} = 3.3 V \pm 0.3 V$ )



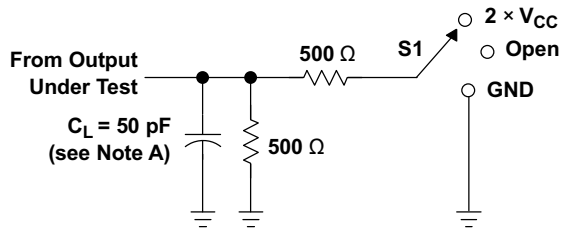
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

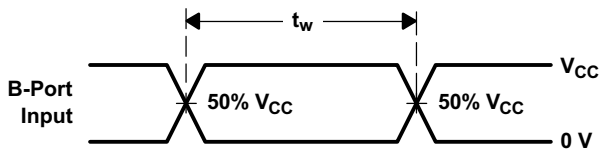
Figure 3. Load Circuit and Voltage Waveforms

7.3 B Port ( $V_{CCA} = 3.6\text{ V}$  and  $V_{CCB} = 5.5\text{ V}$ )

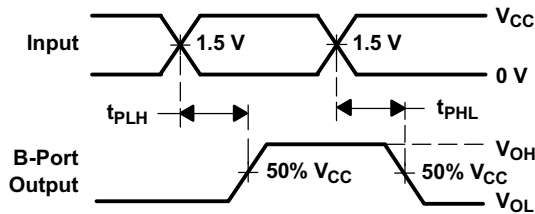


LOAD CIRCUIT

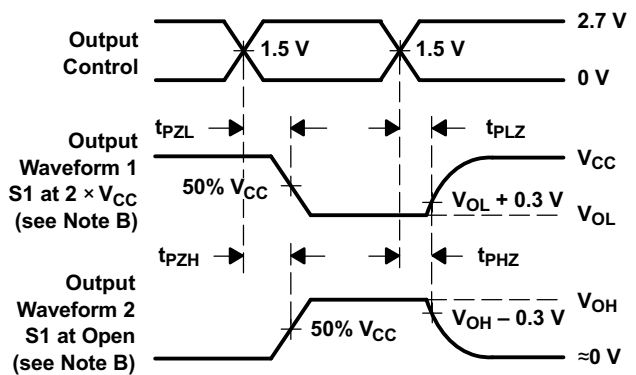
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



VOLTAGE WAVEFORMS  
PULSE DURATION



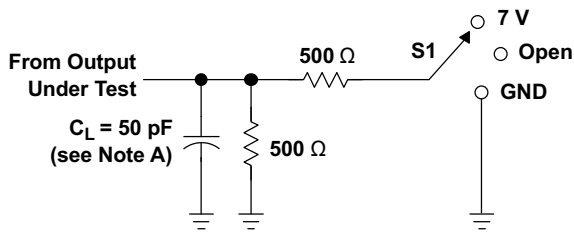
VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
NONINVERTING OUTPUTS



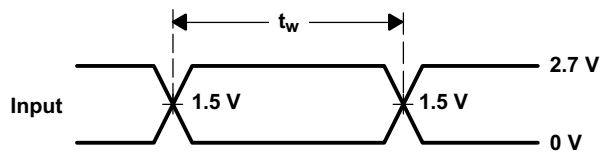
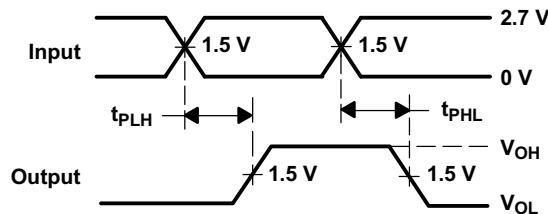
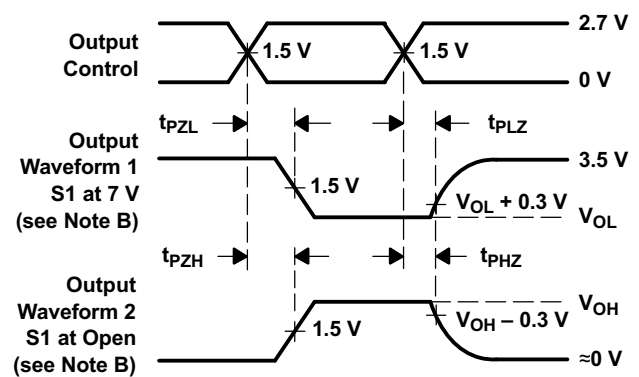
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

**7.4 A and B Port ( $V_{CCA}$  and  $V_{CCB} = 3.6\text{ V}$ )**

**LOAD CIRCUIT**

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open


**VOLTAGE WAVEFORMS  
PULSE DURATION**

**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- All parameters and waveforms are not applicable to all devices.

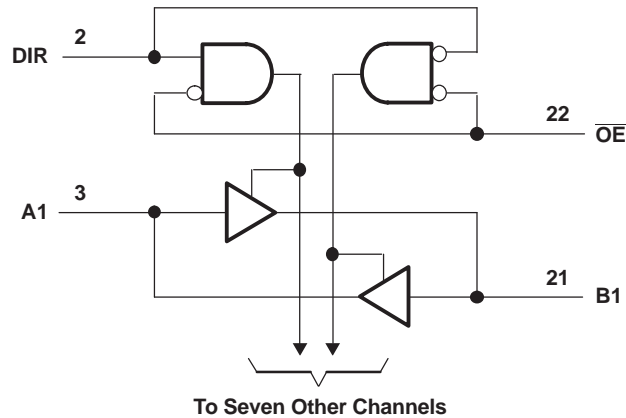
**Figure 5. Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The SN74LVCC3245A device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR,  $\overline{OE}$ ) is powered by  $V_{CCA}$ .

### 8.2 Functional Block Diagram



### 8.3 Feature Description

This device is a bidirectional level translator designed to operate from 2.3 V to 3.6 V on Port A and 3 V to 5.5 V on B port. The control inputs recommended operating specifications are referenced with respect to  $V_{CCA}$  Voltage.

### 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVCC3245A.

Table 1. Function Table (Each Transceiver)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## 9 Application and Implementation

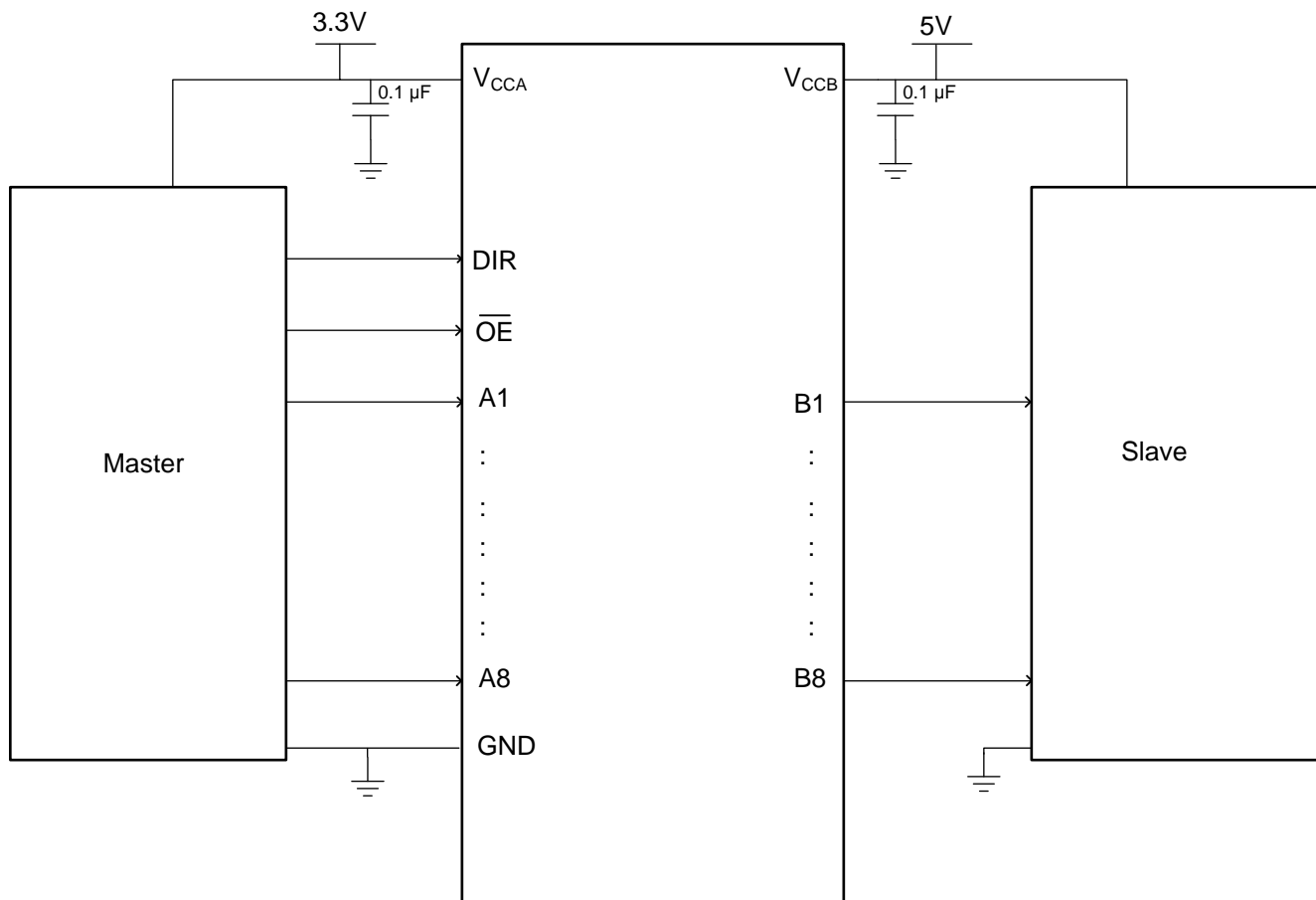
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74LVCC3245A device is a bidirectional level translator designed to operate from 2.3 V to 3.6 V on Port A and 3 V to 5.5 V on B port and designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.

### 9.2 Typical Application



**Figure 6. Typical Application**

#### 9.2.1 Design Requirements

This device can be used as bidirectional level translator depending on the DIR pin. The application describes the level translation of Master with signals at 3.3 V to slave operating at 5 V. The OE pin is low and DIR pin is 3.3-V high.

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

Use the procedure that follows for the design:

1. Recommended Input Conditions
  - Rise time and fall time specs. See ( $\Delta t/\Delta V$ ) in the *Recommended Operating Conditions* table.
  - Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in the *Recommended Operating Conditions* table.
  - Inputs are overvoltage tolerant allowing them to go as high as ( $V_I$  max) in the *Recommended Operating Conditions* table at any valid  $V_{CC}$ .
2. Absolute Maximum Output Conditions
  - Load currents should not exceed ( $I_O$  max) per output and should not exceed total current (continuous current through  $V_{CC}$  or GND) for the part. These limits are located in the *Absolute Maximum Ratings* table.
  - All the voltages on A and B ports should not exceed above  $V_{CCA}$  or  $V_{CCB}$  to prevent the biasing of Electrostatic discharge (ESD) diodes.

### 9.2.3 Application Curve

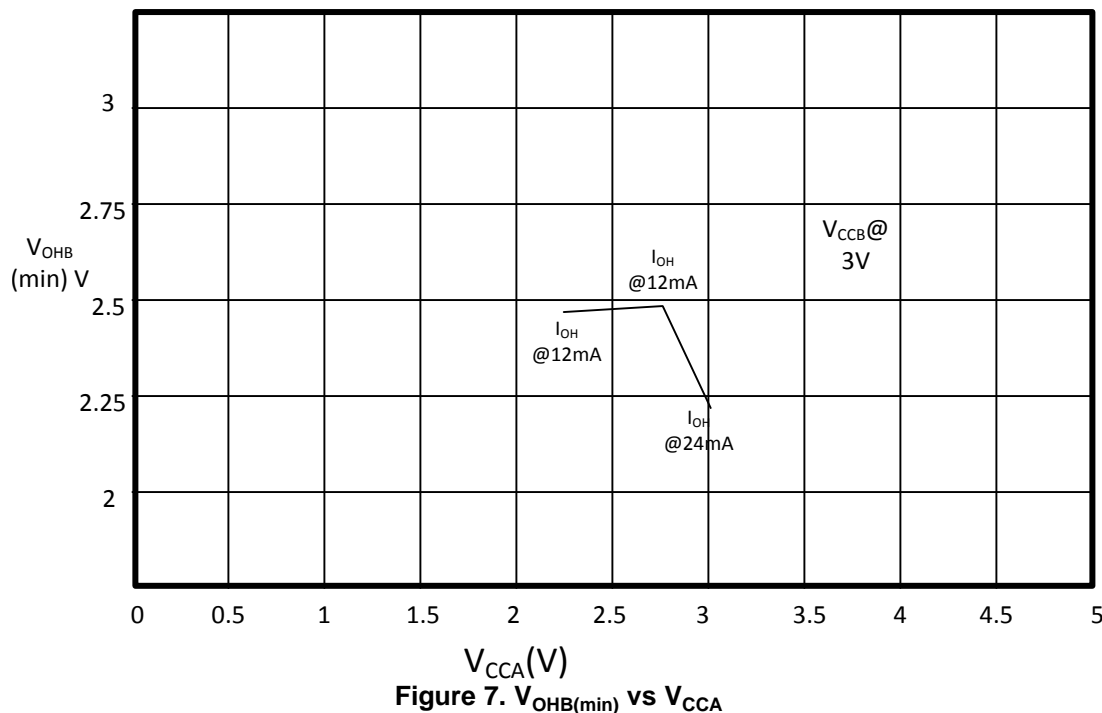


Figure 7.  $V_{OHB}(\min)$  vs  $V_{CCA}$

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

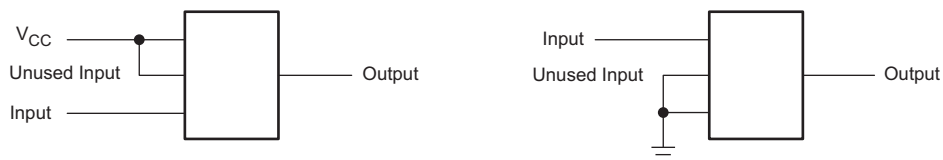
Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu F$  capacitor is recommended and if there are multiple  $V_{CC}$  pins then 0.01- $\mu F$  or 0.022- $\mu F$  capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu F$  and 1- $\mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient.

### 11.2 Layout Example



**Figure 8. Layout Example**

### 11.3 Power-Up Considerations

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device terminals. To guard against such power-up problems, take these precautions:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device ( $V_{CCA}$  for all four of these devices).
3. Tie  $\overline{OE}$  to  $V_{CCA}$  with a pullup resistor so that it ramps with  $V_{CCA}$ .
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with  $V_{CCA}$ . Otherwise, keep DIR low.

Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, [SCEA021](#).

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)
- *Texas Instruments Voltage-Level-Translation Devices*, [SCEA021](#)

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCC3245ADBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCC3245A	<a href="#">Samples</a>
SN74LVCC3245ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	<a href="#">Samples</a>
SN74LVCC3245ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	<a href="#">Samples</a>
SN74LVCC3245ADBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	<a href="#">Samples</a>
SN74LVCC3245ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	<a href="#">Samples</a>
SN74LVCC3245ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	<a href="#">Samples</a>
SN74LVCC3245ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	<a href="#">Samples</a>
SN74LVCC3245ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	<a href="#">Samples</a>
SN74LVCC3245ADWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	<a href="#">Samples</a>
SN74LVCC3245ANSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	<a href="#">Samples</a>
SN74LVCC3245ANSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	<a href="#">Samples</a>
SN74LVCC3245ANSRG4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	<a href="#">Samples</a>
SN74LVCC3245APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	<a href="#">Samples</a>
SN74LVCC3245APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	<a href="#">Samples</a>
SN74LVCC3245APWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	<a href="#">Samples</a>
SN74LVCC3245APWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	<a href="#">Samples</a>
SN74LVCC3245APWT	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCC3245APWTG4	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN74LVCC3245A :

- Enhanced Product: [SN74LVCC3245A-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCC3245ADBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCC3245ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVCC3245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ADWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ANSR	SO	NS	24	2000	330.0	24.4	8.3	15.4	2.6	12.0	24.0	Q1
SN74LVCC3245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVCC3245APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

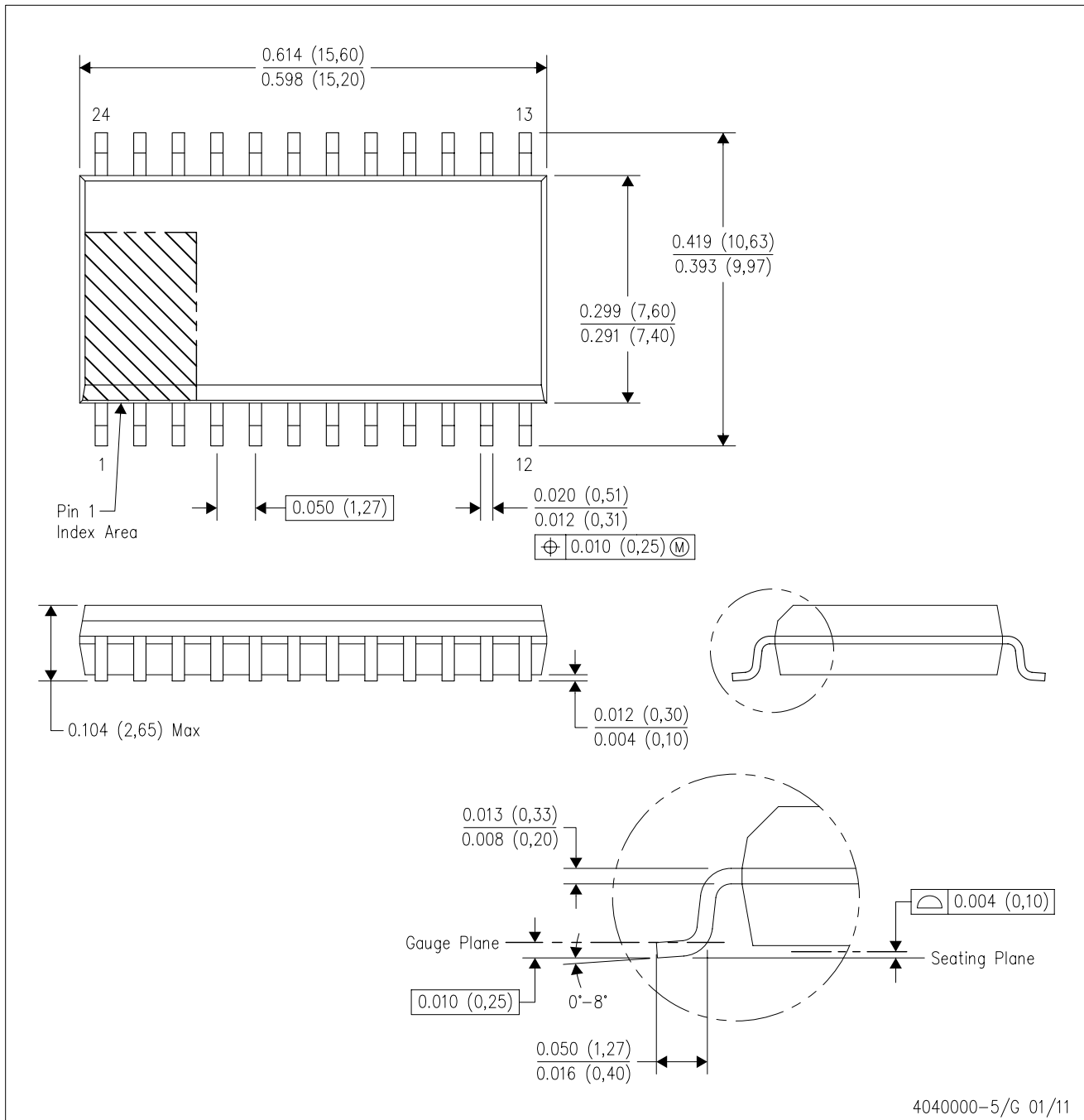
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCC3245ADBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
SN74LVCC3245ADBR	SSOP	DB	24	2000	367.0	367.0	38.0
SN74LVCC3245ADWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVCC3245ADWR	SOIC	DW	24	2000	364.0	364.0	27.0
SN74LVCC3245ADWRG4	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVCC3245ANSR	SO	NS	24	2000	367.0	367.0	45.0
SN74LVCC3245APWR	TSSOP	PW	24	2000	367.0	367.0	38.0
SN74LVCC3245APWT	TSSOP	PW	24	250	367.0	367.0	38.0

DW (R-PDSO-G24)

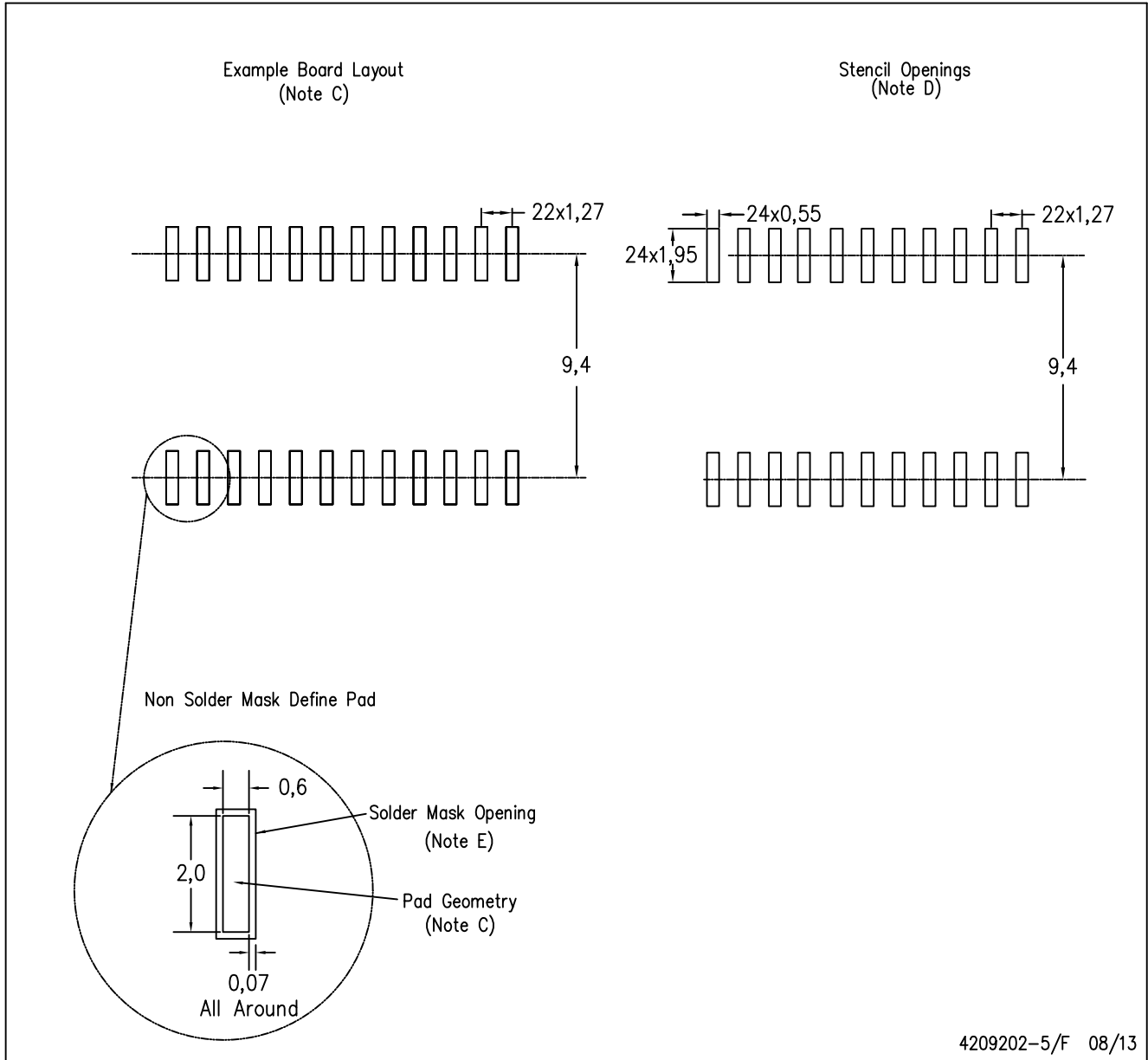
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4209202-5/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

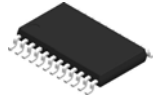
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150



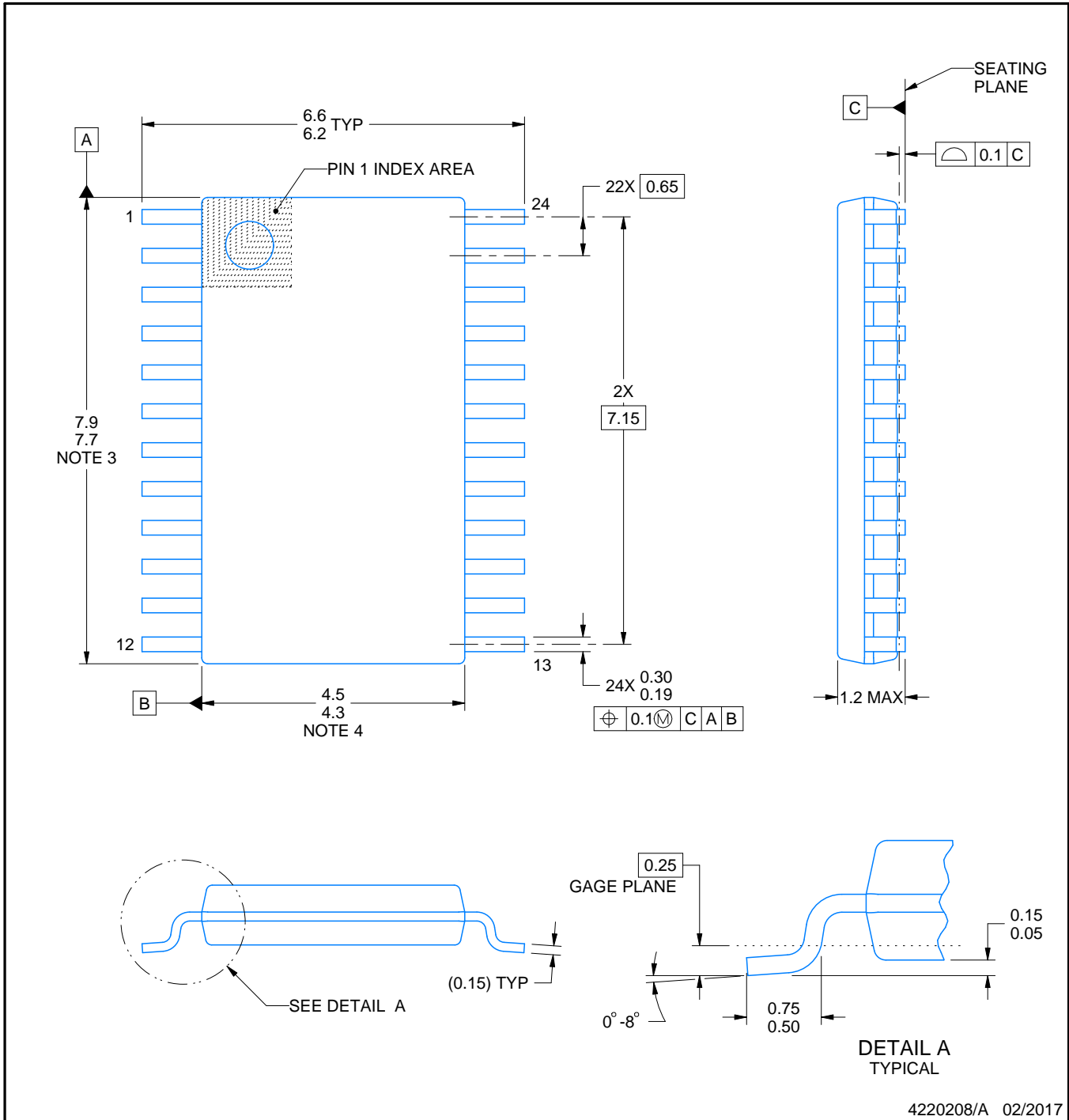
PW0024A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

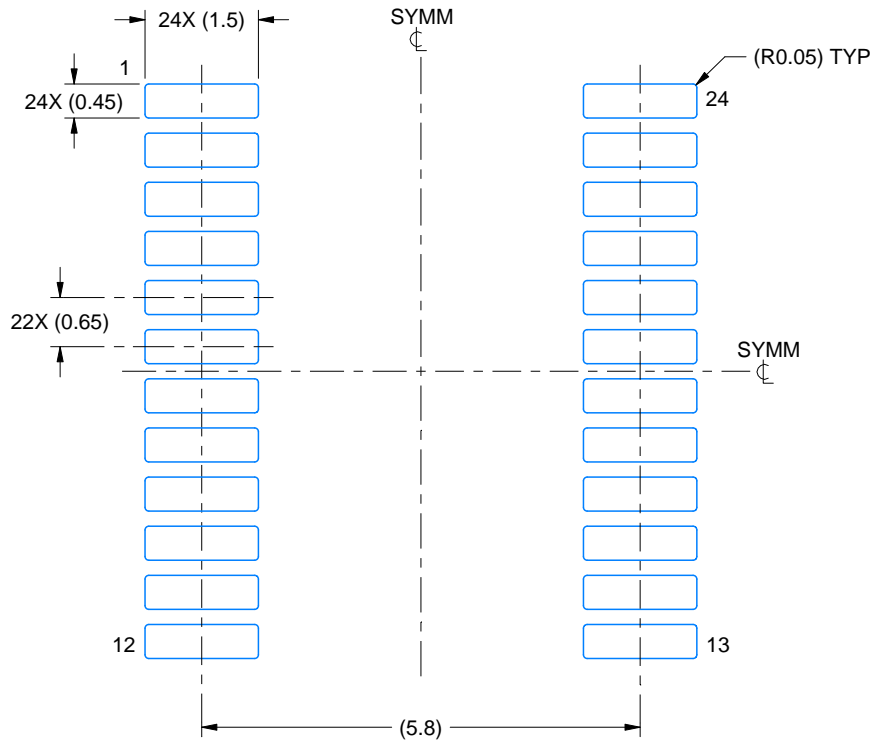
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

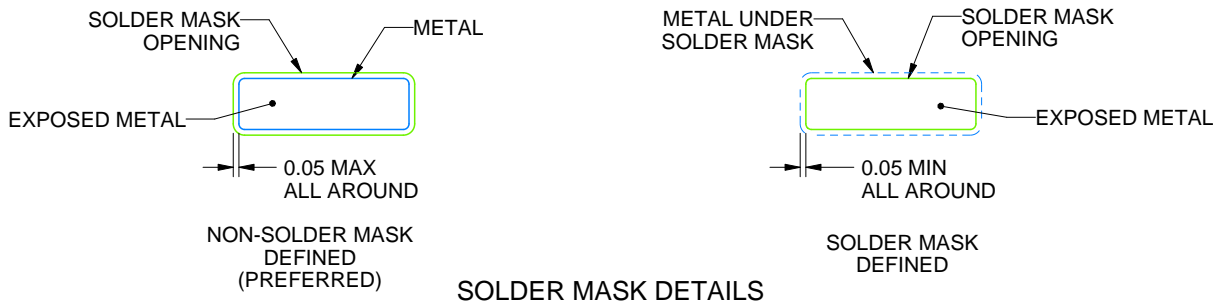
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

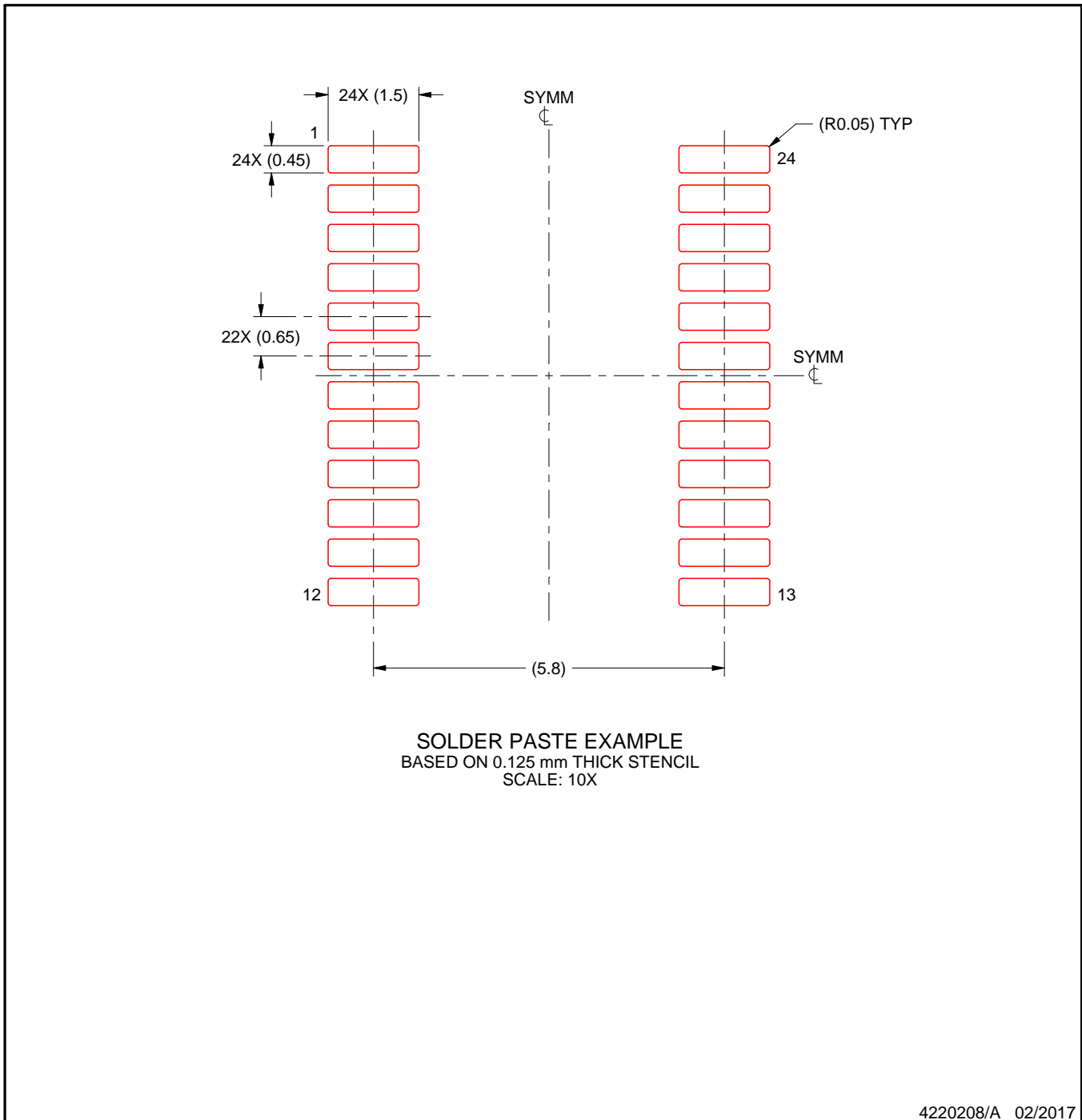
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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