

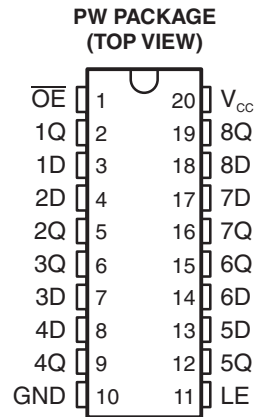


**THE DATASHEET OF  
SN74LV373AIPWRG4Q1**



## FEATURES

- Qualified for Automotive Applications
- 2-V to 5.5-V  $V_{CC}$  Operation
- Maximum  $t_{pd}$  of 8.5 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2.3 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17



## DESCRIPTION/ORDERING INFORMATION

The SN74LV373A device is an octal transparent D-type latch designed for 2-V to 5.5-V  $V_{CC}$  operation.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  shall be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – PW	Reel of 2000	SN74LV373AIPWRQ1	LV373AI

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



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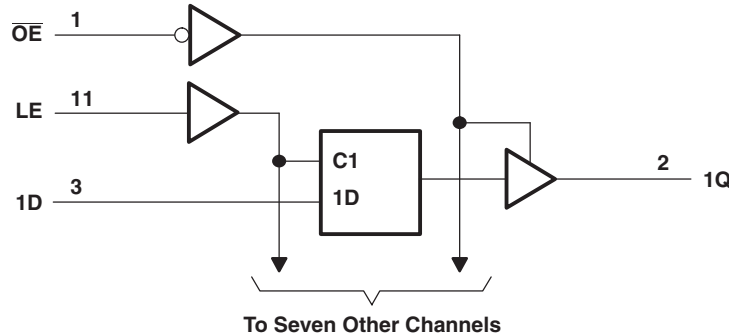
# SN74LV373A-Q1 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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**FUNCTION TABLE  
(EACH LATCH)**

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

**LOGIC DIAGRAM (POSITIVE LOGIC)**



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
$V_O$	Output voltage range <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current		-20	mA
		$V_I < 0$		
$I_{OK}$	Output clamp current		-50	mA
		$V_O < 0$		
$I_O$	Continuous output current		$\pm 35$	mA
		$V_O = 0$ to $V_{CC}$		
	Continuous current through $V_{CC}$ or GND		$\pm 70$	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>		83	$^{\circ}\text{C}/\text{W}$
$T_{stg}$	Storage temperature range	-65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	2	5.5	V	
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.3$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.3$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$		
$V_I$	Input voltage	0	5.5	V	
$V_O$	Output voltage	High or low state	0	$V_{CC}$	V
		3-state	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$	–50	$\mu\text{A}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	–2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	–8		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	–16		
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$	50	$\mu\text{A}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	8		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	16		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	200	ns/V	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	100		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	20		
$T_A$	Operating free-air temperature	–40	85	$^{\circ}\text{C}$	

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	TYP	MAX	UNIT
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	2 V to 5.5 V	$V_{CC} - 0.1$		V	
	$I_{OH} = -2\ \text{mA}$	2.3 V	2			
	$I_{OH} = -8\ \text{mA}$	3 V	2.48			
	$I_{OH} = -16\ \text{mA}$	4.5 V	3.8			
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	2 V to 5.5 V	0.1		V	
	$I_{OL} = 2\ \text{mA}$	2.3 V	0.4			
	$I_{OL} = 8\ \text{mA}$	3 V	0.44			
	$I_{OL} = 16\ \text{mA}$	4.5 V	0.55			
$I_I$	$V_I = 5.5\text{ V or GND}$	0 to 5.5 V	$\pm 1$		$\mu\text{A}$	
$I_{OZ}$	$V_O = V_{CC}\text{ or GND}$	5.5 V	$\pm 5$		$\mu\text{A}$	
$I_{CC}$	$V_I = V_{CC}\text{ or GND, } I_O = 0$	5.5 V	20		$\mu\text{A}$	
$I_{off}$	$V_I\text{ or }V_O = 0\text{ to }5.5\text{ V}$	0	5		$\mu\text{A}$	
$C_i$	$V_I = V_{CC}\text{ or GND}$	3.3 V	2.9		pF	

# SN74LV373A-Q1

## OCTAL TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

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### Timing Requirements

over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

		MIN	MAX	UNIT
$t_w$	Pulse duration, LE high	6.5		ns
$t_{su}$	Setup time, data before LE↓	High or low	5	ns
$t_h$	Hold time, data after LE↓	High or low	1.5	ns

### Timing Requirements

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

		MIN	MAX	UNIT
$t_w$	Pulse duration, LE high	5		ns
$t_{su}$	Setup time, data before LE↓	High or low	4	ns
$t_h$	Hold time, data after LE↓	High or low	1	ns

### Timing Requirements

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

		MIN	MAX	UNIT
$t_w$	Pulse duration, LE high	5		ns
$t_{su}$	Setup time, data before LE↓	High or low	4	ns
$t_h$	Hold time, data after LE↓	High or low	1	ns

### Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	MAX	UNIT
$t_{pd}$	D	Q	$C_L = 15\text{ pF}$	1	17	ns
	LE	Q		1	19	
$t_{en}$	$\overline{OE}$	Q		1	19	ns
$t_{dis}$	$\overline{OE}$	Q		1	15	ns
$t_{pd}$	D	Q	$C_L = 50\text{ pF}$	1	21	ns
	LE	Q		1	22	
$t_{en}$	$\overline{OE}$	Q		1	22	ns
$t_{dis}$	$\overline{OE}$	Q		1	19	ns
$t_{sk(o)}$			$C_L = 50\text{ pF}$		2	ns

### Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	MAX	UNIT
$t_{pd}$	D	Q	$C_L = 15\text{ pF}$	1	13.5	ns
	LE	Q		1	13	
$t_{en}$	$\overline{OE}$	Q		1	13.5	ns
$t_{dis}$	$\overline{OE}$	Q		1	12	ns
$t_{pd}$	D	Q	$C_L = 50\text{ pF}$	1	17	ns
	LE	Q		1	16.5	
$t_{en}$	$\overline{OE}$	Q		1	17	ns
$t_{dis}$	$\overline{OE}$	Q		1	15	ns
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1.5	ns

## Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	MAX	UNIT	
$t_{pd}$	D	Q	$C_L = 15\text{ pF}$	1	8.5	ns	
	LE	Q		1	8.5		
$t_{en}$	$\overline{OE}$	Q		1	9.5	ns	
$t_{dis}$	$\overline{OE}$	Q		1	8.5	ns	
$t_{pd}$	D	Q	$C_L = 50\text{ pF}$	1	10.5	ns	
	LE	Q		1	10.5		
$t_{en}$	$\overline{OE}$	Q		1	11.5	ns	
$t_{dis}$	$\overline{OE}$	Q		1	10.5	ns	
$t_{sk(o)}$				$C_L = 50\text{ pF}$		1	ns

## Noise Characteristics<sup>(1)</sup>

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.6	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

## Operating Characteristics

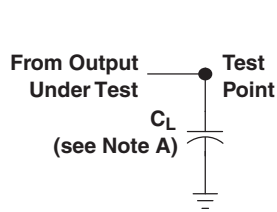
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC}$	TYP	UNIT	
$C_{pd}$	Power dissipation capacitance (outputs enabled)	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	17.4	pF
			5 V	19.5	

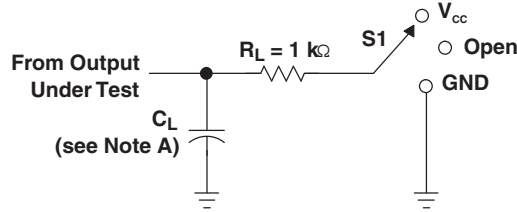
# SN74LV373A-Q1 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION

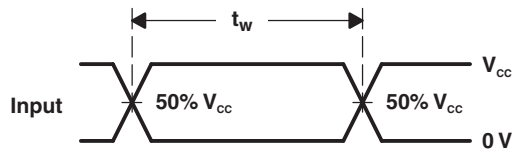


LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

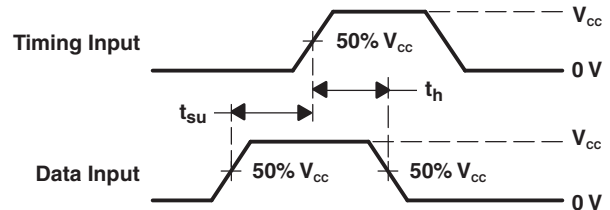


LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS

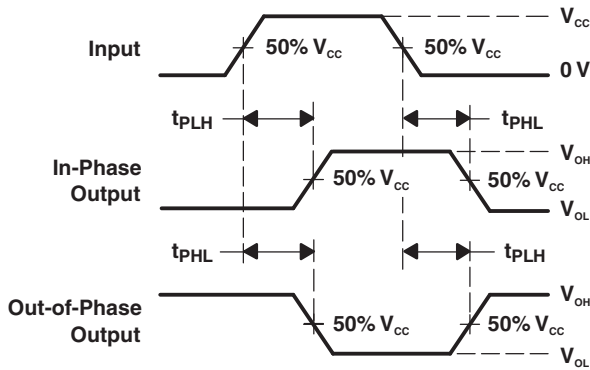
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND
Open Drain	$V_{CC}$



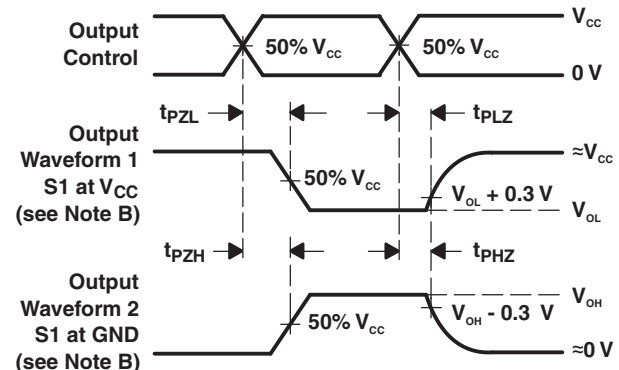
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
  - The outputs are measured one at a time, with one input transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LV373AIPWRG4Q1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV373AI	<a href="#">Samples</a>
SN74LV373AIPWRQ1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	LV373AI	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN74LV373A-Q1 :**

- Catalog: [SN74LV373A](#)

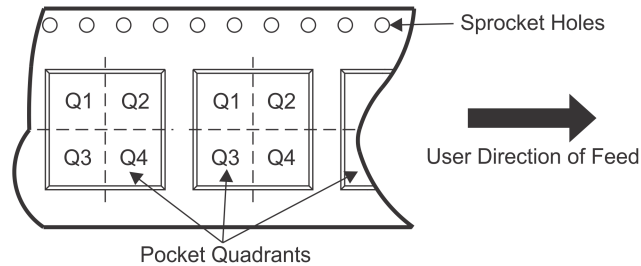
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV373AIPWRG4Q1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV373AIPWRG4Q1	TSSOP	PW	20	2000	367.0	367.0	38.0

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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