



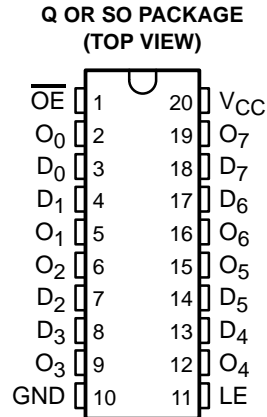
**THE DATASHEET OF  
CY74FCT2373CTSOCT**



# CY74FCT2373T 8-BIT LATCH WITH 3-STATE OUTPUTS

SCCS039B – SEPTEMBER 1994 – REVISED OCTOBER 2001

- Function and Pinout Compatible With the Fastest Bipolar Logic
- 25-Ω Output Series Resistors Reduce Transmission-Line Reflection Noise
- Reduced  $V_{OH}$  (Typically = 3.3 V) Version of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- 3-State Outputs
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Fully Compatible With TTL Input and Output Logic Levels
- 12-mA Output Sink Current  
15-mA Output Source Current



## description

The CY74FCT2373T is an 8-bit, high-speed CMOS, TTL-compatible buffered latch with 3-state outputs that is ideal for driving high-capacitance loads, such as memory and address buffers. On-chip 25-Ω termination resistors at the outputs reduce system noise caused by reflections. The CY74FCT2373T can replace the CY74FCT373T to reduce noise in an existing design.

When the latch-enable (LE) input is high, the flip-flops appear transparent to the data. Data that meets the required setup times are latched when LE transitions from high to low. Data appears on the bus when the output-enable ( $\overline{OE}$ ) input is low. When  $\overline{OE}$  is high, the bus output is in the high-impedance state. In this mode, data can be entered into the latches.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

TA	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	4.7	CY74FCT2373CTQCT	FCT2373C
	SOIC – SO	Tube	4.7	CY74FCT2373CTSOC	FCT2373C
		Tape and reel	4.7	CY74FCT2373CTSOCT	
	QSOP – Q	Tape and reel	5.2	CY74FCT2373ATQCT	FCT2373A
	QSOP – Q	Tape and reel	8	CY74FCT2373TQCT	FCT2373

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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**CY74FCT2373T**  
**8-BIT LATCH**  
**WITH 3-STATE OUTPUTS**

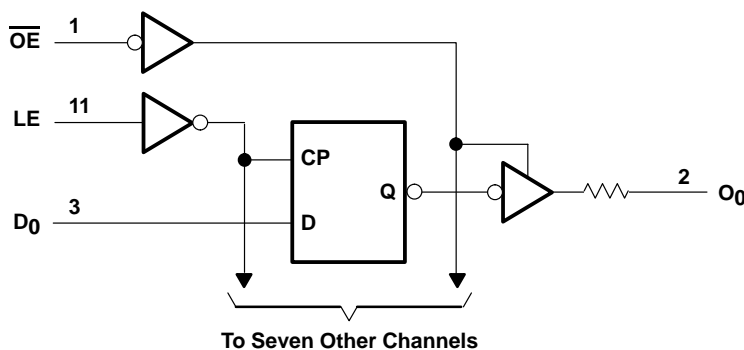
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**FUNCTION TABLE**

INPUTS			OUTPUT
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

H = High logic level, L = Low logic level,  
 X = Don't care, Z = High-impedance  
 state,  $Q_0$  = Previous state of flip flops  
 ( $Q_0-1$ )

**logic diagram**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range to ground potential	-0.5 V to 7 V
DC input voltage range	-0.5 V to 7 V
DC output voltage range	-0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package	68°C/W
SO package	58°C/W
Ambient temperature range with power applied, $T_A$	-65°C to 135°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 2)**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{OH}$ High-level output current			-15	mA
$I_{OL}$ Low-level output current			12	mA
$T_A$ Operating free-air temperature	-40		85	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.



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**CY74FCT2373T**  
**8-BIT LATCH**  
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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{IN} = -18\text{ mA}$		-0.7	-1.2	V
$V_{OH}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -15\text{ mA}$	2.4	3.3		V
$V_{OL}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OL} = 12\text{ mA}$		0.3	0.55	V
$R_{OUT}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OL} = 12\text{ mA}$	20	28	40	$\Omega$
$V_{hys}$	All inputs			0.2		V
$I_I$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = V_{CC}$			5	$\mu\text{A}$
$I_{IH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = 2.7\text{ V}$			$\pm 1$	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = 0.5\text{ V}$			$\pm 1$	$\mu\text{A}$
$I_{OZH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{OUT} = 2.7\text{ V}$			10	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{OUT} = 0.5\text{ V}$			-10	$\mu\text{A}$
$I_{OS}^\ddagger$	$V_{CC} = 5.25\text{ V}$ ,	$V_{OUT} = 0\text{ V}$	-60	-120	-225	mA
$I_{off}$	$V_{CC} = 0\text{ V}$ ,	$V_{OUT} = 4.5\text{ V}$			$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$		0.1	0.2	mA
$\Delta I_{CC}$	$V_{CC} = 5.25\text{ V}$ , $V_{IN} = 3.4\text{ V}^\S$ , $f_1 = 0$ , Outputs open			0.5	2	mA
$I_{CCD}^\parallel$	$V_{CC} = 5.25\text{ V}$ , One input switching at 50% duty cycle, Outputs open, $OE = GND$ , $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$			0.06	0.12	mA/MHz
$I_C^\#$	$V_{CC} = 5.25\text{ V}$ , Outputs open, $OE = GND$ , $LE = V_{CC}$	One input switching at $f_1 = 10\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	0.7	1.4	mA
			$V_{IN} = 3.4\text{ V}$ or GND	1	2.4	
		Eight bits switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	1.3	2.6	
			$V_{IN} = 3.4\text{ V}$ or GND	3.3	10.6	
$C_i$				6	10	pF
$C_o$				8	12	pF

† Typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

§ Per TTL-driven input ( $V_{IN} = 3.4\text{ V}$ ); all other inputs at  $V_{CC}$  or GND

¶ This parameter is derived for use in total power-supply calculations.

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD}(f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4\text{ V}$ )

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_{CC}$  formula.



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**8-BIT LATCH**  
**WITH 3-STATE OUTPUTS**

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

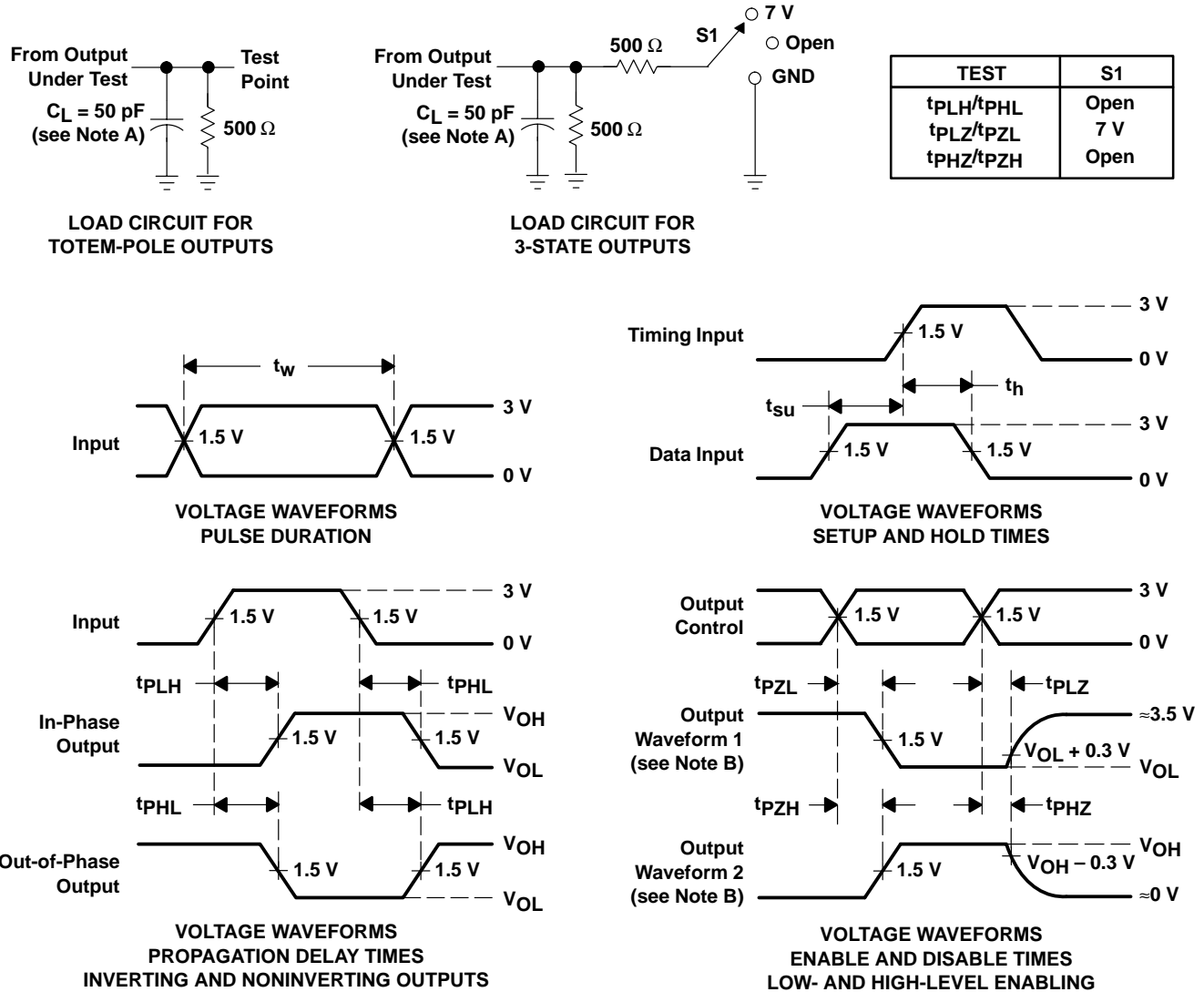
		CY74FCT2373T		CY74FCT2373AT		CY74FCT2373CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, LE high	6		5		5		ns
$t_{su}$	Setup time, D to LE	2		2		2		ns
$t_h$	Hold time, D to LE	1.5		1.5		1.5		ns

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT2373T		CY74FCT2373AT		CY74FCT2373CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	O	1.5	8	1.5	5.2	1.5	4.7	ns
$t_{PHL}$			1.5	8	1.5	5.2	1.5	4.7	
$t_{PLH}$	LE	O	2	13	2	8.5	2	5.5	ns
$t_{PHL}$			2	13	2	8.5	2	5.5	
$t_{PZH}$	$\overline{OE}$	O	1.5	11	1.5	6.5	1.5	5.5	ns
$t_{PZL}$			1.5	11	1.5	6.5	1.5	5.5	
$t_{PHZ}$	$\overline{OE}$	O	1.5	7	1.5	5.5	1.5	5	ns
$t_{PLZ}$			1.5	7	1.5	5.5	1.5	5	



PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT2373CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT2373C	<a href="#">Samples</a>
CY74FCT2573ATQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT2573A	<a href="#">Samples</a>
CY74FCT2573CTQCT	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT2573C	<a href="#">Samples</a>
CY74FCT2573CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT2573C	<a href="#">Samples</a>
CY74FCT2573CTSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT2573C	<a href="#">Samples</a>
CY74FCT2573CTSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT2573C	<a href="#">Samples</a>
CY74FCT2573TSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT2573	<a href="#">Samples</a>
CY74FCT2573TSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT2573	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT2573ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT2573CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT2573CTSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT2573TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

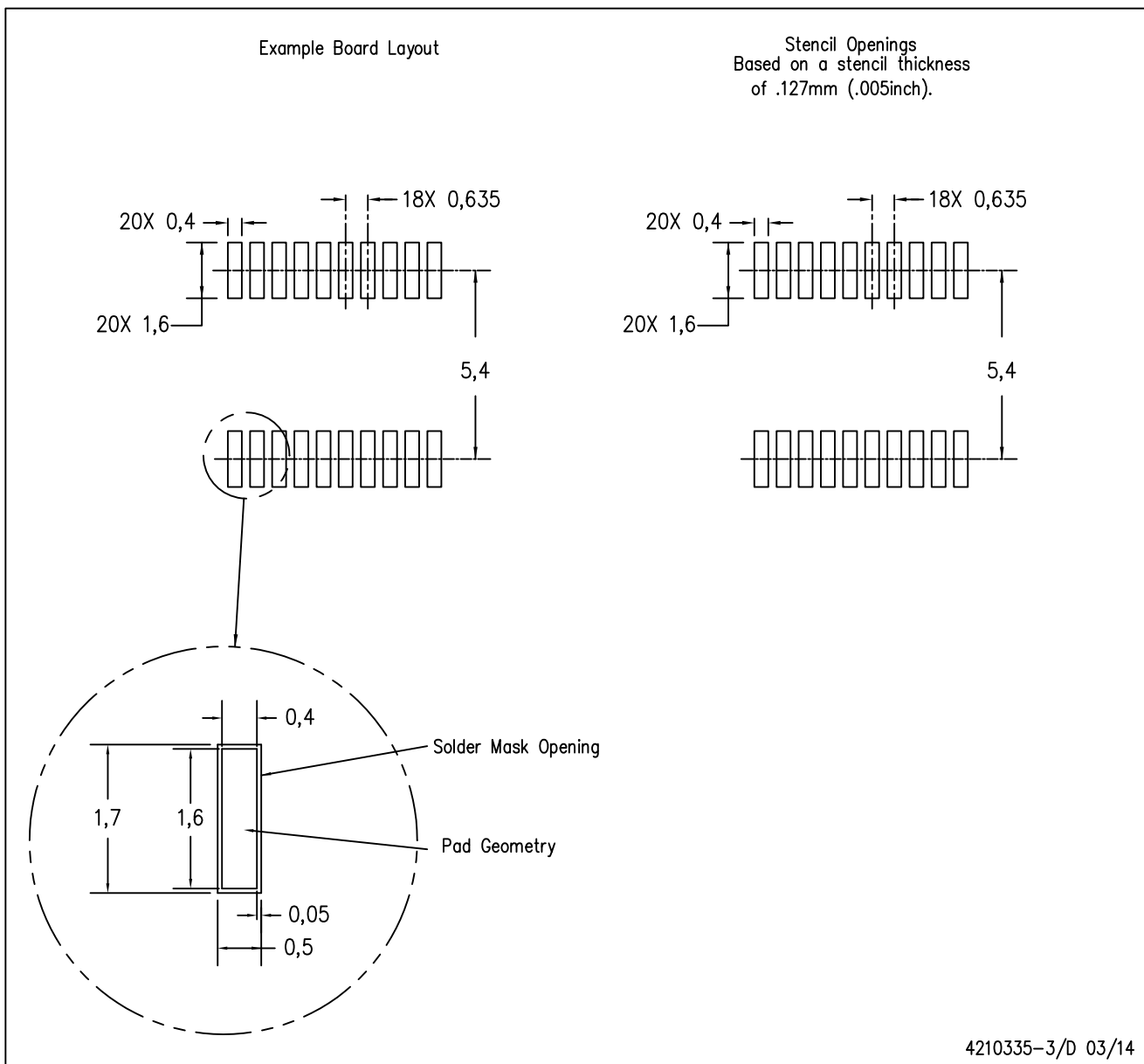

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT2573ATQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT2573CTQCT	SSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT2573CTSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT2573TSOCT	SOIC	DW	20	2000	367.0	367.0	45.0



DBQ (R-PDSO-G20)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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