



**THE DATASHEET OF  
CD40192BCN**



## CD40192BC • CD40193BC

### Synchronous 4-Bit Up/Down Decade Counter • Synchronous 4-Bit Up/Down Binary Counter

#### General Description

The CD40192BC and CD40193BC up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The CD40192BC is a BCD counter, while the CD40193BC is a binary counter.

Counting up and counting down is performed by two count inputs, one being held HIGH while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are enabled when load is a logical "0" and a clear which forces all outputs to "0" when it is at logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

All inputs are protected against damage due to static discharge by clamps to  $V_{DD}$  and  $V_{SS}$ .

#### Features

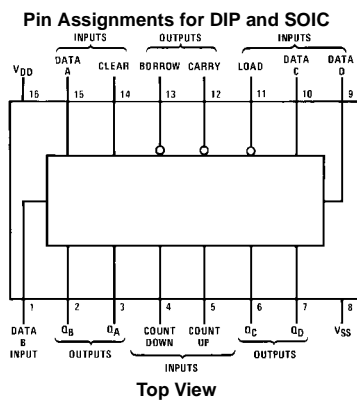
- Wide supply voltage range: 3V to 15V
- High noise immunity:  $0.45 V_{DD}$  (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- Carry and borrow outputs for easy expansion to N-bit by cascading
- Asynchronous clear
- Equivalent to: MM74C192 and MM74C193

#### Ordering Code:

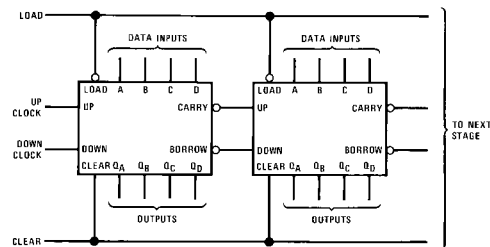
Order Number	Package Number	Package Description
CD40192BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD40193BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD40193BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Connection Diagram

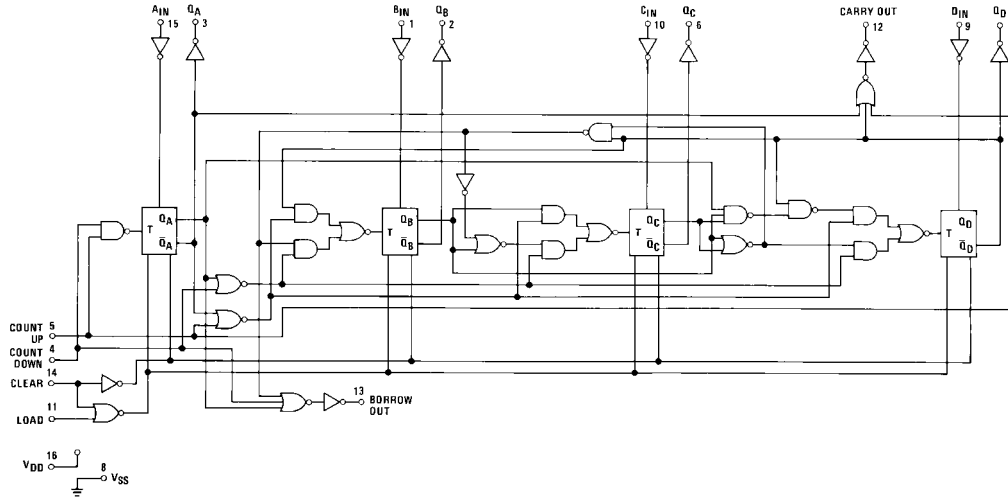


#### Cascading Packages

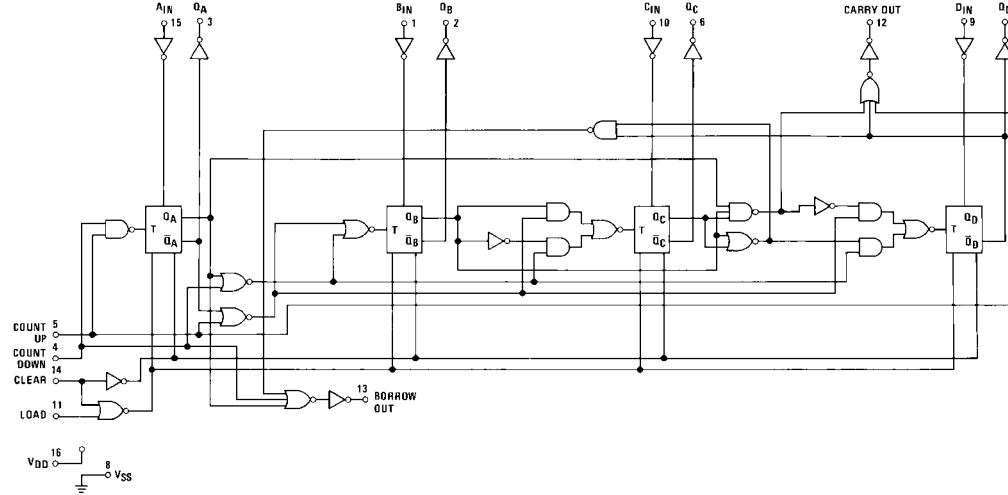


Block Diagrams

CD40192BC Synchronous 4-Bit Up/Down Decade Counter



CD40193BC Synchronous 4-Bit Up/Down Binary Counter



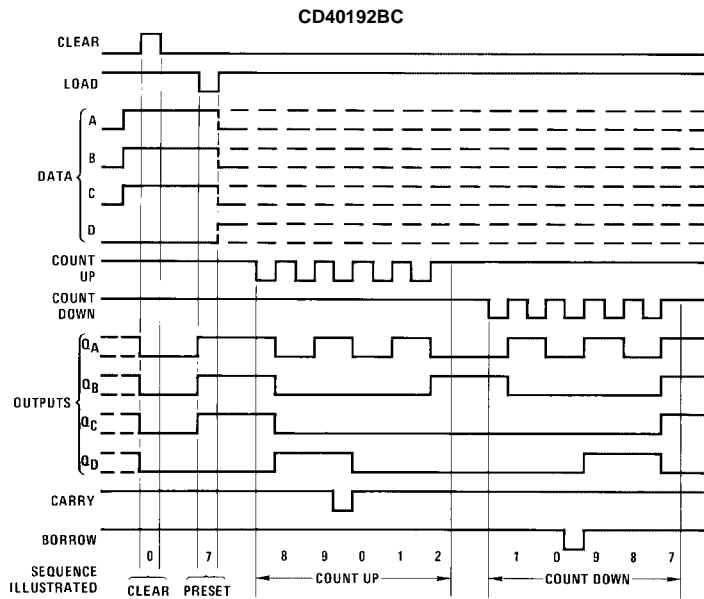
Absolute Maximum Ratings (Note 1)			Recommended Operating Conditions (Note 2)						
(Note 2)			(Note 2)						
DC Supply Voltage ( $V_{DD}$ )	-0.5 to +18 $V_{DC}$		DC Supply Voltage ( $V_{DD}$ )	3 to 15 $V_{DC}$					
Input Voltage ( $V_{IN}$ )	-0.5 to $V_{DD}$ +0.5 $V_{DC}$		Input Voltage ( $V_{IN}$ )	0 to $V_{DD}$ $V_{DC}$					
Storage Temperature Range ( $T_S$ )	-65°C to +150°C		Operating Temperature Range ( $T_A$ )	-55°C to +125°C					
Power Dissipation ( $P_D$ )			CD40192BC, CD40193BC						
Dual-In-Line	700 mW		<b>Note 1:</b> "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Recommended Operating Conditions" and Electrical Characteristics tables provide conditions for actual device operation.						
Small Outline	500 mW		<b>Note 2:</b> $V_{SS} = 0V$ unless otherwise specified.						
Lead Temperature ( $T_L$ )									
(Soldering, 10 seconds)	260°C								
DC Electrical Characteristics (Note 3)									
Symbol	Parameter	Conditions	-55°C		+25°C		+125°C		Units
			Min	Max	Min	Typ	Max	Min	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$ $V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$ $V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$		5 10 20			5 10 20	150 300 600	$\mu A$
$V_{OL}$	LOW Level Output Voltage	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		0.05 0.05 0.05			0.05 0.05 0.05	0.05 0.05 0.05	V
$V_{OH}$	HIGH Level Output Voltage	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$	4.95 9.95 14.95		4.95 9.95 14.95			4.95 9.95 14.95	V
$V_{IL}$	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ $V_{DD} = 10V, V_O = 1V$ or $9V$ $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		1.5 3.0 4.0			1.5 3.0 4.0	1.5 3.0 4.0	V
$V_{IH}$	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ $V_{DD} = 10V, V_O = 1V$ or $9V$ $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	3.5 7.0 11.0		3.5 7.0 11.0			3.5 7.0 11.0	V
$I_{OL}$	LOW Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 0.4V$ $V_{DD} = 10V, V_O = 0.5V$ $V_{DD} = 15V, V_O = 1.5V$	0.64 1.6 4.2		0.51 1.3 3.4	0.88 2.25 8.8		0.36 0.9 2.4	mA
$I_{OH}$	HIGH Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 4.6V$ $V_{DD} = 10V, V_O = 9.5V$ $V_{DD} = 15V, V_O = 13.5V$	-0.64 -1.6 -4.2		-0.51 -1.3 -3.4	-0.88 -2.25 -8.8		-0.36 -0.9 -2.4	mA
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$ $V_{DD} = 15V, V_{IN} = 15V$		-0.1 0.1		$-10^{-5}$ $10^{-5}$	-0.1 0.1	-1.0 1.0	$\mu A$
<b>Note 3:</b> AC Parameters are guaranteed by DC correlated testing.									
<b>Note 4:</b> $I_{OH}$ and $I_{OL}$ are tested one output at a time.									

**AC Electrical Characteristics** (Note 3)T<sub>A</sub> = 25°C, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200 kΩ, input t<sub>r</sub> = t<sub>f</sub> = 20 ns, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>PHL</sub> or t <sub>PLH</sub>	Propagation Delay Time from Count Up or Count Down to Q	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		250 100 80	400 160 130	ns
t <sub>PHL</sub> or t <sub>PLH</sub>	Propagation Delay Time from Count Up to Carry	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		120 50 40	200 80 65	ns
t <sub>PHL</sub> or t <sub>PLH</sub>	Propagation Delay Time from Count Down to Borrow	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		120 50 40	200 80 65	ns
t <sub>SU</sub>	Time Prior to Load That Data Must Be Present	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		100 30 25	160 50 40	ns
t <sub>PHL</sub>	Propagation Delay Time from Clear to Q	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		130 60 50	220 100 80	ns
t <sub>PLH</sub> or t <sub>PHL</sub>	Propagation Delay Time from Load to Q	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		300 120 95	480 190 150	ns
t <sub>TLH</sub> or t <sub>THL</sub>	Output Transition Time	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		100 50 40	200 100 80	ns
f <sub>CL</sub>	Maximum Count Frequency	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V	2.5 6 7.5	4 10 12.5		MHz
t <sub>rCL</sub> or t <sub>fCL</sub>	Maximum Count Rise or Fall Time	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V	15 5 1			μs
t <sub>WH</sub> , t <sub>WL</sub>	Minimum Count Pulse Width	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		120 35 28	200 80 65	ns
t <sub>WH</sub>	Minimum Clear Pulse Width	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		300 120 95	480 190 150	ns
t <sub>WL</sub>	Minimum Load Pulse Width	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		100 40 32	160 65 55	ns
C <sub>IN</sub>	Average Input Capacitance	Load and Data Inputs (A,B,C,D) Count Up, Count Down and Clear		5 10	7.5 15	pF
C <sub>PD</sub>	Power Dissipation Capacity	(Note 5)		100		pF

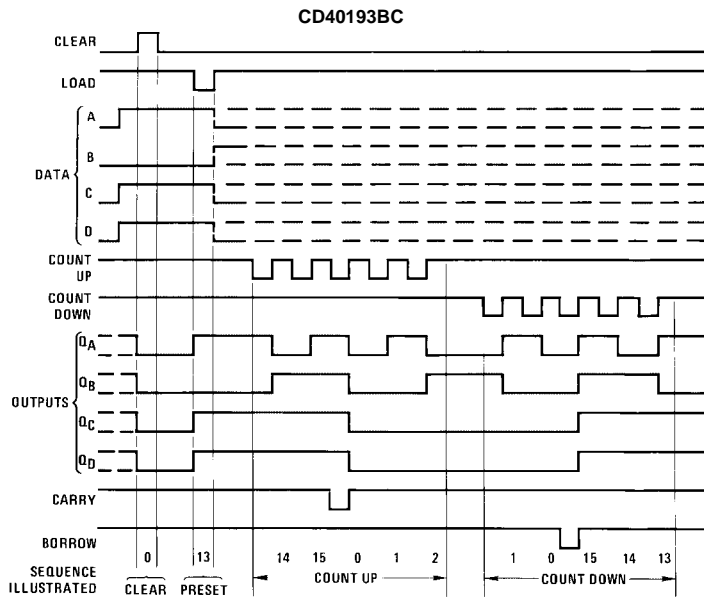
**Note 5:** C<sub>PD</sub> determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics application note, AN-90.

## Timing Diagrams



Sequence:

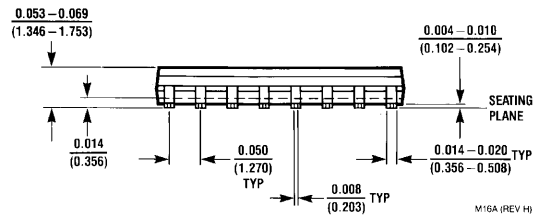
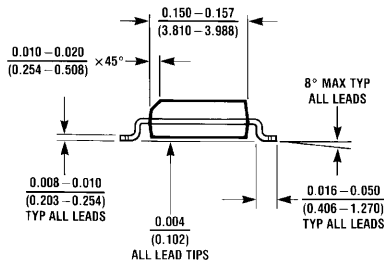
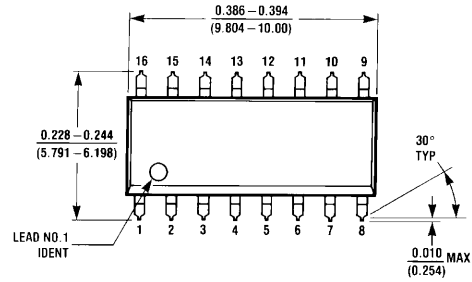
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one and two.
4. Count down to one, zero, borrow, nine, eight and seven.



Sequence:

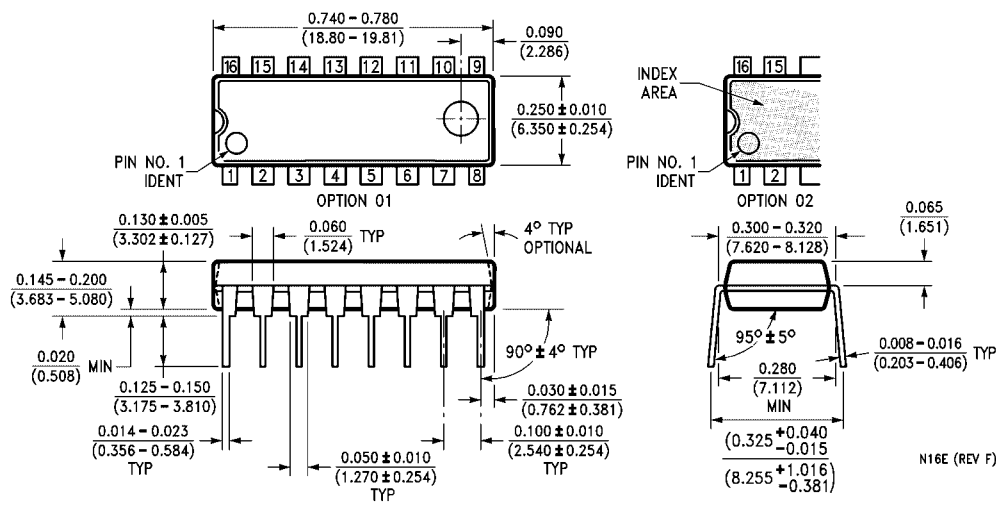
1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one and two.
4. Count down to one, zero, borrow, fifteen, fourteen and thirteen.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N16E**

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