THE DATASHEET OF

NB4N7132DTG

NB4N7132

Link Replicator for Fibre Channel, Gigabit Ethernet, HDTV and SATA

Up to 1.5 Gb/s

Description

The NB4N7132 is a high performance 3.3 V Serial Link Replicator which provides the function of serial loop replication and serial loopback control commonly required in Fibre Channel, GbE, HDTV and SATA applications. Other popular applications include Host Bus Adaptors for routing between internal and external connectors, and hot−pluggable links between redundant switch fabric cards.

IN is sent to both OUT0 and OUT1; each output is enabled by OE0 and OE1 when HIGH. OUT0 can select either IN or IN1 via the MUX0 pin. Likewise, OUT1 can select between IN or IN0 via the MUX1 pin. Out can select between IN0 and IN1.

In Link Replicator applications, such as the Line Card to Switch Card links, IN is transmitted to both OUT0 and OUT1 which either IN0 or IN1 is selected at OUT. In Host Adapter applications, IN goes to OUT0 (an internal connector) which returns data on IN0. IN0 is looped to OUT1 (an external connector) which returns data on IN1 and then back to the SerDes on OUT.

The NB4N7132 is packaged in a 4.7 mm x 9.7 mm TSSOP−28.

Features

- Replicates Fibre Channel, Gigabit Ethernet, HDTV, and Serial ATA (SATA) Links
- T11 Fibre Channel Complaint at 1.0625 Gb/s
- No External Components Required
- IEEE802.3z Gigabit Ethernet Compliant at 1.25 Gb/s
- SMPTE−292M Compliant at 1.485 Gb/s
- 450 mW Maximum Power Dissipation
- Operating Range: V_{CC} = 3.135 V to 3.465 V
- 28−pin, 4.4 mm x 9.7 mm TSSOP Package
- These are Pb−Free Devices

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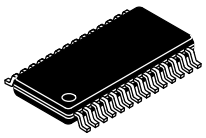
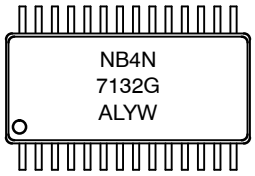


28 Lead TSSOP
DT SUFFIX
CASE 948A

MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

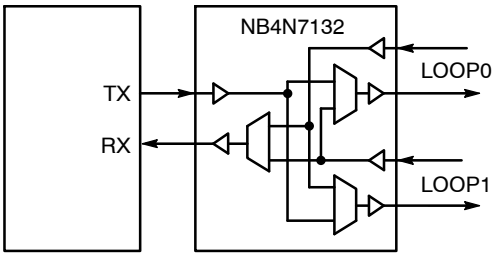


Figure 1. Simplified Application

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

TYPICAL APPLICATIONS CIRCUIT

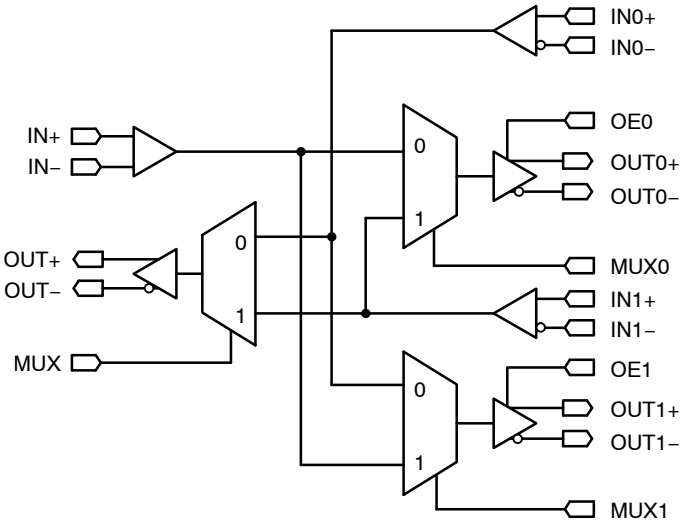


Figure 2. Simplified Block Diagram

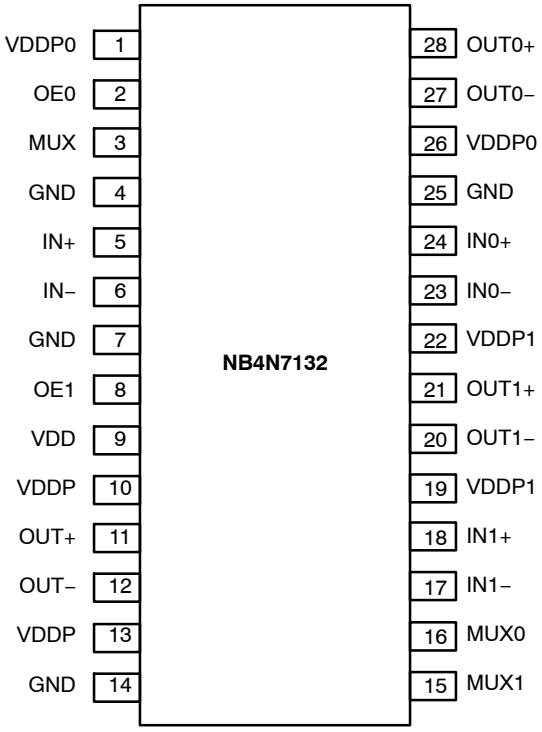


Figure 3. Pin Diagram for TSSOP−28

Table 1. OE, OUTPUT ENABLE FUNCTION

OEx*	Function
1	Outputs Enabled
0	Outputs Disabled OUTn+ = H, OUTn− = H

*Defaults to HIGH when left open

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
5, 6 24, 23 18, 17	IN+, IN− IN0+, IN0− IN1+, IN1−	LVPECL Input LVPECL Input LVPECL Input	Non−inverted, Inverted, Differential Data Inputs internally biased to Approximately 1.2 V.
11, 12 28, 27 21, 20	OUT+, OUT− OUT0+, OUT0− OUT1+, OUT1−	LVPECL Output LVPECL Output LVPECL Output	Non−inverted, Inverted Differential Outputs.
2 8	OE0 OE1	LVTTL Input LVTTL Input	OE0/OE1 enables OUT0/OUT1 when HIGH. When LOW, OUTx are powered down and both OUT+ and OUT− float HIGH.
3	MUX	LVTTL Input	Selects Source for OUT, Selects Either IN0 (LOW) or IN1 (HIGH); defaults HIGH when left open.
15	MUX1	LVTTL Input	Selects Source for OUT1. Selects Either IN (HIGH) or IN0 (LOW); defaults HIGH when left open.
16	MUX0	LVTTL Input	Selects Source for OUT0. Selects either IN (LOW) or IN1 (HIGH); defaults HIGH when left open.
9	VDD	Power Supply	3.3 V Positive Supply Voltage for Digital Logic.
10, 13 1, 26 19, 22	VDDP VDDP0 VDDP1	Power Supply	3.3 V supply for LVPECL output drivers. VDDP is for OUT, VDDP0 is for OUT0, and VDDP1 is for OUT1.
4, 7, 14, 25	GND	Power Supply	Negative Supply Voltage, Connected to Ground

All VDD, VDDPx and GND Pins must be externally connected to appropriate power supply to guarantee proper operation.

Table 3. ATTRIBUTES

Characteristics		Value
Internal Input Pullup Resistor		96 kΩ
ESD Protection	Human Body Model Machine Model	> 1 kV > 100 V
Moisture Sensitivity (Note 1)		Level 3
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		268 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Min	Max	Unit
V_{DD}	Positive Power Supply	GND = 0 V	0.5	4.0	V
V_{INP}	Input Voltage, PECL	GND = 0 V	−0.5	V_{DD} + 0.5	V
V_{INT}	Input Voltage, TTL	GND = 0 V	−0.5	V_{DD} + 0.5	V
I_{OUT}	Output HIGH current, PECL		−50	+50	mA
T_C	Case temperature under bias		−55	+125	°C
TA	Operating Temperature Range		−40	+85	°C
T_{stg}	Storage Temperature Range		−65	+150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−28	76 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 2)	TSSOP−28	25	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 5. DC CHARACTERISTICS V_{DD} = 3.30 V ±5%, GND = 0 V; T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage, 3.30 V ±5%	3.14		3.47	V
I_{DD}	Power Supply Current (Outputs open)		105	125	mA
P_D	Power Dissipation; Outputs Open; $V_{DD} = V_{DDmax}$			450	mW
ΔV_{IN}	Receiver Differential Voltage Amplitude; (IN, IN0, IN1), AC−Coupled, Internally Biased to 1.2 V; Differential Measurement − ($V_{INn+} - V_{INn-}$)	300		2600	mV
ΔV_{OUT50}	Output Differential Voltage Swing, peak−peak; (OUT, OUT0, OUT1) Outputs loaded / terminated with 50 Ω to V_{DD} − 2.0 V Differential Measurement − ($V_{OUTn+} - V_{OUTn-}$)	1000		2200	mV
ΔV_{OUT75}	Output Differential Voltage Swing, peak−peak; (OUT, OUT0, OUT1) Outputs loaded / terminated with 75 Ω to V_{DD} − 2.0 V Differential Measurement − ($V_{OUTn+} - V_{OUTn-}$)	1200		2200	mV
LVCMOS/LVTTL INPUTS					
V_{IH}	Input HIGH Voltage, TTL	2.0		V_{DD} + 0.5	V
V_{IL}	Input LOW Voltage, TTL	0		0.8	V
I_{IH}	Input HIGH Current, TTL; V_{IN} = 2.4 V			100	μA
I_{IL}	Input LOW Current, TTL; V_{IN} = 0.5 V	−100			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. AC CHARACTERISTICS V_{DD} = 3.3 V ±5%, GND = 0 V −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
$f_{IN\ /\ OUT}$	Input / Output Frequency Range			1.5	Gb/s
tr/tf	Output rise and Fall Times (Note 3)		140	175	ps
t_{PD}	Propagation Delay, IN to OUT		0.375	4.0	ns
T_{DJ}	Deterministic Jitter Added to Serial Input Up to 1.5 Gb/s; K28.5± Pattern			40	ps pk−pk

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Measured 20% to 80%

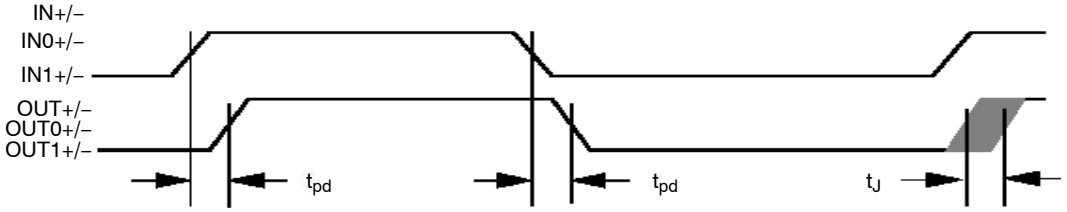


Figure 4. Timing Waveforms

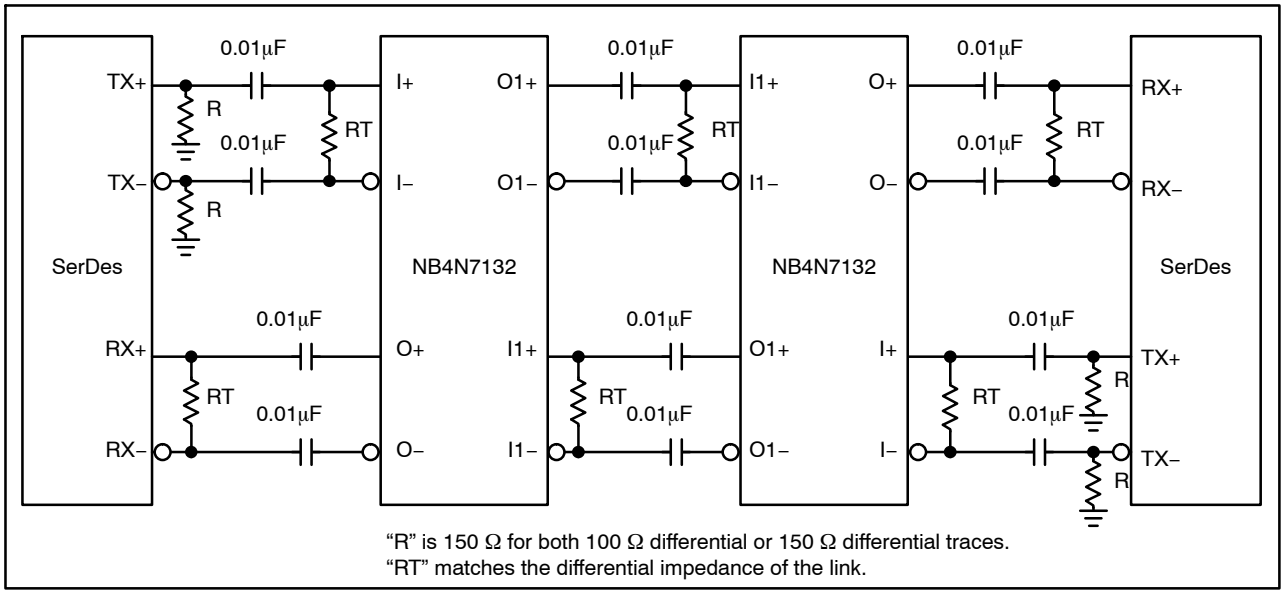


Figure 5. NB4N7132 Application Interface Example

IN+/IN− Input Functionality

The differential inputs are internally biased to ∽1.2 V. In a typical application, the differential inputs are capacitor−coupled and will swing symmetrically above and below 1.2 V, preserving a 50% duty cycle to the outputs.

With this technique, the NB4N7132 will accept any differential input allowing for LVPECL, CML, LVDS, and HSTL input levels.

OUT+ / OUT− Outputs

The OUT+ and OUT− outputs of the NB4N7132 are designed to drive differential transmission lines with nominally 50 Ω or 75 Ω characteristic impedance. These differential output buffers utilize positive emitter coupled logic (PECL) architecture, but they do not require DC output load resistors, and will operate properly with or without the resistors.

OEx Output Enable

The NB4N7132 incorporates output enable pins, OE0 and OE1, that work by powering down the output buffer and associated driving circuitry. Using this approach results in both differential outputs going HIGH, and a reduction in I_{DD} current of approx. 29 mA for each disabled output pair.

When OEx is LOW, outputs are disabled, OUTx+ and OUTx− are set HIGH.

Power Supply Bypass information

A clean power supply will optimize the performance of the device. The NB4N7132 provides separate power supply pins for the digital circuitry (V_{DD}) and LVPECL outputs (VDDPn). Placing a bypass capacitor of 0.01 μF to 0.1 μF on each VDD pin will help ensure a noise free V_{DD} power supply. The purpose of this design technique is to try and isolate the high switching noise of the digital outputs from the relatively sensitive digital core logic.

Resource Reference of Application Notes

AND8002 – Marking and Date Codes

AND8009 – ECLinPS Plus Spice I/O Model Kit

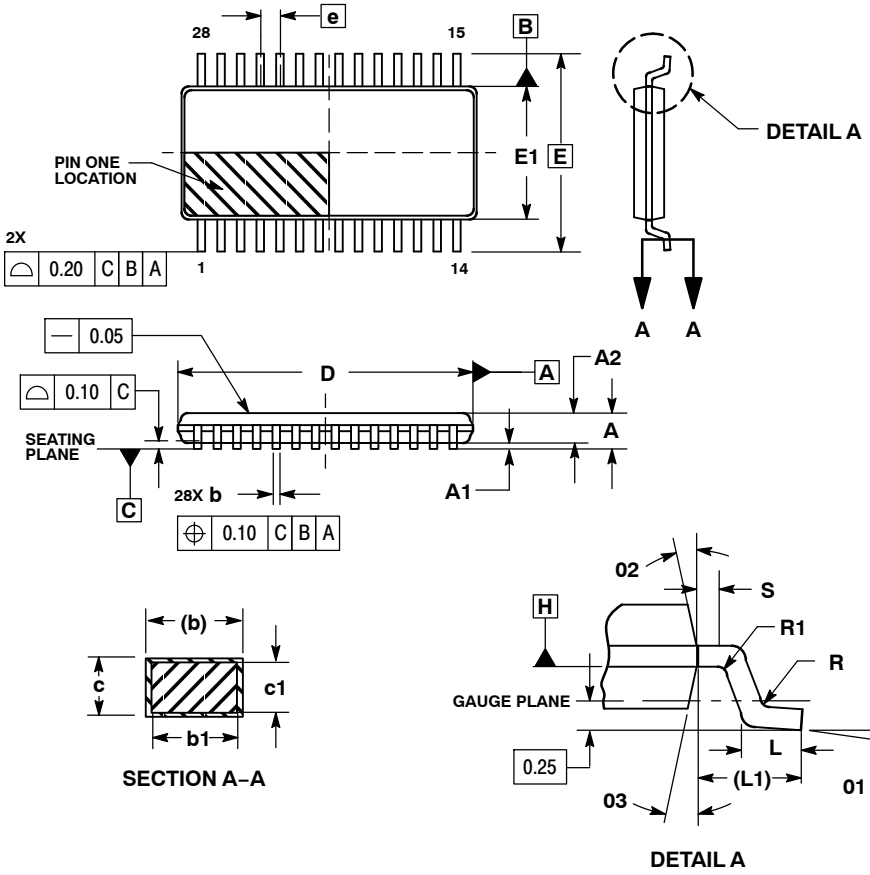
ORDERING INFORMATION

Device	Package	Shipping†
NB4N7132DTG	TSSOP−28 (Pb−Free)	50 Units / Rail
NB4N7132DTR2G	TSSOP−28 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

28 LEAD TSSOP
DT SUFFIX
CASE 948AA−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	9.60	9.80
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.45	0.75
L1	1.00 REF	
R	0.09	−−−
R1	0.09	−−−
S	0.20	−−−
01	0 °	8 °
02	12 ° REF	
03	12 ° REF	

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