THE DATASHEET OF

ADF5901WCCPZ

24 GHz VCO and PGA with 2-Channel PA Output

Data Sheet

ADF5901

FEATURES

- 24 GHz to 24.25 GHz voltage controlled oscillator (VCO)
- 2-channel 24 GHz power amplifier (PA) with 8 dBm output
- Single-ended outputs
- 2-channel muxed outputs with mute function
- Programmable output power
- N divider output (frequency discriminator)
- 24 GHz local oscillator (LO) output buffer
- 250 MHz signal bandwidth
- Power control detector
- Auxiliary 8-bit ADC
- ±5°C temperature sensor
- 4-wire serial peripheral interface (SPI)
- Electrostatic discharge (ESD) performance
  - Human body model (HBM): 2000 V
  - Charged device model (CDM): 250 V
- Qualified for automotive applications

APPLICATIONS

- Automotive radars
- Industrial radars
- Microwave radar sensors
- Industrial sensors
  - Precision instrumentation
  - Tank level sensors
  - Smart sensors
    - Door opening
    - Energy saving
- Commercial sensors: object detection and tracking
  - Cars, boats, aircraft, and UAVs (drones): collision avoidance
  - Intelligent transportation systems: intelligent traffic monitoring and control
  - Surveillance and security

GENERAL DESCRIPTION

The ADF5901 is a 24 GHz Tx monolithic microwave integrated circuit (MMIC) with an on-chip, 24 GHz VCO with PGA and dual Tx channels for radar systems. The on-chip, 24 GHz VCO generates the 24 GHz signal for the two Tx channels and the LO output. Each Tx channel contains a power control circuit. There is also an on-chip temperature sensor.

Control of all the on-chip registers is through a simple 4-wire interface.

The ADF5901 comes in a compact 32-lead, 5 mm × 5 mm LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

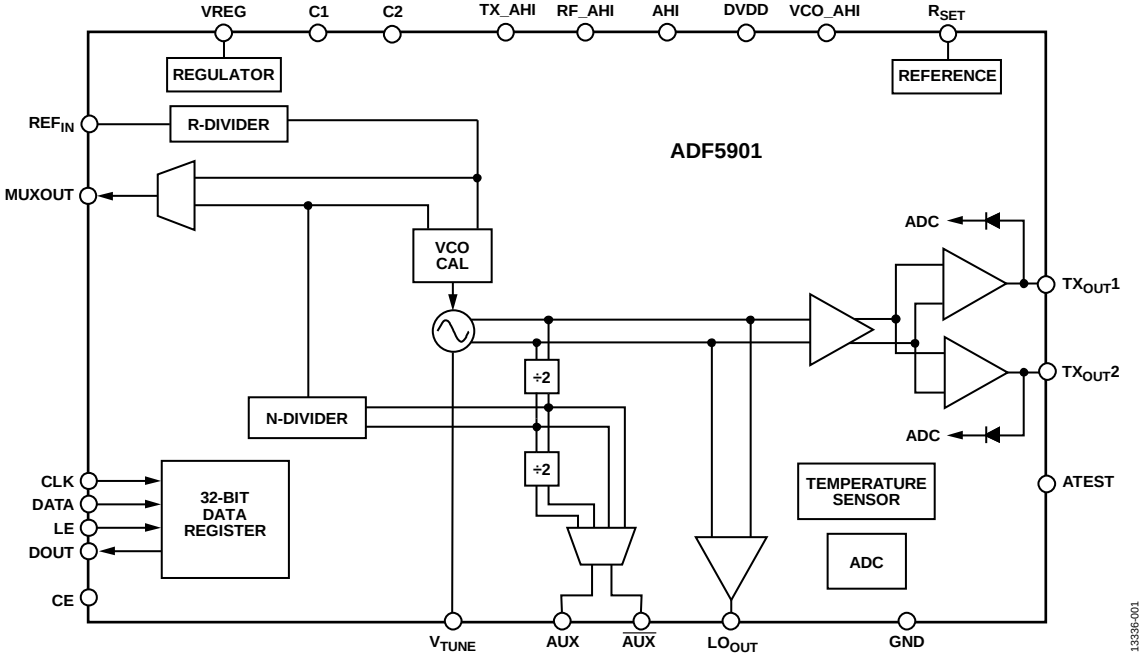

Figure 1.

Rev. B Document Feedback

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REVISION HISTORY

8/2017—Rev. A to Rev. B

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7/2016—Rev. 0 to Rev. A

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12/2015—Revision 0: Initial Version

SPECIFICATIONS

AHI = TX_AHI = RF_AHI = VCO_AHI = DVDD = 3.3 V ± 5%, AGND = 0 V, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted. Operating temperature range is −40°C to +105°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OPERATING CONDITIONS					
RF Frequency Range	24		24.25	GHz	
VCO CHARACTERISITICS					
V_{TUNE}	1		2.8	V	
V_{TUNE} Impedance		100		kΩ	
VCO Phase Noise Performance					
At 100 kHz Offset		−88		dBc/Hz	
At 1 MHz Offset		−108		dBc/Hz	
At 10 MHz Offset		−128		dBc/Hz	
Amplitude Noise		−150		dBc/Hz	At 1 MHz offset
Static Pulling f_{VCO} Change vs. Load		±2		MHz	Open-loop into 2:1 voltage standing wave ratio (VSWR) load
Dynamic Pulling Tx On/Off Switch Change		±10		MHz	Open-loop
Dynamic Pulling Tx to Tx Switch Change		±5		MHz	Open-loop
Pushing f_{VCO} Change vs. AHI Change		±5		MHz/V	Open-loop
Spurious Level Harmonics		−30		dBc	
Spurious Level Nonharmonics		<−70		dBc	
POWER SUPPLIES					
AHI, TX_AHI, RF_AHI, VCO_AHI, DVDD	3.135	3.3	3.465	V	
Total Current, I_{TOTAL}[1]		170		mA	
Software Power-Down Mode		500		µA	
Hardware Power-Down Mode		200		µA	
Tx OUTPUT					
Output Power	2	8	10	dBm	
Output Impedance		50		Ω	
On/Off Isolation		30		dB	Single Tx output switched on/off
Tx to Tx Isolation		25		dB	
Power-Up/Power-Down Time		200		ns	
LO OUTPUT					
Output Power	−7	−1	+5	dBm	
Output Impedance		50		Ω	
On/Off Isolation		30		dB	
AUX PIN OUTPUT					
Output Power	−9	−5	0	dBm	Single-ended
Output Frequency					
Divide by 2 Output	12		12.125	GHz	
Divide by 4 Output	6		6.0625	GHz	
Output Impedance		200		Ω	Differential
On/Off Isolation		30		dB	
AUX to LO Isolation		30		dB	
TEMPERATURE SENSOR					
Analog Accuracy		±5		°C	Following one-point calibration
Digital Accuracy		±5		°C	Following one-point calibration
Sensitivity		6.4		mV/°C	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC					
Resolution		8		Bits	
Integral Nonlinearity (INL)		±1		LSB	
Differential Nonlinearity (DNL)		±1		LSB	
Least Significant Bit (LSB)		7.4		mV	
REFIN CHARACTERISITICS					
REF_{IN} Input Frequency	10		260	MHz	−5 dBm minimum to +9 dBm maximum biased at AHI/2 (ac coupling ensures 1.8/2 bias); for frequencies < 10 MHz, use a dc-coupled, CMOS-compatible square wave with a slew rate > 25 V/µs
REF_{IN} Input Capacitance			1.2	pF	
REF_{IN} Input Current			±100	µA	
LOGIC INPUTS					
Input Voltage					
High (V_{IH})	1.4			V	
Low (V_{IL})			0.6	V	
Input Current (I_{INH}, I_{INL})			±1	µA	
Input Capacitance (C_{IN})			10	pF	
LOGIC OUTPUTS					
Output Voltage					
High (V_{OH})[2]	V_{DD} − 0.4			V	
Low (V_{OL})			0.4	V	
Output Current					
High (I_{OH})			500	µA	
Low (I_{OL})			500	µA	

[1] T_A = 25°C; AHI = 3.3 V; f_{REFIN} = 100 MHz; RF = 24.125 GHz following initialization sequence in the Initialization Sequence section.
[2] V_{DD} selected from IO level bit (DB11 in Register 3).

TIMING SPECIFICATIONS

AHI = TX_AHI = RF_AHI = VCO_AHI = DVDD = 3.3 V ± 5%, AGND = 0 V, dBm referred to 50 Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Operating temperature range is −40°C to +105°C.

Table 2. Write Timing

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Description
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width
t_8	10	ns max	LE setup time to DOUT
t_9	15	ns max	CLK setup time to DOUT

Write Timing Diagram

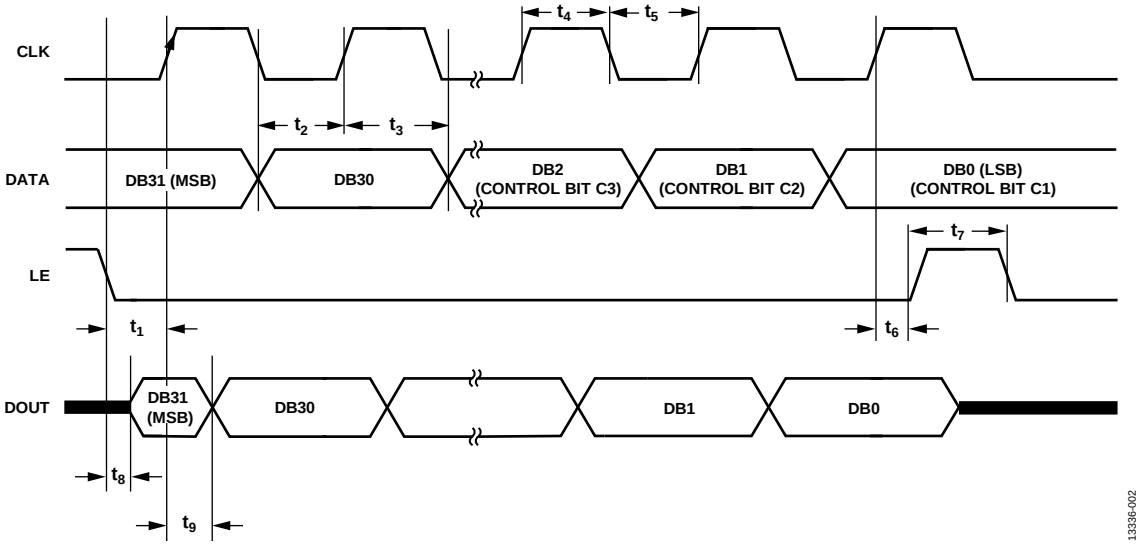

Figure 2. Write Timing Diagram

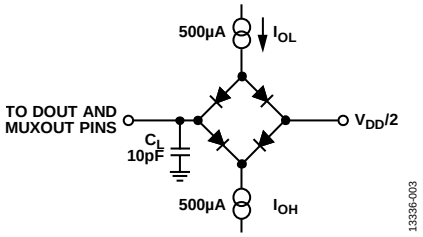

Figure 3. Load Circuit for DOUT/MUXOUT Timing, C_L = 10 pF

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
AHI to GND	−0.3 V to +3.9 V
AHI to TX_AHI	−0.3 V to +0.3 V
AHI to RF_AHI	−0.3 V to +0.3 V
AHI to VCO_AHI	−0.3 V to +0.3 V
AHI to DVDD	−0.3 V to +0.3 V
V_{TUNE} to GND	−0.3 V to +3.6 V
Digital Input/Output Voltage to GND	−0.3 V to DVDD + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
θ_{JA} Thermal Impedance[1] (Paddle Soldered)	40.83 °C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Transistor Count	
CMOS	177,381
Bipolar	2315
ESD	
Charged Device Model	250 V
Human Body Model	2000 V

[1] Two signal planes (that is, on top and bottom surfaces of the board), two buried planes, and nine vias.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

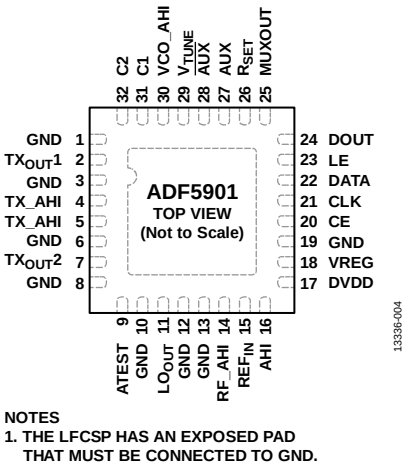

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 6, 8, 10, 12, 13, 19	GND	RF Ground. Tie all ground pins together.
2	$TX_{OUT}1$	24 GHz Tx Output 1.
4, 5	TX_AHI	Voltage Supply for the Tx Section. Connect decoupling capacitors (0.1 µF, 1 nF, and 10 pF) to the ground plane as close as possible to this pin. TX_AHI must be the same value as AHI.
7	$TX_{OUT}2$	24 GHz Tx Output 2.
9	ATEST	Analog Test Pin.
11	LO_{OUT}	LO Output.
14	RF_AHI	Voltage Supply for the RF Section. Connect decoupling capacitors (0.1 µF, 1 nF, and 10 pF) to the ground plane as close as possible to this pin. RF_AHI must be the same value as AHI.
15	REF_{IN}	Reference Input. This pin is a CMOS input with a nominal threshold of DVDD/2 and a dc equivalent input resistance of 100 kΩ. See Figure 14. This input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
16	AHI	Voltage Supply for the Analog Section. Connect decoupling capacitors (0.1 µF, 1 nF, and 10 pF) to the ground plane as close as possible to this pin.
17	DVDD	Digital Power Supply. This supply may range from 3.135 V to 3.465 V. Place decoupling capacitors (0.1 µF, 1 nF, and 10 pF) to the ground plane as close as possible to this pin. DVDD must be the same value as AHI.
18	VREG	Internal 1.8 V Regulator Output. Connect a 220 nF capacitor to ground as close as possible to this pin.
20	CE	Chip Enable. A logic low on this pin powers down the device. Taking the pin high powers up the device, depending on the status of the power-down bit, PD1.
21	CLK	Serial Clock Input. This serial clock input clocks in the serial data to the registers. The data is latched into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
22	DATA	Serial Data Input. The serial data is loaded MSB first with the four LSBs as the control bits. This input is a high impedance CMOS input.
23	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the 16 latches with the latch selected via the control bits.
24	DOUT	Serial Data Output.
25	MUXOUT	Multiplexer Output. This multiplexer output allows either the scaled RF or the scaled reference frequency to be accessed externally.
26	R_{SET}	Resistor Setting Pin. Connecting a 5.1 kΩ resistor between this pin and GND sets an internal current. The nominal voltage potential at the R_{SET} pin is 0.62 V.
27	AUX	Auxiliary Output. The VCO/2 output or VCO/4 is available.
28	$\overline{AUX}$	Complementary Auxiliary Output. The VCO/2 output or VCO/4 is available.

Pin No.	Mnemonic	Description
29	V_{TUNE}	Control Input to the VCO. This voltage determines the output.
30	VCO_AHI	Voltage Supply for the VCO Section. Connect decoupling capacitors (0.1 µF, 1 nF, and 10 pF) to the ground plane as close as possible to this pin. VCO_AHI must be the same value as AHI.
31	C1	Decoupling Capacitor 1. Place a 47 nF capacitor to ground as close as possible to this pin.
32	C2	Decoupling Capacitor 2. Place a 220 nF capacitor to ground as close as possible to this pin.
	EP	Exposed Pad. The LFCSP has an exposed pad that must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

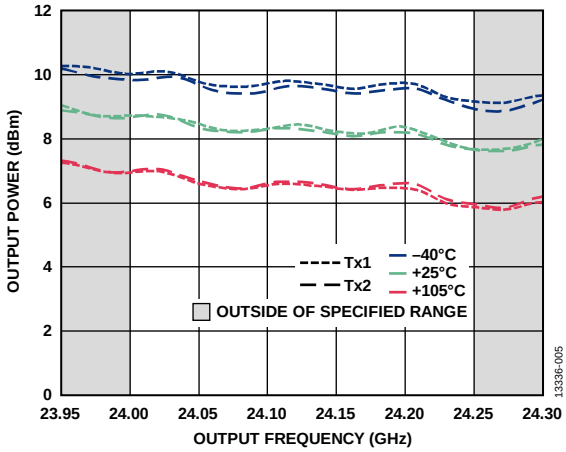

Figure 5. Tx Output Power vs. Output Frequency

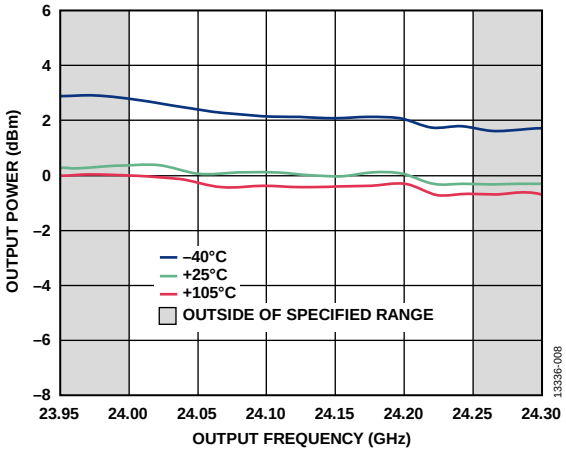

Figure 8. LO Output Power vs. Output Frequency

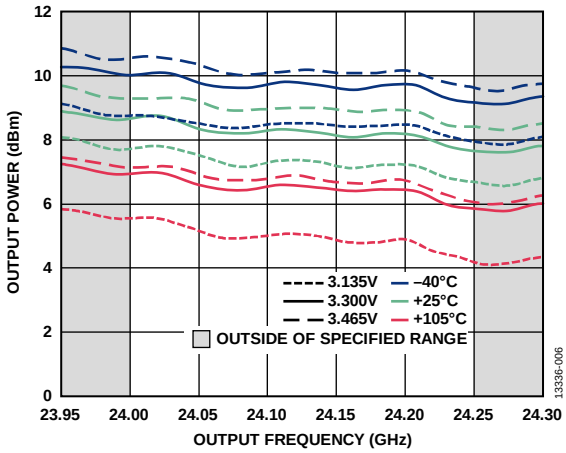

Figure 6. Transmitter 1 (Tx1) Output Power Variation with Temperature and Supply vs. Output Frequency

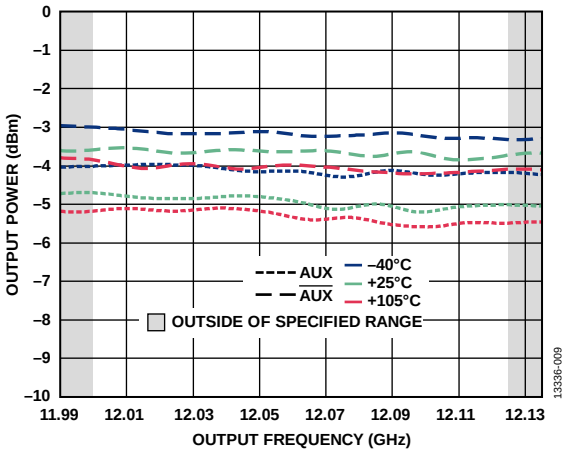

Figure 9. AUX/$\overline{\text{AUX}}$ Output Power vs. Output Frequency with Divide by 2 Selected

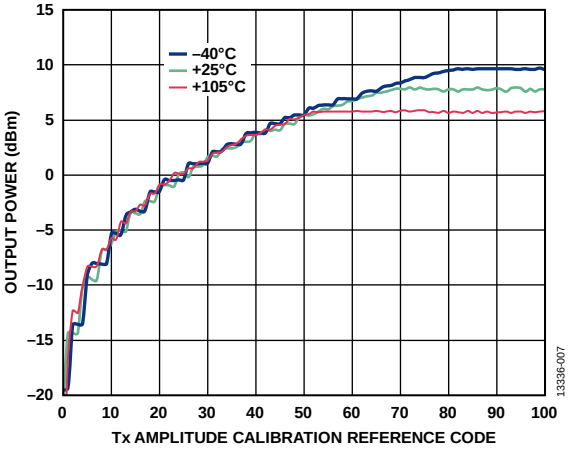

Figure 7. Tx Output Power vs. Tx Amplitude Calibration Reference Code

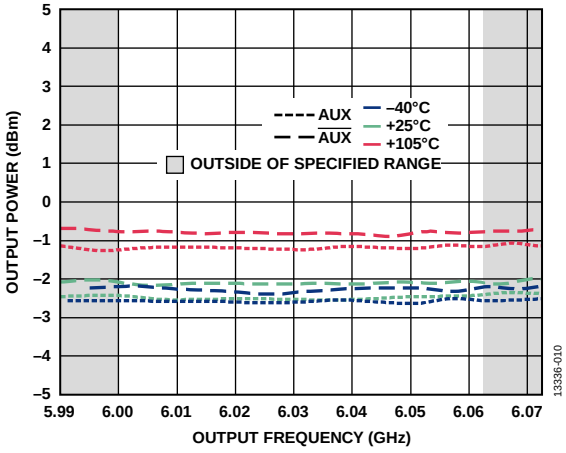

Figure 10. AUX/$\overline{\text{AUX}}$ Output Power vs. Output Frequency with Divide by 4 Selected

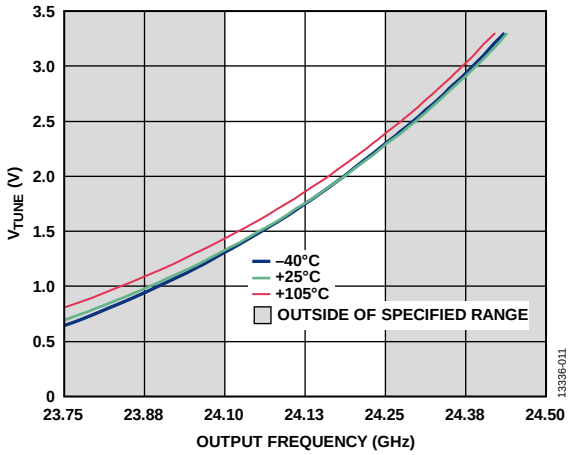

Figure 11. V_{TUNE} Frequency Range

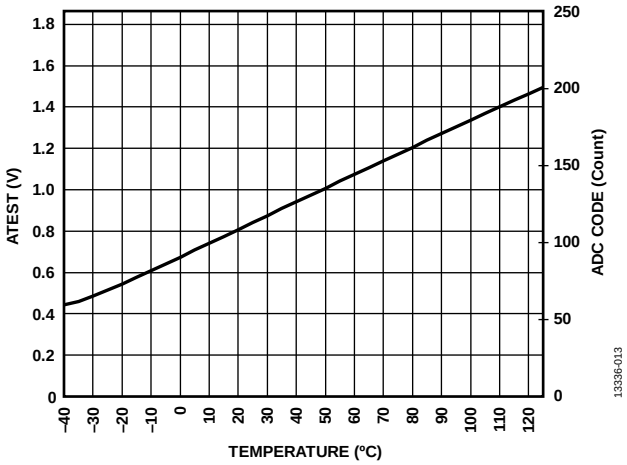

Figure 13. ATEST Voltage and ADC Code vs. Temperature

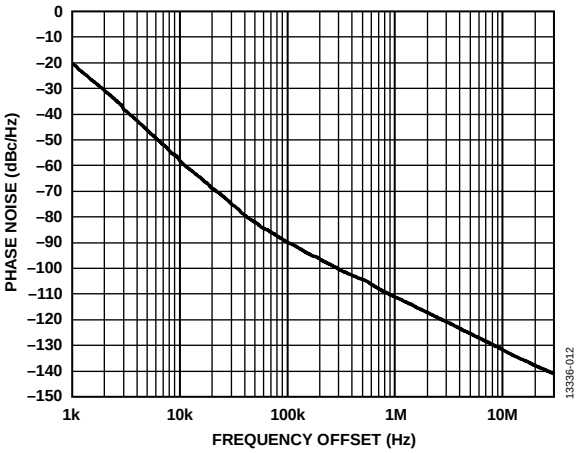

Figure 12. Open-Loop Phase Noise on Tx1 Output at 24.125 GHz

THEORY OF OPERATION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 14. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This configuration ensures that there is no loading of the REF_{IN} pin on power-down.

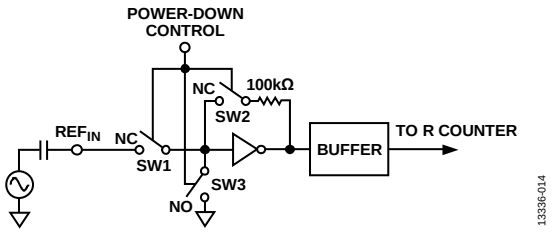

Figure 14. Reference Input Stage

RF INT DIVIDER

The RF INT counter allows a division ratio in the RF feedback counter. Division ratios from 75 to 4095 are allowed.

INT, FRAC, AND R RELATIONSHIP

Generate the RF VCO frequency (RF_{OUT}) using the INT and FRAC values in conjunction with the R counter, as follows:

$$RF_{OUT} = f_{REF} \times (INT + (FRAC/2^{25})) \times 2 \quad (1)$$

where:

RF_{OUT} is the output frequency of internal VCO.

f_{REF} is the internal reference frequency.

INT is the preset divide ratio of the binary 12-bit counter (75 to 4095).

FRAC is the numerator of the fractional division (0 to $2^{25} - 1$).

$$f_{REF} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \quad (2)$$

where:

REF_{IN} is the reference input frequency.

D is the REF_{IN} doubler bit (0 or 1).

R is the preset divide ratio of the binary, 5-bit, programmable reference counter (1 to 32).

T is the REF_{IN} divide by 2 bit (0 or 1).

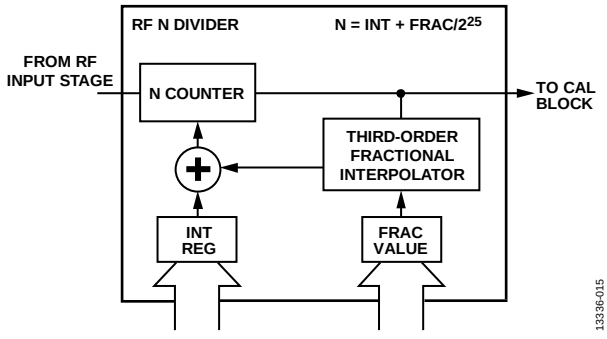

Figure 15. RF N Divider

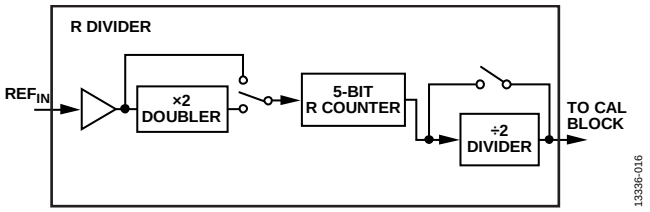

Figure 16. Reference Divider

R COUNTER

The 5-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to supply the reference clock to the VCO calibration block. Division ratios from 1 to 32 are allowed.

INPUT SHIFT REGISTER

The ADF5901 digital section includes a 5-bit RF R counter, a 12-bit RF N counter, and a 25-bit FRAC counter. Data is clocked into the 32-bit input shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the input shift register to one of 12 latches on the rising edge of LE. The destination latch is determined by the state of the five control bits (C5, C4, C3, C2, and C1) in the input shift register. These are the five LSBs (DB4, DB3, DB2, DB1, and DB0, respectively), as shown in Figure 2. Table 5 shows the truth table for these bits. Figure 17 and Figure 18 show a summary of how the latches are programmed.

PROGRAM MODES

Table 5 and Figure 19 through Figure 30 show how to set up the program modes in the ADF5901.

Several settings in the ADF5901 are double buffered. These include the LSB fractional value, R counter value (R divider), reference doubler, clock divider, RDIV2, and MUXOUT. This means that two events must occur before the device uses a new value for any of the double-buffered settings. First, the new value is latched into the device by writing to the appropriate register. Second, a new write must be performed on Register R5.

For example, updating the fractional value can involve a write to the 13 LSB bits in Register R6 and the 12 MSB bits in Register R5. Write to Register R6 first, followed by the write to Register R5. The frequency change begins after the write to Register R0. Double buffering ensures that the bits written to in Register R6 do not take effect until after the write to Register R5.

Table 5. C5, C4, C3, C2, and C1 Truth Table

Control Bits					
C5 (DB4)	**C4 (DB3)**	**C3 (DB2)**	**C2 (DB1)**	**C1 (DB0)**	**Register**
0	0	0	0	0	R0
0	0	0	0	1	R1
0	0	0	1	0	R2
0	0	0	1	1	R3
0	0	1	0	0	R4
0	0	1	0	1	R5
0	0	1	1	0	R6
0	0	1	1	1	R7
0	1	0	0	0	R8
0	1	0	0	1	R9
0	1	0	1	0	R10
0	1	0	1	1	R11

REGISTER MAPS

REGISTER 0 (R0)

RESERVED								AUX BUFFER GAIN			AUX DIV	RESERVED				PUP RCNTR	PUP NCNTR	RESERVED	Tx2 AMP CAL	Tx1 AMP CAL	PUP VCO	VCO CAL	PUP ADC	PUP Tx2	PUP Tx1	PUP LO	CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	0	0	0	0	AG2	AG1	AG0	AD	1	1	1	1	PRC	PNC	1	Tx2C	Tx1C	PVCO	VCAL	PADC	PTx2	PTx1	PLO	C5(0)	C4(0)	C3(0)	C2(0)	C1(0)

REGISTER 1 (R1)

RESERVED																			Tx AMP CAL REF CODE								CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	TAR7	TAR6	TAR5	TAR4	TAR3	TAR2	TAR1	TAR0	C5(0)	C4(0)	C3(0)	C2(0)	C1(1)

REGISTER 2 (R2)

RESERVED																ADC START	ADC AVERAGE		ADC CLOCK DIVIDER								CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	AS	AA0	AA0	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	C5(0)	C4(0)	C3(0)	C2(1)	C1(0)

REGISTER 3 (R3)

RESERVED																MUXOUT DBR[1]			IO LEVEL	READBACK CONTROL							CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	M3	M2	M1	M0	IOL	RC5	RC4	RC3	RC2	RC1	RC0	C5(0)	C4(0)	C3(0)	C2(1)	C1(1)

REGISTER 4 (R4)

RESERVED										N DIV TO MUXOUT EN	RESERVED				TEST BUS TO ADC	TEST BUS TO PIN	ANALOG TEST BUS								CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	NDM	0	0	0	0	TBA	TBP	AB9	AB8	AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0	C5(0)	C4(0)	C3(1)	C2(0)	C1(0)

REGISTER 5 (R5)

RESERVED			INTEGER WORD												FRAC MSB WORD												CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	C5(0)	C4(0)	C3(1)	C2(0)	C1(1)

REGISTER 6 (R6)

RESERVED														FRAC LSB WORD DBR[1]												CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0	C5(0)	C4(0)	C3(1)	C2(1)	C1(0)

[1]DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 5.

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Figure 17. Register Summary (Register 0 to Register 6)

REGISTER 7 (R7)

RESERVED						MASTER RESET	RESERVED	CLOCK DIVIDER DBR[1]										RDIV2 DBR[1]	REF DOUBLER DBR[1]	R DIVIDER DBR[1]					CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	MR	1	C1D11	C1D10	C1D9	C1D8	C1D7	C1D6	C1D5	C1D4	C1D3	C1D2	C1D1	C1D0	RD2	RD	R4	R3	R2	R1	R0	C5(0)	C4(0)	C3(1)	C2(1)	C1(1)

REGISTER 8 (R8)

RESERVED																	FREQENCY CAL DIVIDER										CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FC9	FC8	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	C5(0)	C4(1)	C3(0)	C2(0)	C1(0)

REGISTER 9 (R9)

RESERVED																											CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	1	0	0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	C5(0)	C4(1)	C3(0)	C2(0)	C1(1)

REGISTER 10 (R10)

RESERVED																											CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	1	0	0	1	1	0	0	1	0	1	0	1	0	0	1	1	0	0	1	0	C5(0)	C4(1)	C3(0)	C2(1)	C1(0)

REGISTER 11 (R11)

RESERVED																									CNTR RESET	CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CR	C5(0)	C4(1)	C3(0)	C2(1)	C1(1)

[1]DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 5.

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Figure 18. Register Summary (Register 7 to Register 11)

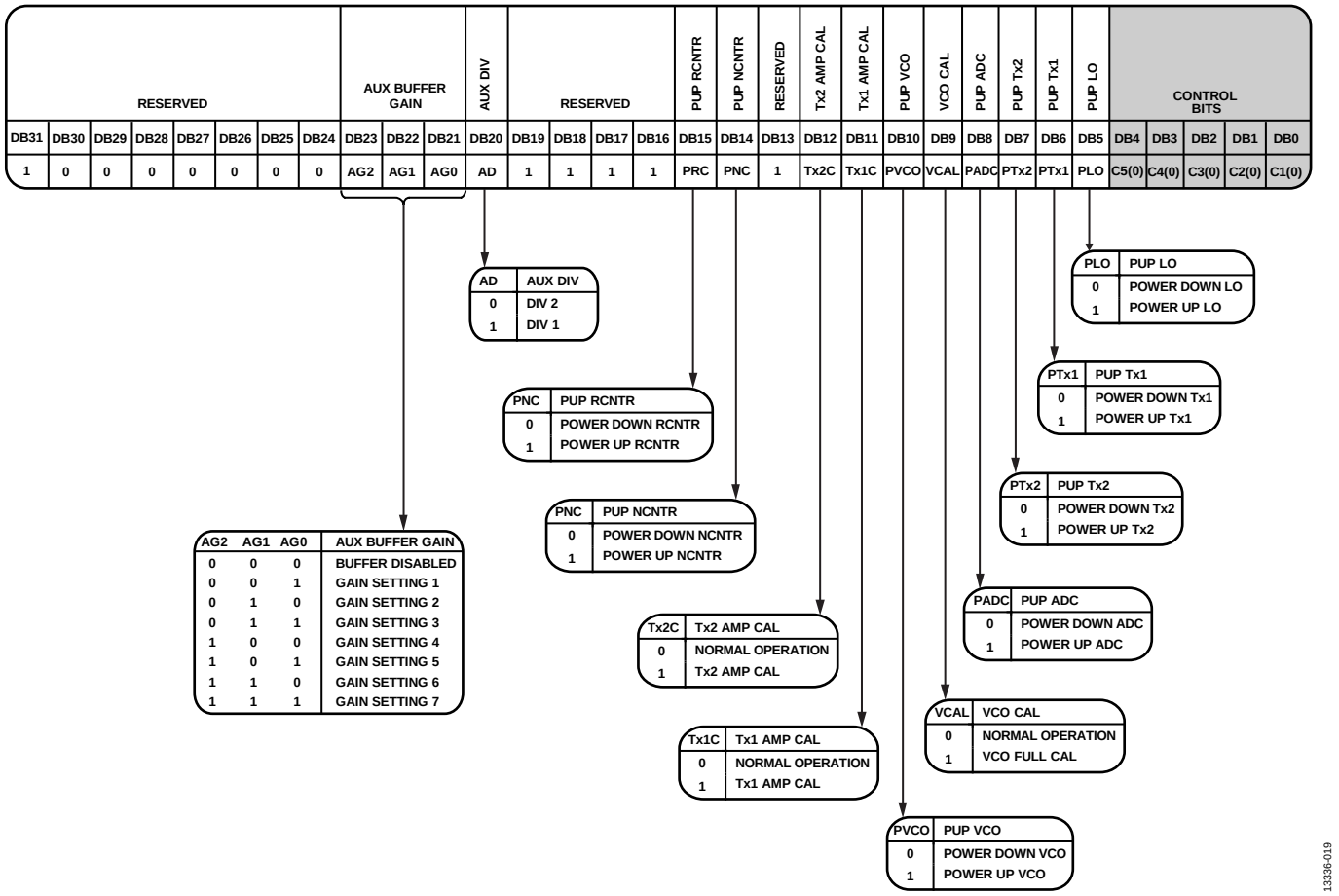


Figure 19. Register 0 (R0)

REGISTER 0

Control Bits

With Bits[C5:C1] set to 00000, Register R0 is programmed. Figure 19 shows the input data format for programming this register.

Auxiliary Buffer Gain

Bits[DB23:DB21] set the auxiliary output buffer gain (see Figure 19).

Auxiliary Divide by 2

Bit DB20 selects the auxiliary output divider. Setting this bit to 0 selects divide by 2 (6 GHz output). Setting the bit to 1 selects divide by 1 (12 GHz output).

Power-Up R Counter

Bit DB15 provides the power-up bit for the R counter block. Setting this bit to 0 performs a power-down of the counter block. Setting this bit to 1 returns the counter block to normal operation.

Power-Up N Counter

Bit DB14 provides the power-up bit for the N counter block. Setting this bit to 0 performs a power-down of the counter block. Setting this bit to 1 returns the counter block to normal operation.

Tx2 Amplitude Calibration

Bit DB12 provides the control bit for amplitude calibration of the Transmitter 2 (Tx2) output. Set this bit to 0 for normal operation. Setting this bit to 1 performs an amplitude calibration of the Tx2 output.

Tx1 Amplitude Calibration

Bit DB11 provides the control bit for amplitude calibration of the Tx1 output. Set this bit to 0 for normal operation. Setting this bit to 1 performs an amplitude calibration of the Tx1 output.

Power-Up VCO

Bit DB10 provides the power-up bit for the VCO. Setting this bit to 0 performs a power-down of the VCO. Setting this bit to 1 performs a power-up of the VCO.

VCO Calibration

Bit DB9 provides the control bit for frequency calibration of the VCO. Set this bit to 0 for normal operation. Setting this bit to 1 performs a VCO frequency and amplitude calibration.

Power-Up ADC

Bit DB8 provides the power-up bit for the ADC. Setting this bit to 0 performs a power-down of the ADC. Setting this bit to 1 performs a power-up of the ADC.

Power-Up Tx2 Output

Bit DB7 provides the power-up bit for the Tx2 output. Setting this bit to 0 performs a power-down of the Tx2 output. Setting this bit to 1 performs a power-up of the Tx2 output. Only one Tx output can be powered up at any time, either Tx1 (DB6) or Tx2 (DB7).

Power-Up Tx1 Output

Bit DB6 provides the power-up bit for the Tx1 output. Setting this bit to 0 performs a power-down of the Tx1 output. Setting this bit to 1 performs a power-up of the Tx1 output. Only one Tx output can be powered up at any time, either Tx1 (DB6) or Tx2 (DB7).

Power-Up LO Output

Bit DB5 provides the power-up bit for the LO output. Setting this bit to 0 performs a power-down of the LO output. Setting this bit to 1 performs a power-up of the LO output.

REGISTER 1

Control Bits

With Bits[C5:C1] set to 00001, Register R1 is programmed. Figure 20 shows the input data format for programming this register.

Tx Amplitude Calibration Reference Code

Bits[DB12:DB5] set the Tx amplitude calibration reference code (see Figure 20) for the two Tx outputs during calibration. Calibrate the output power on the Tx outputs from −20 dBm to 8 dBm by setting the Tx amplitude calibration reference code (see Figure 7).

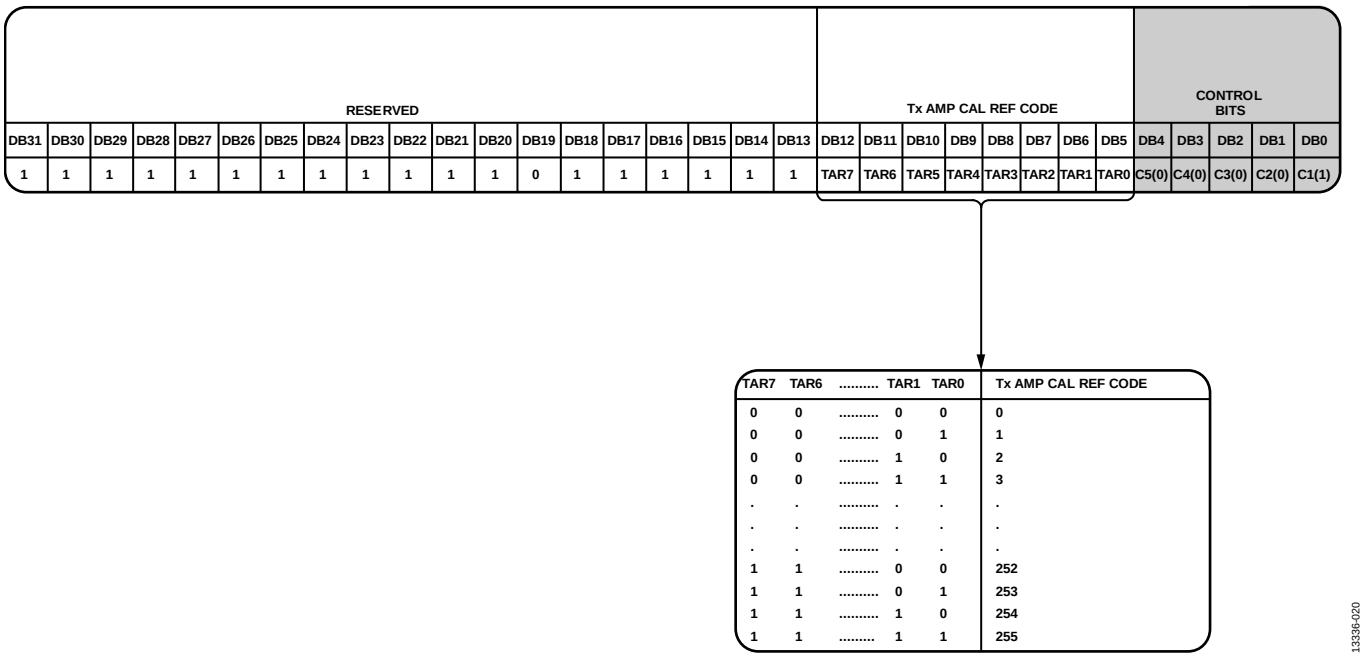


Figure 20. Register 1 (R1)

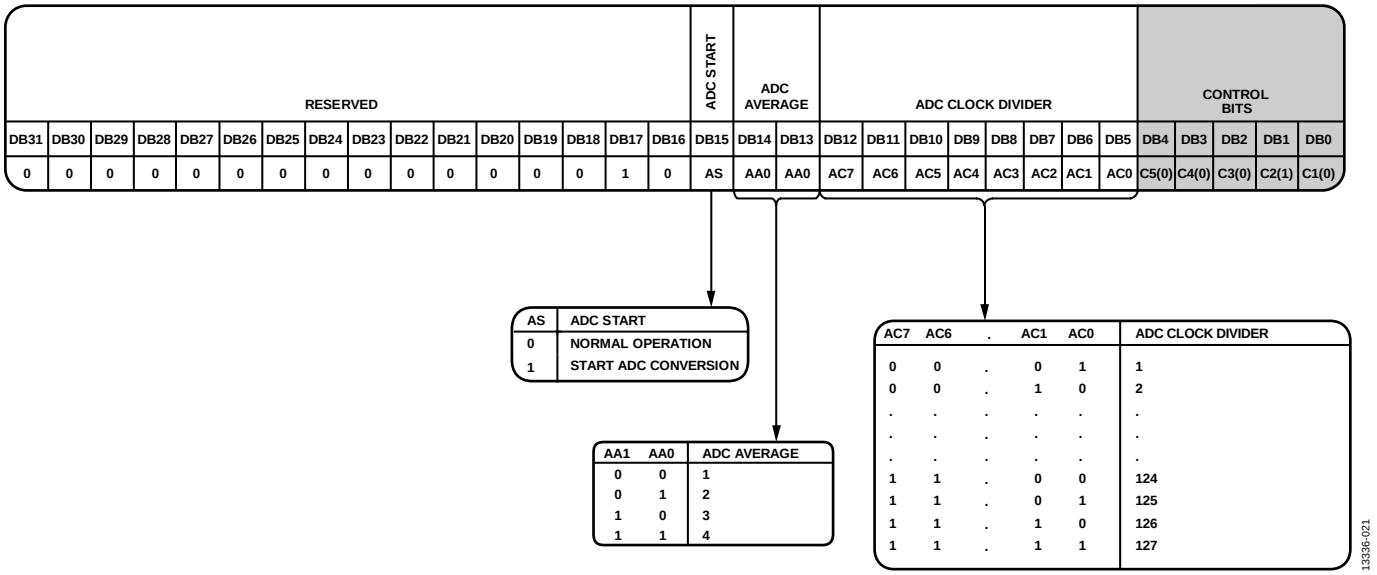


Figure 21. Register 2 (R2)

REGISTER 2

Control Bits

With Bits[C5:C1] set to 00010, Register R2 is programmed. Figure 21 shows the input data format for programming this register.

ADC Start

Bit DB15 starts the ADC conversion. Setting this bit to 1 starts an ADC conversion.

ADC Average

Bits[DB14:DB13] program the ADC average, which is the number of averages of the ADC output (see Figure 21).

ADC Clock Divider

Bits[DB12:DB5] program the clock divider, which is used as the sampling clock for the ADC (see Figure 21). The output of the R divider block clocks the ADC clock divider. Program a divider value to ensure the ADC sampling clock is 1 MHz.

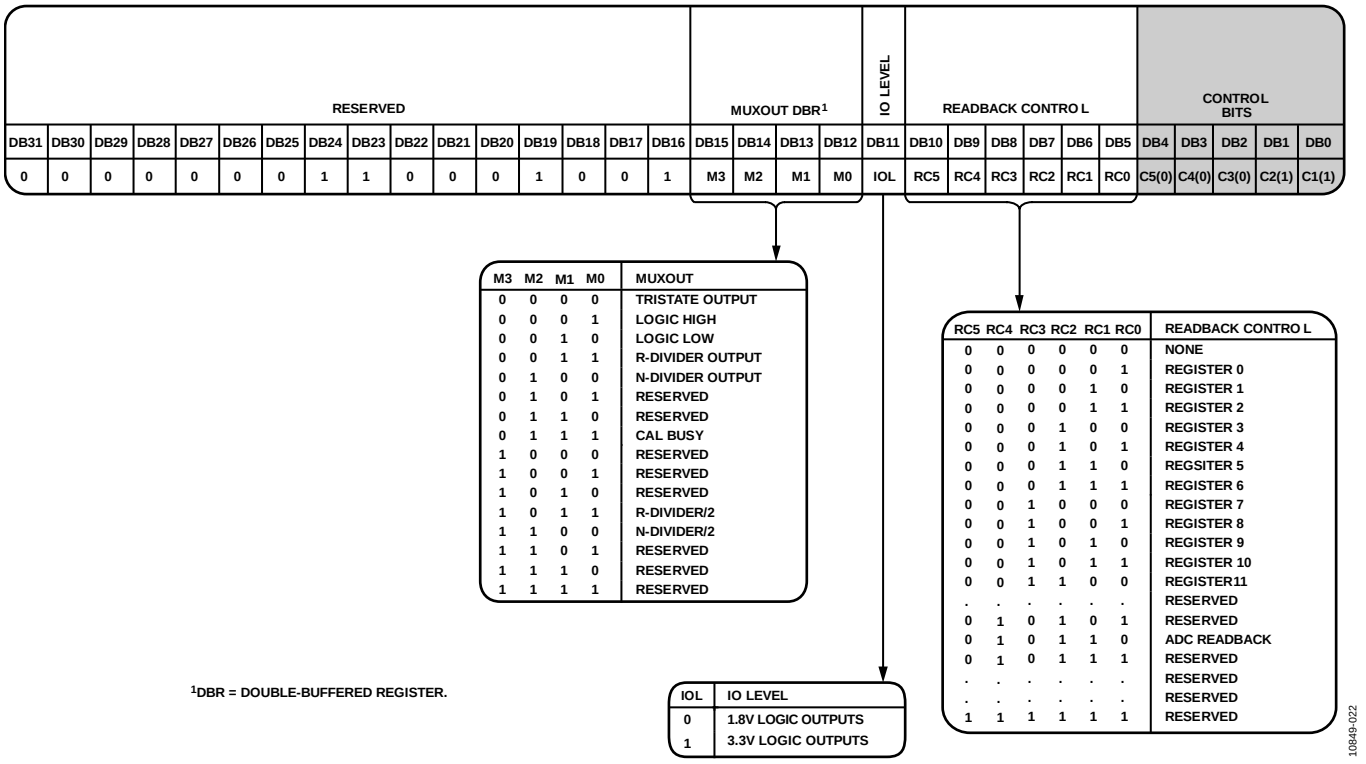


Figure 22. Register 3 (R3)

REGISTER 3

Control Bits

With Bits[C5:C1] set to 00011, Register R3 is programmed. Figure 22 shows the input data format for programming this register.

MUXOUT Control

Bits[DB15:DB12] control the on-chip multiplexer of the ADF5901. See Figure 22 for the truth table.

Input/Output (IO) Level

Bit DB11 controls the DOUT logic levels. Setting this bit to 0 sets the DOUT logic level to 1.8 V. Setting this bit to 1 sets the DOUT logic level to 3.3 V.

Readback Control

Bits[DB10:DB5] control the readback data to DOUT on the ADF5901. See Figure 22 for the truth table.

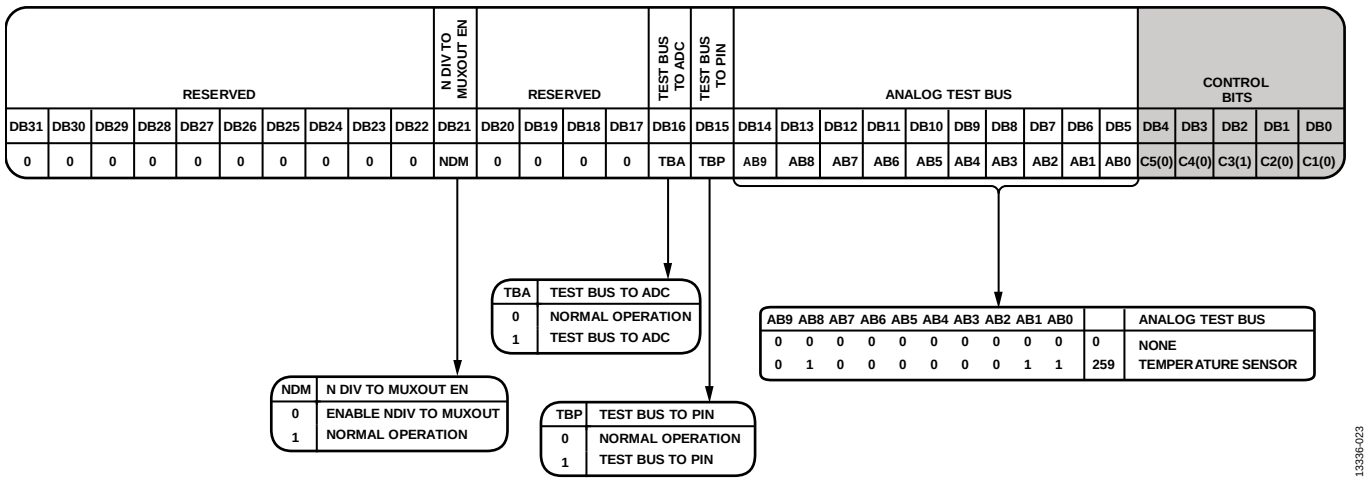


Figure 23. Register 4 (R4)

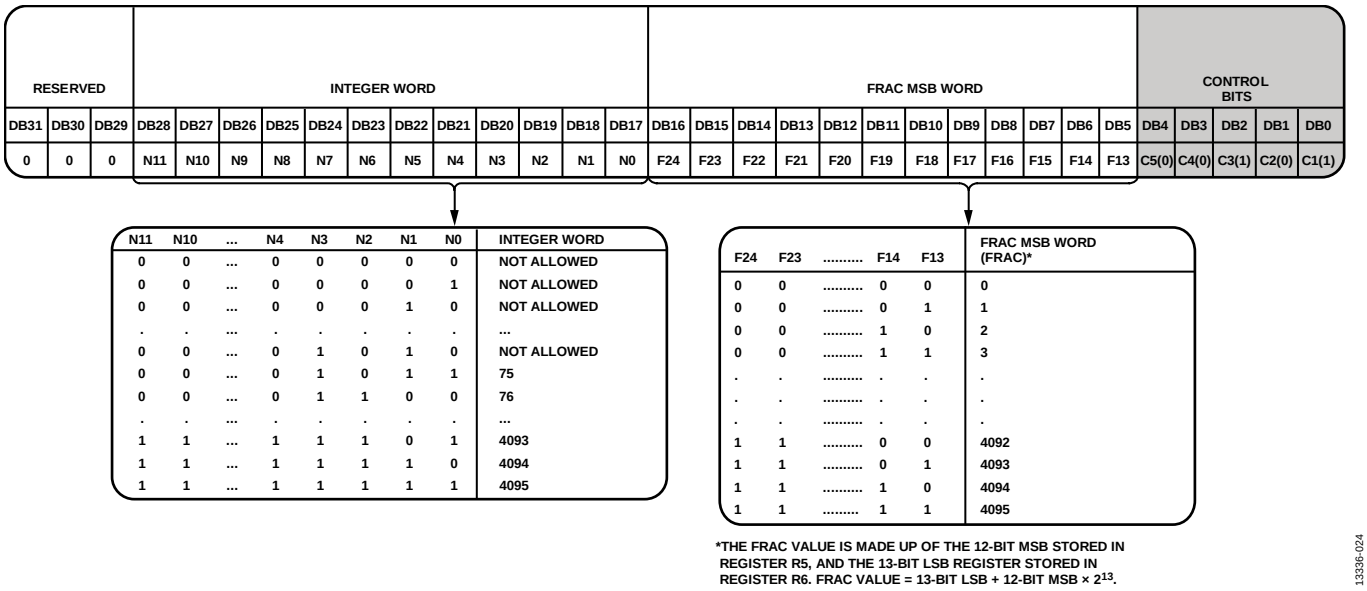


Figure 24. Register 5 (R5)

REGISTER 4

Control Bits

With Bits[C5:C1] set to 00100, Register R4 is programmed. Figure 23 shows the input data format for programming this register.

N Divider to MUXOUT Enable

Bit DB21 controls the internal N divider signal for MUXOUT. Setting this bit to 0 enables the internal N divider signal to MUXOUT. Setting this bit to 1 returns the device to normal operation.

Test Bus to ADC

Bit DB16 controls the ATEST pin. Set this bit to 0 for normal operation. Setting this bit to 1 connects the analog test bus to the ADC input.

Test Bus to Pin

Bit DB15 controls the ATEST pin. Setting this bit to 0 sets the ATEST pin to high impedance. Setting this bit to 1 connects the analog test bus to the ATEST pin.

Analog Test Bus

Bits[DB14:DB5] control the analog test bus. This analog test bus allows access to internal test signals for the temperature sensor. See Figure 23 for the truth table.

REGISTER 5

Control Bits

With Bits[C5:C1] set to 00101, Register R5 is programmed. Figure 24 shows the input data format for programming this register.

12-Bit Integer Value (INT)

These 12 bits (Bits[DB28:DB17]) set the INT value, which determines the integer part of the RF division factor. This INT value is used in Equation 5. See the RF Synthesis: a Worked Example section for more information. All integer values from 75 to 4095 are allowed.

12-Bit MSB Fractional Value (FRAC)

These 12 bits (Bits[DB16:DB5]), together with Bits[DB17:DB5] (FRAC LSB word) in Register R6, control what is loaded as the FRAC value into the fractional interpolator. This FRAC value partially determines the overall RF division factor. It is also used in Equation 1. These 12 bits are the most significant bits (MSB) of the 25-bit FRAC value, and Bits[DB17:DB5] (FRAC LSB word) in Register R6 are the least significant bits (LSB). See the RF Synthesis: a Worked Example section for more information.

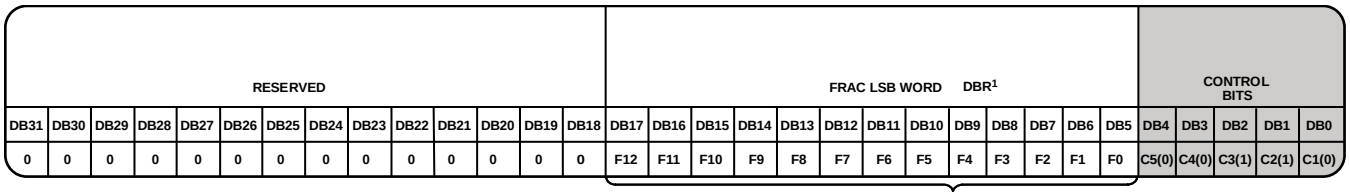
REGISTER 6

Control Bits

With Bits[C5:C1] set to 00110, Register R6 is programmed. Figure 25 shows the input data format for programming this register.

13-Bit LSB FRAC Value

These 13 bits (Bits[DB17:DB5]), together with Bits[DB16:DB5] (FRAC MSB word) in Register R5, control what is loaded as the FRAC value into the fractional interpolator. This FRAC value partially determines the overall RF division factor. It is also used in Equation 1. These 13 bits are the least significant bits (LSB) of the 25-bit FRAC value, and Bits[DB14:DB3] (FRAC MSB word) in Register R5 are the most significant bits (MSB). See the RF Synthesis: a Worked Example section for more information.



F12	F11	.....	F1	F0	FRAC LSB WORD (FRAC)*
0	0	.....	0	0	0
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	8188
1	1	.....	0	1	8189
1	1	.....	1	0	8190
1	1	.....	1	1	8191

*THE FRAC VALUE IS MADE UP OF THE 12-BIT MSB STORED IN REGISTER R5, AND THE 13-BIT LSB REGISTER STORED IN REGISTER R6. FRAC VALUE = 13-BIT LSB + 12-BIT MSB × 2^{13}.

[1]DBR = DOUBLE-BUFFERED REGISTER.

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Figure 25. Register 6 (R6)

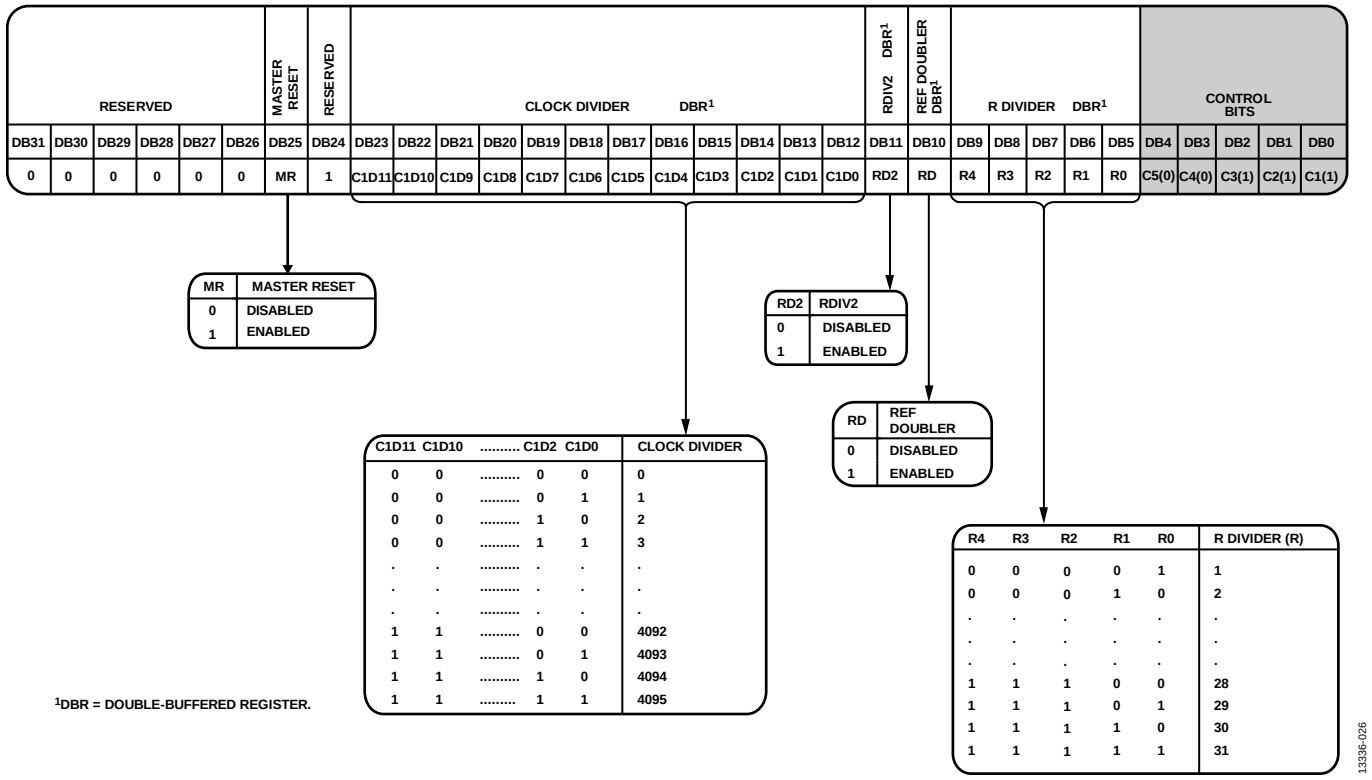

Figure 26. Register 7 (R7)

REGISTER 7

Control Bits

With Bits[C5:C1] set to 00111, Register R7 is programmed. Figure 26 shows the input data format for programming this register.

Master Reset

Bit DB25 provides a master reset bit for the device. Setting this bit to 1 performs a reset of the device and all register maps. Setting this bit to 0 returns the device to normal operation.

Clock Divider

Bits[DB23:DB12] set a divider for the VCO frequency calibration. Load the divider such that the time base is 10 µs (see Figure 26).

Divide by 2 (RDIV2)

Setting the DB11 bit to 1 inserts a divide by 2 toggle flip flop between the R counter and VCO calibration block.

Reference Doubler

Setting DB10 to 0 feeds the REF_{IN} signal directly to the 5-bit R counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before the REF_{IN} signal is fed into the 5-bit R counter.

The maximum allowable REF_{IN} frequency when the doubler is enabled is 50 MHz.

5-Bit R Divider

The 5-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the VCO calibration block. Division ratios from 1 to 31 are allowed.

RESERVED																FREQENCY CAL DIVIDER										CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FC9	FC8	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	C5(0)	C4(1)	C3(0)	C2(0)	C1(0)

FC9	FC8	...	FC4	FC3	FC2	FC1	FC0	FREQUENCY CAL DIVIDER
0	0	...	0	0	0	0	0	0
0	0	...	0	0	0	0	1	1
0	0	...	0	0	0	1	0	2
.	.	...	.	.	.	.	.	...
.	.	...	.	.	.	.	.	...
1	1	...	1	1	1	0	1	1021
1	1	...	1	1	1	1	0	1023
1	1	...	1	1	1	1	1	1024

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Figure 27. Register 8 (R8)

RESERVED																										CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	1	0	0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	C5(0)	C4(1)	C3(0)	C2(0)	C1(1)

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Figure 28. Register 9 (R9)

REGISTER 8

Control Bits

With Bits[C5:C1] set to 01000, Register R8 is programmed. Figure 27 shows the input data format for programming this register.

Frequency Calibration Clock

Bits[DB14:DB5] set a divider for the VCO frequency calibration clock. Load the divider such that the time base is 10 µs (see Figure 27).

REGISTER 9

Control Bits

With Bits[C5:C1] set to 01001, Register R9 is programmed. Figure 28 shows the input data format for programming this register.

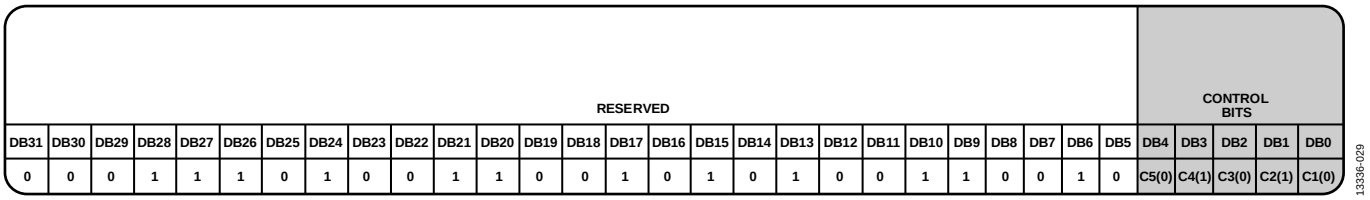

Figure 29. Register 10 (R10)

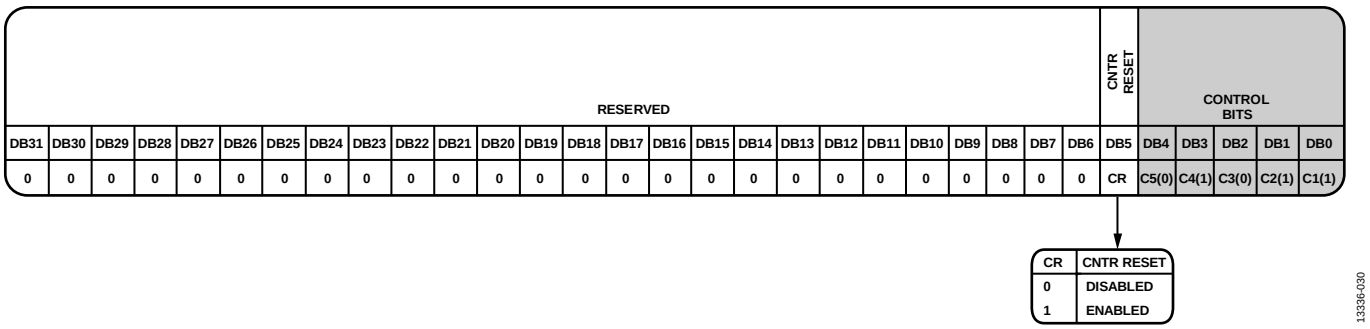

Figure 30. Register 11 (R11)

REGISTER 10

Control Bits

With Bits[C5:C1] set to 01010, Register R10 is programmed. Figure 29 shows the input data format for programming this register.

REGISTER 11

Control Bits

With Bits[C5:C1] set to 01011, Register R11 is programmed. Figure 30 shows the input data format for programming this register.

Counter Reset

Bit DB5 provides a counter reset bit for the counters. Setting this bit to 1 performs a counter reset of the device counters. Setting this bit to 0 returns the device to normal operation.

INITIALIZATION SEQUENCE

After powering up the device, administer the following programming sequence. The following sequence locks the VCO to 24.125 GHz with a 100 MHz reference and a 50 MHz reference divider frequency:

1. Write 0x02000007 to Register R7 to perform a master reset.
2. Write 0x0000002B to Register R11 to reset the counters.
3. Write 0x0000000B to Register R11 to enable the counters.
4. Write 0x1D32A64A to Register R10.
5. Write 0x2A20B929 to Register R9.
6. Write 0x40003E88 to Register R8 to set the frequency calibration divider clock to 100 kHz.
7. Write 0x809FE520 to Register R0 to power up the device and LO (10 µs).
8. Write 0x011F4827 to Register R7 to set the R counter clock to 50 MHz and the calibration clock to 100 kHz.
9. Write 0x00000006 to Register R6 to set the LSB FRAC = 0.
10. Write 0x01E28005 to Register R5 to set INT = 241 and MSB FRAC = 1024. Therefore, N = 240.25.
11. Write 0x00200004 to Register R4 to set the ATEST pin to high impedance.
12. Write 0x01890803 to Register R3 to set the IO level to V_{DD} = 3.3 V.
13. Write 0x00020642 to Register R2 to set the ADC clock to 1 MHz.
14. Write 0xFFF7FFE1 to Register R1 to set the Tx amplitude level.
15. Write 0x809FE720 to Register R0 to set the VCO frequency calibration (800 µs).
16. Write 0x809FE560 to Register R0 to power Tx1 on, Tx2 off, and LO on.
17. Write 0x809FED60 to Register R0 to set the Tx1 amplitude calibration (400 µs).
18. Write 0x809FE5A0 to Register R0 to turn Tx1 off, Tx2 on, and LO on.
19. Write 0x809FF5A0 to Register R0 to set the Tx2 amplitude calibration (400 µs).
20. Write 0x2800B929 to Register R9.
21. Write 0x809F25A0 to Register R0 to disable the R and N counters.

RECALIBRATION SEQUENCE

The ADF5901 can be recalibrated after the initialization sequence is complete and the device is powered up. The recalibration sequence must be run for every 10°C temperature change; the temperature can be monitored using the temperature sensor (see the Temperature Sensor section).

1. Write 0x809FE520 to Register R0 to enable the counters. Tx1 and Tx2 are off, and LO is on.
2. Write 0x2A20B929 to Register R9.

3. Write 0xFFF7FFE1 to Register R1 to set the Tx amplitude level.
4. Write 0x809FE720 to Register R0 to set the VCO frequency calibration (800 µs).
5. Write 0x809FE560 to Register R0 to power Tx1 on, Tx2 off, and LO on.
6. Write 0x809FED60 to Register R0 to set the Tx1 amplitude calibration (400 µs).
7. Write 0x89FE5A0 to Register R0 to power Tx1 off, Tx2 on, and LO on.
8. Write 0x809FF5A0 to Register R0 to set the Tx2 amplitude calibration (400 µs).
9. Write 0x2800B929 to Register R9.
10. Write 0x809F25A0 to Register R0 to disable the R and N counters.

TEMPERATURE SENSOR

The ADF5901 has an on-chip temperature sensor that can be accessed on the ATEST pin or as a digital word on DOUT following an ADC conversion. The temperature sensor operates over the full operating temperature range of −40°C to +105°C. The accuracy can be improved by performing a one-point calibration at room temperature and storing the result in memory.

With the temperature sensor on the analog test bus and test bus connected to the ATEST pin (Register 4 set to 0x0000A064) the ATEST voltage can be converted to temperature with the following equation:

$$Temperature\ (^{\circ}\mathrm{C}) = \frac{(V_{ATEST} - V_{OFF})}{V_{GAIN}} \quad (3)$$

where:
V_{ATEST} is the voltage on the ATEST pin.
V_{OFF} = 0.699 V, the offset voltage.
$V_{GAIN} = 6.4 \times 10^{-3}$, the voltage gain.

The temperature sensor result can be converted to a digital word with the ADC and readback on DOUT with the following sequence:

1. Write 0x809FA5A0 to Register R0 to enable the counters.
2. Write 0x00012064 to Register R4 to connect the analog test bus to the ADC and V_{TEMP} to the analog test bus.
3. Write 0x00028C82 to Register R2 to start the ADC conversion.
4. Write 0x018902C3 to Register R3 to set the output ADC data to DOUT.
5. Read back DOUT.
6. Write 0x809F25A0 to Register R0 to disable R and N counters.

Convert the DOUT word to temperature with the following equation:

$$Temperature\ (^{\circ}\mathrm{C}) = \frac{((ADC \times V_{LSB}) - V_{OFF})}{V_{GAIN}} \quad (4)$$

where:
ADC is the ADC code read back on DOUT.
V_{LSB} = 7.33 mV, the ADC LSB voltage.
V_{OFF} = 0.699 V, the offset voltage.
$V_{GAIN} = 6.4 \times 10^{-3}$, the voltage gain.

RF SYNTHESIS: A WORKED EXAMPLE

The following equation governs how to program the ADF5901:

$$RF_{OUT} = (INT + (FRAC/2^{25})) \times (f_{REF}) \times 2 \quad (5)$$

where:
RF_{OUT} is the RF frequency output.
INT is the integer division factor.
FRAC is the fractionality.

$$f_{REF} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \quad (6)$$

where:
REF_{IN} is the reference frequency input.
D is the reference doubler bit, DB10 in Register R7 (0 or 1).
R is the reference division factor.
T is the reference divide by 2 bit, DB11 in Register R7 (0 or 1).

For example, in a system where a 24.125 GHz RF frequency output (RF_{OUT}) is required and a 100 MHz reference frequency input (REF_{IN}) is available, f_{REF} is set to 50 MHz.

From Equation 6,

$$f_{REF} = (100\ \mathrm{MHz} \times (1 + 0)/(1 \times (1 + 1)) = 50\ \mathrm{MHz}$$

From Equation 5,

$$24.125\ \mathrm{GHz} = 50\ \mathrm{MHz} \times (N + FRAC/2^{25}) \times 2$$

Calculating the N and FRAC values,

$$N = \mathrm{int}(RF_{OUT}/(f_{REF} \times 2)) = 241$$
$$FRAC = F_{MSB} \times 2^{13} + F_{LSB}$$
$$F_{MSB} = \mathrm{int}(((RF_{OUT}/(f_{REF} \times 2)) - \mathrm{N}) \times 2^{12}) = 1024$$
$$F_{LSB} = \mathrm{int}((((RF_{OUT}/(f_{REF} \times 2)) - \mathrm{N}) \times 2^{12}) - F_{MSB}) \times 2^{13}) = 0$$

where:
F_{MSB} is the 12-bit MSB FRAC value in Register R5.
F_{LSB} is the 13-bit LSB FRAC value in Register R6.
int() makes an integer of the argument in parentheses.

APPLICATIONS INFORMATION

APPLICATION OF THE ADF5901 IN FMCW RADAR

Figure 31 shows the application of the ADF5901 in a frequency modulated continuous wave (FMCW) radar system.

In the FMCW radar system, the ADF4159 generates the sawtooth or triangle ramps necessary for this type of radar to operate.

The ADF4159 controls the V_{TUNE} pin on the ADF5901 (Tx) MMIC and thus the frequency of the VCO and the Tx output signal on $TX_{OUT}1$ or $TX_{OUT}2$. The LO signal from the ADF5901 is fed to the LO input on the ADF5904.

The ADF5904 downconverts the signal from the four receiver antennas to baseband with the LO signal from the Tx MMIC.

The downconverted baseband signals from the four receiver channels on the ADF5904 are fed to the ADAR7251 4-channel, continuous time, Σ-Δ analog-to-digital converter (ADC).

A digital signal processor (DSP) follows the ADC to handle the target information processing.

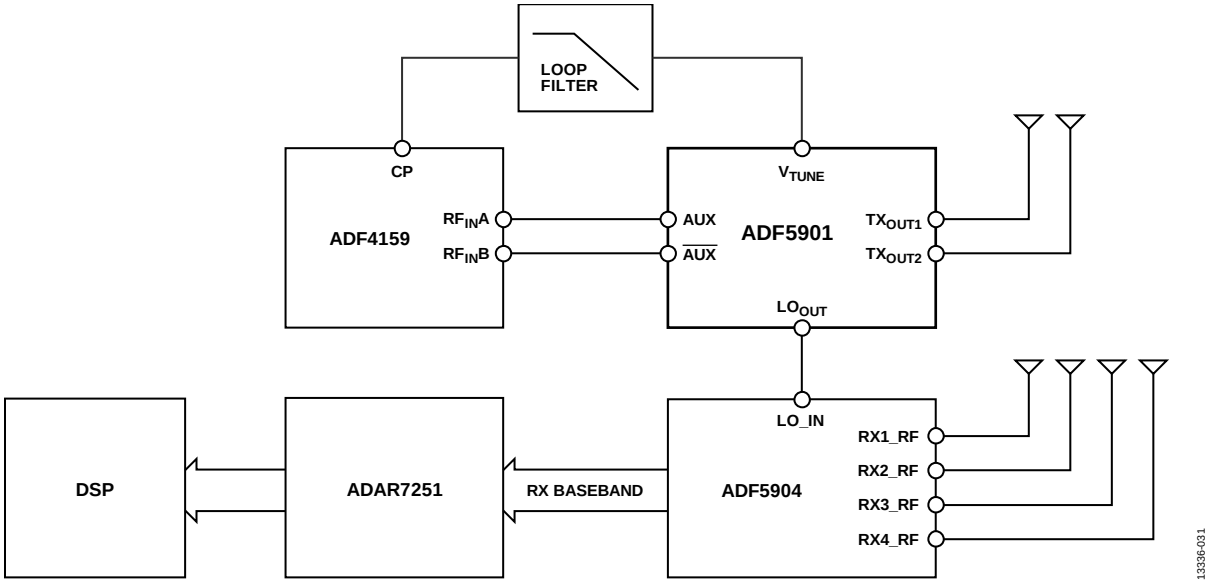

Figure 31. FMCW Radar with ADF5901

OUTLINE DIMENSIONS

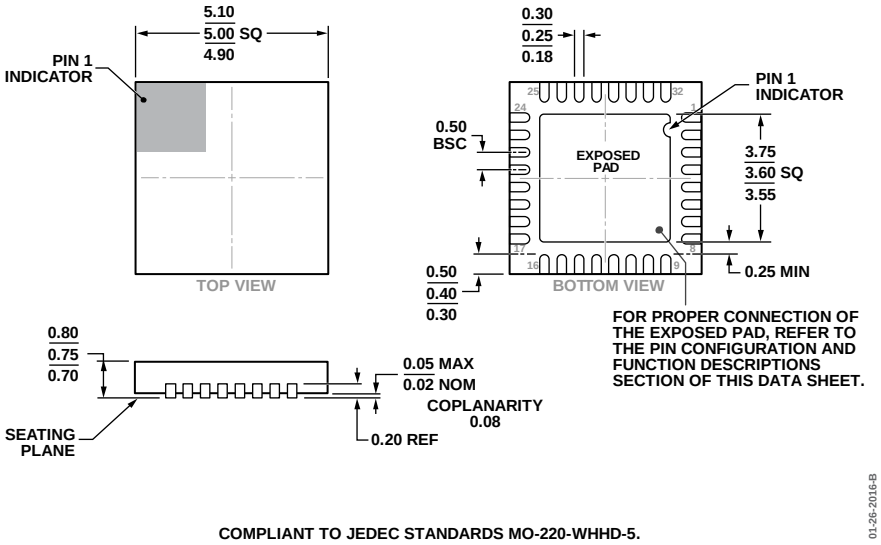

Figure 32. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-12)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF5901ACPZ	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADF5901ACPZ-RL7	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADF5901WCCPZ	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADF5901WCCPZ-RL7	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
EV-ADF5901SD2Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

AUTOMOTIVE PRODUCTS

The ADF5901W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

D13336-0-8/17(B)

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