THE DATASHEET OF

MSP430F4784IPZR

SLAS545C – MAY 2007 – REVISED MARCH 2011

- **Low Supply-Voltage Range, 1.8 V to 3.6 V**
- **Ultra-Low Power Consumption:**
  - **Active Mode: 280 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 1.1 μA**
  - **Off Mode (RAM Retention): 0.2 μA**
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in Less Than 6 μs**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Three or Four 16-Bit Sigma-Delta Analog-to-Digital (A/D) Converters With Differential PGA Inputs**
- **16-Bit Timer_B With Three Capture/Compare-With-Shadow Registers**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **On-Chip Comparator**
- **Four Universal Serial Communication Interfaces (USCI)**
  - **USCI_A0 and USCI_A1**
    - **Enhanced UART Supporting Auto-Baudrate Detection**
    - **IrDA Encoder and Decoder**
    - **Synchronous SPI**
  - **USCI_B0 and USCI_B1**
    - **I^2C**
    - **Synchronous SPI**
- **Integrated LCD Driver With Contrast Control For Up To 160 Segments**
- **32-Bit Hardware Multiplier**
- **Brownout Detector**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Bootstrap Loader**
- **On Chip Emulation Module**
- **Family Members Include:**
  MSP430F4783: 48KB + 256B Flash
  2KB RAM
  3 Sigma-Delta ADCs
  MSP430F4793: 60KB + 256B Flash
  2.5KB RAM
  3 Sigma-Delta ADCs
  MSP430F4784: 48KB + 256B Flash
  2KB RAM
  4 Sigma-Delta ADCs
  MSP430F4794: 60KB + 256B Flash
  2.5KB RAM
  4 Sigma-Delta ADCs
  MSP430F47x3 and MSP430F47x4 Available In 100-Pin Plastic Quad Flatpack (QFP) Package
- **For Complete Module Descriptions, See the *MSP430x4xx Family User's Guide,* Literature Number SLAU056**

description

The Texas Instruments MSP430 family of ultra-low power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6μs.

The MSP430F47xx series are microcontroller configurations targeted to single phase electricity meters with three or four 16-bit sigma-delta A/D converters. Each channel has a differential input pair and programmable input gain. Also integrated are two 16-bit timers, three universal serial communication interfaces (USCI), 72 I/O pins, and a liquid crystal driver (LCD) with integrated contrast control.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	PLASTIC 100-PIN QFP (PZ)
–40°C to 85°C	MSP430F4783IPZ MSP430F4793IPZ MSP430F4784IPZ MSP430F4794IPZ

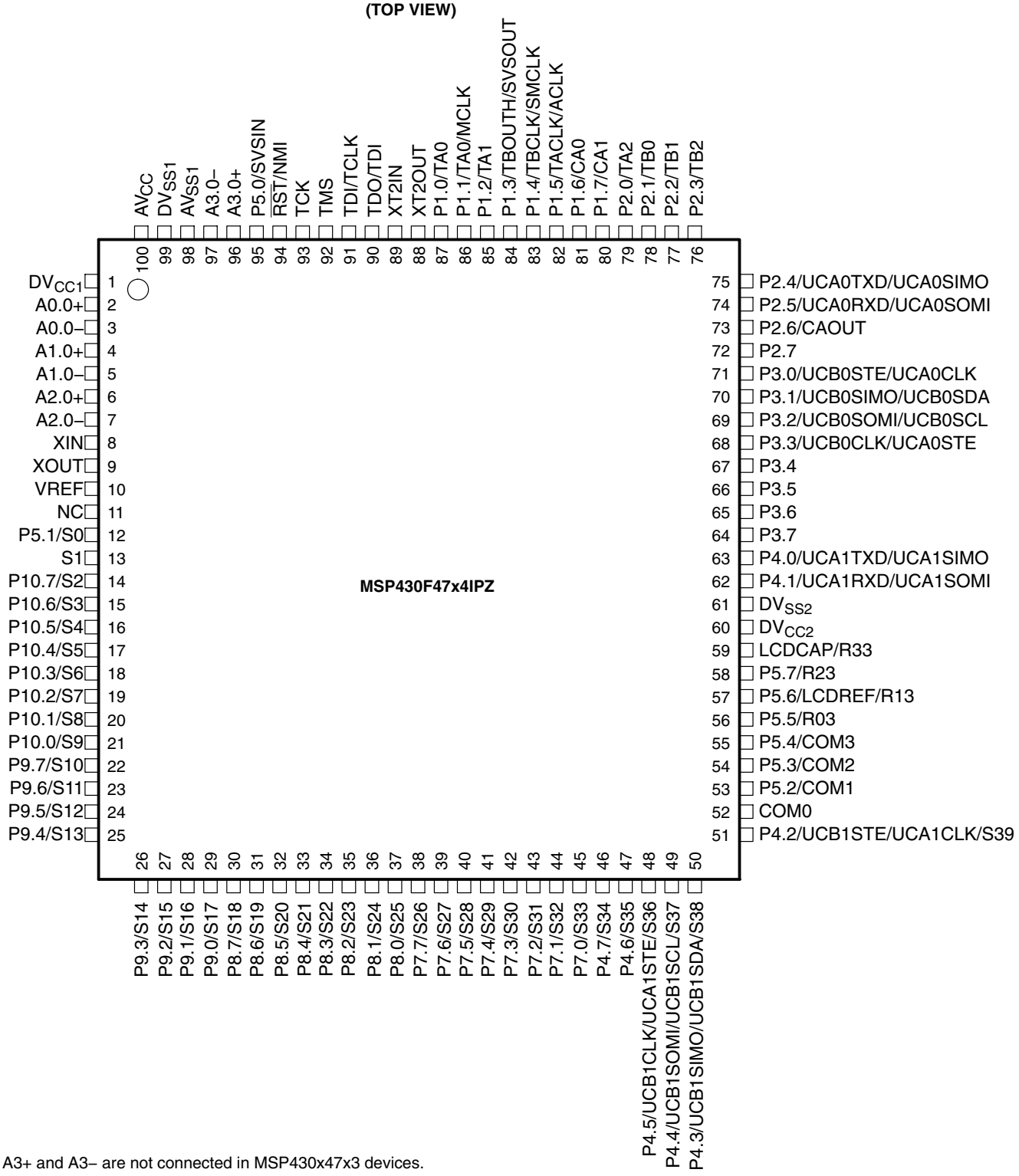
DEVELOPMENT TOOL SUPPORT

All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy to use development tools. Recommended hardware options include the following:

- Debugging and Programming Interface
  - MSP–FET430UIF (USB)
  - MSP–FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP–FET430U100
- Production Programmer
  - MSP–GANG430

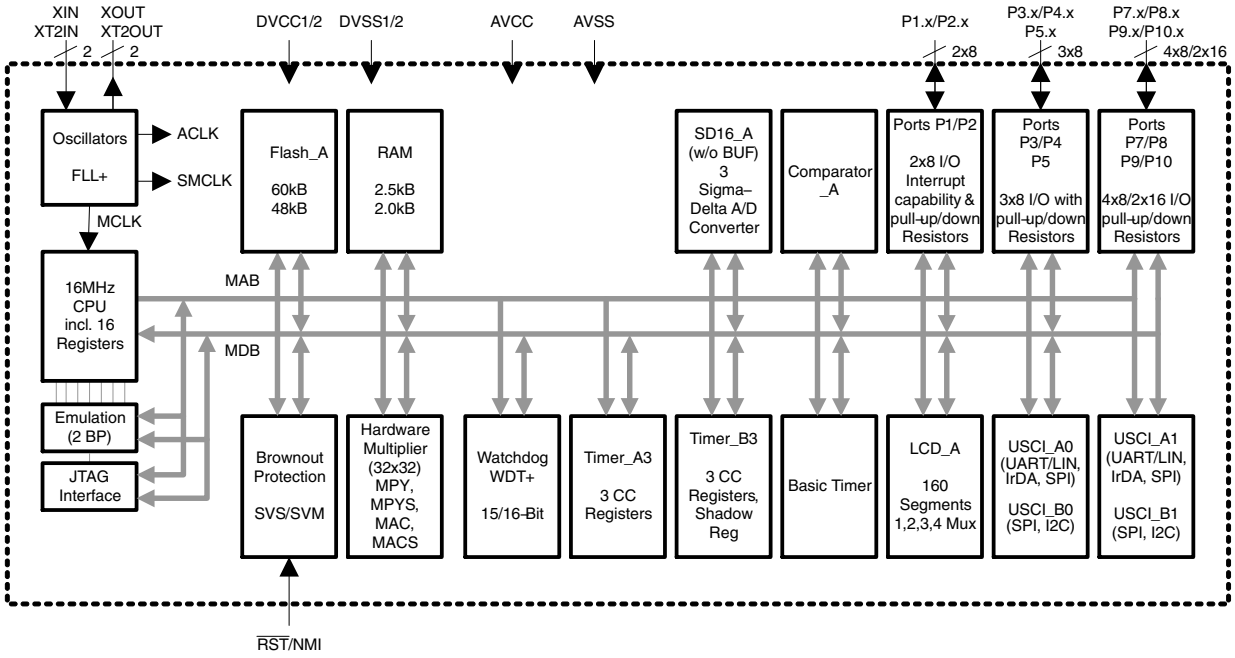
pin designation, MSP430F47xxIPZ

PZ PACKAGE
(TOP VIEW)

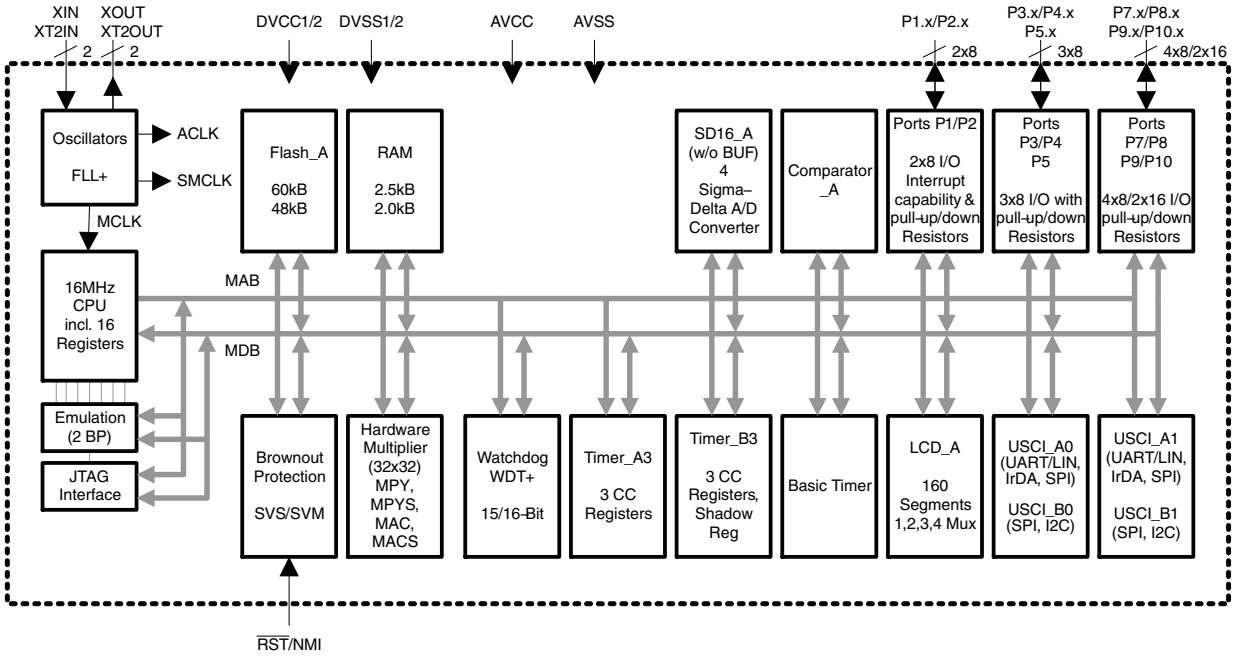


A3+ and A3– are not connected in MSP430x47x3 devices.

MSP430F47x3 functional block diagram



MSP430F47x4 functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
DV_{CC1}	1		Digital supply voltage, positive terminal.
A0.0+	2	I	SD16_A positive analog input A0.0 (see Note 1)
A0.0–	3	I	SD16_A negative analog input A0.0 (see Note 1)
A1.0+	4	I	SD16_A positive analog input A1.0 (see Note 1)
A1.0–	5	I	SD16_A negative analog input A1.0 (see Note 1)
A2.0+	6	I	SD16_A positive analog input A2.0 (see Note 1)
A2.0–	7	I	SD16_A negative analog input A2.0 (see Note 1)
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1
V_{REF}	10	I/O	Input for an external reference voltage / Internal reference voltage output (can be used as mid-voltage)
NC	11		Internally not connected. Can be connected to V_{SS}.
P5.1/S0	12	I/O	General-purpose digital I/O / LCD segment output 0
S1	13	O	LCD segment output 1
P10.7/S2	14	I/O	General-purpose digital I/O / LCD segment output 2
P10.6/S3	15	I/O	General-purpose digital I/O / LCD segment output 3
P10.5/S4	16	I/O	General-purpose digital I/O / LCD segment output 4
P10.4/S5	17	I/O	General-purpose digital I/O / LCD segment output 5
P10.3/S6	18	I/O	General-purpose digital I/O / LCD segment output 6
P10.2/S7	19	I/O	General-purpose digital I/O / LCD segment output 7
P10.1/S8	20	I/O	General-purpose digital I/O / LCD segment output 8
P10.0/S9	21	I/O	General-purpose digital I/O / LCD segment output 9
P9.7/S10	22	I/O	General-purpose digital I/O / LCD segment output 10
P9.6/S11	23	I/O	General-purpose digital I/O / LCD segment output 11
P9.5/S12	24	I/O	General-purpose digital I/O / LCD segment output 12
P9.4/S13	25	I/O	General-purpose digital I/O / LCD segment output 13
P9.3/S14	26	I/O	General-purpose digital I/O / LCD segment output 14
P9.2/S15	27	I/O	General-purpose digital I/O / LCD segment output 15
P9.1/S16	28	I/O	General-purpose digital I/O / LCD segment output 16
P9.0/S17	29	I/O	General-purpose digital I/O / LCD segment output 17
P8.7/S18	30	I/O	General-purpose digital I/O / LCD segment output 18
P8.6/S19	31	I/O	General-purpose digital I/O / LCD segment output 19
P8.5/S20	32	I/O	General-purpose digital I/O / LCD segment output 20
P8.4/S21	33	I/O	General-purpose digital I/O / LCD segment output 21
P8.3/S22	34	I/O	General-purpose digital I/O / LCD segment output 22
P8.2/S23	35	I/O	General-purpose digital I/O / LCD segment output 23
P8.1/S24	36	I/O	General-purpose digital I/O / LCD segment output 24
P8.0/S25	37	I/O	General-purpose digital I/O / LCD segment output 25
P7.7/S26	38	I/O	General-purpose digital I/O / LCD segment output 26
P7.6/S27	39	I/O	General-purpose digital I/O / LCD segment output 27
P7.5/S28	40	I/O	General-purpose digital I/O / LCD segment output 28
P7.4/S29	41	I/O	General-purpose digital I/O / LCD segment output 29
P7.3/S30	42	I/O	General-purpose digital I/O / LCD segment output 30

NOTE 1: Open connection recommended for all unused analog inputs.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P7.2/S31	43	I/O	General-purpose digital I/O / LCD segment output 31
P7.1/S32	44	I/O	General-purpose digital I/O / LCD segment output 32
P7.0/S33	45	I/O	General-purpose digital I/O / LCD segment output 33
P4.7/S34	46	I/O	General-purpose digital I/O / LCD segment output 34
P4.6/S35	47	I/O	General-purpose digital I/O / LCD segment output 35
P4.5/ UCB1CLK/UCA1STE/ S36	48	I/O	General-purpose digital I/O / USCI_B1 clock input/output / USCI_A1 slave transmit enable / LCD segment output 36
P4.4/ UCB1SOMI/UCB1SCL/ S37	49	I/O	General-purpose digital I/O / USCI_B1 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode / LCD segment output 37
P4.3/ UCB1SIMO/UCB1SDA/ S38	50	I/O	General-purpose digital I/O / USCI_B1 slave in/master out in SPI mode, SDA I^2C data in I^2C mode / LCD segment output 38
P4.2/ UCB1STE/UCA1CLK/ S39	51	I/O	General-purpose digital I/O / USCI_B1 slave transmit enable / USCI_A1 clock input/output / LCD segment output 39
COM0	52	O	COM0–3 are used for LCD backplanes.
P5.2/COM1	53	I/O	General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.
P5.3/COM2	54	I/O	General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.
P5.4/COM3	55	I/O	General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.
P5.5/R03	56	I/O	General-purpose digital I/O / Input port of lowest analog LCD level (V5)
P5.6/LCDREF/R13	57	I/O	General-purpose digital I/O / External reference voltage input for regulated LCD voltage / Input port of third most positive analog LCD level (V4 or V3)
P5.7/R23	58	I/O	General-purpose digital I/O / Input port of second most positive analog LCD level (V2)
LCDCAP/R33	59	I	LCD Capacitor connection / Input/output port of most positive analog LCD level (V1)
DV_{CC2}	60		Digital supply voltage, positive terminal.
DV_{SS2}	61		Digital supply voltage, negative terminal.
P4.1/ UCA1RXD/UCA1SOMI	62	I/O	General-purpose digital I/O / USCI_A1 receive data input in UART mode, slave out/master in in SPI mode
P4.0/ UCA1TXD/UCA1SIMO	63	I/O	General-purpose digital I/O / USCI_A1 transmit data output in UART mode, slave in/master out in SPI mode
P3.7	64	I/O	General-purpose digital I/O
P3.6	65	I/O	General-purpose digital I/O
P3.5	66	I/O	General-purpose digital I/O
P3.4	67	I/O	General-purpose digital I/O
P3.3/ UCB0CLK/UCA0STE	68	I/O	General-purpose digital I/O / USCI_B0 clock input/output / USCI_A0 slave transmit enable
P3.2/ UCB0SOMI/UCB0SCL	69	I/O	General-purpose digital I/O / USCI_B1 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P3.1/ UCB0SIMO/UCB0SDA	70	I/O	General-purpose digital I/O / USCI_B1 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P3.0/ UCB0STE/UCA0CLK	71	I/O	General-purpose digital I/O / USCI_B0 slave transmit enable / USCI_A0 clock input/output
P2.7	72	I/O	General-purpose digital I/O
P2.6/CAOUT	73	I/O	General-purpose digital I/O / Comparator_A output

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P2.5/ UCA0RXD/UCA0SOMI	74	I/O	General-purpose digital I/O / USCI_A0 receive data input in UART mode, slave out/master in in SPI mode
P2.4/ UCA0TXD/UCA0SIMO	75	I/O	General-purpose digital I/O / USCI_A0 transmit data output in UART mode, slave in/master out in SPI mode
P2.3/TB2	76	I/O	General-purpose digital I/O / Timer_B3 CCR2. Capture: CCI2A/CCI2B input, compare: Out2 output
P2.2/TB1	77	I/O	General-purpose digital I/O / Timer_B3 CCR1. Capture: CCI1A/CCI1B input, compare: Out1 output
P2.1/TB0	78	I/O	General-purpose digital I/O / Timer_B3 CCR0. Capture: CCI0A/CCI0B input, compare: Out0 output
P2.0/TA2	79	I/O	General-purpose digital I/O / Timer_A Capture: CCI2A input, compare: Out2 output
P1.7/CA1	80	I/O	General-purpose digital I/O / Comparator_A input
P1.6/CA0	81	I/O	General-purpose digital I/O / Comparator_A input
P1.5/TACLK/ ACLK	82	I/O	General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8)
P1.4/TBCLK/ SMCLK	83	I/O	General-purpose digital I/O / input clock TBCLK—Timer_B3 / submain system clock SMCLK output
P1.3/TBOUTH/ SVSOUT	84	I/O	General-purpose digital I/O / switch all PWM digital output ports to high impedance—Timer_B3 TB0 to TB2 / SVS: output of SVS comparator
P1.2/TA1	85	I/O	General-purpose digital I/O / Timer_A, Capture: CCI1A input, compare: Out1 output
P1.1/TA0/MCLK	86	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0B input / MCLK output. Note: TA0 is only an input on this pin / BSL receive
P1.0/TA0	87	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0A input, compare: Out0 output / BSL transmit
XT2OUT	88	O	Output terminal of crystal oscillator XT2
XT2IN	89	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
TDO/TDI	90	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TDI/TCLK	91	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TMS	92	I	Test mode select. TMS is used as an input port for device programming and test.
TCK	93	I	Test clock. TCK is the clock input port for device programming and test.
$\overline{\text{RST}}$/NMI	94	I	Reset input or nonmaskable interrupt input port
P5.0/SVSIN	95	I/O	General-purpose digital I/O / analog input to supply voltage supervisor
A3.0+ (MSP430x47x4 only)	96	I	SD16_A positive analog input A3.0 (see Note 2) Not connected in MSP430x47x3 devices, open connection recommended.
A3.0– (MSP430x47x4 only)	97	I	SD16_A negative analog input A3.0 (see Note 2) Not connected in MSP430x47x3 devices, open connection recommended.
AV_{SS}	98		Analog supply voltage, negative terminal.
DV_{SS1}	99		Digital supply voltage, negative terminal.
AV_{CC}	100		Analog supply voltage, positive terminal. Must not power up prior to DV_{CC1}/DV_{CC2}.

NOTE 2: Open connection recommended for all unused analog inputs.

short-form description

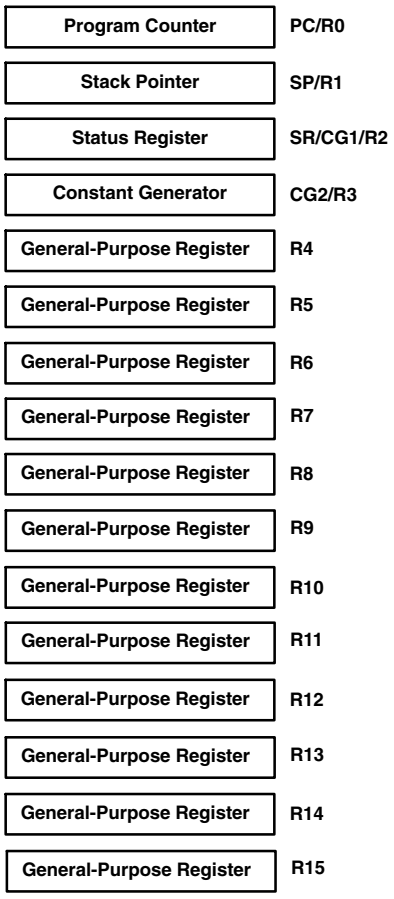
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4, R5	R4 + R5 –––> R5
Single operands, destination only	e.g., CALL R8	PC –––>(TOS), R8–––> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs, Rd	MOV R10, R11	R10 –––> R11
Indexed	●	●	MOV X(Rn), Y(Rm)	MOV 2(R5), 6(R6)	M(2+R5)–––> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE, TONI		M(EDE) –––> M(TONI)
Absolute	●	●	MOV &MEM, &TCDAT		M(MEM) –––> M(TCDAT)
Indirect	●		MOV @Rn, Y(Rm)	MOV @R10, Tab(R6)	M(R10) –––> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+, Rm	MOV @R10+, R11	M(R10) –––> R11 R10 + 2–––> R10
Immediate	●		MOV #X, TONI	MOV #45, TONI	#45 –––> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled.
  - ACLK and SMCLK remain active.
  - MCLK is disabled.
  - FLL+ loop control remains active
- Low-power mode 1(LPM1)
  - CPU is disabled.
  - FLL+ loop control is disabled.
  - ACLK and SMCLK remain active.
  - MCLK is disabled.
- Low-power mode 2 (LPM2)
  - CPU is disabled.
  - MCLK, FLL+ loop control, and DCOCLK are disabled.
  - DCO's dc generator remains enabled.
  - ACLK remains active.
- Low-power mode 3 (LPM3)
  - CPU is disabled.
  - MCLK, FLL+ loop control, and DCOCLK are disabled.
  - DCO's dc generator is disabled.
  - ACLK remains active.
- Low-power mode 4 (LPM4)
  - CPU is disabled.
  - ACLK is disabled.
  - MCLK, FLL+ loop control, and DCOCLK are disabled.
  - DCO's dc generator is disabled.
  - Crystal oscillator is stopped.

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (e.g., flash is not programmed) the CPU goes into LPM4 immediately after power-up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Flash Memory PC Out–of–Range (see Note 4)	PORIFG RSTIFG WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash Memory Access Violation	NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1 and 3)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
Timer_B3	TBCCR0 CCIFG (see Note 2)	Maskable	0FFFAh	13
Timer_B3	TBCCR1 to TBCCR2 CCIFGs TBIFG (see Notes 1 and 2)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF6h	11
Watchdog Timer	WDTIFG	Maskable	0FFF4h	10
USCI_A0/B0 Receive	UCA0RXIFG, UCB0RXIFG (see Note 1 and 5)	Maskable	0FFF2h	9
USCI_A0/B0 Transmit	UCA0TXIFG, UCB0TXIFG (see Note 1 and 6)	Maskable	0FFF0h	8
SD16_A	SD16CCTLx SD16OVIFG, SD16CCTLx SD16IFG (see Notes 1 and 2)	Maskable	0FFEEh	7
Timer_A3	TACCR0 CCIFG (see Note 2)	Maskable	0FFECh	6
Timer_A3	TACCR1 and TACCR2 CCIFGs, TAIFG (see Notes 1 and 2)	Maskable	0FFEAh	5
I/O Port P1 (Eight Flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	Maskable	0FFE8h	4
USCI_A1/B1 Receive	UCA1RXIFG, UCB1RXIFG (see Notes 1 and 2)	Maskable	0FFE6h	3
USCI_A1/B1 Transmit	UCA1TXIFG, UCB1TXIFG (see Notes 1 and 2)	Maskable	0FFE4h	2
I/O Port P2 (Eight Flags)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	Maskable	0FFE2h	1
Basic Timer1	BTIFG	Maskable	0FFE0h	0, lowest

NOTES:
1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: The individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
4. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh).
5. In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG in register UCB0STAT.
6. In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
7. In SPI mode: UCB1RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG in register UCB1STAT.
8. In UART/SPI mode: UCB1TXIFG. In I2C mode: UCB1RXIFG, UCB1TXIFG.

special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw–0	rw–0			rw–0	rw–0

WDTIE Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

OFIE Oscillator fault enable

NMIIE (Non)maskable interrupt enable

ACCVIE Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h	BTIE				UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
	rw–0				rw–0	rw–0	rw–0	rw–0

UCA0RXIE USCI_A0 receive interrupt enable

UCA0TXIE USCI_A0 transmit interrupt enable

UCB0RXIE USCI_B0 receive interrupt enable

UCB0TXIE USCI_B0 transmit interrupt enable

BTIE Basic timer interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw–0	rw–(0)	rw–(1)	rw–1	rw–(0)

WDTIFG Set on watchdog timer overflow or security key violation.
Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.

OFIFG Flag set on oscillator fault

RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up.

PORIFG Power-on interrupt flag. Set on V_{CC} power-up.

NMIIFG Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h	BTIFG				UCB0 TXIFG	UCB0 RXIFG	UCA0 TXIFG	UCA0 RXIFG
	rw–0				rw–1	rw–0	rw–1	rw–0

UCA0RXIFG USCI_A0 receive interrupt flag

UCA0TXIFG USCI_A0 transmit interrupt flag

UCB0RXIFG USCI_B0 receive interrupt flag

UCB0TXIFG USCI_B0 transmit interrupt flag

BTIFG Basic Timer1 interrupt flag

Legend		
	rw:	Bit can be read and written.
	rw-0, 1:	Bit can be read and written. It is Reset or Set by PUC.
	rw-(0, 1):	Bit can be read and written. It is Reset or Set by POR.
		SFR bit is not present in device

memory organization

		MSP430F4783/MSP430F4784	MSP430F4793/MSP430F4794
Memory Main: interrupt vector Main: code memory	Size Flash Flash	48KB 0FFFFh to 0FFE0h 0FFFFh to 04000h	60KB 0FFFFh to 0FFE0h 0FFFFh to 01100h
Information memory	Size Flash	256 Byte 010FFh to 01000h	256 Byte 010FFh to 01000h
Boot memory	Size ROM	1KB 0FFFh to 0C00h	1KB 0FFFh to 0C00h
RAM	Size	2KB 09FFh to 0200h	2.5KB 0BFFh to 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh to 0100h 0FFh to 010h 0Fh to 00h	01FFh to 0100h 0FFh to 010h 0Fh to 00h

bootstrap loader (BSL)

The BSL enables users to program the flash memory or RAM using a UART serial interface. Access to device memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the application report *Features of the MSP430 Bootstrap Loader*, literature number SLAA089.

BSL FUNCTION	PZ PACKAGE PINS
Data transmit	87 - P1.0
Data receive	86 - P1.1

flash memory, flash

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called *information memory.*
- Segment A might contain calibration data. After reset, segment A is protected against programming or erasing. It can be unlocked but care should be taken not to erase this segment if the calibration data is required.

peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x4xx Family User's Guide*, literature number SLAU056.

digital I/O

There are nine 8-bit I/O ports implemented—ports P1 through P5 and P7 through P10.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Ports P7/P8 and P9/P10 can be accessed word-wise as ports PA and PB respectively.
- Each I/O has an individually programmable pullup/pulldown resistor.

oscillator and system clock

The clock system in the MSP430x47xx is supported by the FLL+ module, which includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO), and a 8-MHz high-frequency crystal oscillator (XT1), plus a 16-MHz high-frequency crystal oscillator (XT2). The FLL+ clock module is designed to meet the requirements of both low system cost and low power consumption. The FLL+ features digital frequency-locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

brownout, supply voltage supervisor (SVS)

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must ensure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

hardware multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

watchdog timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

universal serial communication interfaces (USCI_A0, USCI_B0, USCI_A1, USCI_B1)

The universal serial communication interface (USCI) module is used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin), I2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI_A0 and USCI_A1 provide support for SPI (3-pin or 4-pin), UART, enhanced UART, and IrDA.

USCI_B0 and USCI_B1 provide support for SPI (3-pin or 4-pin) and I2C.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_A3 SIGNAL CONNECTIONS					
INPUT PIN NUMBER	**DEVICE INPUT SIGNAL**	**MODULE INPUT NAME**	**MODULE BLOCK**	**MODULE OUTPUT SIGNAL**	**OUTPUT PIN NUMBER**
82 - P1.5	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
82 - P1.5	$\overline{\text{TACLK}}$	INCLK			
87 - P1.0	TA0	CCI0A	CCR0	TA0	87 - P1.0
86 - P1.1	TA0	CCI0B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
85 - P1.2	TA1	CCI1A	CCR1	TA1	85 - P1.2
	CAOUT (internal)	CCI1B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
79 - P2.0	TA2	CCI2A	CCR2	TA2	79 - P2.0
	ACLK (internal)	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_B3 SIGNAL CONNECTIONS					
INPUT PIN NUMBER	**DEVICE INPUT SIGNAL**	**MODULE INPUT NAME**	**MODULE BLOCK**	**MODULE OUTPUT SIGNAL**	**OUTPUT PIN NUMBER**
83 - P1.4	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
83 - P1.4	$\overline{\text{TBCLK}}$	INCLK			
78 - P2.1	TB0	CCI0A	CCR0	TB0	78 - P2.1
78 - P2.1	TB0	CCI0B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
77 - P2.2	TB1	CCI1A	CCR1	TB1	77 - P2.2
77 - P2.2	TB1	CCI1B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
76 - P2.3	TB2	CCI2A	CCR2	TB2	76 - P2.3
76 - P2.3	TB2	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

comparator_A

The primary function of the comparator_A module is to support precision slope A/D conversions, battery-voltage supervision, and monitoring of external analog signals.

SD16_A

The SD16_A module integrates three (in MSP430F47x3) or four (in MSP430F47x4) independent 16-bit sigma–delta A/D converters. Each channel is designed with a fully differential analog input pair and programmable-gain amplifier input stage. In addition to external analog inputs, an internal V_{CC} sense and temperature sensor are also available.

Basic Timer1

The Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Basic Timer1 can be used to generate periodic interrupts and a clock for the LCD module.

LCD driver with regulated charge pump

The LCD_A driver generates the segment and common signals required to drive an LCD display. The LCD_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage via an integrated charge pump. Furthermore, it is possible to control the level of the LCD voltage and, thus, contrast in software.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog timer control	WDTCTL	0120h
Flash_A	Flash control 4	FCTL4	01BEh
	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Timer_B3	Capture/compare register 2	TBCCR2	0196h
	Capture/compare register 1	TBCCR1	0194h
	Capture/compare register 0	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 2	TBCCTL2	0186h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 0	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A3	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
32-bit Hardware Multiplier	MPY32 control 0	MPY32CTL0	015Ch
	64-bit result 3 – most significant word	RES3	015Ah
	64-bit result 2	RES2	0158h
	64-bit result 1	RES1	0156h
	64-bit result 0 – least significant word	RES0	0154h
	Second 32-bit operand, high word	OP2H	0152h
	Second 32-bit operand, low word	OP2L	0150h
	Multiply signed + accumulate/ 32-bit operand1, high word	MACS32H	014Eh
	Multiply signed + accumulate/ 32-bit operand1, low word	MACS32L	014Ch
	Multiply + accumulate/ 32-bit operand1, high word	MAC32H	014Ah
	Multiply + accumulate/ 32-bit operand1, low word	MAC32L	0148h
	Multiply signed/32-bit operand1, high word	MPYS32H	0146h
	Multiply signed/32-bit operand1, low word	MPYS32L	0144h
	Multiply unsigned/32-bit operand1, high word	MPY32H	0142h
	Multiply unsigned/32-bit operand1, low word	MPY32L	0140h

peripheral file map (continued)

PERIPHERALS WITH WORD ACCESS (CONTINUED)			
32-bit Hardware Multiplier	Sum extend	SUMEXT	013Eh
	Result high word	RESHI	013Ch
	Result low word	RESLO	013Ah
	Second operand	OP2	0138h
	Multiply signed + accumulate/operand1	MACS	0136h
	Multiply + accumulate/operand1	MAC	0134h
	Multiply signed/operand1	MPYS	0132h
	Multiply unsigned/operand1	MPY	0130h
USCI_B0 (see also: Peripherals with Byte Access)	USCI_B0 I2C own address	UCB0I2COA	016Ch
	USCI_B0 I2C slave address	UCB0I2CSA	016Eh
USCI_B1 (see also: Peripherals with Byte Access)	USCI_B1 I2C own address	UCB1I2COA	017Ch
	USCI_B1 I2C slave address	UCB1I2CSA	017Eh
SD16_A (see also: Peripherals with Byte Access)	General control	SD16CTL	0100h
	Channel 0 control	SD16CCTL0	0102h
	Channel 1 control	SD16CCTL1	0104h
	Channel 2 control	SD16CCTL2	0106h
	Channel 3 control	SD16CCTL3	0108h
	Interrupt vector word register	SD16IV	0110h
	Channel 0 conversion memory	SD16MEM0	0112h
	Channel 1 conversion memory	SD16MEM1	0114h
	Channel 2 conversion memory	SD16MEM2	0116h
	Channel 3 conversion memory	SD16MEM3	0118h
Port PA	Port PA resistor enable	PAREN	014h
	Port PA selection	PASEL	03Eh
	Port PA direction	PADIR	03Ch
	Port PA output	PAOUT	03Ah
	Port PA input	PAIN	038h
Port PB	Port PB resistor enable	PBREN	016h
	Port PB selection	PBSEL	00Eh
	Port PB direction	PBDIR	00Ch
	Port PB output	PBOUT	00Ah
	Port PB input	PBIN	008h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
SD16_A (see also: Peripherals with Word Access)	Channel 0 input control	SD16INCTL0	0B0h
	Channel 1 input control	SD16INCTL1	0B1h
	Channel 2 input control	SD16INCTL2	0B2h
	Channel 3 input control	SD16INCTL3	0B3h
	Channel 0 preload	SD16PRE0	0B8h
	Channel 1 preload	SD16PRE1	0B9h
	Channel 2 preload	SD16PRE2	0BAh
	Channel 3 preload	SD16PRE3	0BBh
	Reserved (internal SD16 Configuration 1)	SD16CONF1	0BFh
LCD_A	LCD voltage control 1	LCDAVCTL1	0AFh
	LCD voltage control 0	LCDAVCTL0	0AEh
	LCD voltage port control 1	LCDAPCTL1	0ADh
	LCD voltage port control 0	LCDAPCTL0	0ACh
	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDACTL	090h
USCI_A0	USCI_A0 transmit buffer	UCA0TXBUF	067h
	USCI_A0 receive buffer	UCA0RXBUF	066h
	USCI_A0 status	UCA0STAT	065h
	USCI_A0 modulation control	UCA0MCTL	064h
	USCI_A0 baud rate control 1	UCA0BR1	063h
	USCI_A0 baud rate control 0	UCA0BR0	062h
	USCI_A0 control 1	UCA0CTL1	061h
	USCI_A0 control 0	UCA0CTL0	060h
	USCI_A0 IrDA receive control	UCA0IRRCTL	05Fh
	USCI_A0 IrDA transmit control	UCA0IRTCTL	05Eh
	USCI_A0 auto baud rate control	UCA0ABCTL	05Dh
USCI_B0	USCI_B0 transmit buffer	UCB0TXBUF	06Fh
	USCI_B0 receive buffer	UCB0RXBUF	06Eh
	USCI_B0 status	UCB0STAT	06Dh
	USCI_B1 I2C interrupt enable	UCB0I2CIE	06Ch
	USCI_B0 bit rate control 1	UCB0BR1	06Bh
	USCI_B0 bit rate control 0	UCB0BR0	06Ah
	USCI_B0 control 1	UCB0CTL1	069h
	USCI_B0 control 0	UCB0CTL0	068h
USCI_A1	USCI_A1 transmit buffer	UCA1TXBUF	0D7h
	USCI_A1 receive buffer	UCA1RXBUF	0D6h
	USCI_A1 status	UCA1STAT	0D5h
	USCI_A1 modulation control	UCA1MCTL	0D4h
	USCI_A1 baud rate control 1	UCA1BR1	0D3h
	USCI_A1 baud rate control 0	UCA1BR0	0D2h
	USCI_A1 control 1	UCA1CTL1	0D1h
	USCI_A1 control 0	UCA1CTL0	0D0h
	USCI_A1 IrDA receive control	UCA1IRRCTL	0CFh
	USCI_A1 IrDA transmit control	UCA1IRTCTL	0CEh
	USCI_A1 auto baud rate control	UCA1ABCTL	0CDh
	USCI_A1 interrupt flag	UC1IFG	007h
	USCI_A1 interrupt enable	UC1IE	006h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
USCI_B1	USCI_B1 transmit buffer	UCB1TXBUF	0DFh
	USCI_B1 receive buffer	UCB1RXBUF	0DEh
	USCI_B1 status	UCB1STAT	0DDh
	USCI_B1 I2C interrupt enable	UCB1I2CIE	0DCh
	USCI_B1 bit rate control 1	UCB1BR1	0DBh
	USCI_B1 bit rate control 0	UCB1BR0	0DAh
	USCI_B1 control 1	UCB1CTL1	0D9h
	USCI_B1 control 0	UCB1CTL0	0D8h
	USCI_A1 interrupt flag	UC1IFG	007h
	USCI_A1 interrupt enable	UC1IE	006h
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control2	CACTL2	05Ah
	Comparator_A control1	CACTL1	059h
BrownOUT, SVS	SVS control register (reset by brownout signal)	SVSCTL	056h
FLL+ Clock	FLL+ control 2	FLL_CTL2	055h
	FLL+ control 1	FLL_CTL1	054h
	FLL+ control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
Basic Timer1	BT counter 2	BTCNT2	047h
	BT counter 1	BTCNT1	046h
	BT control	BTCTL	040h
Port P10	Port P10 resistor enable	P10REN	017h
	Port P10 selection	P10SEL	00Fh
	Port P10 direction	P10DIR	00Dh
	Port P10 output	P10OUT	00Bh
	Port P10 input	P10IN	009h
Port P9	Port P9 resistor enable	P9REN	016h
	Port P9 selection	P9SEL	00Eh
	Port P9 direction	P9DIR	00Ch
	Port P9 output	P9OUT	00Ah
	Port P9 input	P9IN	008h
Port P8	Port P8 resistor enable	P8REN	015h
	Port P8 selection	P8SEL	03Fh
	Port P8 direction	P8DIR	03Dh
	Port P8 output	P8OUT	03Bh
	Port P8 input	P8IN	039h
Port P7	Port P7 resistor enable	P7REN	014h
	Port P7 selection	P7SEL	03Eh
	Port P7 direction	P7DIR	03Ch
	Port P7 output	P7OUT	03Ah
	Port P7 input	P7IN	038h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Port P5	Port P5 resistor enable	P5REN	012h
	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 resistor enable	P4REN	011h
	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 resistor enable	P3REN	010h
	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 resistor enable	P2REN	02Fh
	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 resistor enable	P1REN	027h
	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special functions	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

absolute maximum ratings (see Note 1)

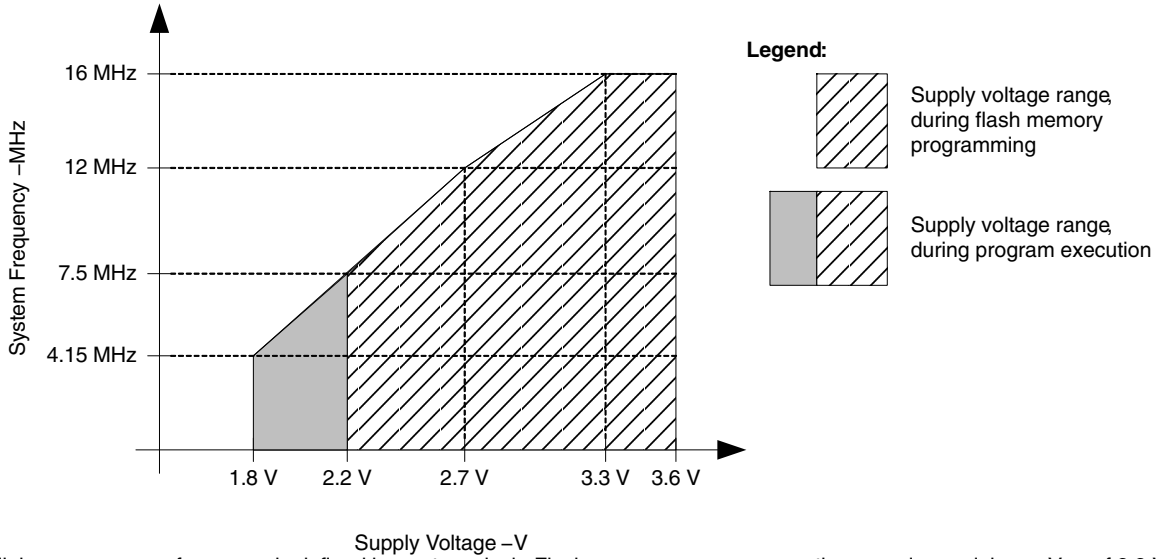
Voltage applied at V_{CC} to V_{SS} . . . . . –0.3 V to 4.1 V
Voltage applied to any pin (see Note 2) . . . . . –0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, T_{stg}: (unprogrammed device, see Note 3) . . . . . –55°C to 150°C
(programmed device, see Note 3) . . . . . –40°C to 85°C

NOTES: 1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.
3. Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage during program execution, V_{CC} (AV_{CC} = DV_{CC} = V_{CC}) (see Note 1)		1.8		3.6	V
Supply voltage during program execution, SVS enabled, PORON = 1, V_{CC} (AV_{CC} = DV_{CC} = V_{CC}) (see Notes 1, 2)		2.0		3.6	V
Supply voltage during program/erase flash memory, V_{CC} (AV_{CC} = DV_{CC} = V_{CC}) (see Note 1)		2.2		3.6	V
Supply voltage, V_{SS}			0		V
Operating free-air temperature range, T_A		–40		85	°C
Processor frequency f_{SYSTEM} (Maximum MCLK frequency) (see Notes 3, 4 and Figure 1)	V_{CC} = 1.8 V, Duty Cycle = 50% ±10%	dc		4.15	MHz
	V_{CC} = 2.2 V, Duty Cycle = 50% ±10%	dc		7.5	MHz
	V_{CC} = 2.7 V, Duty Cycle = 50% ±10%	dc		12	MHz
	$V_{CC} \geq$ 3.3 V, Duty Cycle = 50% ±10%	dc		16	

NOTES: 1. It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
2. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing supply voltage. POR is going inactive when the supply voltage is raised abve minimum supply voltage plus the hysteresis of the SVS circuitry.
3. The MSP430 CPU is clocked directly with MCLK.
Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
4. Modules might have a different maximum input clock specification. Refer to the specification of the respective module in this datasheet.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Operating Area

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32, 768 Hz XTS_FLL = 0, SELM = (0, 1) (Program executes from flash)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		280	350	µA
			V_{CC} = 3 V		420	560	
$I_{(LPM0)}$	Low-power mode, (LPM0) (see Notes 1, 4)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		45	70	µA
			V_{CC} = 3 V		75	110	
$I_{(LPM2)}$	Low-power mode, (LPM2), $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32, 768 Hz, SCG0 = 0 (see Notes 2, 4)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
			V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32, 768 Hz, SCG0 = 1 Basic Timer1 enabled, ACLK selected LCD_A enabled, LCDCPEN = 0, (static mode, $f_{LCD} = f_{(ACLK)}$ /32) (see Notes 2, 3, 4)	T_A = –40°C	V_{CC} = 2.2 V		1.0	2.0	µA
		T_A = 25°C			1.1	2.0	
		T_A = 60°C			2.0	3.0	
		T_A = 85°C			3.0	6.0	
		T_A = –40°C	V_{CC} = 3 V		1.2	3.0	µA
		T_A = 25°C			1.3	3.0	
		T_A = 60°C			2.5	3.5	
		T_A = 85°C			3.5	7.5	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32, 768 Hz, SCG0 = 1 Basic Timer1 enabled, ACLK selected LCD_A enabled, LCDCPEN = 0, (4–mux mode, $f_{LCD} = f_{(ACLK)}$ /32) (see Notes 2, 3, 4)	T_A = –40°C	V_{CC} = 2.2 V		3.5	5.5	µA
		T_A = 25°C			3.5	5.5	
		T_A = 60°C			5.5	7.0	
		T_A = 85°C			11.0	17.0	
		T_A = –40°C	V_{CC} = 3 V		4.0	8.0	µA
		T_A = 25°C			4.0	6.5	
		T_A = 60°C			6.0	8.0	
		T_A = 85°C			13.0	20.0	
$I_{(LPM4)}$	Low-power mode, (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1 (see Notes 2, 4)	T_A = –40°C	V_{CC} = 2.2 V		0.1	1.0	µA
		T_A = 25°C			0.2	1.0	
		T_A = 60°C			1.0	2.0	
		T_A = 85°C			1.8	5.0	
		T_A = –40°C	V_{CC} = 3 V		0.1	2.0	µA
		T_A = 25°C			0.2	2.0	
		T_A = 60°C			1.5	2.5	
		T_A = 85°C			2.0	6.0	

NOTES: 1. Timer_A is clocked by $f_{(DCOCLK)} = f_{(DCO)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
2. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
3. The LPM3 currents are characterized with a Micro Crystal CC4V–T1A (9 pF) crystal and OSCCAPx = 1h.
4. Current for brownout included.

typical characteristics – active mode supply current (into V_{CC})

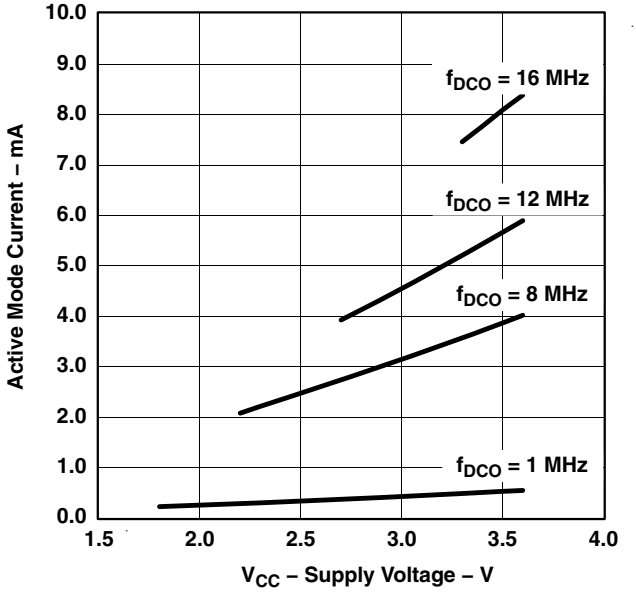


Figure 2. Active mode current vs V_{CC}, T_A = 25°C

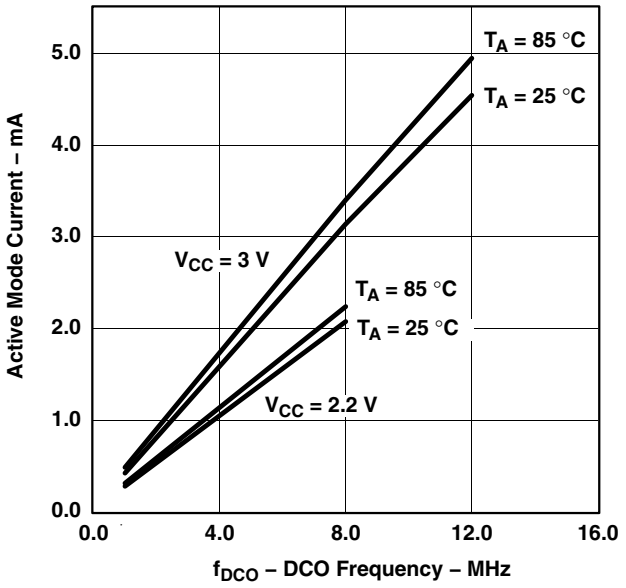


Figure 3. Active mode current vs DCO frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – Ports P1 through P5, P7 through P10, RST/NMI, JTAG: TCK, TMS, TDI/TCLK, TDO/TDI

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45		0.75	V_{CC}
			2.2 V	1.00		1.65	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25		0.55	V_{CC}
			2.2 V	0.55		1.20	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})		2.2 V	0.2		1.0	V
			3 V	0.3		1.0	
R_{Pull}	Pull–up/pull–down resistor (not RST/NMI and JTAG pins)	For pull–up: $V_{IN} = V_{SS}$, For pull–down: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input Capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

inputs – Ports P1, P2

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger puls width to set interrupt flag, (see Note 1)	2.2 V/3 V	20		ns

NOTES: 1. An external signal sets the interrupt flag every time the minimum interrupt puls width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

leakage current – Ports P1 through P5, P7 through P10

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	see Notes 1 and 2	2.2 V/3 V		±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1 through P5, P7 through P10

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1.5 mA (see Notes 1)	2.2 V	V_{CC}–0.25	V_{CC}	V
		$I_{(OHmax)}$ = –6 mA (see Notes 2)	2.2 V	V_{CC}–0.6	V_{CC}	
		$I_{(OHmax)}$ = –1.5 mA (see Notes 1)	3 V	V_{CC}–0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA (see Notes 2)	3 V	V_{CC}–0.6	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1.5 mA (see Notes 1)	2.2 V	V_{SS}	V_{SS}+0.25	V
		$I_{(OLmax)}$ = 6 mA (see Notes 2)	2.2 V	V_{SS}	V_{SS}+0.6	
		$I_{(OLmax)}$ = 1.5 mA (see Notes 1)	3 V	V_{SS}	V_{SS}+0.25	
		$I_{(OLmax)}$ = 6 mA (see Notes 2)	3 V	V_{SS}	V_{SS}+0.6	

NOTES: 1. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
2. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

output frequency – Ports P1 through P5, P7 through P10

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.4/TBCLK/SMCLK, C_L = 20 pF, R_L = 1 kΩ against V_{CC}/2 (see Note 1 and 2)	2.2 V		10	MHz
			3 V		12	MHz
f_{Port_CLK}	Clock output frequency	P1.1/TA0/MCLK, P1.5/TACLK/ACLK, P1.4/TBCLK/SMCLK, C_L = 20 pF (see Note 2)	2.2 V		12	MHz
			3 V		16	MHz

NOTES: 1. Alternatively a resistive divider with 2 times 2 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
2. The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – outputs

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

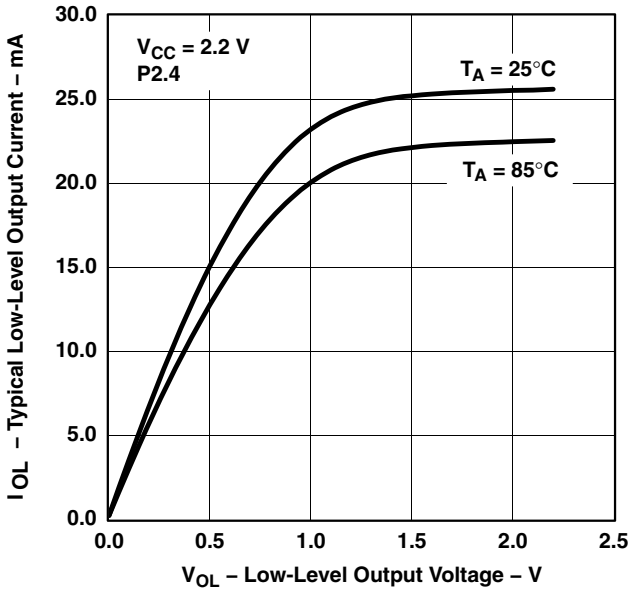


Figure 4

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

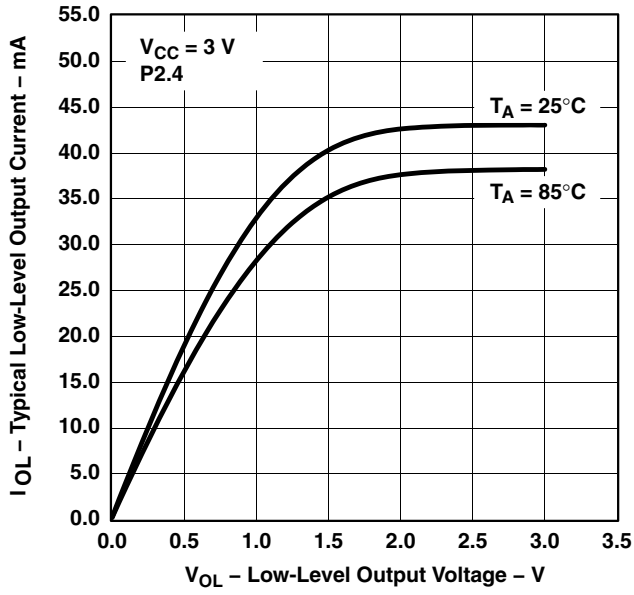


Figure 5

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

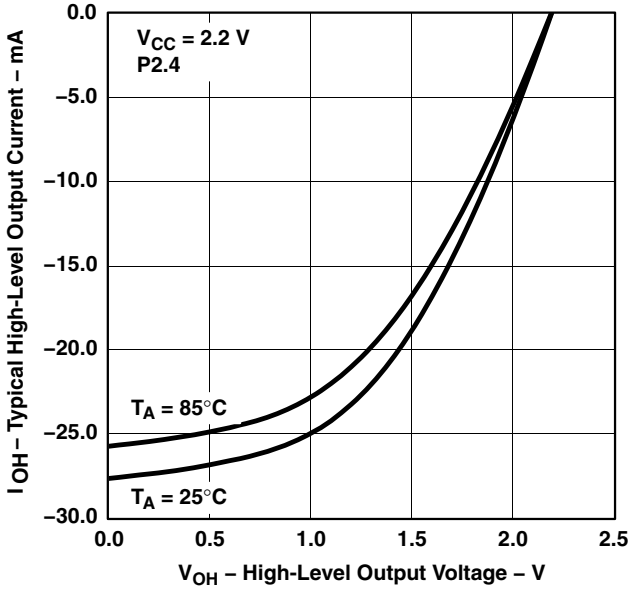


Figure 6

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

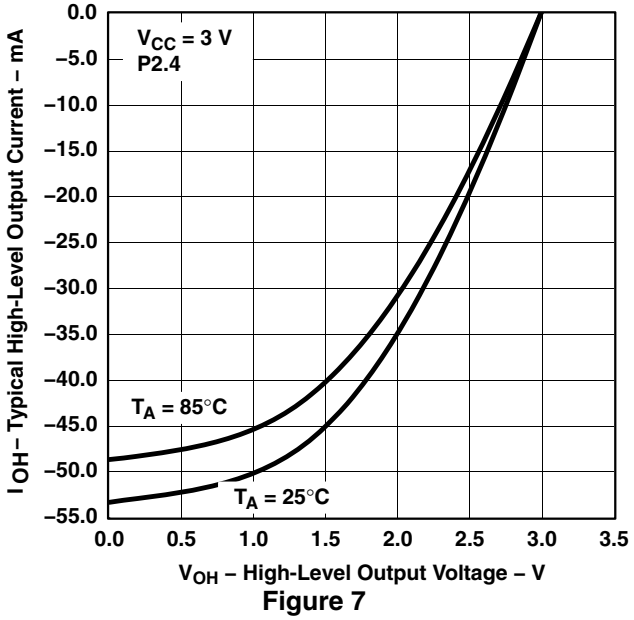


Figure 7

NOTE: One output loaded at a time.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	(see Figure 8)	$dV_{CC}/dt \le 3$ V/s			$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	(see Figure 8 through Figure 10)	$dV_{CC}/dt \le 3$ V/s				1.71	V
$V_{hys(B\_IT-)}$	(see Figure 8)	$dV_{CC}/dt \le 3$ V/s		70	130	180	mV
$t_{d(BOR)}$	(see Figure 8)					2000	µs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally		2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8V.

2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide (SLAU056)* for more information on the brownout/SVS circuit.

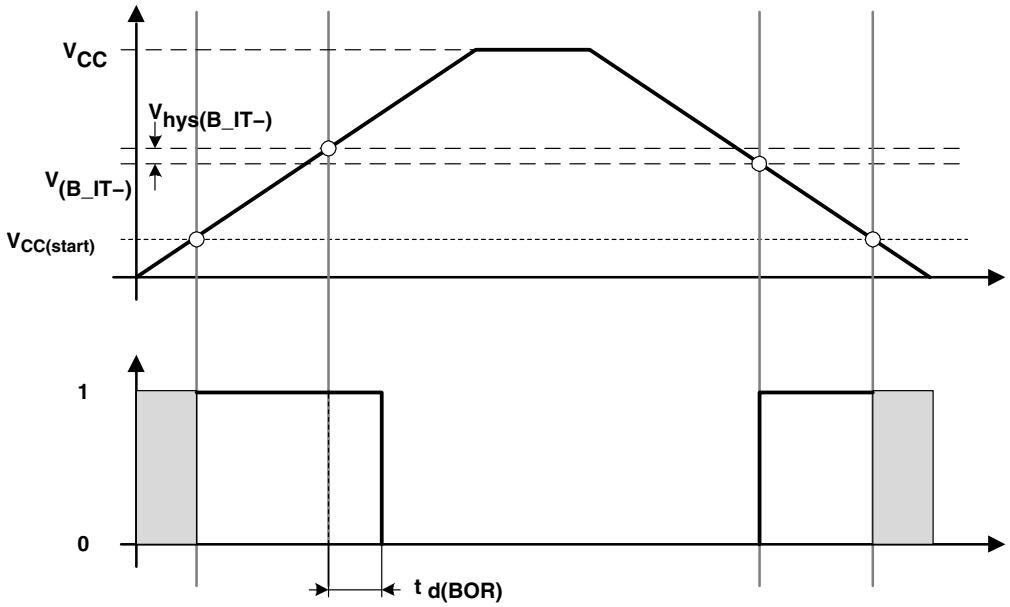


Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – POR/brownout reset (BOR)

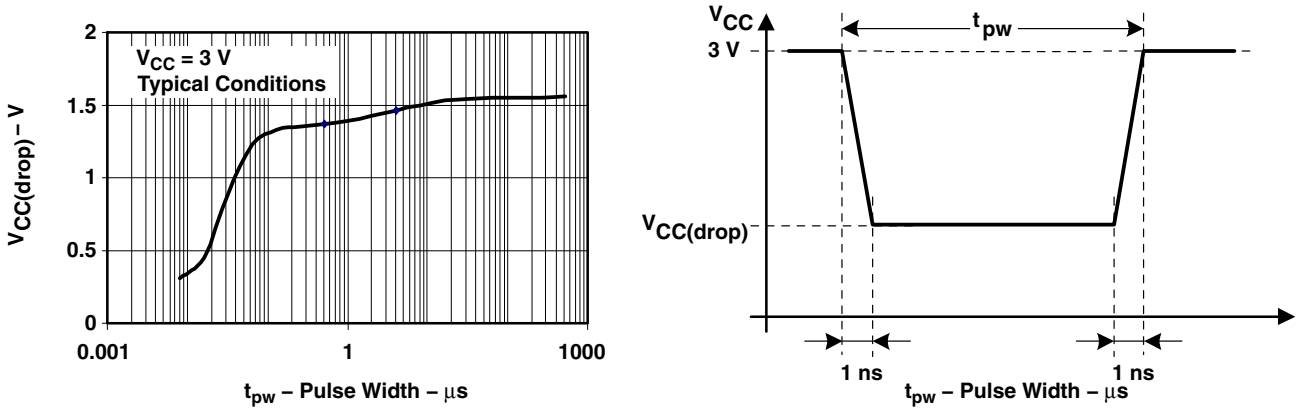


Figure 9. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

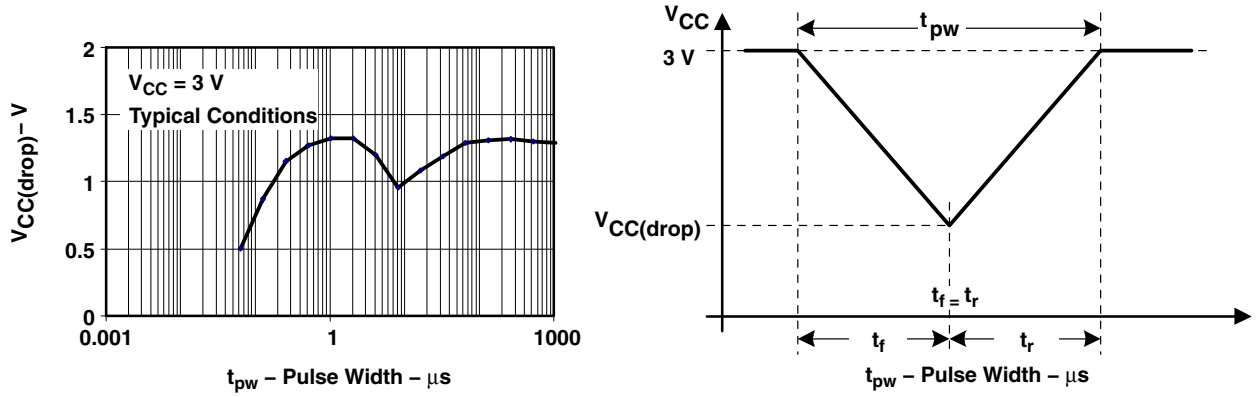


Figure 10. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

SVS (supply voltage supervisor/monitor) (see Note 1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	$dV_{CC}/dt > 30$ V/ms (see Figure 11)		5		150	µs
	$dV_{CC}/dt \le 30$ V/ms				2000	
$t_{d(SVSon)}$	SVSon, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V			150	300	µs
t_{settle}	VLD ≠ 0 (see Note 2)				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \le 3$ V/s (see Figure 11)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 11)	VLD = 1	70	120	155	mV
		VLD = 2 .. 14	$V_{(SVS\_IT-)}$ x 0.001		$V_{(SVS\_IT-)}$ x 0.016	
	$V_{CC}/dt \le 3$ V/s (see Figure 11), external voltage applied on A7	VLD = 15	4.4		10.4	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 11)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61†	
		VLD = 13	3.24	3.5	3.76†	
		VLD = 14	3.43	3.7†	3.99†	
	$V_{CC}/dt \le 3$ V/s (see Figure 11), external voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (see Note 1)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	µA

† The recommended operating voltage range is limited to 3.6 V.

NOTES: 1. The current consumption of the SVS module is not included in the I_{CC} current consumption data.

2. t_{settle} is the settling time that the comparator output needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.

typical characteristics

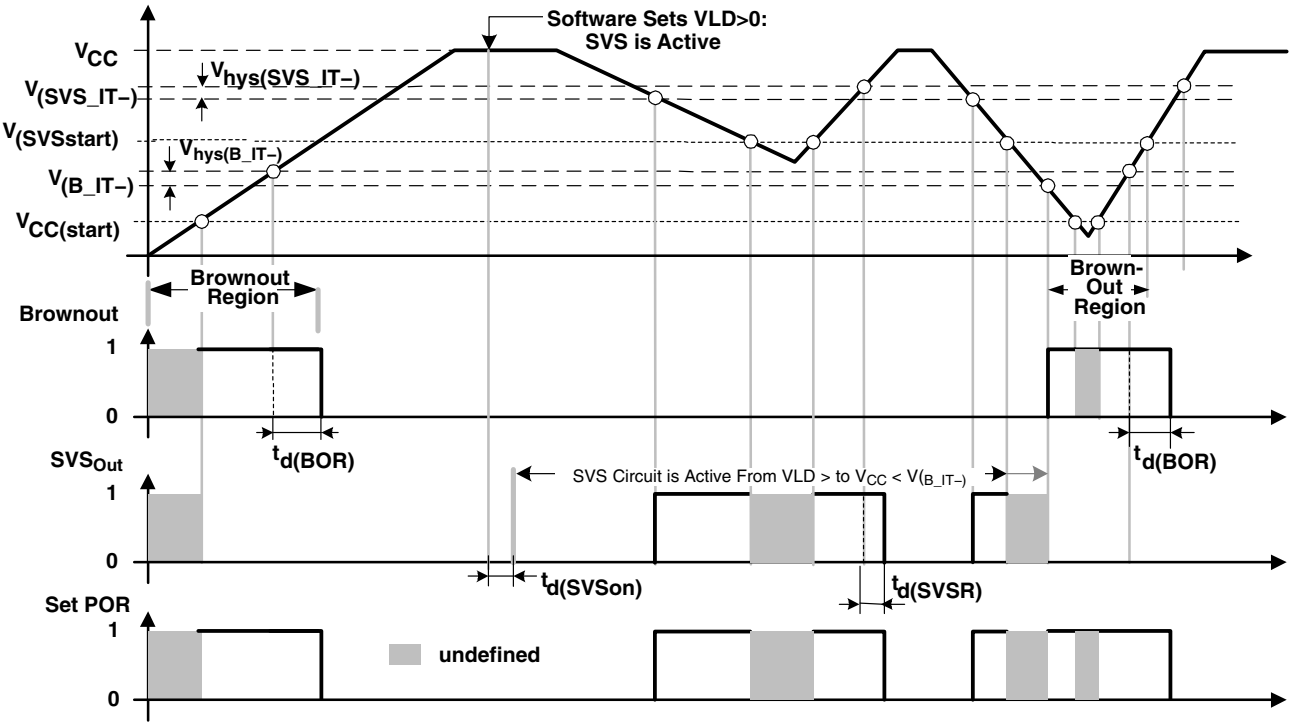


Figure 11. SVS Reset (SVSR) vs Supply Voltage

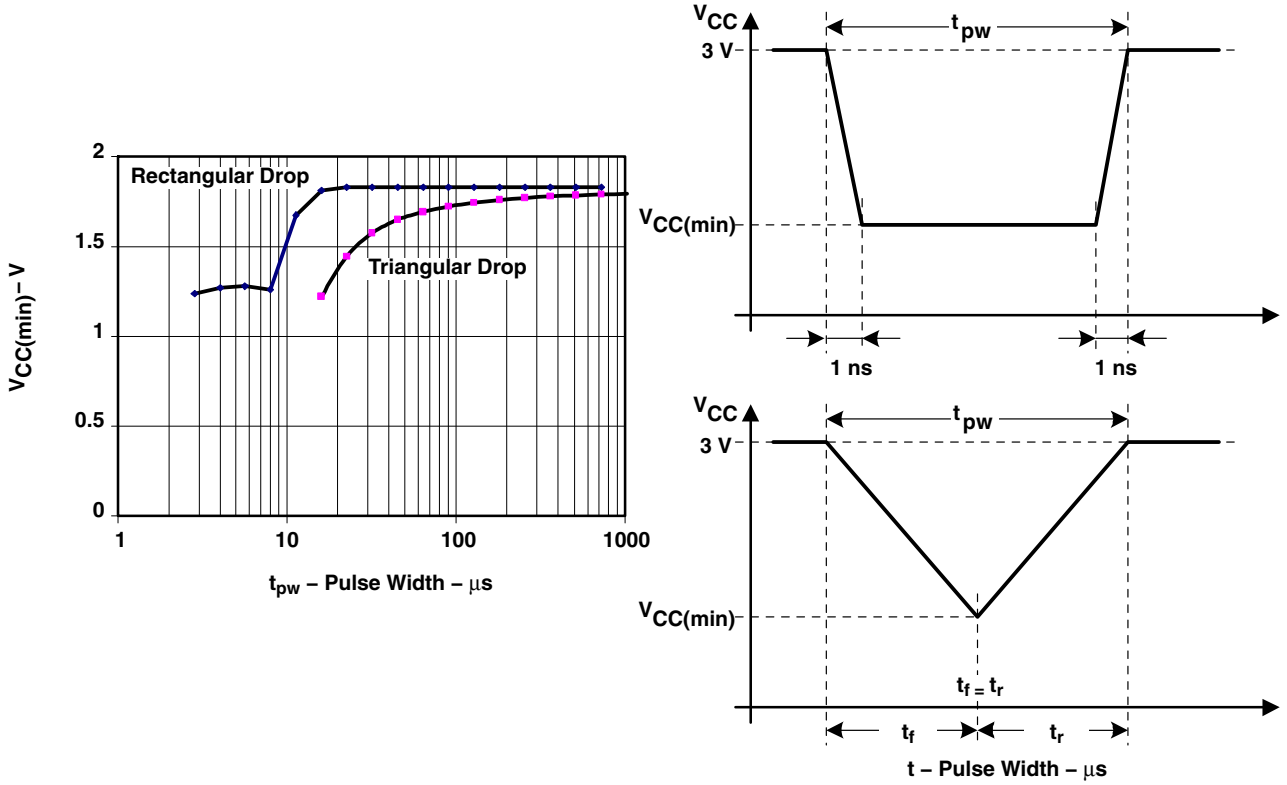


Figure 12. $V_{CC(min)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

DCO

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0		2.2 V/3 V		1		MHz
$f_{(DCO = 2)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1		2.2 V	0.3	0.65	1.25	MHz
			3 V	0.3	0.7	1.3	
$f_{(DCO = 27)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1		2.2 V	2.5	5.6	10.5	MHz
			3 V	2.7	6.1	11.3	
$f_{(DCO = 2)}$	FN_8 = FN_4 = FN_3 = 0, FN_2 = 1, DCOPLUS = 1		2.2 V	0.7	1.3	2.3	MHz
			3 V	0.8	1.5	2.5	
$f_{(DCO = 27)}$	FN_8 = FN_4 = FN_3 = 0, FN_2 = 1, DOPLUS = 1		2.2 V	5.7	10.8	18	MHz
			3 V	6.5	12.1	20	
$f_{(DCO = 2)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1		2.2 V	1.2	2	3	MHz
			3 V	1.3	2.2	3.5	
$f_{(DCO = 27)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1		2.2 V	9	15.5	25	MHz
			3 V	10.3	17.9	28.5	
$f_{(DCO = 2)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1		2.2 V	1.8	2.8	4.2	MHz
			3 V	2.1	3.4	5.2	
$f_{(DCO = 27)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1		2.2 V	13.5	21.5	33	MHz
			3 V	16	26.6	41	
$f_{(DCO = 2)}$	FN_8 = 1, FN_4 = FN_3 = FN_2 = x, DCOPLUS = 1		2.2 V	2.8	4.2	6.2	MHz
			3 V	4.2	6.3	9.2	
$f_{(DCO = 27)}$	FN_8 = 1, FN_4 = FN_3 = FN_2 = x, DCOPLUS = 1		2.2 V	21	32	46	MHz
			3 V	30	46	70	
S_n	Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$ (see Figure 14 for taps 21 to 27)	1 < TAP ≤ 20		1.06		1.11	
		TAP = 27		1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0		2.2 V	–0.2	–0.3	–0.4	%/°C
			3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0		2.2 V/3 V	0	5	15	%/V

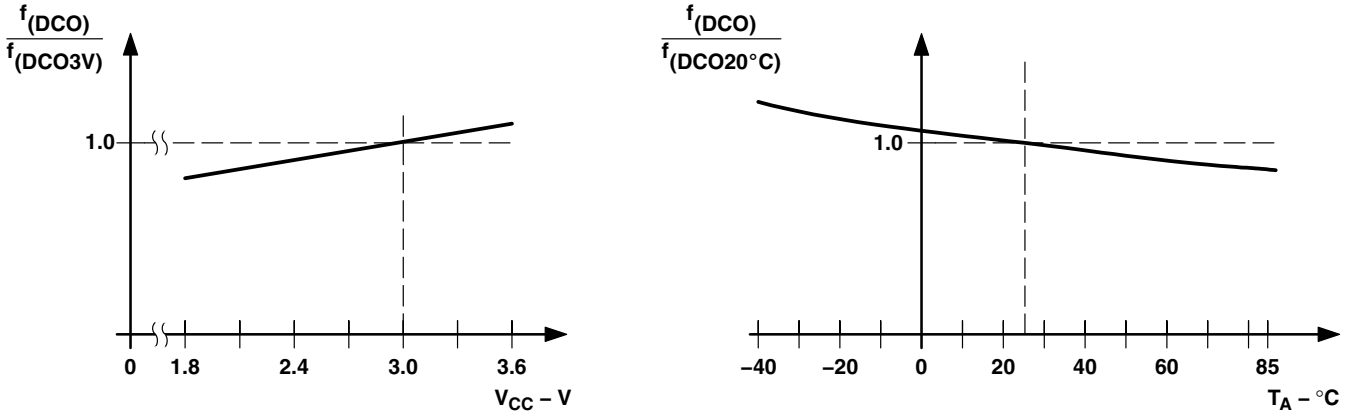


Figure 13. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

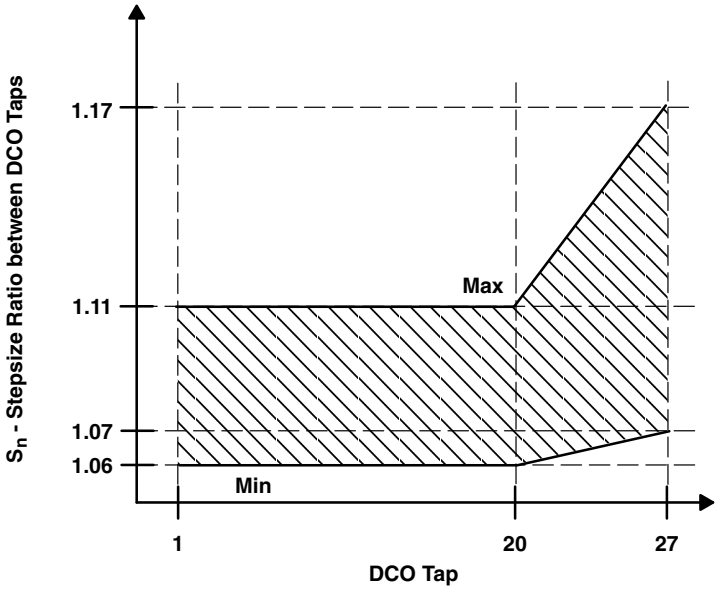


Figure 14. DCO Tap Step Size

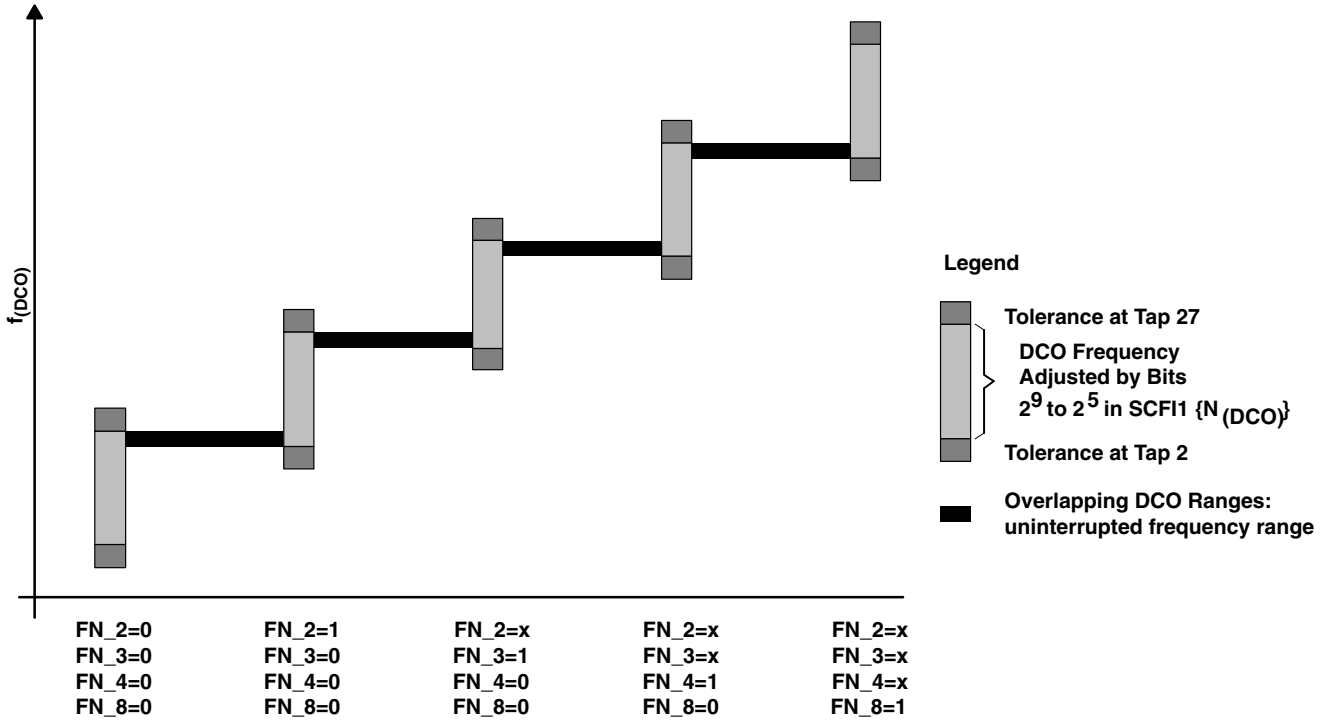


Figure 15. Five Overlapping DCO Ranges Controlled by FN_x Bits

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, low-frequency modes (see Note 4)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1, LF}$	LFXT1 oscillator crystal frequency, LF mode	XTS_FLL = 0, LFXT1DIG = 0	1.8 V–3.6 V		32, 768		Hz
$f_{LFXT1, LF, logic}$	LFXT1 oscillator logic level square-wave input frequency, LF mode	XTS_FLL = 0, LFXT1DIG = 1, XCAPx = 0	1.8 V–3.6 V	10, 000	32, 768		Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS_FLL = 0, LFXT1DIG = 0, $f_{LFXT1, LF}$ = 32,768 kHz, $C_{L, eff}$ = 6 pF			500		kΩ
		XTS_FLL = 0, LFXT1DIG = 0, $f_{LFXT1, LF}$ = 32,768 kHz, $C_{L, eff}$ = 12 pF			200		
$C_{L, eff}$	Integrated effective load capacitance, LF mode (see Note 1)	XTS_FLL = 0, XCAPx = 0			1		pF
		XTS_FLL = 0, XCAPx = 1			5.5		
		XTS_FLL = 0, XCAPx = 2			8.5		
		XTS_FLL = 0, XCAPx = 3			11		
Duty Cycle	LF mode	XTS_FLL = 0, Measured at P1.4/ACLK, $f_{LFXT1, LF}$ = 32, 768 Hz	2.2 V/3 V	30	50	70	%
$f_{Fault, LF}$	Oscillator fault frequency, LF mode (see Note 3)	XTS_FLL = 0 (see Note 2)	2.2 V/3 V	10		10, 000	Hz

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Measured with logic level input frequency but also applies to operation with crystals.
3. Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
4. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   – Keep as short of a trace as possible between the device and the crystal.
   – Design a good ground plane around the oscillator pins.
   – Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   – Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   – Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   – If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   – Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

crystal oscillator, LFXT1, high-frequency mode

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{XT1}	XT1 oscillator crystal frequency	XTS_FLL = 1, Ceramic resonator	1.8 V–3.6 V	0.45		4	MHz
			2.7 V–3.6 V	0.45		8	
f_{XT1}	XT1 oscillator crystal frequency	XTS_FLL = 1, Crystal	1.8 V–3.6 V	1		4	MHz
			2.7 V–3.6 V	1		8	
$C_{L, eff}$	Integrated effective Load Capacitance (see Note 1)	XTS_FLL = 1, XCAPx = 0 (see Note 2)			1		pF
Duty Cycle		Measured at P1.4/ACLK	2.2 V/3 V	40	50	60	%

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, XT2 oscillator (see Note 5)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{XT2, 0}$	XT2 oscillator crystal frequency, mode 0	XT2Sx = 0	1.8 V – 3.6 V	0.4		1	MHz
$f_{XT2, 1}$	XT2 oscillator crystal frequency, mode 1	XT2Sx = 1	1.8 V – 3.6 V	1		4	MHz
$f_{XT2, 2}$	XT2 oscillator crystal frequency, mode 2	XT2Sx = 2	1.8 V – 3.6 V	2		10	MHz
			2.2 V – 3.6 V	2		12	
			3.0 V – 3.6 V	2		16	
$f_{XT2, logic}$	XT2 oscillator logic level square-wave input frequency	XT2Sx = 3	1.8 V – 3.6 V	0.4		10	MHz
			2.2 V – 3.6 V	0.4		12	
			3.0 V – 3.6 V	0.4		16	
OA_{XT2}	Oscillation allowance for HF crystals (see Figure 16)	XT2Sx = 0, f_{XT2} = 1 MHz, $C_{L, eff}$ = 15 pF			2700		Ω
		XT2Sx = 1, $f_{LFXT1, HF}$ = 4 MHz, $C_{L, eff}$ = 15 pF			800		
		XT2Sx = 2, $f_{LFXT1, HF}$ = 16 MHz, $C_{L, eff}$ = 15 pF			300		
$C_{L, eff}$	Integrated effective load capacitance (see Note 1)	(see Note 2)			1		pF
Duty cycle		Measured at P1.4/ACLK, f_{XT2} = 10 MHz	2.2 V/3 V	40	50	60	%
		Measured at P1.4/ACLK, f_{XT2} = 16 MHz	3 V	40	50	60	
$f_{Fault, XT2}$	Oscillator fault frequency (see Note 4)	XT2Sx = 3 (see Note 3)	2.2 V/3 V	30		300	kHz

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
3. Measured with logic level input frequency but also applies to operation with crystals.
4. Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
5. To improve EMI on the XT2 oscillator the following guidelines should be observed.
   - Keep traces as short as possible between the device and the crystal.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – XT2 oscillator

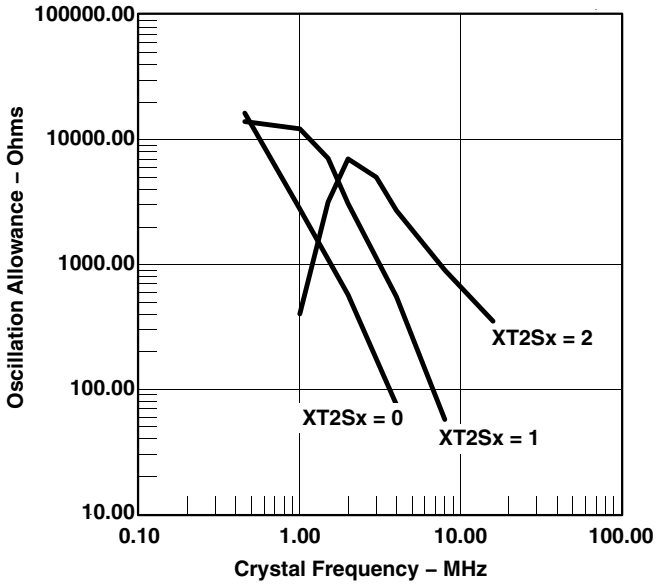


Figure 16. Oscillation Allowance vs Crystal Frequency, $C_{L, eff}$ = 15 pF, T_A = 25°C

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

wake-up LPM3

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V/3 V			6	µs
		f = 2 MHz				6	
		f = 3 MHz				6	

LCD_A

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(LCD)}$	Supply voltage range	Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)		2.2		3.6	V
C_{LCD}	Capacitor on LCDCAP (see Note 1)	Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)		4.7			µF
$I_{CC(LCD)}$	Supply current	$V_{LCD(typ)}$ = 3V, LCDCPEN = 1, VLCDx = 1000, All segments on, f_{LCD} = f_{ACLK}/32, No LCD connected (see Note 2), T_A = 25°C	2.2 V		3.8		µA
f_{LCD}	LCD frequency					1.1	kHz
V_{LCD}	LCD voltage	VLCDx = 0000			V_{CC}		V
		VLCDx = 0001			2.60		
		VLCDx = 0010			2.66		
		VLCDx = 0011			2.72		
		VLCDx = 0100			2.78		
		VLCDx = 0101			2.84		
		VLCDx = 0110			2.90		
		VLCDx = 0111			2.96		
		VLCDx = 1000			3.02		
		VLCDx = 1001			3.08		
		VLCDx = 1010			3.14		
		VLCDx = 1011			3.20		
		VLCDx = 1100			3.26		
		VLCDx = 1101			3.32		
		VLCDx = 1110			3.38		
		VLCDx = 1111			3.44	3.60	
R_{LCD}	LCD driver output impedance	V_{LCD} = 3V, LCDCPEN = 1, VLCDx = 1000, I_{LOAD} = ±10µA	2.2 V			10	kΩ

NOTES: 1. Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.
2. Connecting an actual display will increase the current consumption depending on the size of the LCD.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Comparator_A (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(CC)}$		CAON = 1, CARSEL = 0, CAREF = 0	2.2 V		25	40	µA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P1.6/CA0 and P1.7/CA1	2.2 V		30	50	µA
			3 V		45	80	
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P1.6/CA0 and P1.7/CA1	2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5 } V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P1.6/CA0 and P1.7/CA1	2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	See Figure 17 and Figure 18	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P1.6/CA0 and P1.7/CA1, $T_{A\ =}$ 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
V_{IC}	Common-mode input voltage range	CAON = 1	2.2 V/3 V	0		V_{CC}–1	V
V_p–V_S	Offset voltage	See Note 2	2.2 V/3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON = 1	2.2 V/3 V	0	0.7	1.4	mV
$t_{(response\ LH\ and\ HL)}$, see Note 3		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	2.2 V	80	165	300	ns
			3 V	70	120	240	
		T_A = 25°C Overdrive 10 mV, with filter: CAF = 1	2.2 V	1.4	1.9	2.8	µs
			3 V	0.9	1.5	2.2	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.
3. The response time is measured at P1.6/CA0 with an input voltage step and the Comparator_A already enabled (CAON = 1). If CAON is set at the same time, a settling time of up to 300 ns is added to the response time.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

typical characteristics

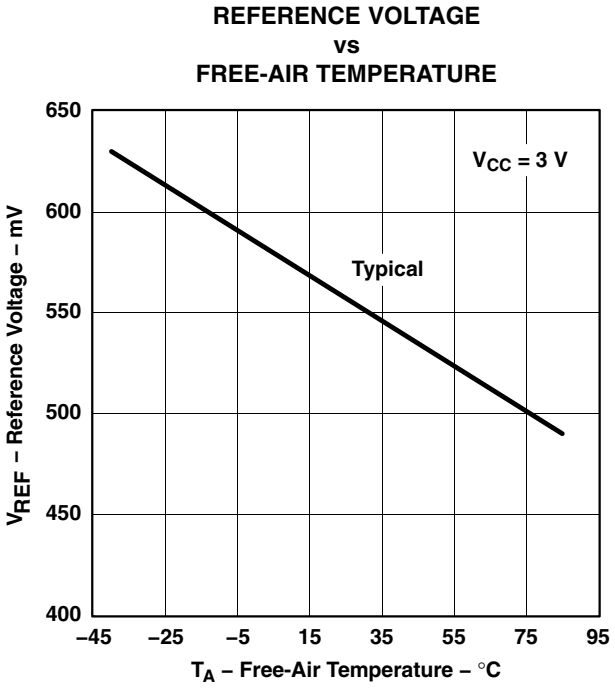


Figure 17. $V_{(RefVT)}$ vs Temperature

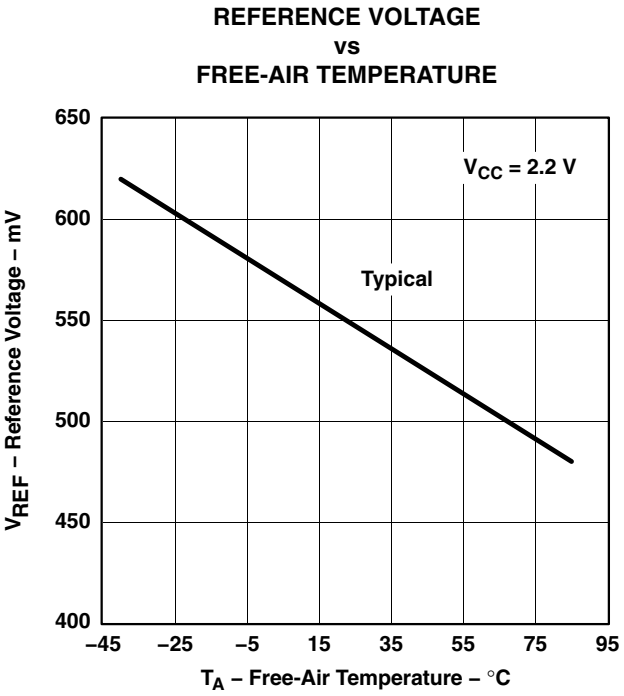


Figure 18. $V_{(RefVT)}$ vs Temperature

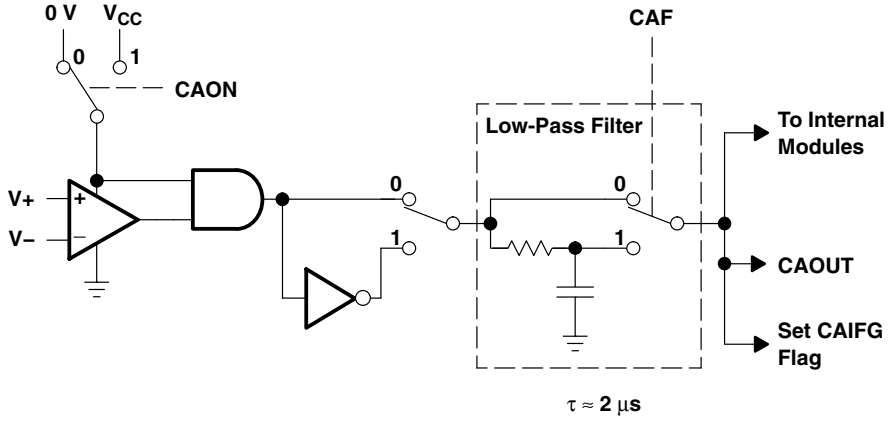


Figure 19. Block Diagram of Comparator_A Module

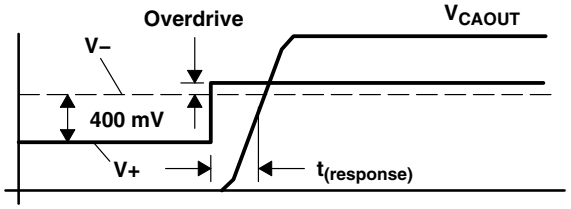


Figure 20. Overdrive Definition

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Timer_A

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK, External: TACLK, INCLK, Duty Cycle = 50% ±10%	2.2 V		10	MHz
			3 V		16	
$t_{TA, cap}$	Timer_A, capture timing	TA0, TA1, TA2	2.2 V/3 V	20		ns

Timer_B

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TB}	Timer_B clock frequency	Internal: SMCLK, ACLK, External: TBCLK, Duty Cycle = 50% ±10%	2.2 V		10	MHz
			3 V		16	
$t_{TB, cap}$	Timer_B, capture timing	TB0, TB1, TB2	2.2 V/3 V	20		ns

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (UART mode)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty Cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals Baudrate in MBaud)		2.2V /3 V			1	MHz
t_τ	UART receive deglitch time (see Note 1)		2.2 V	50	150	600	ns
			3 V	50	100	600	ns

NOTES: 1. Pulses on the UART receive input (UCxRX) shorter than the UART receive deglich time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

USCI (SPI master mode) (see Figure 21 and Figure 22)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty Cycle = 50% ± 10%			f_{SYSTEM}	MHz
$t_{SU, MI}$	SOMI input data setup time		2.2 V	110		ns
			3 V	75		ns
$t_{HD, MI}$	SOMI input data hold time		2.2 V	0		ns
			3 V	0		ns
$t_{VALID, MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V		30	ns
			3 V		20	ns

NOTE: $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.

For the slave's parameters $t_{SU, SI(Slave)}$ and $t_{VALID, SO(Slave)}$ see the SPI parameters of the attached slave.

USCI (SPI slave mode) (see Figure 23 and Figure 24)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE, LEAD}$	STE lead time STE low to clock		2.2 V/3 V		50		ns
$t_{STE, LAG}$	STE lag time Last clock to STE high		2.2 V/3 V	10			ns
$t_{STE, ACC}$	STE access time STE low to SOMI data out		2.2 V/3 V		50		ns
$t_{STE, DIS}$	STE disable time STE high to SOMI high impedance		2.2 V/3 V		50		ns
$t_{SU, SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			ns
$t_{HD, SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			ns
$t_{VALID, SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	ns

NOTE: $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.

For the master's parameters $t_{SU, MI(Master)}$ and $t_{VALID, MO(Master)}$ see the SPI parameters of the attached master.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

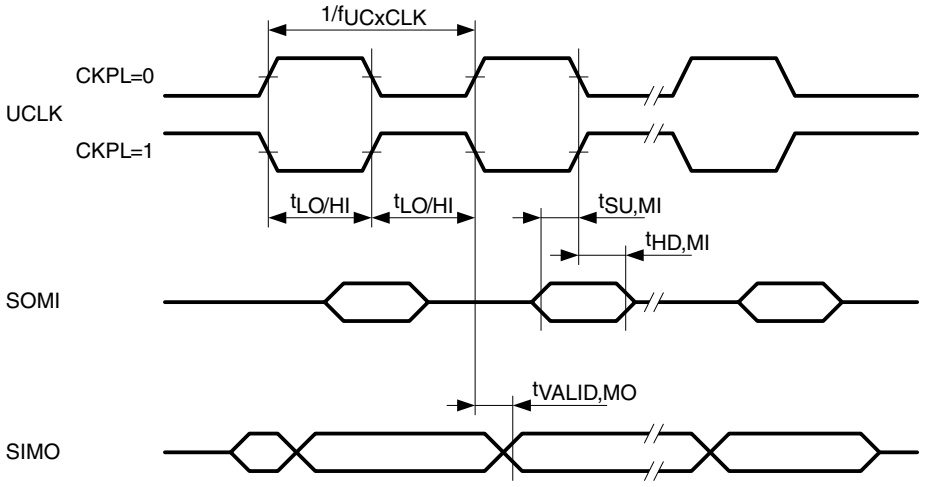


Figure 21. SPI Master Mode, CKPH = 0

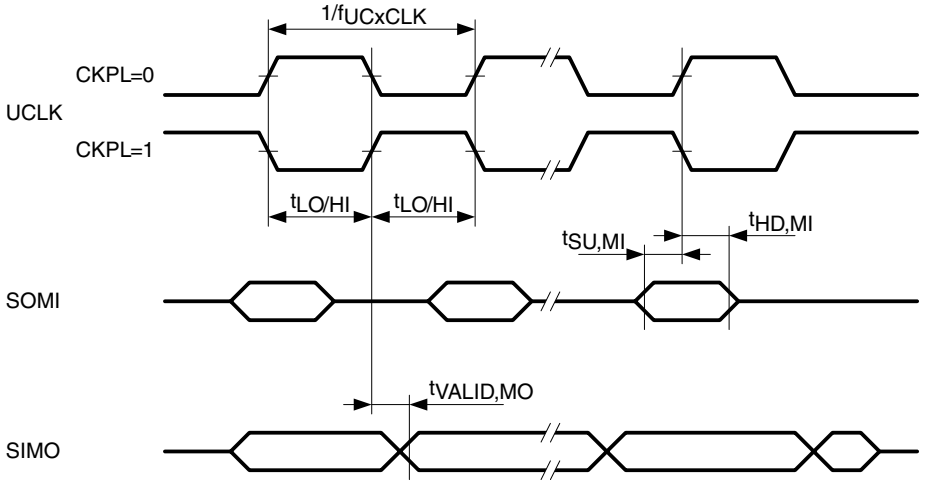


Figure 22. SPI Master Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

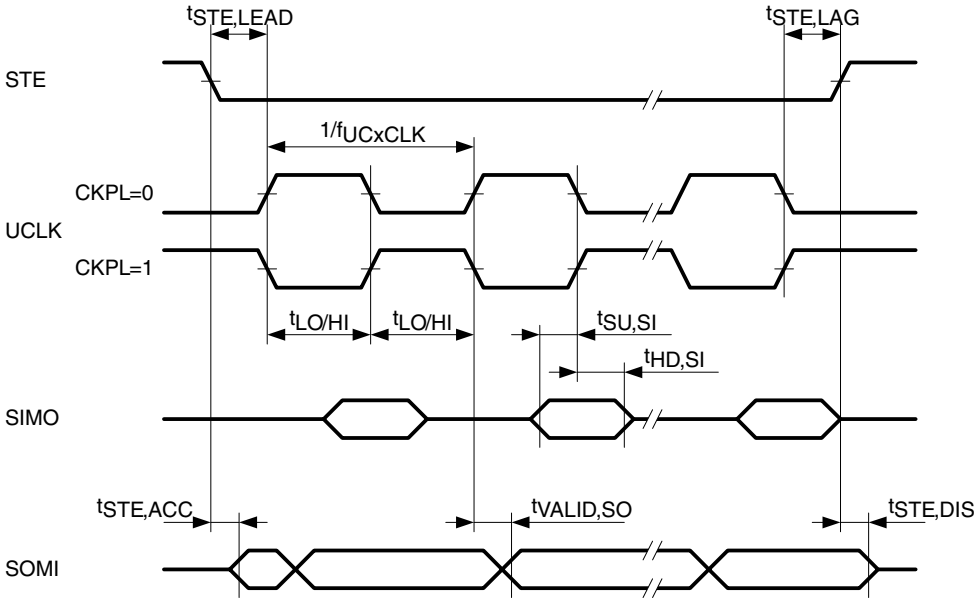


Figure 23. SPI Slave Mode, CKPH = 0

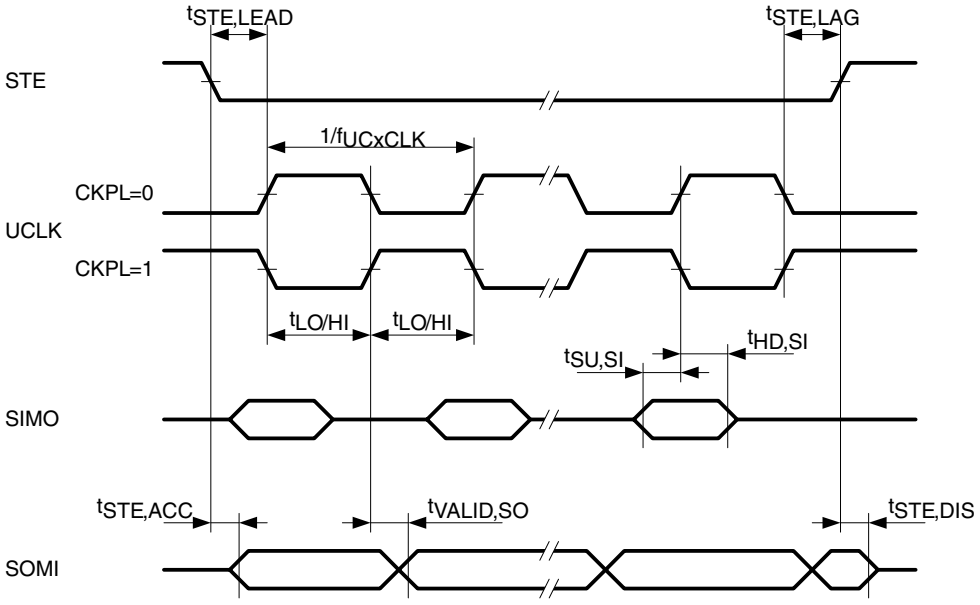


Figure 24. SPI Slave Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (I2C mode) (see Figure 25)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V/3 V	0		400	kHz
$t_{HD, STA}$	Hold time (repeated) START	$f_{SCL} \le 100$ kHz	2.2 V/3 V	4.0			us
		$f_{SCL} > 100$ kHz	2.2 V/3 V	0.6			
$t_{SU, STA}$	Setup time for a repeated START	$f_{SCL} \le 100$ kHz	2.2 V/3 V	4.7			us
		$f_{SCL} > 100$ kHz	2.2 V/3 V	0.6			
$t_{HD, DAT}$	Data hold time		2.2 V/3 V	0			ns
$t_{SU, DAT}$	Data setup time		2.2 V/3 V	250			ns
$t_{SU, STO}$	Setup time for STOP		2.2 V/3 V	4.0			us
t_{SP}	Pulse width of spikes suppressed by input filter		2.2 V	50	150	600	ns
			3 V	50	100	600	

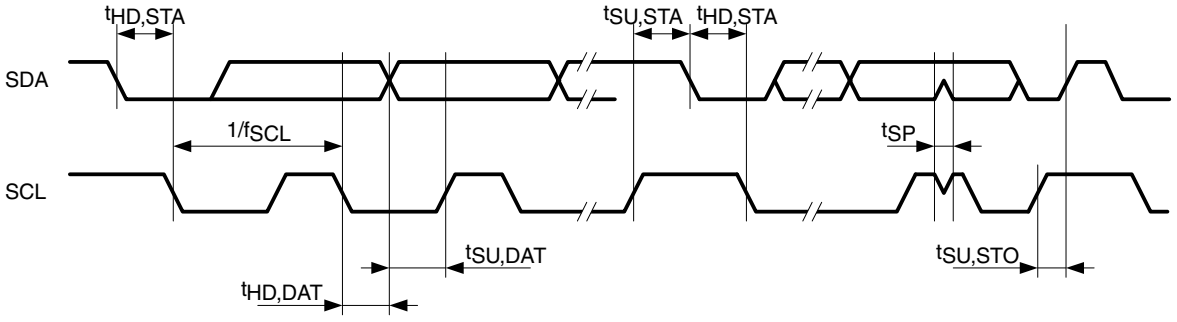


Figure 25. I2C Mode Timing

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SD16_A, power supply and recommended operating conditions

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$ $AV_{SS} = DV_{SS} = 0V$			2.5		3.6	V
I_{SD16}	Analog supply current: 1 active SD16_A channel including internal reference	SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	GAIN: 1, 2	3 V		730	1050	µA
			GAIN: 4, 8, 16	3 V		810	1150	
			GAIN: 32	3 V		1160	1700	
		SD16LP = 1, f_{SD16} = 0.5 MHz, SD16OSR = 256	GAIN: 1	3 V		720	1030	
			GAIN: 32	3 V		810	1150	
f_{SD16}	Analog front-end input clock frequency	SD16LP = 0 (Low power mode disabled)		3 V	0.03	1	1.1	MHz
		SD16LP = 1 (Low power mode enabled)		3 V	0.03	0.5		

SD16_A, input range (see Note 1)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{ID, FSR}$	Differential full scale input voltage range	Bipolar mode, SD16UNI = 0			$-V_{REF}/2GAIN$		$+V_{REF}/2GAIN$	mV
		Unipolar mode, SD16UNI = 1			0		$+V_{REF}/2GAIN$	
V_{ID}	Differential input voltage range for specified performance (see Note 2)	SD16REFON = 1	SD16GAINx = 1			±500		mV
			SD16GAINx = 2			±250		
			SD16GAINx = 4			±125		
			SD16GAINx = 8			±62		
			SD16GAINx = 16			±31		
			SD16GAINx = 32			±15		
Z_I	Input impedance (one input pin to AV_{SS})	f_{SD16} = 1 MHz	SD16GAINx = 1	3 V		200		kΩ
			SD16GAINx = 32	3 V		75		
Z_{ID}	Differential input impedance (IN+ to IN–)	f_{SD16} = 1 MHz	SD16GAINx = 1	3 V	300	400		kΩ
			SD16GAINx = 32	3 V	100	150		
V_I	Absolute input voltage range				AV_{SS} -1V		AV_{CC}	V
V_{IC}	Common-mode input voltage range				AV_{SS} -1V		AV_{CC}	V

NOTES: 1. All parameters pertain to each SD16_A channel.
2. The analog input range depends on the reference voltage applied to V_{REF}. If V_{REF} is sourced externally, the full-scale range is defined by $V_{FSR+} = +(V_{REF}/2)/GAIN$ and $V_{FSR-} = -(V_{REF}/2)/GAIN$. The analog input range should not exceed 80% of V_{FSR+} or V_{FSR-}.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SD16_A, performance (f_{SD16} = 1MHz, SD16OSRx = 256, SD16REFON = 1)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD16GAINx = 1, Signal Amplitude V_{PP} = 500 mV	f_{IN} = 50 Hz, 100 Hz (see Notes 1 and 2)	3 V	83	85		dB
		SD16GAINx = 2, Signal Amplitude V_{PP} = 250 mV		3 V	81	84		
		SD16GAINx = 4, Signal Amplitude V_{PP} = 125 mV		3 V	76	79		
		SD16GAINx = 8, Signal Amplitude V_{PP} = 62 mV		3 V	70	75		
		SD16GAINx = 16, Signal Amplitude V_{PP} = 31 mV		3 V	66	70		
		SD16GAINx = 32, Signal Amplitude V_{PP} = 15 mV		3 V	62	65		
G	Nominal gain	SD16GAINx = 1		3 V	0.97	1.00	1.02	
		SD16GAINx = 2		3 V	1.90	1.96	2.02	
		SD16GAINx = 4		3 V	3.76	3.86	3.96	
		SD16GAINx = 8		3 V	7.36	7.62	7.84	
		SD16GAINx = 16		3 V	14.56	15.04	15.52	
		SD16GAINx = 32		3 V	27.20	28.35	29.76	
E_{OS}	Offset error	SD16GAINx = 1		3 V			±0.2	%FSR
		SD16GAINx = 32		3 V			±1.5	
dE_{OS}/dT	Offset error temperature coefficient	SD16GAINx = 1		3 V		±4	±20	ppm FSR/°C
		SD16GAINx = 32		3 V		±20	±100	
CMRR	Common-mode rejection ratio	SD16GAINx = 1, Common-mode input signal: V_{ID} = 500 mV, f_{IN} = 50 Hz, 100 Hz		3 V		>90		dB
		SD16GAINx = 32, Common-mode input signal: V_{ID} = 16 mV, f_{IN} = 50 Hz, 100 Hz		3 V		>75		
AC PSRR	AC power supply rejection ratio	SD16GAINx = 1, V_{CC} = 3V ± 100mV, f_{Vcc} = 50 Hz		3 V		>80		dB
X_T	Crosstalk	SD16GAINx = 1, V_{ID} = 500 mV, f_{IN} = 50 Hz, 100 Hz		3 V		<–100		dB

NOTES: 1. The following voltages were applied to the SD16 inputs:
$V_{IN, A+}(t) = 1.2V + V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
$V_{IN, A-}(t) = 1.2V - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{diff} = V_{IN, A+}(t) - V_{IN, A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$

2. The SINAD performance of the SD16_A maybe degraded. See errata sheet.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – SD16_A SNR/SINAD performance over OSR

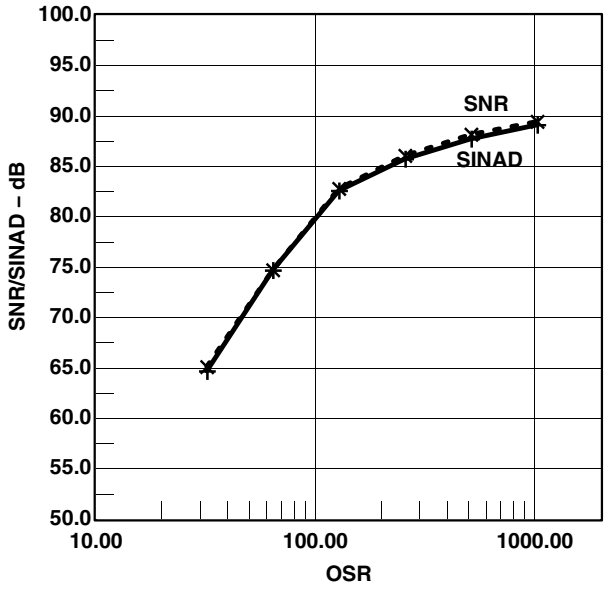


Figure 26. SNR/SINAD performance over OSR, f_{SD16} = 1MHz, SD16REFON = 1, SD16GAINx = 1
$V_{IN}(t) = 1.2V + 500mV \times \sin(2\pi \times 50Hz \times t)$

SD16_A, temperature sensor and built-in V_{CC} sense

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
TC_{Sensor}	Sensor temperature coefficient			1.18	1.32	1.46	mV/K
$V_{Offset, sensor}$	Sensor offset voltage			–100		100	mV
V_{Sensor}	Sensor output voltage (see Note 2)	Temperature sensor voltage at T_A = 85°C	3 V	435	475	515	mV
		Temperature sensor voltage at T_A = 25°C	3 V	355	395	435	
		Temperature sensor voltage at T_A = 0°C	3 V	320	360	400	
$V_{CC, Sense}$	V_{CC} divider at input 5	f_{SD16} = 32kHz, SD16OSRx = 256, SD16REFON = 1		0.08	1/11	0.10	V_{CC}
$R_{Source, VCC}$	Source resistance of V_{CC} divider at input 5				500		kΩ

NOTES: 1. The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor, typ} = TC_{Sensor} (273 + T [°C]) + V_{Offset, sensor}$ [mV]
2. Results based on characterization and/or production test, not TC_{Sensor} or $V_{Offset, sensor}$.
Measured with f_{SD16} = 1MHz, SD16OSRx = 256, SD16REFON = 1.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SD16_A, built-in voltage reference

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference voltage	SD16REFON = 1, SD16VMIDON = 0	3 V	1.14	1.20	1.26	V
I_{REF}	Reference supply current	SD16REFON = 1, SD16VMIDON = 0	3 V		175	260	µA
TC	Temperature coefficient	SD16REFON = 1, SD16VMIDON = 0 (see Note 1)	3 V		18	50	ppm/K
C_{REF}	V_{REF} load capacitance	SD16REFON = 1, SD16VMIDON = 0 (see Note 2)			100		nF
I_{LOAD}	$V_{REF(I)}$ maximum load current	SD16REFON = 1, SD16VMIDON = 0	3 V			±200	nA
t_{ON}	Turn on time	SD16REFON = 0–>1, SD16VMIDON = 0, C_{REF} = 100nF	3 V		5		ms
DC PSR	DC Power Supply Rejection $\Delta V_{REF}/\Delta V_{CC}$	SD16REFON = 1, SD16VMIDON = 0, V_{CC} = 2.5V - 3.6V			100		uV/V

NOTES: 1. Calculated using the box method: (MAX(-40...85°C) – MIN(-40...85°C)) / MIN(–40...85°C) / (85°C – (-40°C))
2. There is no capacitance required on V_{REF}. However, a capacitance of at least 100nF is recommended to reduce any reference voltage noise.

SD16_A, reference output buffer

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF, BUF}$	Reference buffer output voltage	SD16REFON = 1, SD16VMIDON = 1	3 V		1.2		V
$I_{REF, BUF}$	Reference Supply + Reference output buffer quiescent current	SD16REFON = 1, SD16VMIDON = 1	3 V		385	600	µA
$C_{REF(O)}$	Required load capacitance on V_{REF}	SD16REFON = 1, SD16VMIDON = 1		470			nF
$I_{LOAD, Max}$	Maximum load current on V_{REF}	SD16REFON = 1, SD16VMIDON = 1	3 V			±1	mA
	Maximum voltage variation vs. load current	$\|I_{LOAD}\|$ = 0 to 1mA	3 V	–15		+15	mV
t_{ON}	Turn on time	SD16REFON = 0–>1, SD16VMIDON = 0–>1, C_{REF} = 470nF	3 V		100		µs

SD16_A, external reference input

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	SD16REFON = 0	3 V	1.0	1.25	1.5	V
$I_{REF(I)}$	Input current	SD16REFON = 0	3 V			50	nA

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

flash memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.2		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V/3.6 V		3	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V/3.6 V		3	7	mA
t_{CPT}	Cumulative program time (see Note 1)		2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 2			30		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				25		
$t_{Block, 1-63}$	Block program time for each additional byte or word				18		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				10593		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (see Note 1)	CPU halted	1.6			V

NOTE 1: This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
f_{TCK}	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-up resistance on TMS, TCK, TDI/TCLK	see Note 2	2.2 V/ 3 V	20	35	50	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

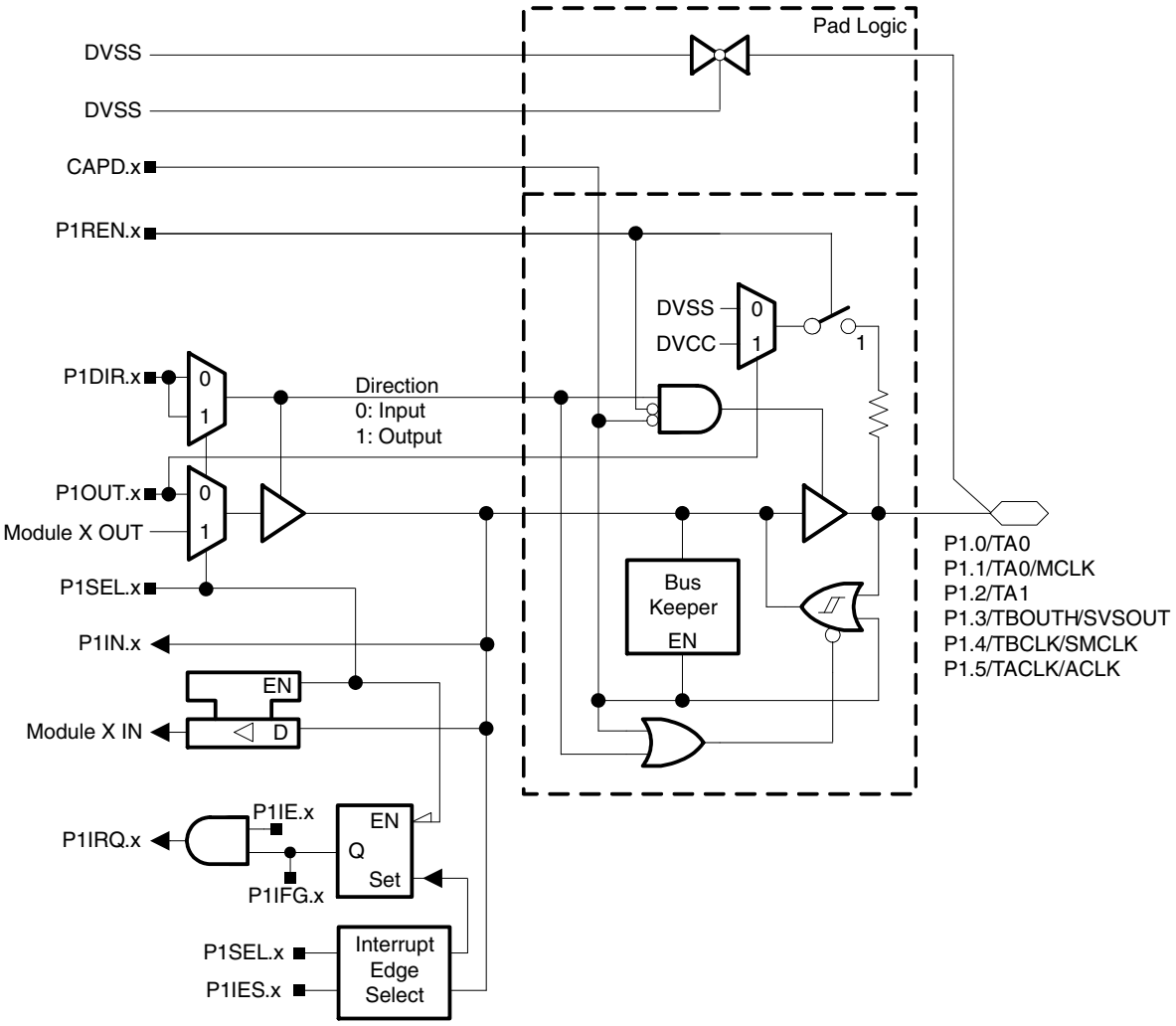
JTAG fuse (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5		V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow: F versions			6	7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow				100	mA
t_{FB}	Time to blow fuse				1	ms

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

APPLICATION INFORMATION

Port P1, P1.0 to P1.5, input/output with Schmitt trigger

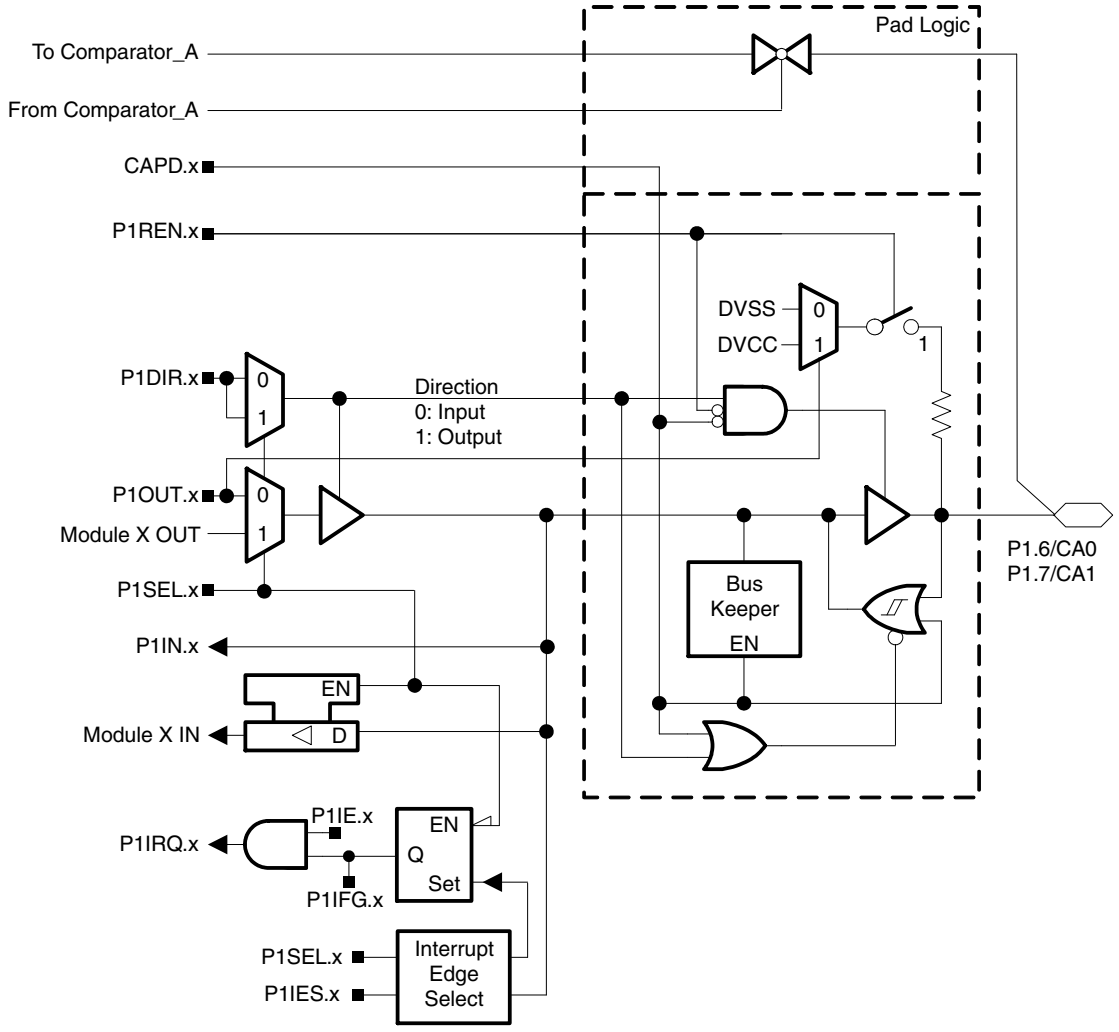


Port P1 (P1.0 to P1.5) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	CAPD.x
P1.0/TA0	0	P1.0 (I/O)	I: 0, O: 1	0	0
		Timer_A3.CCI0A	0	1	0
		Timer_A3.TA0	1	1	0
		Input buffer disabled (see Note 2)	X	X	1
P1.1/TA0/MCLK	1	P1.1 (I/O)	I: 0, O: 1	0	0
		Timer_A3.CCI0B	0	1	0
		MCLK	1	1	0
		Input buffer disabled (see Note 2)	X	X	1
P1.2/TA1	2	P1.2 (I/O)	I: 0, O: 1	0	0
		Timer_A3.CCI1A	0	1	0
		Timer_A3.TA1	1	1	0
		Input buffer disabled (see Note 2)	X	X	1
P1.3/ TBOUTH/SVSOUT	3	P1.3 (I/O)	I: 0, O: 1	0	0
		Timer_B7.TBOUTH	0	1	0
		SVSOUT	1	1	0
		Input buffer disabled (see Note 2)	X	X	1
P1.4/TBCLK/SMCLK	4	P1.4 (I/O)	I: 0, O: 1	0	0
		Timer_B7.TBCLK	0	1	0
		SMCLK	1	1	0
		Input buffer disabled (see Note 2)	X	X	1
P1.5/TACLK/ACLK	5	P1.5 (I/O)	I: 0, O: 1	0	0
		Timer_A3.TACLK	0	1	0
		ACLK	1	1	0
		Input buffer disabled (see Note 2)	X	X	1

NOTES: 1. X: Don't care.
2. Setting the CAPD.x bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P1, P1.6, P1.7, input/output with Schmitt trigger

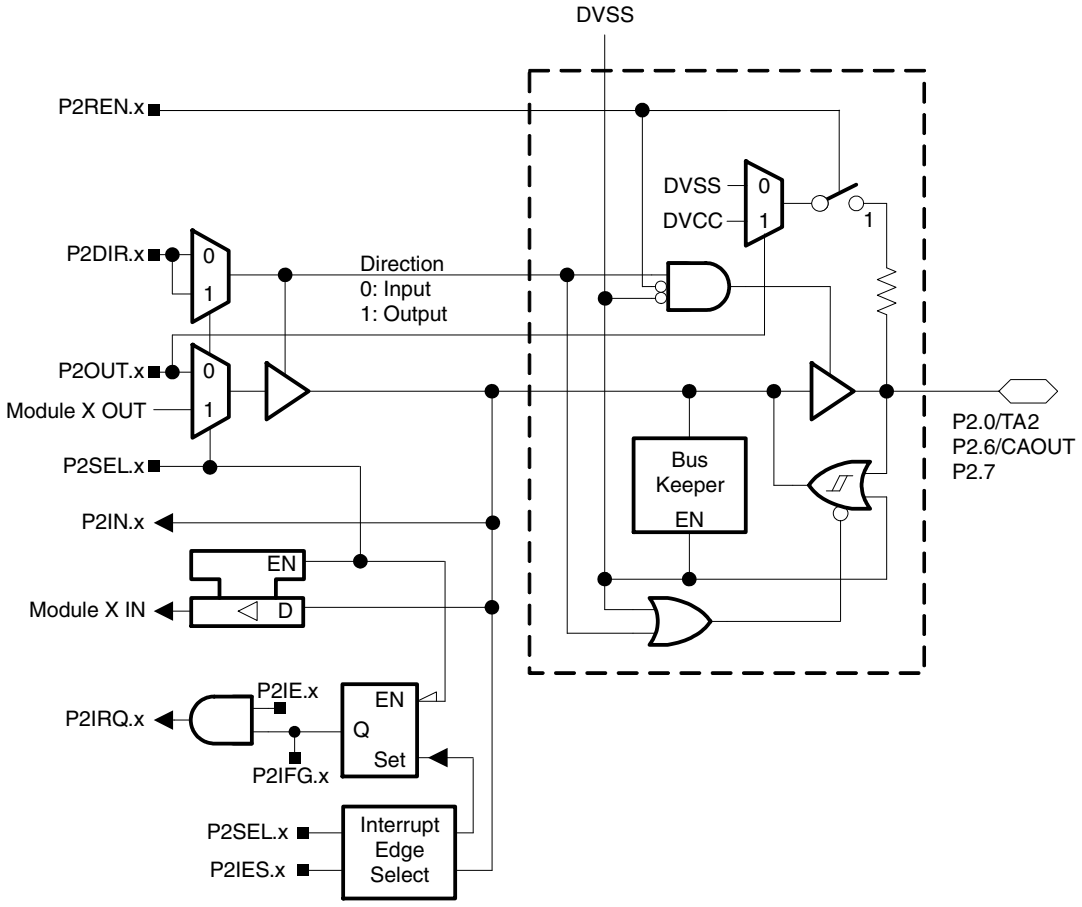


Port P1 (P1.6 and P1.7) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	CAPD.x
P1.6/CA0	6	P1.6 (I/O)	I: 0, O: 1	0	0
		CA0 (see Note 2)	X	X	1
P1.7/CA1	7	P1.7 (I/O)	I: 0, O: 1	0	0
		CA1 (see Note 2)	X	X	1

NOTES: 1. X: Don't care.
2. Setting the CAPD.x bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

port P2, P2.0, P2.6 to P2.7, input/output with Schmitt trigger

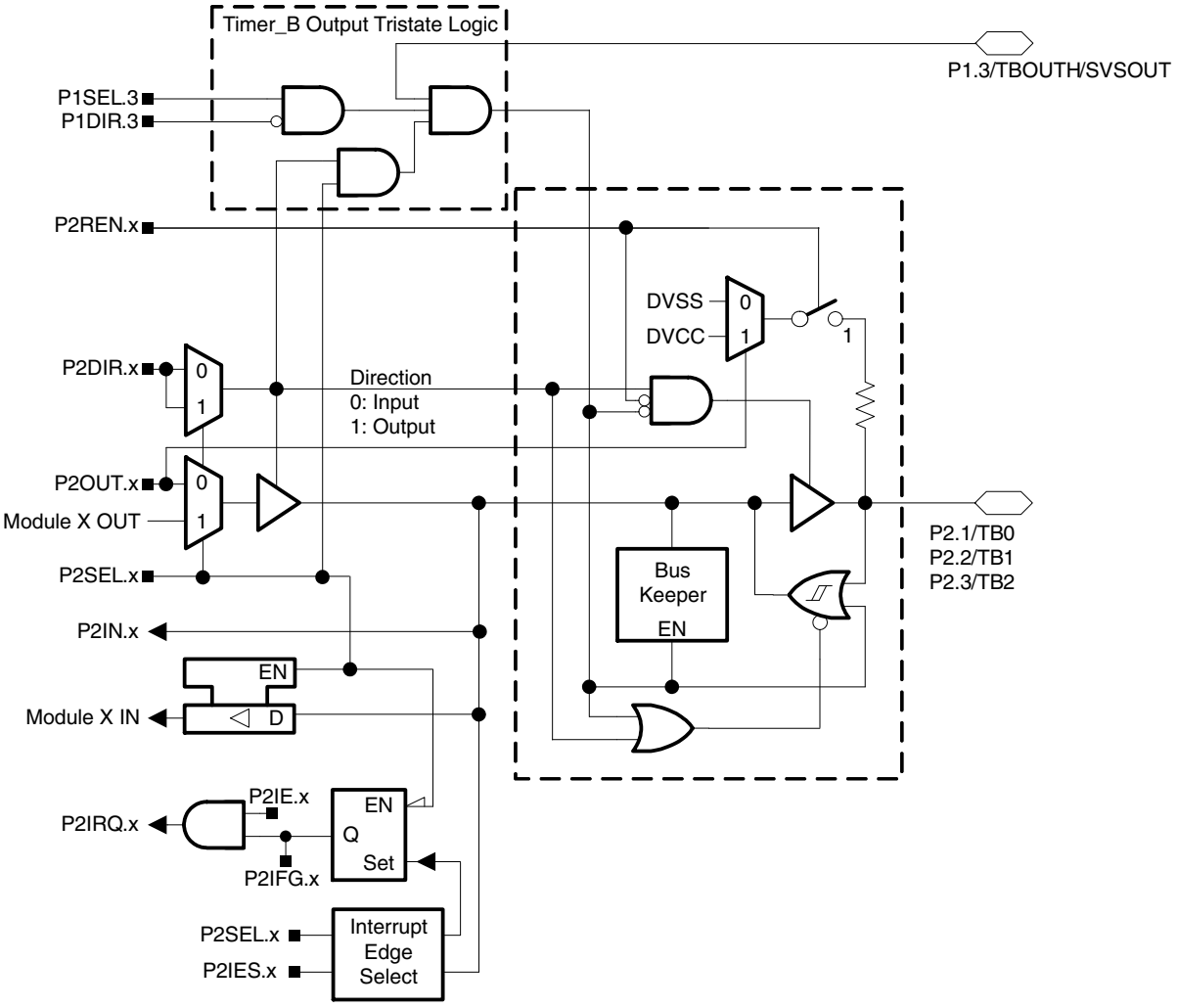


Port P2 (P2.0, P2.6 and P2.7) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.0/TA2	0	P2.0 (I/O)	I: 0, O: 1	0
		Timer_A3.CCI2A	0	1
		Timer_A3.TA2	1	1
P2.6/CAOUT	6	P2.6 (I/O)	I: 0, O: 1	0
		N/A	0	1
		CAOUT	1	1
P2.7	7	P2.7 (I/O)	I: 0, O: 1	0
		N/A	0	1
		DVSS	1	1

NOTES: 1. N/A: Not available or not applicable
2. Setting TBOUTH causes all Timer_B outputs to be set to high impedance.

port P2, P2.1 to P2.3, input/output with Schmitt trigger

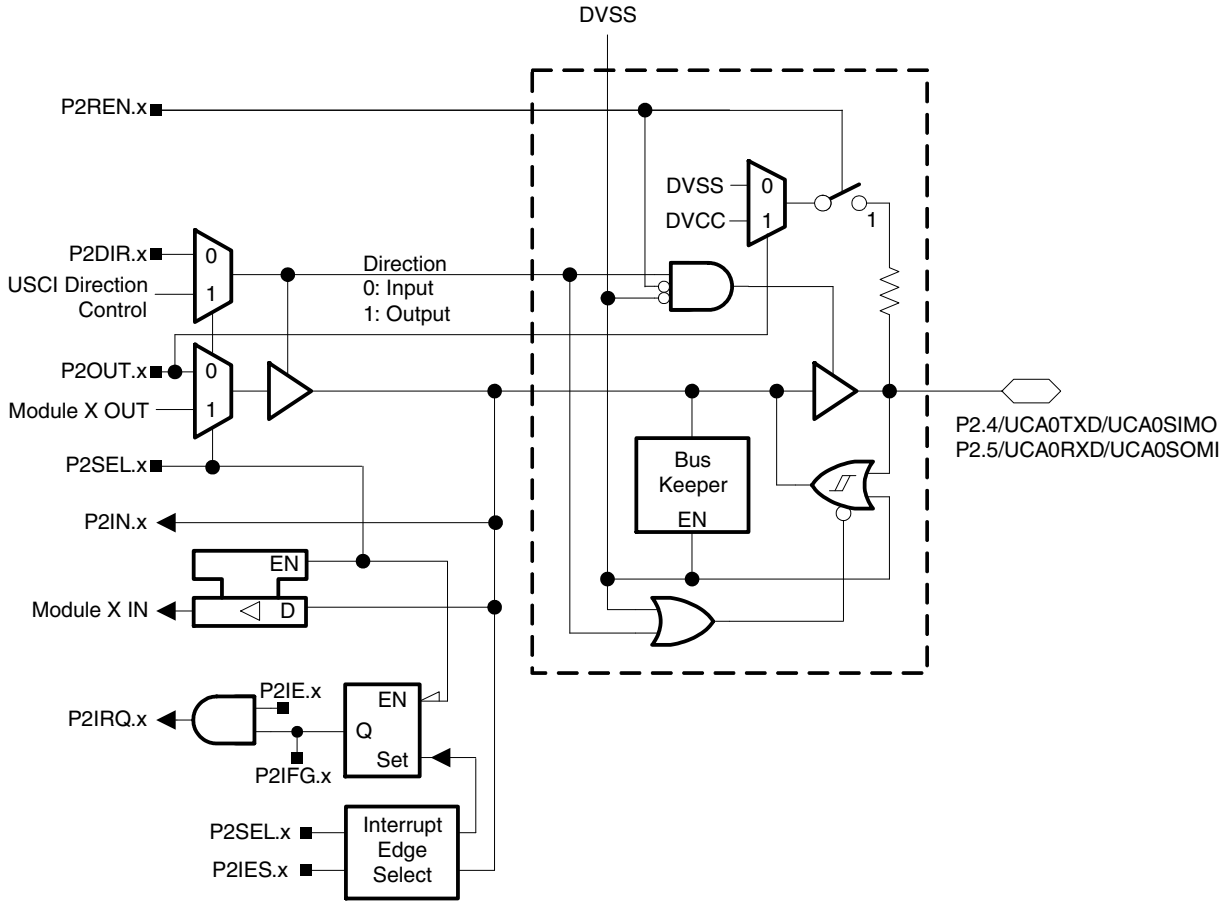


Port P2 (P2.1 to P2.3) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.1/TB0	1	P2.1 (I/O)	I: 0, O: 1	0
		Timer_B7.CCI0A and Timer_B7.CCI0B	0	1
		Timer_B7.TB0 (see Note 2)	1	1
P2.2/TB1	2	P2.2 (I/O)	I: 0, O: 1	0
		Timer_B7.CCI1A and Timer_B7.CCI1B	0	1
		Timer_B7.TB1 (see Note 2)	1	1
P2.3/TB3	3	P2.3 (I/O)	I: 0, O: 1	0
		Timer_B7.CCI2A and Timer_B7.CCI2B	0	1
		Timer_B7.TB3 (see Note 2)	1	1

NOTES: 1. N/A: Not available or not applicable
2. Setting TBOUTH causes all Timer_B outputs to be set to high impedance.

port P2, P2.4 to P2.5, input/output with Schmitt trigger

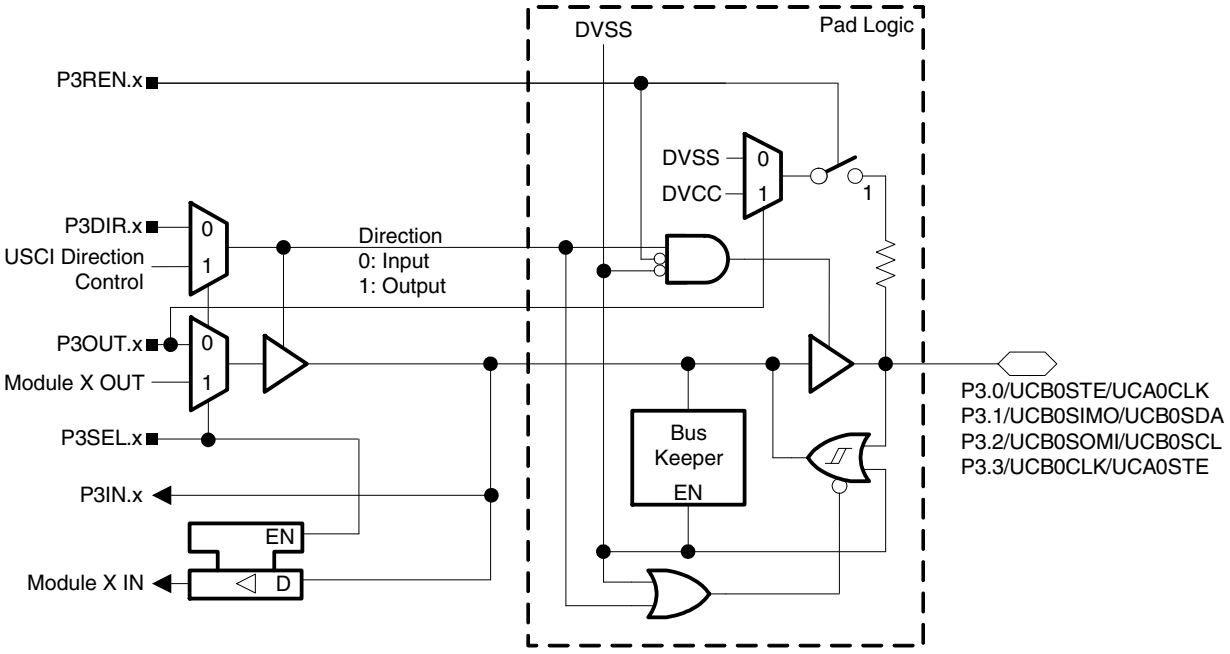


Port P2 (P2.4 and P2.5) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.4/ UCA0TXD/UCA0SIMO	4	P2.4 (I/O)	I: 0, O: 1	0
		UCA0TXD/UCA0SIMO (see Note 1, 2)	X	1
P2.5/ UCA0RXD/UCA0SOMI	5	P2.5 (I/O)	I: 0, O: 1	0
		UCA0RXD/UCA0SOMI (see Note 1, 2)	X	1

NOTES: 1. X: Don't care.
2. The pin direction is controlled by the USCI module.

port P3, P3.0 to P3.3, input/output with Schmitt trigger

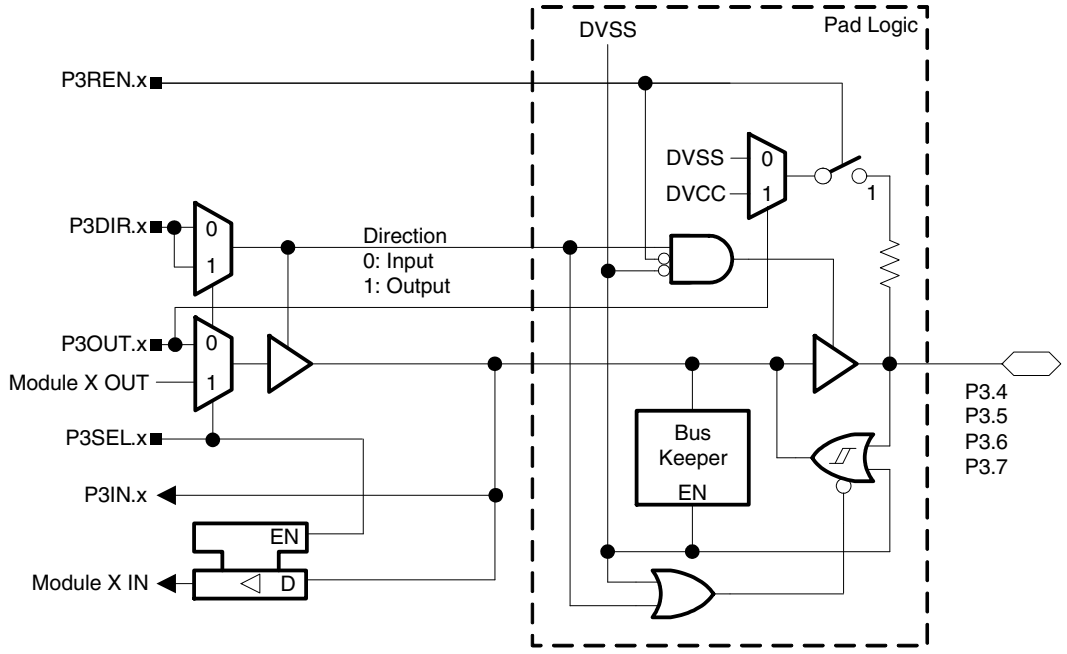


Port P3 (P3.0 to P3.3) pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P3DIR.x	P3SEL.x
P3.0/ UCA0CLK/UCB0STE	0	P3.0 (I/O)	I: 0, O: 1	0
		UCA0CLK/UCB0STE (see Notes 1, 2, 3)	X	1
P3.1/ UCB0SIMO/ UCB0SDA	1	P3.1 (I/O)	I: 0, O: 1	0
		UCB0SIMO/UCB0SDA (see Notes 1, 2, 4)	X	1
P3.2/ UCB0SOMI/ UCB0SCL	2	P3.2 (I/O)	I: 0, O: 1	0
		UCB0SOMI/UCB0SCL (see Notes 1, 2, 4)	X	1
P3.3/ UCB0CLK/UCA0STE	3	P3.3 (I/O)	I: 0, O: 1	0
		UCB0CLK (see Notes 1, 2, 5)	X	1

NOTES: 1. X: Don't care.
2. The pin direction is controlled by the USCI module.
3. UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output USCI_B0 will be forced to 3-wire SPI mode even if 4-wire SPI mode is selected.
4. In case the I2C functionality is selected the output drives only the logical 0 to V_{SS} level.
5. UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output USCI_A0 will be forced to 3-wire SPI mode even if 4-wire SPI mode is selected.

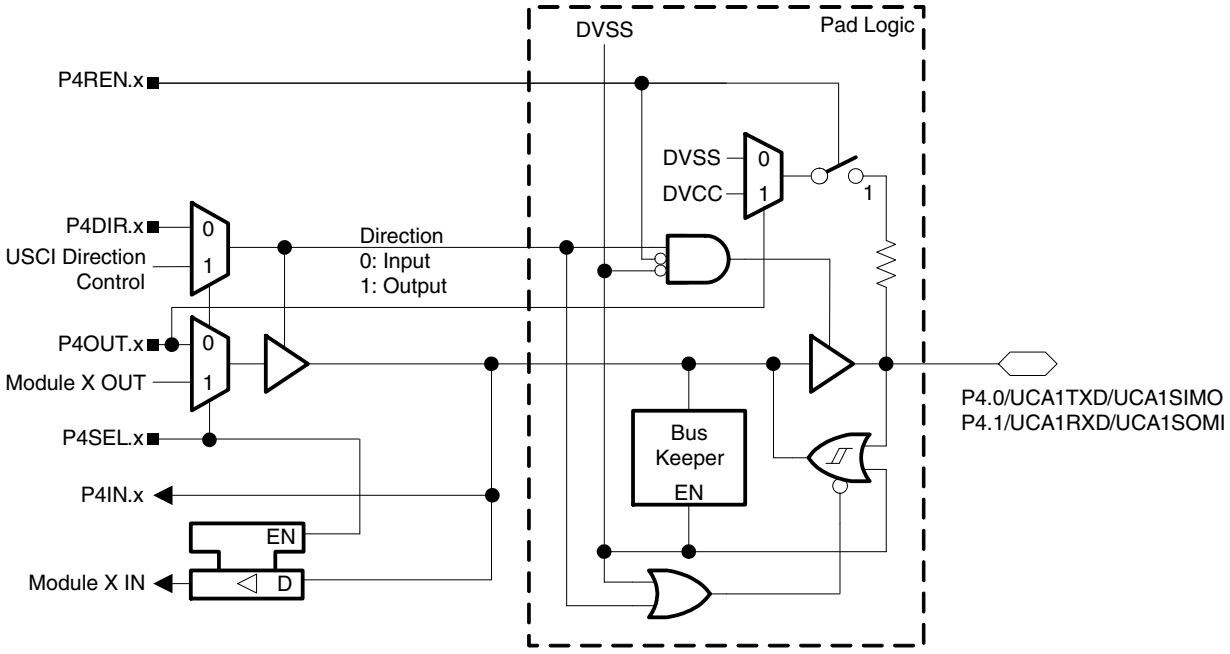
port P3, P3.4 to P3.7, input/output with Schmitt trigger



Port P3 (P3.4 to P3.7) pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P3DIR.x	P3SEL.x
P3.4	4	P3.4 (I/O)	I: 0, O: 1	0
		N/A	0	1
		DVSS	1	1
P3.5	5	P3.5 (I/O)	I: 0, O: 1	0
		N/A	0	1
		DVSS	1	1
P3.6	6	P3.6 (I/O)	I: 0, O: 1	0
		N/A	0	1
		DVSS	1	1
P3.7	7	P3.7 (I/O)	I: 0, O: 1	0
		N/A	0	1
		DVSS	1	1

port P4, P4.0 to P4.1, input/output with Schmitt trigger

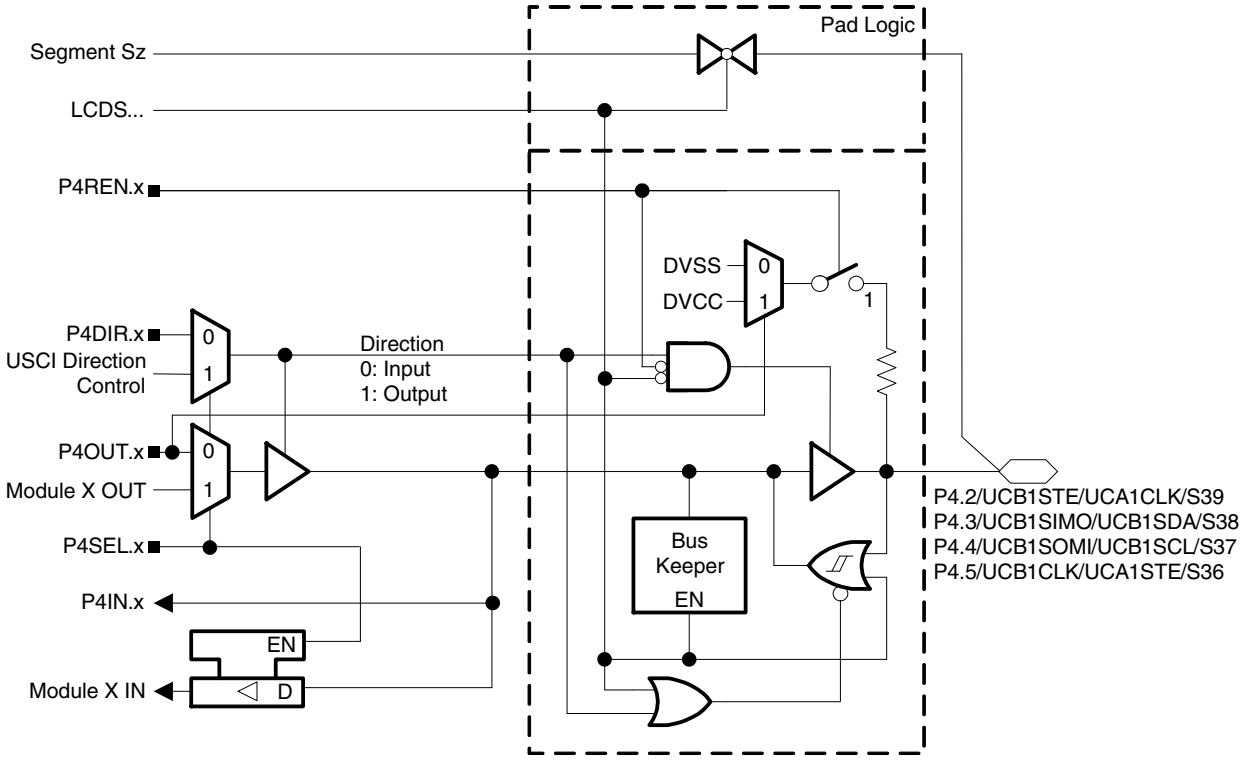


Port P4 (P4.0 to P4.1) pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/ UCA1TXD/UCA1SIMO	0	P4.0 (I/O)	I: 0, O: 1	0
		UCA1TXD/UCA1SIMO (see Notes 1, 2)	X	1
P4.1/ UCA1RXD/UCA1SOMI	1	P4.1 (I/O)	I: 0, O: 1	0
		UCA1RXD/UCA1SOMI (see Notes 1, 2)	X	1

NOTES: 1. X: Don't care.
2. The pin direction is controlled by the USCI module.

port P4, P4.2 to P4.5, input/output with Schmitt trigger

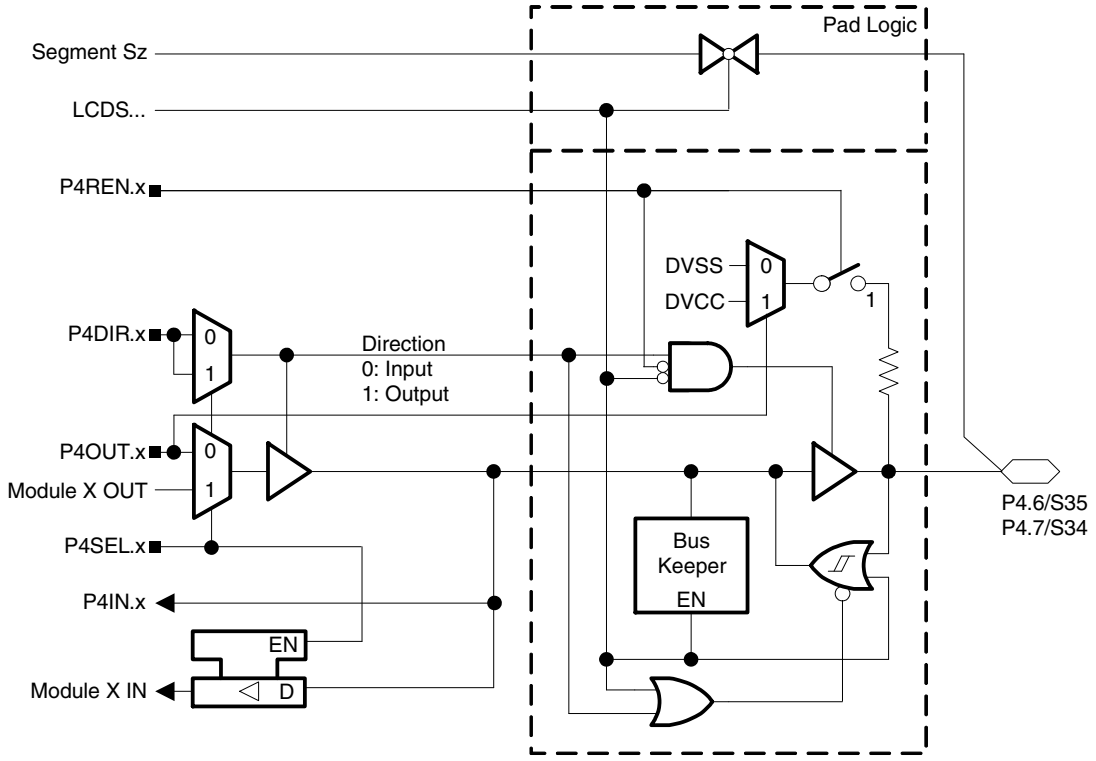


Port P4 (P4.2 to P4.5) pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P4DIR.x	P4SEL.x	LCDS36
P4.2/ UCA1CLK/UCB1STE/ S39	2	P4.2 (I/O)	I: 0, O: 1	0	0
		UCA1CLK/UCB1STE (see Notes 2, 3)	X	1	0
		S39	X	X	1
P4.3/ UCB1SIMO/UCB1SDA/ S38	3	P4.3 (I/O)	I: 0, O: 1	0	0
		UCB1SIMO/UCB1SDA (see Notes 2, 4)	X	1	0
		S38	X	X	1
P4.4/ UCB1SOMI/UCB1SCL/ S37	4	P4.4 (I/O)	I: 0, O: 1	0	0
		UCB1SOMI/UCB1SCL (see Notes 2, 4)	X	1	0
		S37	X	X	1
P4.5/ UCB1CLK/UCA1STE/ S36	5	P4.5 (I/O)	I: 0, O: 1	0	0
		UCB1CLK/UCA1STE (see Notes 2, 5)	X	1	0
		S36	X	X	1

NOTES: 1. X: Don't care.
2. The pin direction is controlled by the USCI module.
3. UCA1CLK function takes precedence over UCB1STE function. If the pin is required as UCA1CLK input or output USCI_B1 will be forced to 3-wire SPI mode even if 4-wire SPI mode is selected.
4. In case the I2C functionality is selected the output drives only the logical 0 to V_{SS} level.
5. UCB1CLK function takes precedence over UCA1STE function. If the pin is required as UCB1CLK input or output USCI_A1 will be forced to 3-wire SPI mode even if 4-wire SPI mode is selected.

port P4, P4.6 to P4.7, input/output with Schmitt trigger

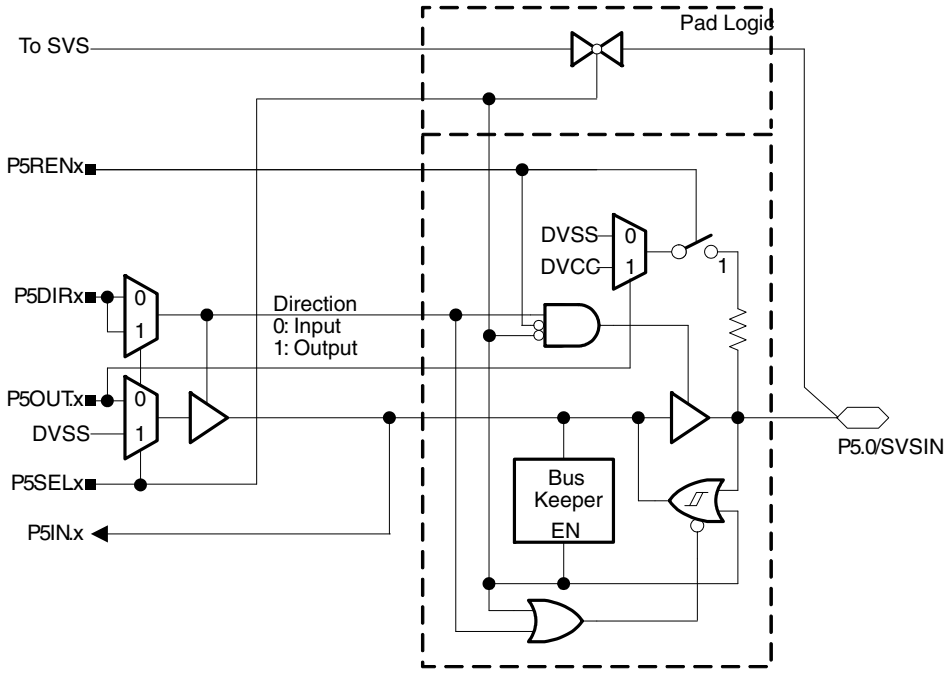


Port P4 (P4.6 to P4.7) pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P4DIR.x	P4SEL.x	LCDS32
P4.6/S35	6	P4.6 (I/O)	I: 0, O: 1	0	0
		S35	X	X	1
P4.7/S34	7	P4.7 (I/O)	I: 0, O: 1	0	0
		S34	X	X	1

NOTES: 1. X: Don't care.

port P5, P5.0, input/output with Schmitt trigger

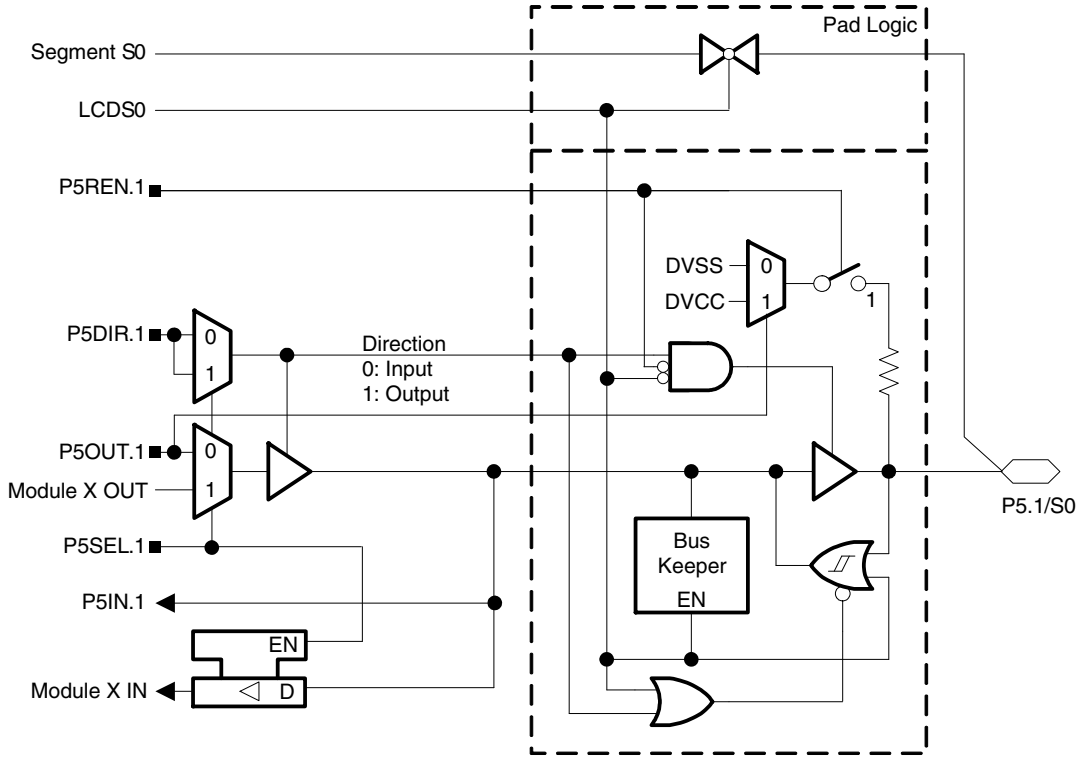


Port P5 (P5.0) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.0/SVSIN	0	P5.0 (I/O) (see Note 1)	I: 0, O: 1	0
		SVSIN (see Notes 1, 3)	X	1

NOTES: 1. X: Don't care.
2. N/A: Not available or not applicable.
3. Setting the P5SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

port P5, P5.1, input/output with Schmitt trigger

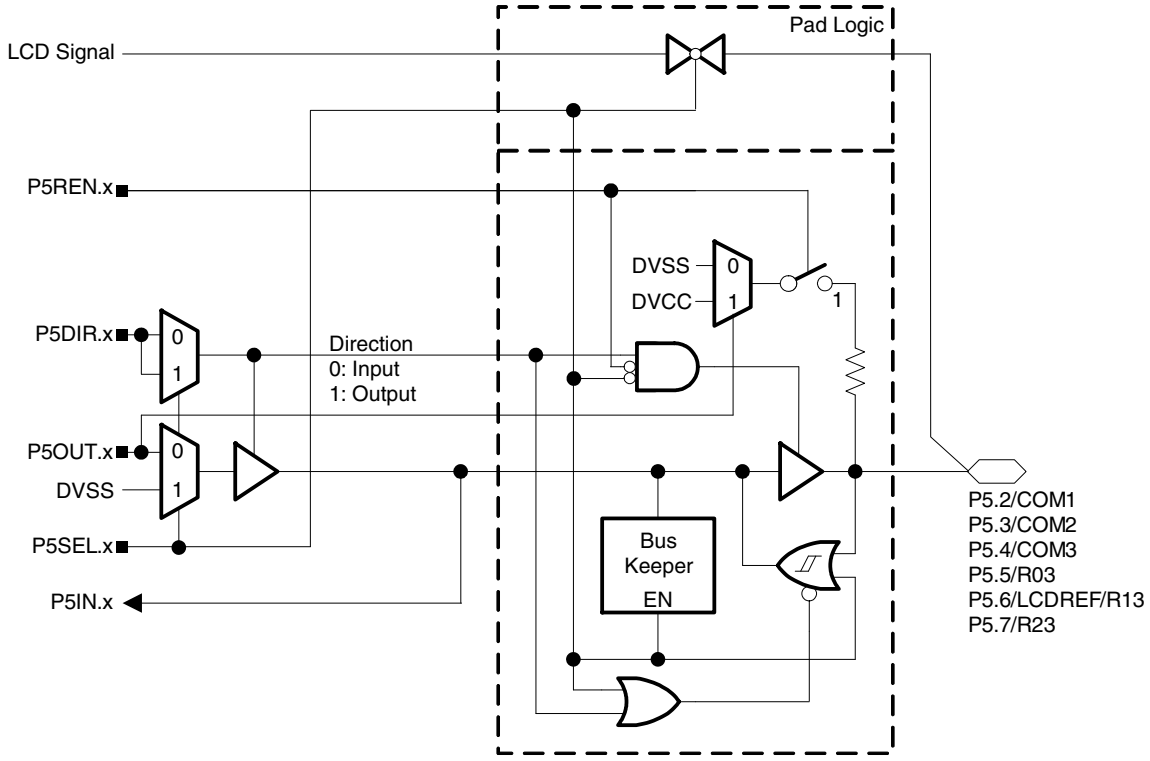


Port P5 (P5.1) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P5DIR.x	P5SEL.x	LCDS0
P5.1/S0	1	P5.1 (I/O)	I: 0, O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S0	X	X	1

NOTES: 1. X: Don't care.
2. N/A: Not available or not applicable.

port P5, P5.2 to P5.7, input/output with Schmitt trigger

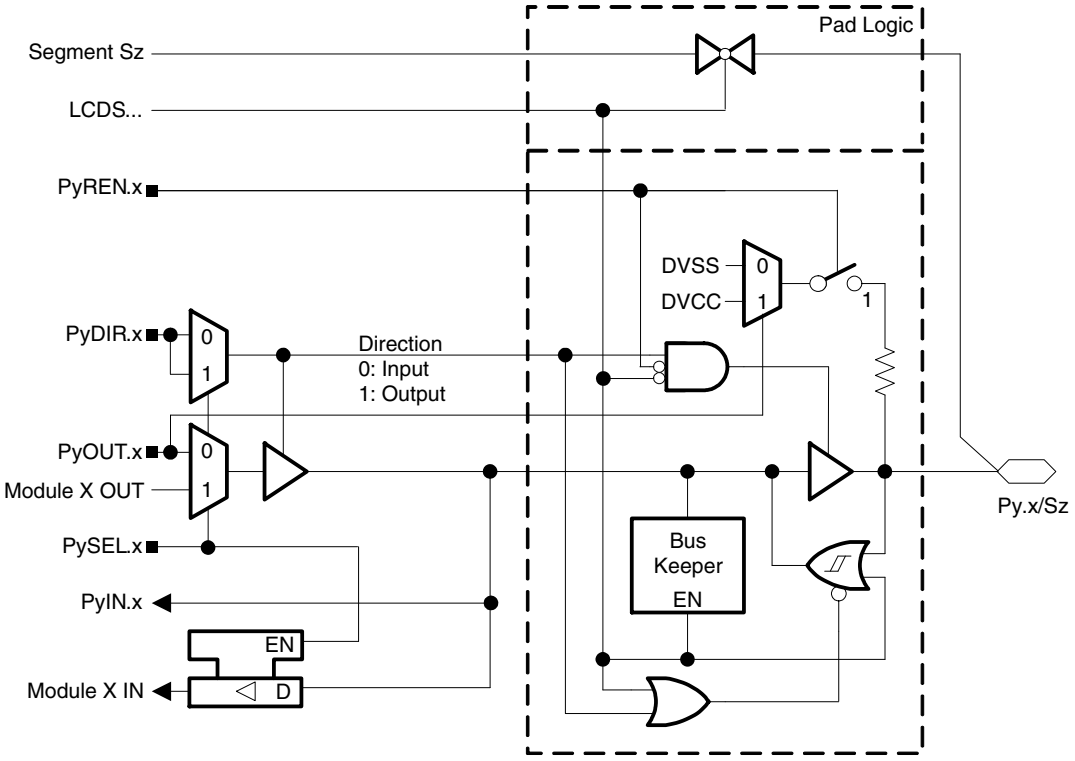


Port P5 (P5.2 to P5.4) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.2/COM1	2	P5.2 (I/O)	I: 0, O: 1	0
		COM1 (see Note 2)	X	1
P5.3/COM2	3	P5.3 (I/O)	I: 0, O: 1	0
		COM2 (see Note 2)	X	1
P5.4/COM3	4	P5.4 (I/O)	I: 0, O: 1	0
		COM3 (see Note 2)	X	1
P5.5/R03	5	P5.5 (I/O)	I: 0, O: 1	0
		R03 (see Note 2)	X	1
P5.6/LCDREF/R13	6	P5.6 (I/O)	I: 0, O: 1	0
		R13 or LCDREF (see Notes 2, 3)	X	1
P5.7/R23	7	P5.7 (I/O)	I: 0, O: 1	0
		R23 (see Note 2)	X	1

NOTES: 1. X: Don't care.
2. Setting the P5SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
3. External reference for the LCD_A charge pump is applied when VLCDREFx = 01. Otherwise R13 is selected.

port P7 to port P10, input/output with Schmitt trigger



Port P7 (P7.0 to P7.1) pin functions

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P7DIR.x	P7SEL.x	LCDS32
P7.0/S33	0	P7.0 (I/O)	I: 0, O: 1	0	0
		S33	X	X	1
P7.1/S32	1	P7.1 (I/O)	I: 0, O: 1	0	0
		S32	X	X	1

NOTES: 1. X: Don't care.

Port P7 (P7.4 to P7.5) pin functions

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P7DIR.x	P7SEL.x	LCDS28
P7.2/S31	2	P7.2 (I/O)	I: 0, O: 1	0	0
		S31	X	X	1
P7.3/S30	3	P7.3 (I/O)	I: 0, O: 1	0	0
		S30	X	X	1
P7.4/S29	4	P7.4 (I/O)	I: 0, O: 1	0	0
		S29	X	X	1
P7.5/S28	5	P7.5 (I/O)	I: 0, O: 1	0	0
		S28	X	X	1

NOTES: 1. X: Don't care.

Port P7 (P7.6 to P7.7) pin functions

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P7DIR.x	P7SEL.x	LCDS24
P7.6/S27	6	P7.6 (I/O)	I: 0, O: 1	0	0
		S27	X	X	1
P7.7/S26	7	P7.7 (I/O)	I: 0, O: 1	0	0
		S26	X	X	1

NOTES: 1. X: Don't care.

Port P8 (P8.0 to P8.1) pin functions

PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P8DIR.x	P8SEL.x	LCDS24
P8.0/S25	0	P8.0 (I/O)	I: 0, O: 1	0	0
		S25	X	X	1
P8.1/S24	1	P8.0 (I/O)	I: 0, O: 1	0	0
		S24	X	X	1

NOTES: 1. X: Don't care.

Port P8 (P8.2 to P8.5) pin functions

PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P8DIR.x	P8SEL.x	LCDS20
P8.2/S23	2	P8.2 (I/O)	I: 0, O: 1	0	0
		S23	X	X	1
P8.3/S22	3	P8.3 (I/O)	I: 0, O: 1	0	0
		S22	X	X	1
P8.4/S21	4	P8.4 (I/O)	I: 0, O: 1	0	0
		S21	X	X	1
P8.5/S20	5	P8.5 (I/O)	I: 0, O: 1	0	0
		S23	X	X	1

NOTES: 1. X: Don't care.

Port P8 (P8.6 to P8.7) pin functions

PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P8DIR.x	P8SEL.x	LCDS16
P8.6/S19	6	P8.6 (I/O)	I: 0, O: 1	0	0
		S19	X	X	1
P8.7/S18	7	P8.7 (I/O)	I: 0, O: 1	0	0
		S18	X	X	1

NOTES: 1. X: Don't care.

Port P9 (P9.0 to P9.1) pin functions

PIN NAME (P9.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P9DIR.x	P9SEL.x	LCDS16
P9.0/S17	0	P9.0 (I/O)	I: 0, O: 1	0	0
		S17 (see Note 1)	X	X	1
P9.1/S16	1	P9.1 (I/O)	I: 0, O: 1	0	0
		S16 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.

Port P9 (P9.2 to P9.5) pin functions

PIN NAME (P9.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P9DIR.x	P9SEL.x	LCDS12
P9.2/S15	2	P9.2 (I/O)	I: 0, O: 1	0	0
		S15	X	X	1
P9.3/S14	3	P9.3 (I/O)	I: 0, O: 1	0	0
		S14	X	X	1
P9.4/S13	4	P9.4 (I/O)	I: 0, O: 1	0	0
		S13	X	X	1
P9.5/S12	5	P9.5 (I/O)	I: 0, O: 1	0	0
		S12	X	X	1

NOTES: 1. X: Don't care.

Port P9 (P9.6 to P9.7) pin functions

PIN NAME (P9.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P9DIR.x	P9SEL.x	LCDS8
P9.6/S11	6	P9.6 (I/O)	I: 0, O: 1	0	0
		S11	X	X	1
P9.7/S10	7	P9.7 (I/O)	I: 0, O: 1	0	0
		S10	X	X	1

NOTES: 1. X: Don't care.

Port P10 (P10.0 to P10.1) pin functions

PIN NAME (P10.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P10DIR.x	P10SEL.x	LCDS8
P10.0/S8	0	P10.0 (I/O)	I: 0, O: 1	0	0
		S8	X	X	1
P10.1/S7	1	P10.1 (I/O)	I: 0, O: 1	0	0
		S7	X	X	1

NOTES: 1. X: Don't care.

Port P10 (P10.2 to P10.5) pin functions

PIN NAME (P10.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P10DIR.x	P10SEL.x	LCDS4
P10.2/S7	2	P10.2 (I/O)	I: 0, O: 1	0	0
		S7	X	X	1
P10.3/S6	3	P10.3 (I/O)	I: 0, O: 1	0	0
		S6	X	X	1
P10.4/S5	4	P10.4 (I/O)	I: 0, O: 1	0	0
		S5	X	X	1
P10.5/S4	5	P10.5 (I/O)	I: 0, O: 1	0	0
		S4	X	X	1

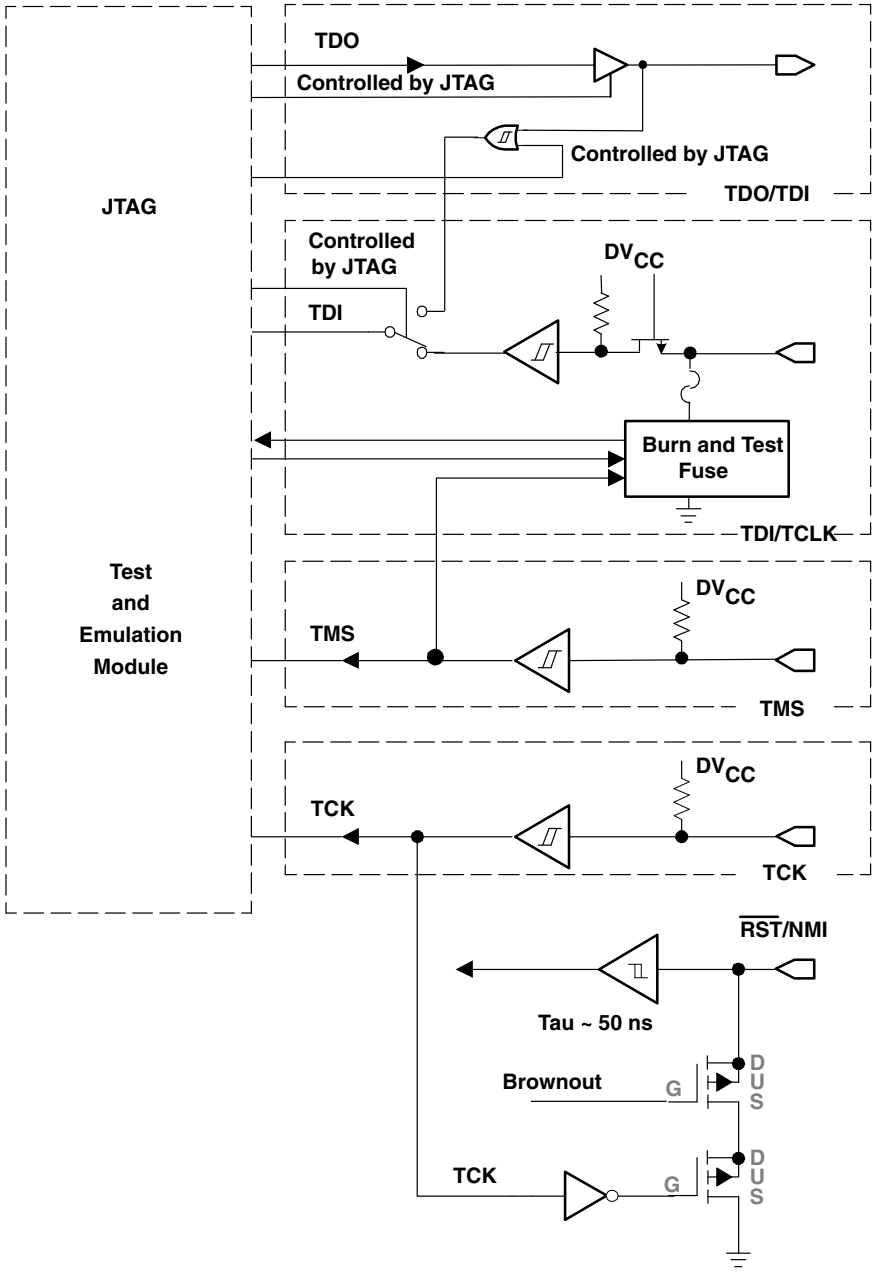
NOTES: 1. X: Don't care.

Port P10 (P10.6 to P10.7) pin functions

PIN NAME (P10.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P10DIR.x	P10SEL.x	LCDS0
P10.6/S3	6	P10.6 (I/O)	I: 0, O: 1	0	0
		S3	X	X	1
P10.7/S2	7	P10.7 (I/O)	I: 0, O: 1	0	0
		S2	X	X	1

NOTES: 1. X: Don't care.

JTAG pins (TMS, TCK, TDI/TCLK, TDO/TDI), input/output with Schmitt trigger or output



JTAG fuse check mode

Devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse-check current ($I_{(TF)}$) of 1 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse-check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse-check mode. After deactivation, the fuse-check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 27). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and, therefore, do not require external termination.

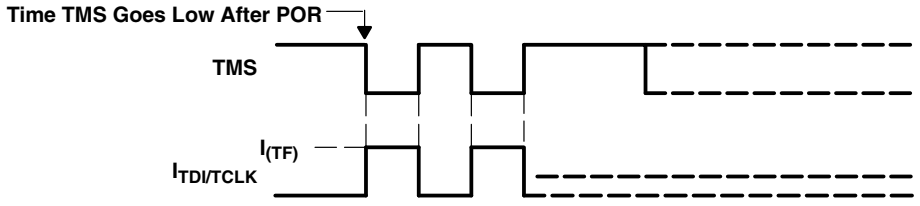


Figure 27. Fuse-Check Mode Current

Data Sheet Revision History

Literature Number	Summary
SLAS545	PRODUCT PREVIEW data sheet
SLAS545A	PRODUCTION DATA data sheet
SLAS545B	Section DEVELOPMENT TOOL SUPPORT added, page 2. Split XT1 frequency ranges depending on supply voltage range, page 36. Added parameter $f_{LFXT1, LF, logic}$ to LFXT1, low frequency modes characteristics, page 36.
SLAS545C	Changed limits on $t_{d(SVSon)}$ parameter (page 32)

NOTE: Page and figure numbers refer to the specified revision and may differ in other revisions.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F4783IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4783	Samples
MSP430F4783IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4783	Samples
MSP430F4784IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4784	Samples
MSP430F4784IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4784	Samples
MSP430F4793IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4793	Samples
MSP430F4793IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4793	Samples
MSP430F4794IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4794	Samples
MSP430F4794IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4794	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

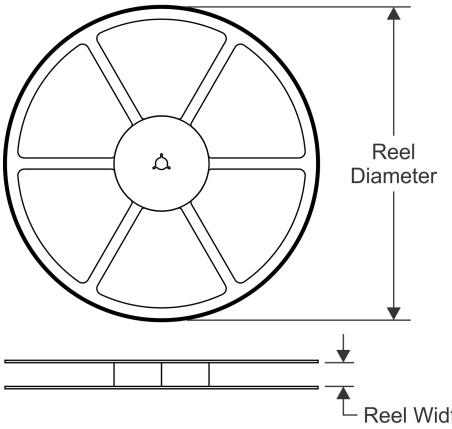
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

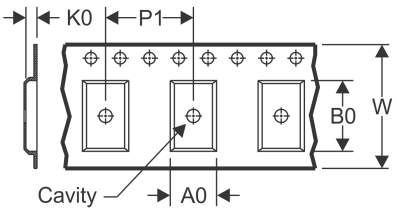
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

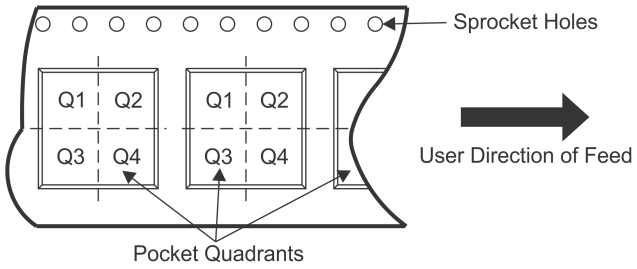


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

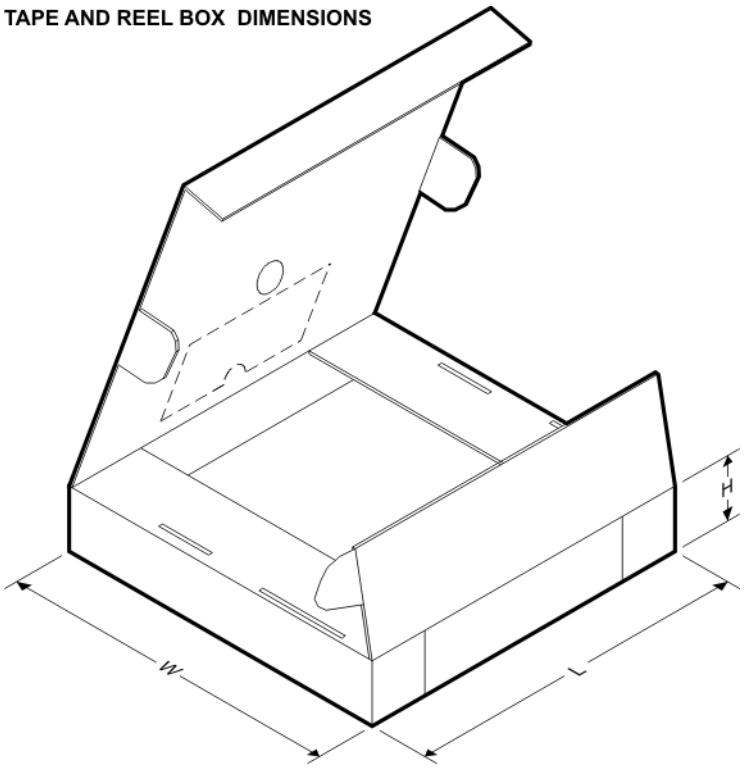
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F4783IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430F4784IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430F4793IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430F4794IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

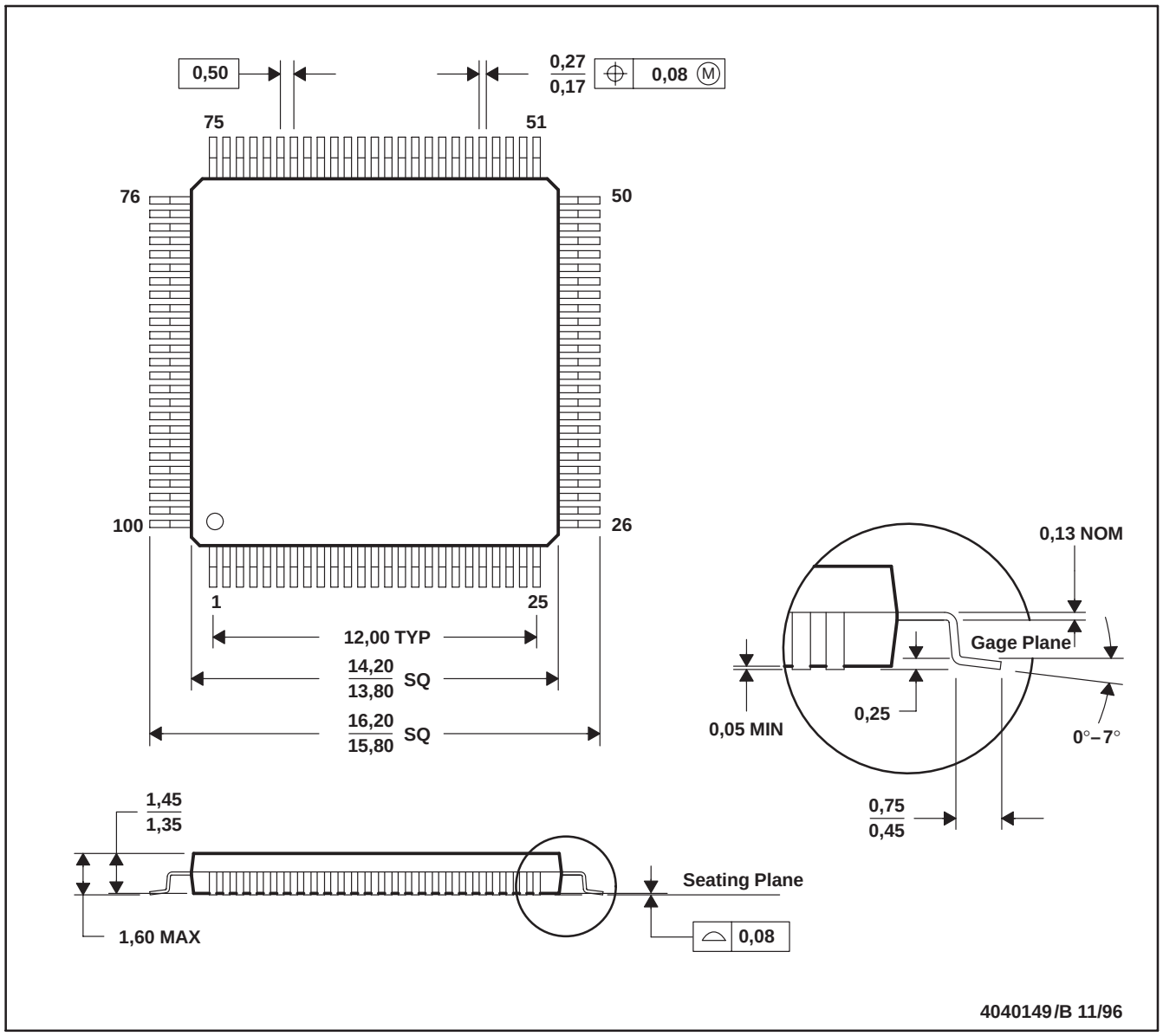


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F4783IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0
MSP430F4784IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0
MSP430F4793IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0
MSP430F4794IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0

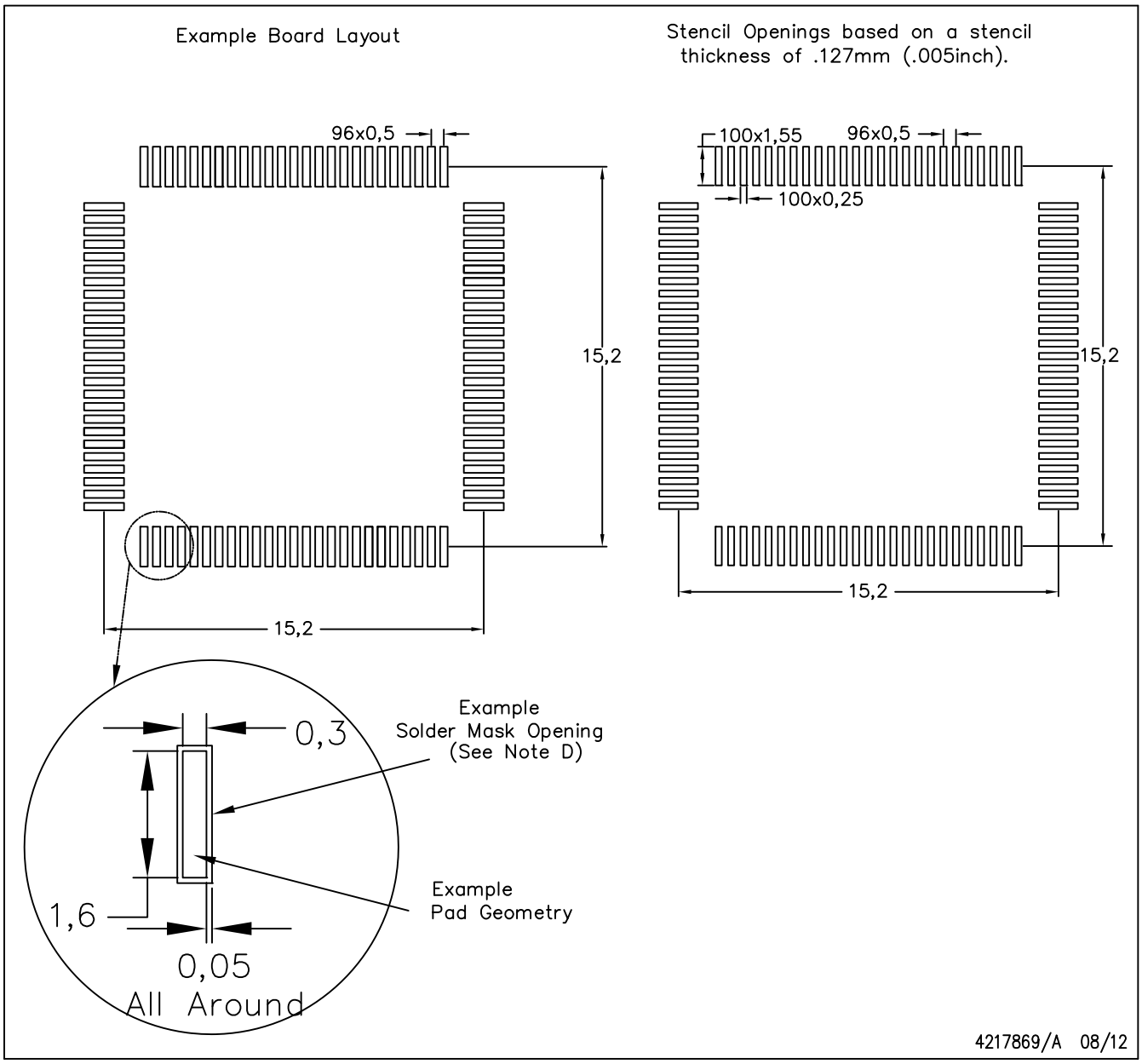
MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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