WINSOURCE
ELECTRONICS

THE DATASHEET OF

THS4031CDRG4

THS403x 100-MHz Low-Noise High-Speed Amplifiers

1 Features

- Ultra-Low 1.6 nV/√Hz Voltage Noise
- High Speed:
  - 100-MHz Bandwidth [G = 2 (–1), –3 dB]
  - 100-V/µs Slew Rate
- Very Low Distortion
  - THD = –72 dBc (f = 1 MHz, R_L = 150 Ω)
  - THD = –90 dBc (f = 1 MHz, R_L = 1 kΩ)
- Low 0.5-mV (Typical) Input Offset Voltage
- 90-mA Output Current Drive (Typical)
- Typical Operation from ±5 V to ±15 V
- Available in Standard SOIC and MSOP-PowerPAD™, Packages
- Evaluation Module Available

2 Applications

- Low-Noise, Wideband Amplifier for Industrial Applications
- Voltage-Controlled Oscillators
- Active Filters
- Video Amplifiers
- Cable Drivers

3 Description

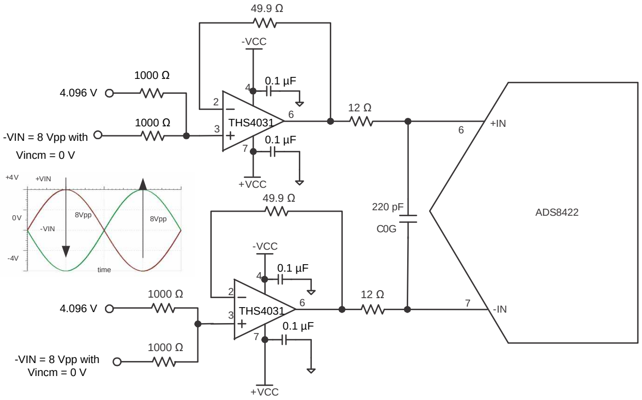
The THS4031 and THS4032 are ultra-low voltage noise, high-speed voltage feedback amplifiers that are ideal for applications requiring low voltage noise, including communications and imaging. The single amplifier THS4031 and the dual amplifier THS4032 offer good AC performance with 100-MHz bandwidth (G = 2), 100-V/µs slew rate, and 60-ns settling time (0.1%). The THS4031 and THS4032 are unity-gain stable with 275-MHz bandwidth. These amplifiers have a high drive capability of 90 mA and draw only 8.5-mA supply current per channel. With –90 dBc of total harmonic distortion (THD) at f = 1 MHz and a very low noise of 1.6 nV/√Hz, the THS4031 and THS4032 are designed for applications requiring low distortion and low noise such as buffering analog-to-digital converters.

Device Information[1]

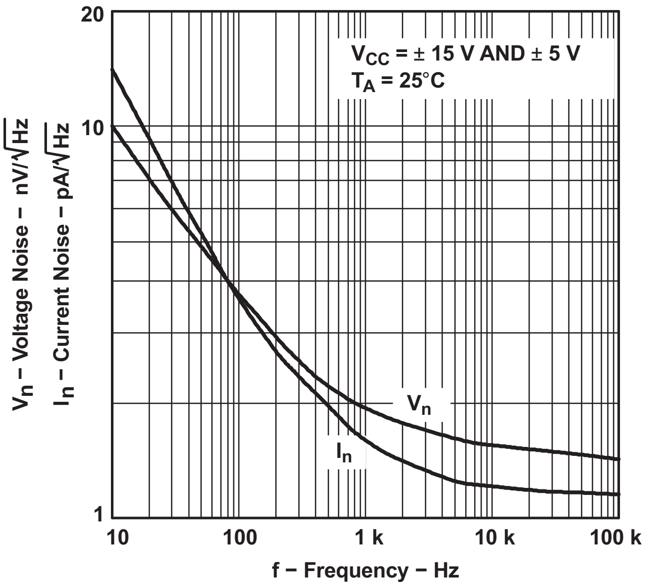
PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS4031, THS4032	SOIC (8)	4.90 mm × 3.91 mm
	MSOP-PowerPAD (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

High-Performance, Low-Noise Driver for 16-Bit SAR ADCs



Voltage Noise and Current Noise vs Frequency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (March 2016) to Revision I **Page**

- Deleted *Available Options* table (POA information) 3
- Corrected mathematical symbols inside square root symbol of Equation 1 21

Changes from Revision G (March 2010) to Revision H **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Removed obselete JG and FK packages 1
- Deleted Lead temperature row for JG package and case temperature row for FK package from *Absolute Maximum Ratings* 4
- Changed *Thermal Information* tables 5
- Removed the graphs in the *General PowerPAD™ Design Considerations* section 29
- Moved the information in the *Related Devices* table to the *Development Support* section 32

Changes from Revision F (September 2008) to Revision G **Page**

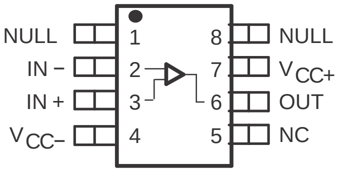
- Changed units for input voltage noise parameter (full range of T_A specifications) from nA/√Hz to nV√Hz 8

Changes from Revision E (June 2007) to Revision F **Page**

- Deleted bullet point for *Stable in Gain of 2 (–1) or greater* 1
- Editorial changes to paragraph format 28

5 Pin Configuration and Functions

THS4031 D or DGN Package
8-Pin SOIC or HVSSOP
Top View

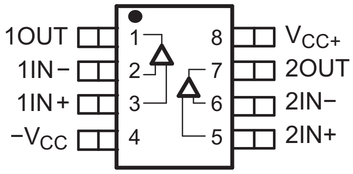


NC - No internal connection

Pin Functions: THS4031

PIN		I/O	DESCRIPTION
NAME	NO.		
IN–	2	I	Inverting input
IN+	3	I	Noninverting input
NC	5	—	No connection
NULL	1, 8	I	Voltage offset adjust
OUT	6	O	Output of amplifier
V_{CC+}	7	—	Positive power supply
V_{CC-}	4	—	Negative power supply

THS4032 D or DGN Package
8-Pin SOIC or HVSSOP
Top View



Cross-Section View Showing
PowerPAD™ Option (DGN)

Pin Functions: THS4032

PIN		I/O	DESCRIPTION
NAME	NO.		
1OUT	1	O	Channel 1 output
1IN–	2	I	Channel 1 inverting input
1IN+	3	I	Channel 1 noninverting input
2IN+	5	I	Channel 2 noninverting input
2IN–	6	I	Channel 2 inverting input
2OUT	7	O	Channel 2 output
V_{CC+}	8	—	Positive power supply
$–V_{CC}$	4	—	Negative power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC+} to V_{CC-}, V_{CC}			33	V
Input voltage, V_I			$\pm V_{CC}$	
Output current, I_O			150	mA
Differential input voltage, V_{IO}			±4	V
Continuous total power dissipation		See *General PowerPAD™ Design Considerations*		
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	–40	85	
	M-suffix	–55	125	
Maximum junction temperature (any condition), T_J			150	°C
Maximum junction temperature, continuous operation, long term reliability(2)			130	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device. Does not apply to the JG package or FK package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC+} and V_{CC-}	Supply voltage	Dual-supply	±4.5	±15	±16	V
		Single-supply	9	30	32	
T_A	Operating free-air temperature	C-suffix	0	25	70	°C
		I-suffix	–40	25	85	
		M-suffix	–55	25	125	

6.4 Thermal Information: THS4031

THERMAL METRIC[1]		THS4031		UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.9	61.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.9	53.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.2	43.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.7	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	68.8	42.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	14.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: THS4032

THERMAL METRIC[1]		THS4032		UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.2	56.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.8	48.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.4	37.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.2	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61	37.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	9.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics: R_L = 150 Ω

at T_A = 25°C, V_{CC} = ±15 V, and R_L = 150 Ω for the THS403xC, THS403xI (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (–3 dB)	V_{CC} = ±15 V Gain = –1 or 2			100		MHz
		V_{CC} = ±5 V Gain = –1 or 2			90		
	Bandwidth for 0.1-dB flatness	V_{CC} = ±15 V Gain = –1 or 2			50		MHz
		V_{CC} = ±5 V Gain = –1 or 2			45		
	Full power bandwidth (2)	$V_{O(pp)}$ = 20 V V_{CC} = ±15 V R_L = 1 kΩ			2.3		MHz
		$V_{O(pp)}$ = 5 V V_{CC} = ±5 V R_L = 1 kΩ			7.2		
SR	Slew rate (3)	V_{CC} = ±15 V 20-V step, gain = –1			100		V/µs
		V_{CC} = ±5 V 5-V step, gain = –1			80		
t_S	Settling time to 0.1%	V_{CC} = ±15 V 5-V step, gain = –1			60		ns
		V_{CC} = ±5 V 2.5-V step, gain = –1			45		
	Settling time to 0.01%	V_{CC} = ±15 V 5-V step, gain = –1			90		ns
		V_{CC} = ±5 V 2.5-V step, gain = –1			80		
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	THS4031: V_{CC} = ±5 V or ±15 V, f = 1 MHz $V_{O(pp)}$ = 2 V, gain = 2	R_L = 150 Ω		–81		dBc
			R_L = 1 kΩ		–96		
		THS4032: V_{CC} = ±5 V or ±15 V, f = 1 MHz $V_{O(pp)}$ = 2 V, gain = 2	R_L = 150 Ω		–72		
			R_L = 1 kΩ		–90		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V, f > 10 kHz			1.6		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V, f > 10 kHz			1.2		pA/√Hz
	Differential gain error	V_{CC} = ±15 V	Gain = 2 40 IRE modulation NTSC and PAL ±100 IRE ramp		0.015%		
		V_{CC} = ±5 V			0.02%		
	Differential phase error	V_{CC} = ±15 V			0.025		°
		V_{CC} = ±5 V			0.03		
	Channel-to-channel crosstalk (THS4032 only)	V_{CC} = ±5 V or ±15 V, f = 1 MHZ			–61		dBc
DC PERFORMANCE							
	Open loop gain	V_{CC} = ±15 V R_L = 1 kΩ V_O = ±10 V	T_A = 25°C	93	98		dB
			T_A = Full range	92			
		V_{CC} = ±5 V R_L = 1 kΩ V_O = ±2.5 V	T_A = 25°C	90	95		
			T_A = Full range	89			

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(1) Full range = 0°C to 70°C for THS403xC and –40°C to +85°C for THS403xI suffix.
(2) Full power bandwidth = slew rate / [$\sqrt{2}\,\pi V_{OC(Peak)}$].
(3) Slew rate is measured from an output level range of 25% to 75%.

Electrical Characteristics: R_L = 150 Ω (continued)

at T_A = 25°C, V_{CC} = ±15 V, and R_L = 150 Ω for the THS403xC, THS403xI (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		30	250	nA
			T_A = Full range			400	
	Offset voltage drift	V_{CC} = ±5 V or ±15 V T_A = Full range			2		µV/°C
	Input offset current drift	V_{CC} = ±5 V or ±15 V T_A = Full range			0.2		nA/°C
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V		±13.5	±14		V
		V_{CC} = ±5 V		±3.8	±4		
CMRR	Common-mode rejection ratio	V_{CC} = ±15 V V_{ICR} = ±12.V	T_A = 25°C	85	95		dB
			T_A = Full range	80			
		V_{CC} = ±5 V V_{ICR} = ±2.5 V	T_A = 25°C	90	100		
			T_A = Full range	85			
r_i	Input resistance				2		MΩ
C_i	Input capacitance				1.5		pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.6		V
		V_{CC} = ±5 V		±3.4	±3.8		
		V_{CC} = ±15 V, R_L = 150 Ω		±12	±12.9		
		V_{CC} = ±5 V, R_L = 250 Ω		±3	±3.5		
I_O	Output current (4)	V_{CC} = ±15 V	R_L = 20 Ω	60	90		mA
		V_{CC} = ±5 V		50	70		
I_{SC}	Short-circuit current (4)	V_{CC} = ±15 V			150		mA
R_O	Output resistance	Open loop			13		Ω
POWER SUPPLY							
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	V_{CC} = ±15 V	T_A = 25°C		8.5	10	mA
			T_A = Full range			11	
		V_{CC} = ±5 V	T_A = 25°C		7.5	9	
			T_A = Full range			10.5	
PSRR	Power-supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	85	95		dB
			T_A = Full range	80			

(4) Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the *Absolute Maximum Ratings* in this data sheet for more information.

6.7 Electrical Characteristics: R_L = 1 kΩ

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [1]		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Unity-gain bandwidth	V_{CC} = ±15 V, closed loop R_L = 1 kΩ		100 [2]	120		MHz
	Small-signal bandwidth (–3 dB)	V_{CC} = ±15 V Gain = –1 or 2			100		MHz
		V_{CC} = ±5 V Gain = –1 or 2			90		
	Bandwidth for 0.1-dB flatness	V_{CC} = ±15 V Gain = –1 or 2			50		MHz
		V_{CC} = ±5 V Gain = –1 or 2			45		
	Full power bandwidth [3]	$V_{O(pp)}$ = 20 V V_{CC} = ±15 V R_L = 1 kΩ			2.3		MHz
		$V_{O(pp)}$ = 5 V V_{CC} = ±5 V R_L = 1 kΩ			7.1		
SR	Slew rate	V_{CC} = ±15 V R_L = 1 kΩ		80 [2]	100		V/µs
t_S	Settling time to 0.1%	V_{CC} = ±15 V 5-V step, gain = –1			60		ns
		V_{CC} = ±5 V 2.5-V step, gain = –1			45		
	Settling time to 0.01%	V_{CC} = ±15 V 5-V step, gain = –1			90		ns
		V_{CC} = ±5 V 2.5-V step, gain = –1			80		
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	V_{CC} = ±5 V or ±15 V f = 1 MHz, gain = 2 $V_{O(pp)}$ = 2 V T_A = 25°C	R_L = 150 Ω		–81		dBc
			R_L = 1 kΩ		96		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V T_A = 25°C f > 10 kHz, R_L = 150 Ω			1.6		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V T_A = 25°C, f > 10 kHz, R_L = 150 Ω			1.2		pA/√Hz
	Differential gain error	Gain = 2, 40 IRE modulation, T_A = 25°C, NTSC and PAL, ±100 IRE ramp, R_L = 150 Ω	V_{CC} = ±5 V		0.015%		
			V_{CC} = ±15 V		0.02%		
	Differential phase error		V_{CC} = ±5 V		0.025		°
			V_{CC} = ±15 V		0.03		
DC PERFORMANCE							
	Open loop gain	V_{CC} = ±15 V, R_L = 1 kΩ, V_O = ±10 V	T_A = 25°C	93	98		dB
			T_A = Full range	92			
		V_{CC} = ±15 V, R_L = 1 kΩ, V_O = ±2.5 V	T_A = 25°C	92	95		
			T_A = Full range	91			
V_{OS}	Input offset voltage	V_{CC} =±5 V or ±15 V	T_A = 25°C		0.5	2	mV
			T_A = Full range			3	
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		3	6	µA
			T_A = Full range			8	

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(1) Full range = 0°C to 70°C for THS403xC and –40°C to +85°C for THS403xI suffix.
(2) This parameter is not tested.
(3) Full power bandwidth = slew rate / [$\sqrt{2}\ \pi V_{OC(Peak)}$].

Electrical Characteristics: R_L = 1 kΩ (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [1]		MIN	TYP	MAX	UNIT
I_{OS}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		30	250	nA
			T_A = Full range			400	
	Offset voltage drift	V_{CC} = ±5 V or ±15 V, T_A = full range			2		µV/°C
	Input offset current drift	V_{CC} = ±5 V or ±15 V, T_A = full range			0.2		nA/°C
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V		±13.5	±14.3		V
		V_{CC} = ±5 V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V_{CC} = ±15 V, V_{ICR} = ±12 V	T_A = 25°C	85	95		dB
			T_A = Full range	80			
		V_{CC} = ±5 V, V_{ICR} = ±2.5 V	T_A = 25°C	90	100		
			T_A = Full range	85			
r_i	Input resistance				2		MΩ
C_d	Input capacitance				1.5		pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	V_{CC} = ±15 V, R_L = 1 kΩ		±13	±13.6		V
		V_{CC} = ±5 V, R_L = 1 kΩ		±3.4	±3.8		
		V_{CC} = ±15 V, R_L = 150 Ω		±12	±12.9		
		V_{CC} = ±5 V, R_L = 250 Ω		±3	±3.5		
I_O	Output current [4]	V_{CC} = ±15 V, R_L = 20 Ω		60	90		mA
		V_{CC} = ±5 V, R_L = 20 Ω		50	70		
I_{SC}	Short-circuit current [4]	V_{CC} = ±15 V			150		mA
R_O	Output resistance	Open loop			13		Ω
POWER SUPPLY							
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	V_{CC} = ±15 V	T_A = 25°C		8.5	10	mA
			T_A = Full range			11	
		V_{CC} = ±5 V	T_A = 25°C		7.5	9	
			T_A = Full range			10	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	85	95		dB
			T_A = Full range	80			

(4) Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the Absolute Maximum Ratings in this data sheet for more information.

6.8 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
Input Offset Voltage Distribution		Figure 1, Figure 2
Input Offset Voltage	vs Free-Air Temperature	Figure 3
Input Bias Current	vs Free-Air Temperature	Figure 4
Output Voltage Swing	vs Supply Voltage	Figure 5
Maximum Output Voltage Swing	vs Free-Air Temperature	Figure 6
Maximum Output Current	vs Free-Air Temperature	Figure 7
Supply Current	vs Free-Air Temperature	Figure 8
Common-Mode Input Voltage	vs Supply Voltage	Figure 9
Closed-Loop Output Impedance	vs Frequency	Figure 10
Open-Loop Gain and Phase Response	vs Frequency	Figure 11
Power-Supply Rejection Ratio	vs Frequency	Figure 12
Common-Mode Rejection Ratio	vs Frequency	Figure 13
Crosstalk	vs Frequency	Figure 14
Harmonic Distortion	vs Frequency	Figure 15, Figure 16
Harmonic Distortion	vs Peak-to-Peak Output Voltage	Figure 17, Figure 18
Slew Rate	vs Free-Air Temperature	Figure 19
0.1% Settling Time	vs Output Voltage Step Size	Figure 20
Small-Signal Frequency Response with Varying Feedback Resistance	Gain = 1, V_{CC} = ±15 V, R_L = 1 kΩ	Figure 21
Frequency Response with Varying Output Voltage Swing	Gain = 1, V_{CC} = ±15 V, R_L = 1 kΩ	Figure 22
Small-Signal Frequency Response with Varying Feedback Resistance	Gain = 1, V_{CC} = ±15 V, R_L = 150 kΩ	Figure 23
Frequency Response with Varying Output Voltage Swing	Gain = 1, V_{CC} = ±15 V, R_L = 150 kΩ	Figure 24
Small-Signal Frequency Response with Varying Feedback Resistance	Gain = 1, V_{CC} = ±5 V, R_L = 1 kΩ	Figure 25
Frequency Response with Varying Output Voltage Swing	Gain = 1, V_{CC} = ±5 V, R_L = 1 kΩ	Figure 26
Small-Signal Frequency Response with Varying Feedback Resistance	Gain = 1, V_{CC} = ±5 V, R_L = 150 kΩ	Figure 27
Frequency Response with Varying Output Voltage Swing	Gain = 1, V_{CC} = ±5 V, R_L = 150 kΩ	Figure 28
Small-Signal Frequency Response with Varying Feedback Resistance	Gain = 2, V_{CC} = ±5 V, R_L = 150 kΩ	Figure 29
Small-Signal Frequency Response with Varying Feedback Resistance	Gain = 2, V_{CC} = ±5 V, R_L = 150 kΩ	Figure 30
Small-Signal Frequency Response with Varying Feedback Resistance	Gain = –1, V_{CC} = ±15 V, R_L = 150 kΩ	Figure 31
Frequency Response with Varying Output Voltage Swing	Gain = –1, V_{CC} = ±5 V, R_L = 150 kΩ	Figure 32
Small-Signal Frequency Response	Gain = 5, V_{CC} = ±15 V, ±5 V	Figure 33
Output Amplitude	vs Frequency, Gain = 2, V_S = ±15 V	Figure 34
Output Amplitude	vs Frequency, Gain = 2, V_S = ±5 V	Figure 35
Output Amplitude	vs Frequency, Gain = –1, V_S = ±15 V	Figure 36
Output Amplitude	vs Frequency, Gain = –1, V_S = ±5 V	Figure 37
Differential Phase	vs Number of 150-Ω Loads	Figure 38, Figure 39
Differential Gain	vs Number of 150-Ω Loads	Figure 40, Figure 41
1-V Step Response	vs Time	Figure 42, Figure 43
4-V Step Response	vs Time	Figure 44
20-V Step Response	vs Time	Figure 45

6.9 Typical Characteristics

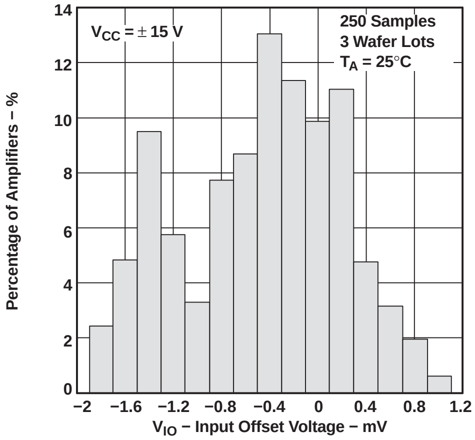


Figure 1. Input Offset Voltage Distribution

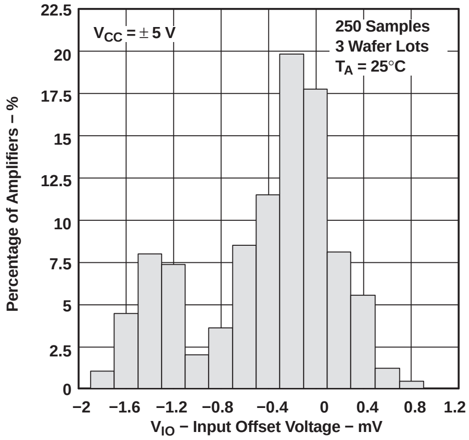


Figure 2. Input Offset Voltage Distribution

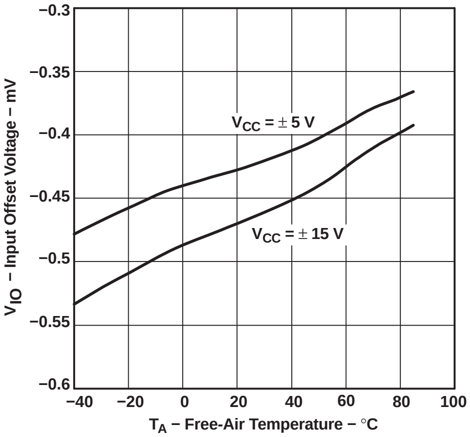


Figure 3. Input Offset Voltage vs Free-Air Temperature

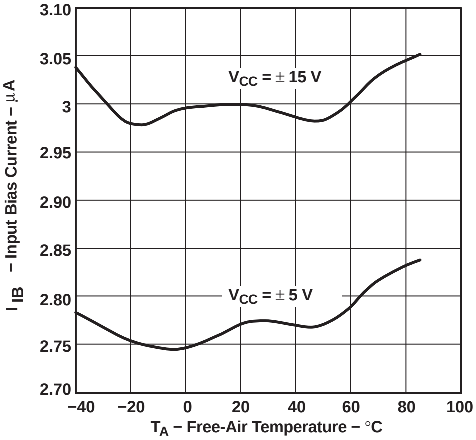


Figure 4. Input Bias Current vs Free-Air Temperature

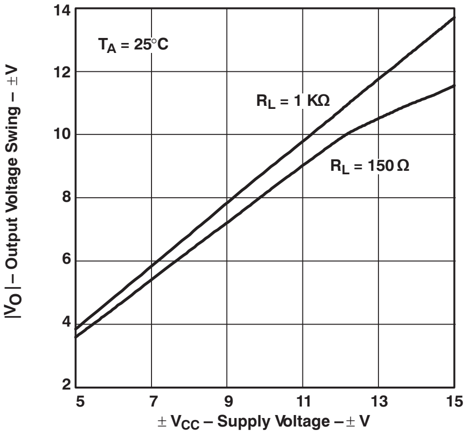


Figure 5. Output Voltage Swing vs Supply Voltage

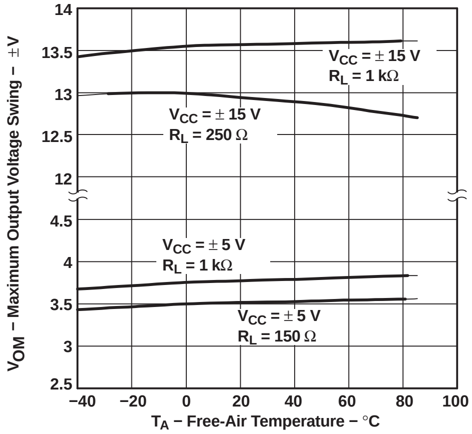


Figure 6. Maximum Output Voltage Swing vs Free-Air Temperature

Typical Characteristics (continued)

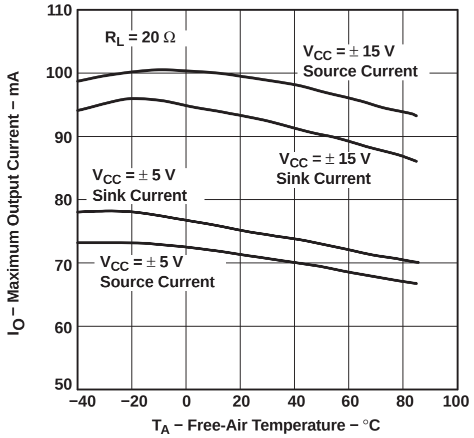


Figure 7. Maximum Output Current vs Free-Air Temperature

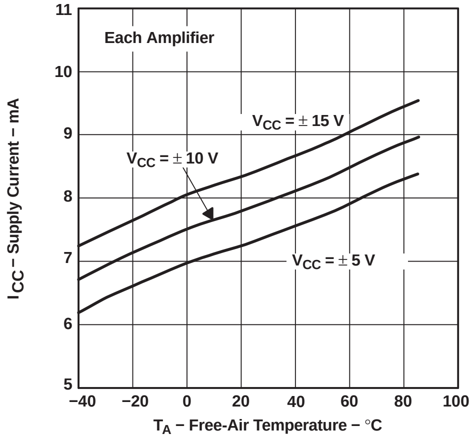


Figure 8. Supply Current vs Free-Air Temperature

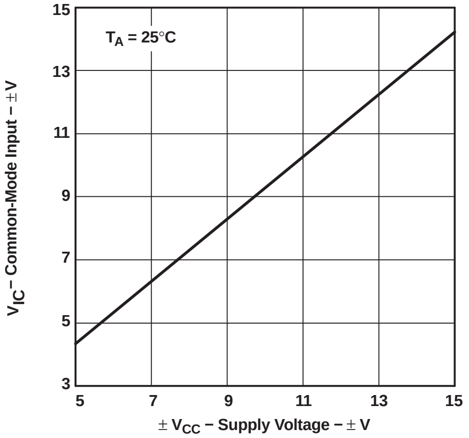


Figure 9. Common-Mode Input Voltage vs Supply Voltage

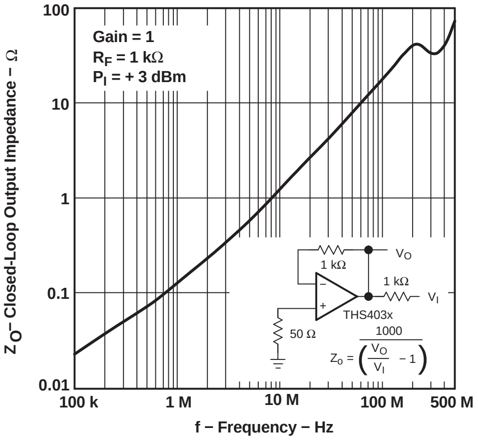


Figure 10. Closed-Loop Output Impedance vs Frequency

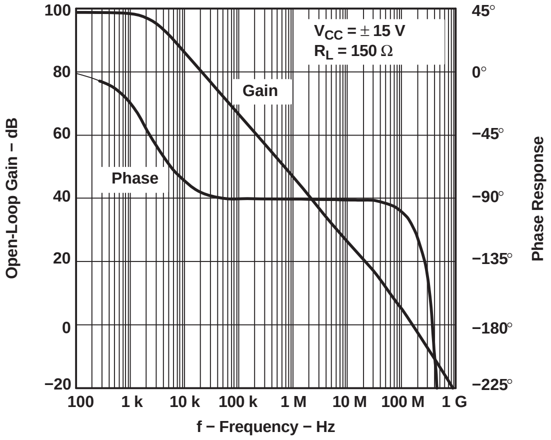


Figure 11. Open-Loop Gain and Phase Response

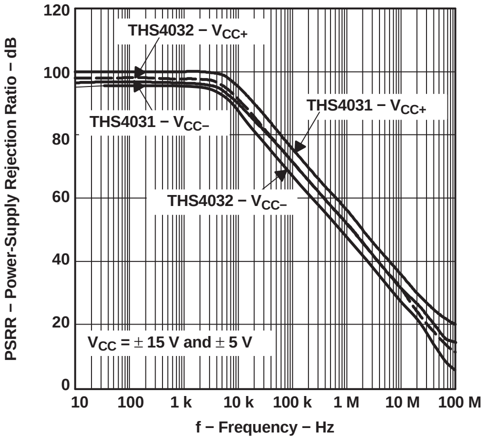


Figure 12. Power-Supply Rejection Ratio vs Frequency

Typical Characteristics (continued)

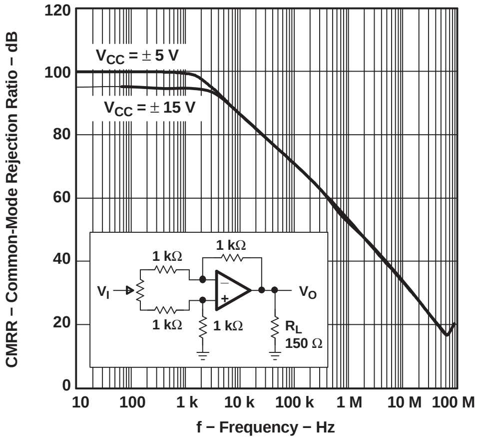


Figure 13. Common-Mode Rejection Ratio vs Frequency

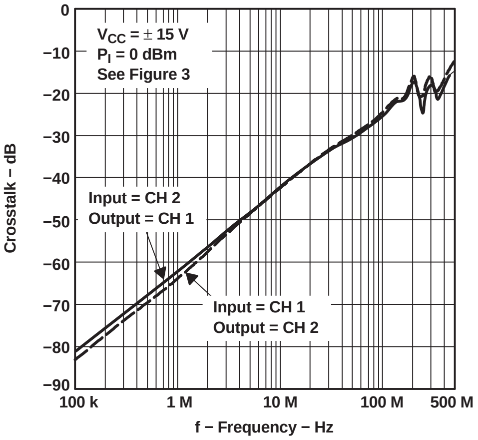


Figure 14. THS4032 Crosstalk vs Frequency

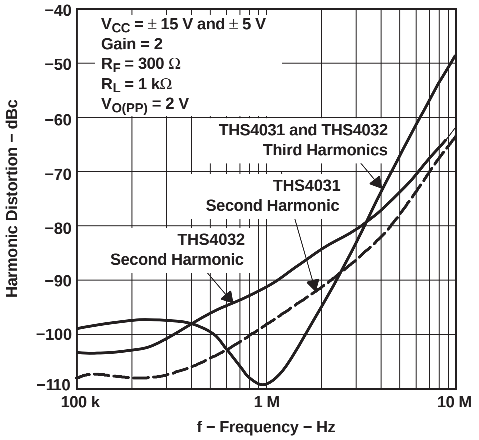


Figure 15. Harmonic Distortion vs Frequency

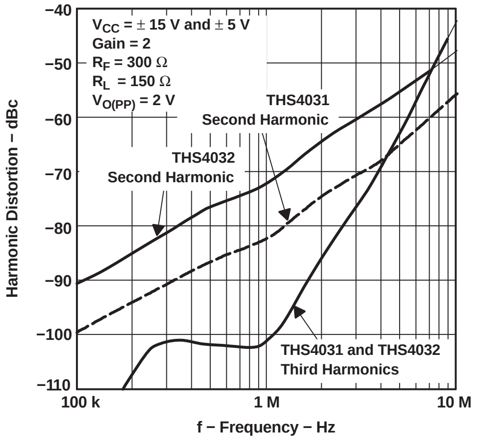


Figure 16. Harmonic Distortion vs Frequency

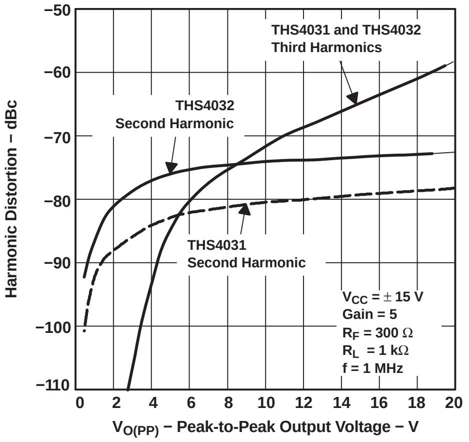


Figure 17. Harmonic Distortion vs Peak-to-Peak Output Voltage

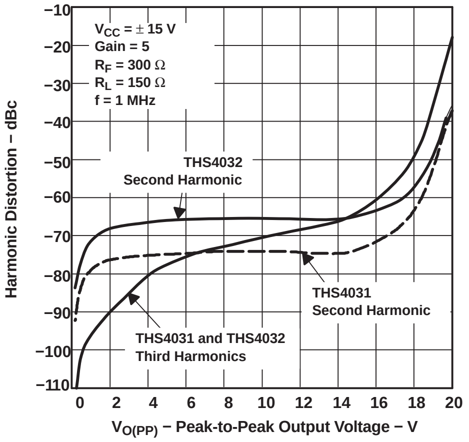


Figure 18. Harmonic Distortion vs Peak-to-Peak Output Voltage

Typical Characteristics (continued)

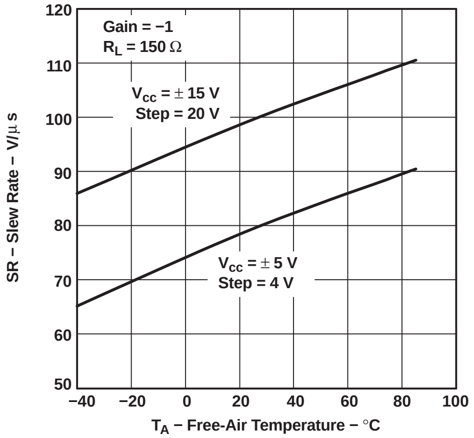


Figure 19. Slew Rate vs Free-Air temperature

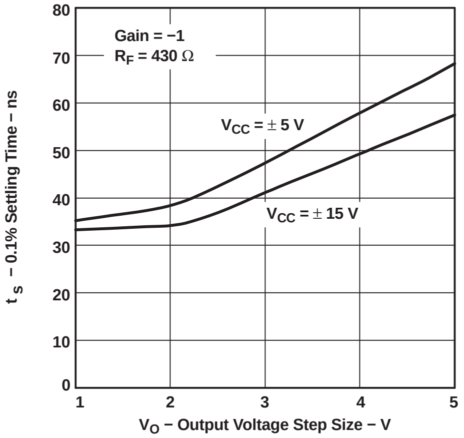


Figure 20. 0.1% Settling Time vs Output Voltage Step Size

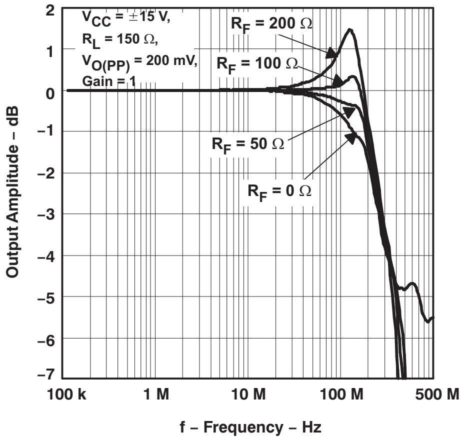


Figure 21. Small Signal Frequency Response With Varying Feedback Resistance

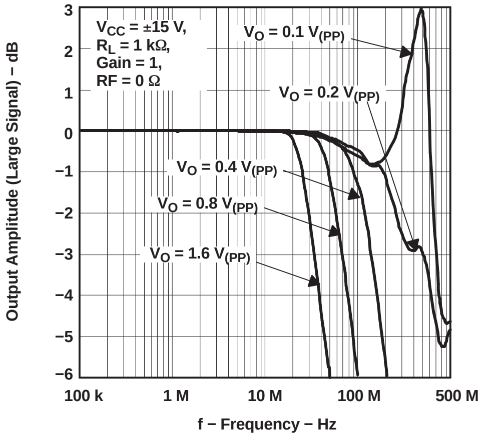


Figure 22. Frequency Response With Varying Output Voltage Swing

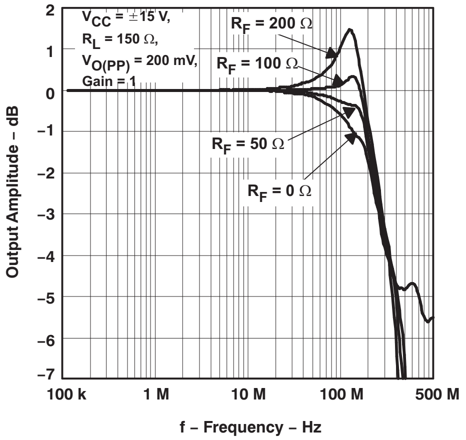


Figure 23. Small Signal Frequency Response With Varying Feedback Resistance

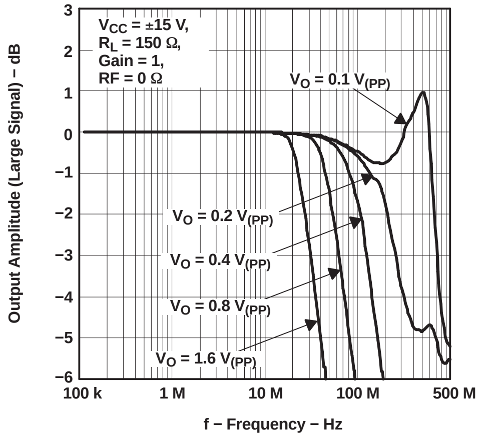


Figure 24. Frequency Response With Varying Output Voltage Swing

Typical Characteristics (continued)

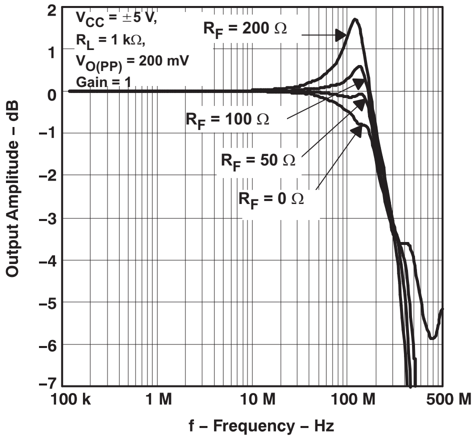


Figure 25. Small Signal Frequency Response With Varying Feedback Resistance

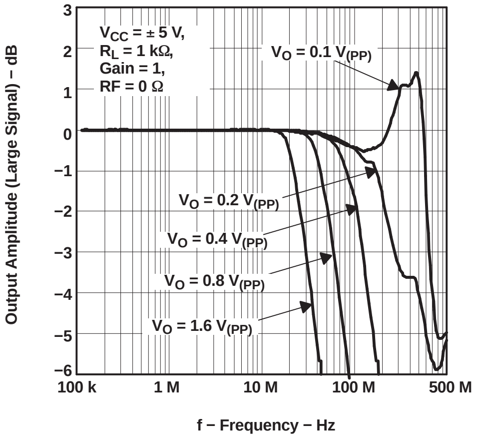


Figure 26. Frequency Response With Varying Output Voltage Swing

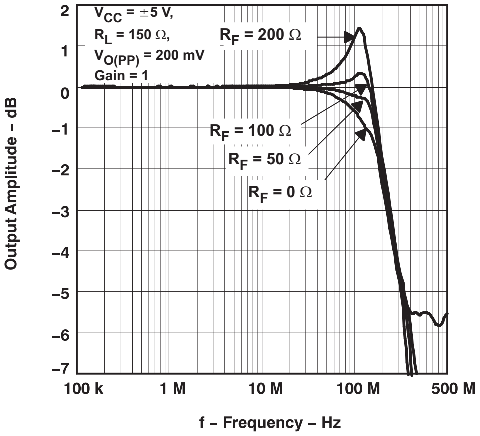


Figure 27. Small Signal Frequency Response With Varying Feedback Resistance

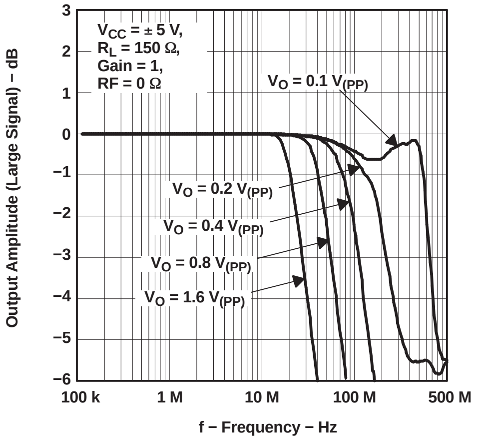


Figure 28. Frequency Response With Varying Output Voltage Swing

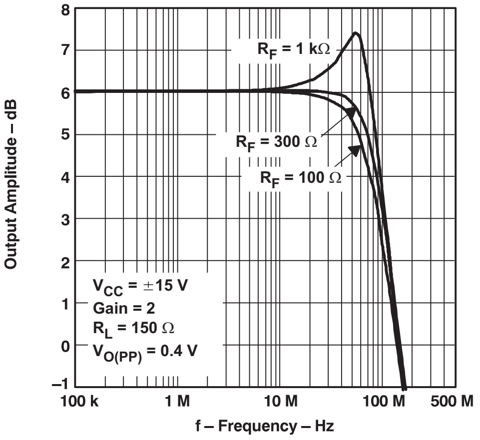


Figure 29. Small-Signal Frequency Response With Varying Feedback Resistance

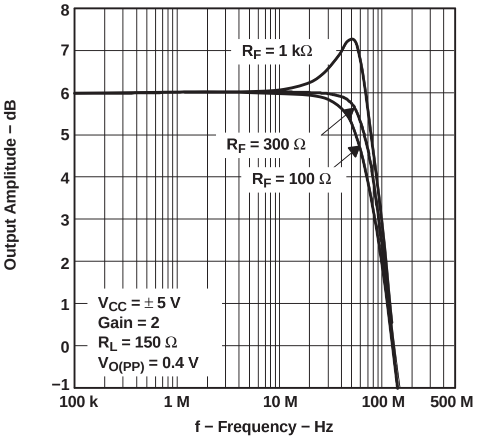


Figure 30. Small-Signal Frequency Response With Varying Feedback Resistance

Typical Characteristics (continued)

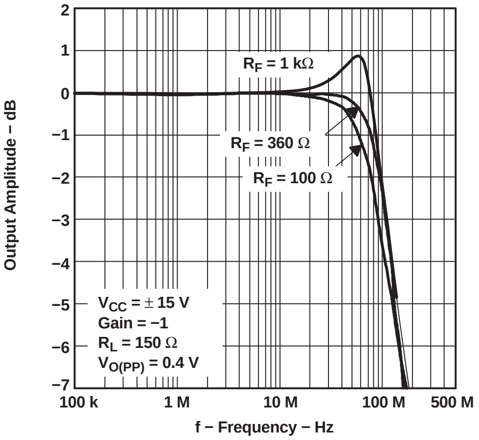


Figure 31. Small-Signal Frequency Response With Varying Feedback Resistance

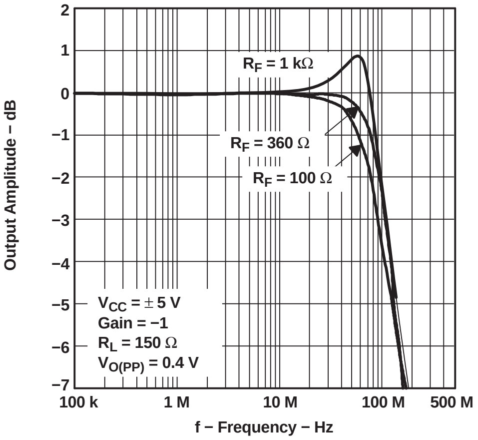


Figure 32. Small-Signal Frequency Response With Varying Feedback Resistance

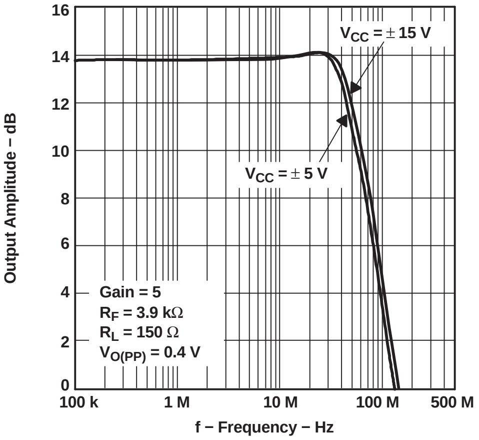


Figure 33. Small-Signal Frequency Response

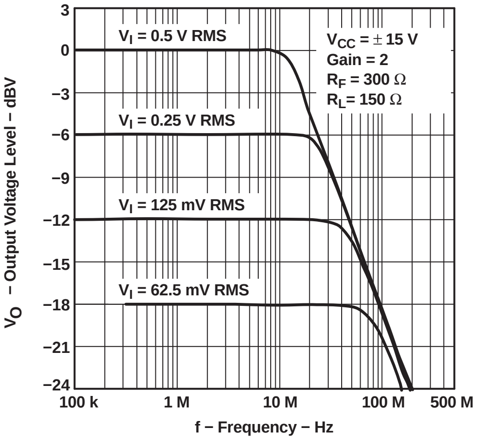


Figure 34. Output Amplitude vs Frequency

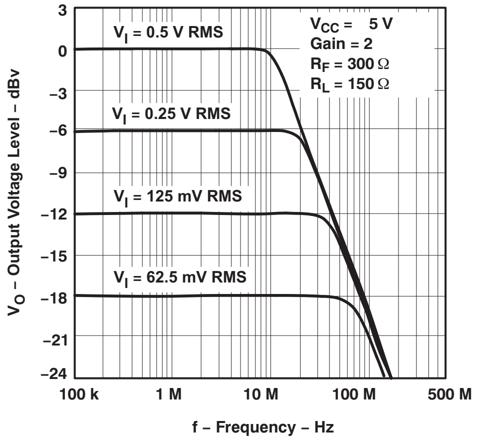


Figure 35. Output Amplitude vs Frequency

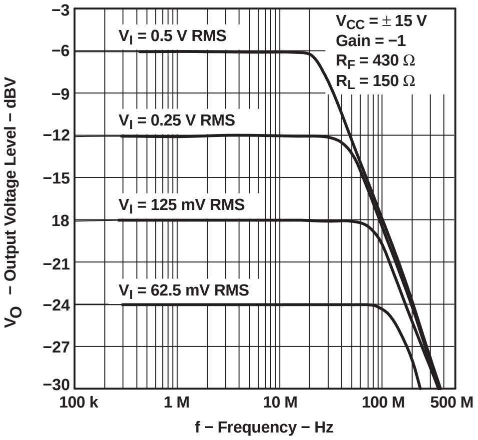


Figure 36. Output Amplitude vs Frequency

Typical Characteristics (continued)

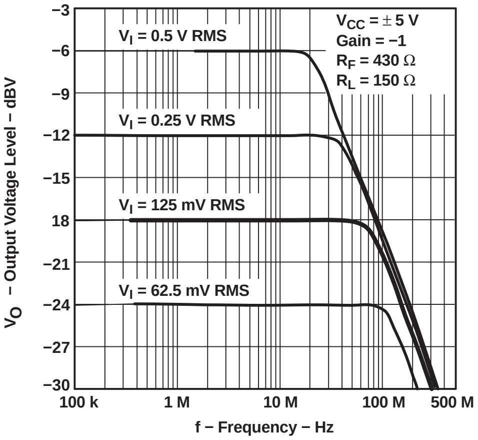


Figure 37. Output Amplitude vs Frequency

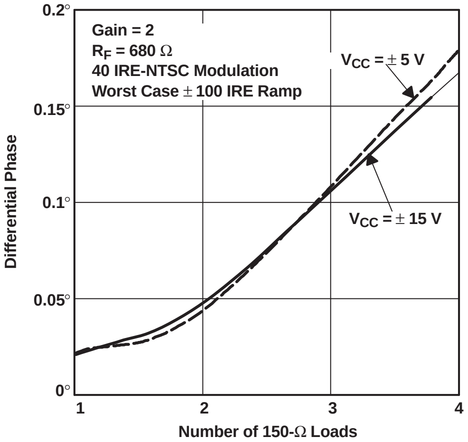


Figure 38. Differential Phase vs Number of 150-Ω Loads

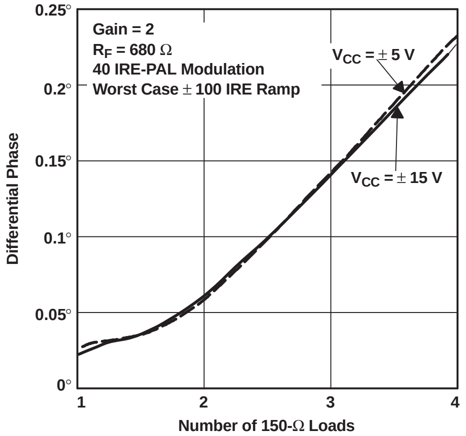


Figure 39. Differential Phase vs Number of 150-Ω Loads

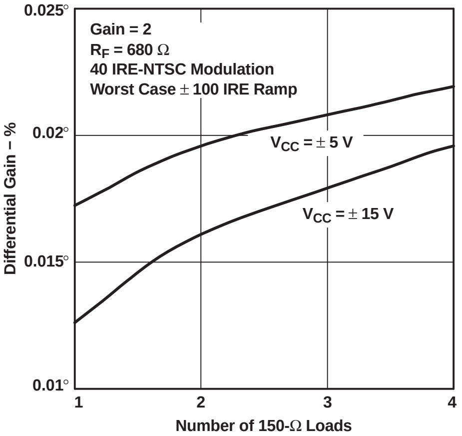


Figure 40. Differential Gain vs Number of 150-Ω Loads

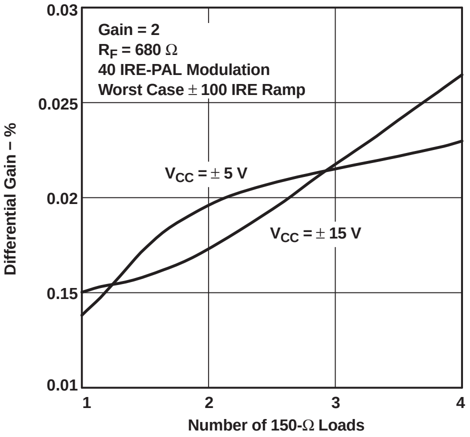


Figure 41. Differential Gain vs Number of 150-Ω Loads

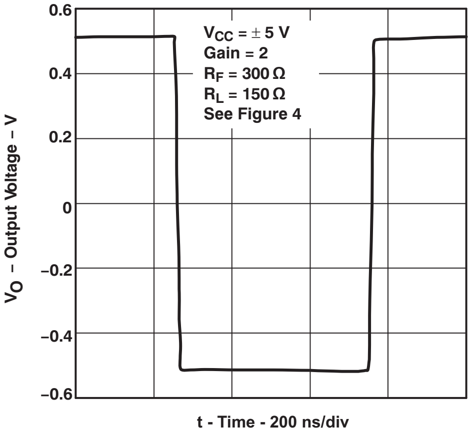


Figure 42. 1-V Step Response

Typical Characteristics (continued)

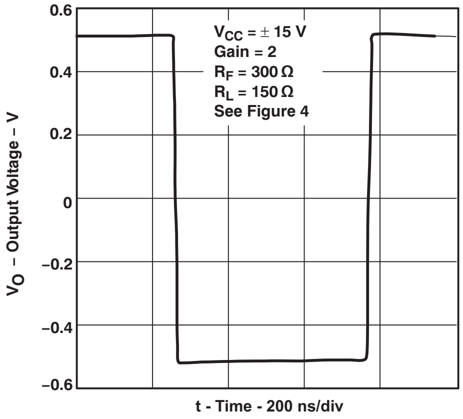


Figure 43. 1-V Step Response

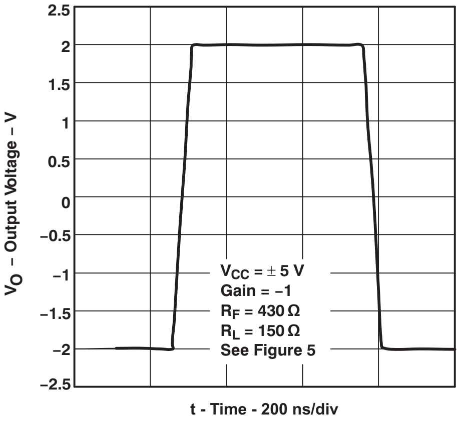


Figure 44. 4-V Step Response

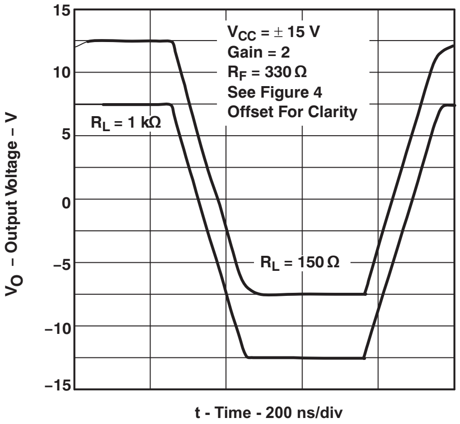


Figure 45. 20-V Step Response

7 Parameter Measurement Information

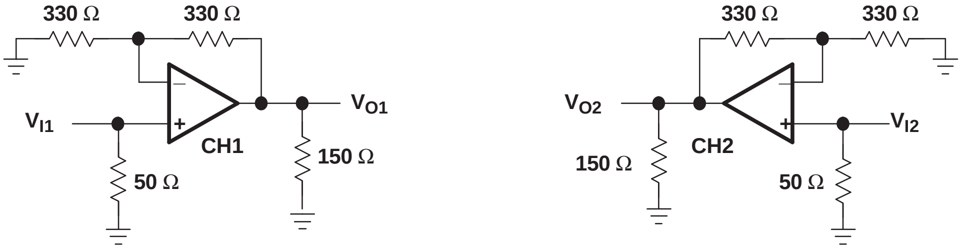


Figure 46. THS4032 Crosstalk Test Circuit

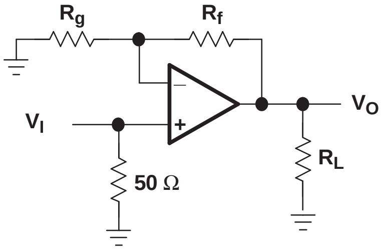


Figure 47. Step Response Test Circuit

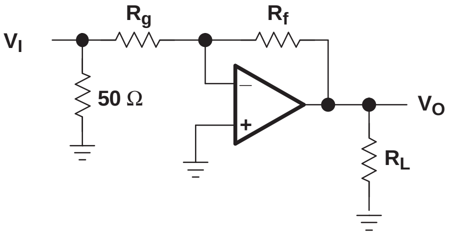


Figure 48. Step Response Test Circuit

8 Detailed Description

8.1 Overview

The THS403x is a high-speed operational amplifier configured in a voltage feedback architecture. The family is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors that possess f_Ts of several GHz. This results in an exceptionally high-performance amplifier that features wide bandwidth, high slew rate, fast settling time, and low distortion. Figure 49 shows a simplified schematic.

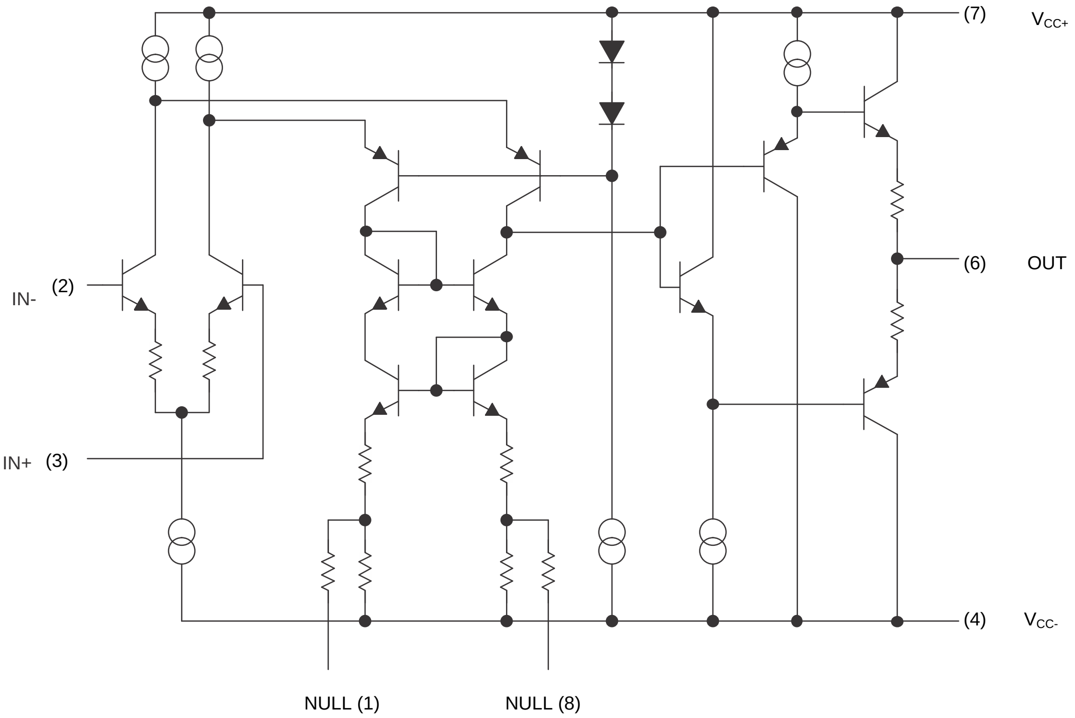
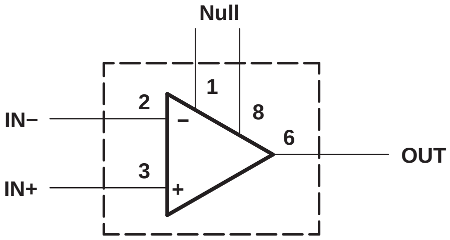
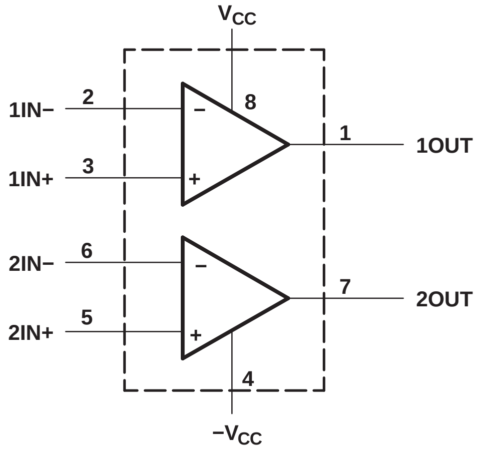


Figure 49. THS4031 Simplified Schematic

8.2 Functional Block Diagrams



Functional Block Diagrams (continued)



8.3 Feature Description

8.3.1 Noise Calculations and Noise Figure

Noise can cause errors on small signals. This is especially true when amplifying small signals. The noise model for the THS403x (shown in Figure 50) includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise ($\text{nV}/\sqrt{\text{Hz}}$)
- IN+ = Noninverting current noise ($\text{pA}/\sqrt{\text{Hz}}$)
- IN– = Inverting current noise ($\text{pA}/\sqrt{\text{Hz}}$)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

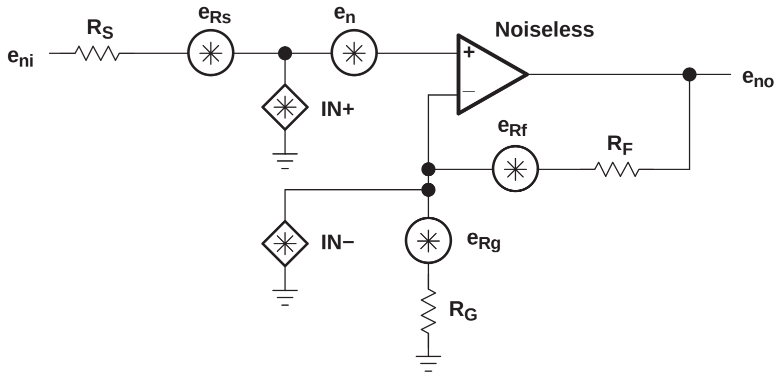


Figure 50. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using Equation 1:

$$e_{ni} = \sqrt{\left(e_n\right)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4kTR_s + 4kT\left(R_F \parallel R_G\right)}$$

where:

- k = Boltzmann's constant = 1.380658×10^{-23}
- T = Temperature in degrees Kelvin (273+°C)
- $R_F \parallel R_G$ = Parallel resistance of R_F and R_G (1)

To calculate the equivalent output noise of the amplifier, multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V) in Equation 2.

Feature Description (continued)

$$e_{no} = e_{ni} A_V = e_{ni} \left(1 + \frac{R_F}{R_G}\right) \left(\text{Noninverting Case}\right) \tag{2}$$

As the previous equations show, to keep noise at a minimum, use resistors with a small value. As the closed-loop gain increases (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. As a result, the general conclusion is that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This advantage can simplify the formula and noise calculations.

For more information on noise analysis, see the *Noise Analysis for High-Speed Op Amps* application note.

8.3.2 Optimizing Frequency Response

Internal frequency compensation of the THS403x was selected to provide very wide bandwidth performance and still maintain a very low noise floor. To meet these performance requirements, the THS403x must have a minimum gain of 2 (–1). Because everything is referred to the noninverting pin of an operational amplifier, the noise gain in a G = –1 configuration is the same as a G = 2 configuration.

One of the keys to maintaining a smooth frequency response, and and as a result, a stable pulse response, is to pay particular attention to the inverting pin. Any stray capacitance at this node causes peaking in the frequency response (see Figure 51 and Figure 52). There are two techniques to minimize this effect. The first is to remove any ground planes under the inverting pin of the amplifier, including the trace that connects to this terminal. Additionally, the length of this trace must be minimized. The capacitance at this node causes a lag in the voltage feedback due to the charging and discharging of the stray capacitance. If this lag becomes too long, the amplifier is unable to correctly keep the noninverting pin voltage at the same potential as the voltage of the inverting pin. Peaking and possible oscillations can occur if this happens.

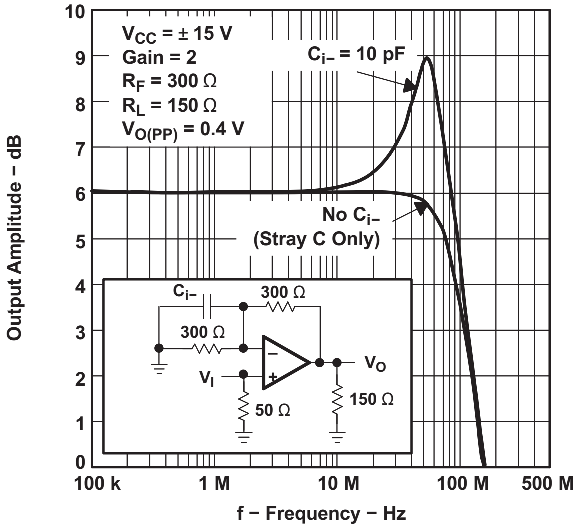


Figure 51. Output Amplitude vs Frequency

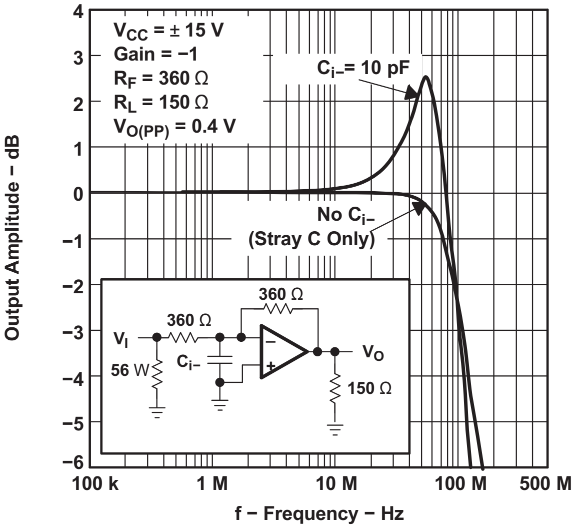


Figure 52. Output Amplitude vs Frequency

The second precaution to help maintain a smooth frequency response is to keep the feedback resistor (R_f) and the gain resistor (R_g) values low. These two resistors are in parallel when looking at the AC small-signal response. But, as Figure 21 through Figure 32 show, an insufficient value reduces the bandwidth of the amplifier. Table 2 shows some recommended feedback resistors to use with the THS403x.

Table 2. Recommended Feedback Resistors

GAIN	R_f FOR V_{CC} = ±15 V AND ±5 V
1	50 Ω
2	300 Ω
–1	360 Ω
5	3.3 kΩ (low stray-c PCB only)

8.3.3 Driving a Capacitive Load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS403x is internally compensated to maximize the bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the phase margin of the device, which results in high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, TI recommends placing a resistor in series with the output of the amplifier, as Figure 53 shows. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω isolates any capacitance loading and provides the proper line impedance matching at the source end.

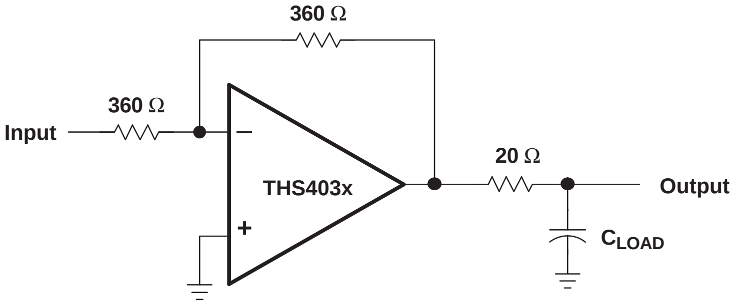
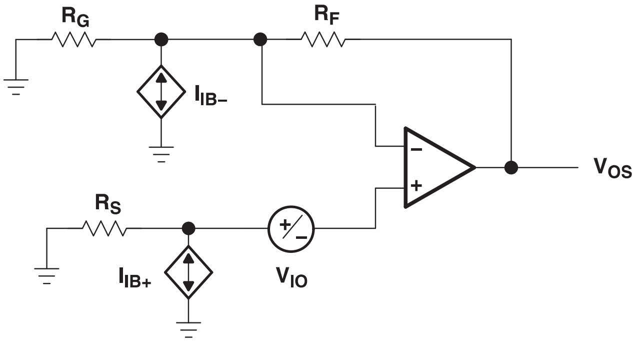


Figure 53. Driving a Capacitive Load

8.3.4 Offset Voltage

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. Figure 54 shows a schematic and formula that can be used to calculate the output offset voltage:

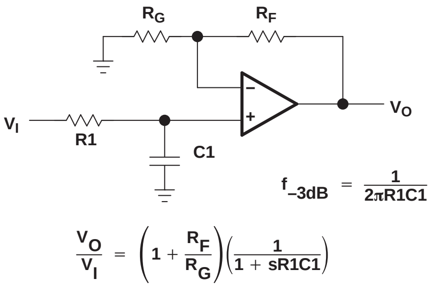


$$V_{OS} = \left(\pm V_{IO} \pm I_{IB+} R_S\right)\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} R_F$$

Figure 54. Output Offset Voltage Model

8.3.5 General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting pin of the amplifier (see Figure 55).

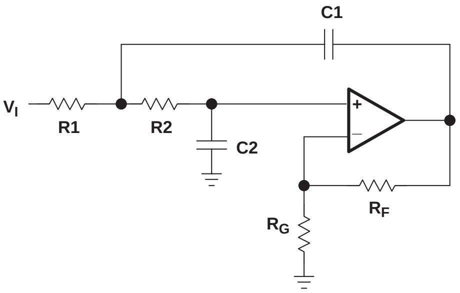


$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 55. Single-Pole Low-Pass Filter

If even more attenuation is required, a multiple-pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier must have a bandwidth that is eight to 10 times the filter frequency bandwidth. Otherwise, phase shift of the amplifier can occur.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 56. Two-Pole Low-Pass Sallen-Key Filter

8.4 Device Functional Modes

8.4.1 Offset Nulling

The THS403x has low input offset voltage for a high-speed amplifier. However, if additional correction is required, the designer can use an offset nulling function provided on the THS4031. By placing a potentiometer between pins 1 and 8 of the device and tying the wiper to the negative supply, the input offset can be adjusted. This is shown in Figure 57.

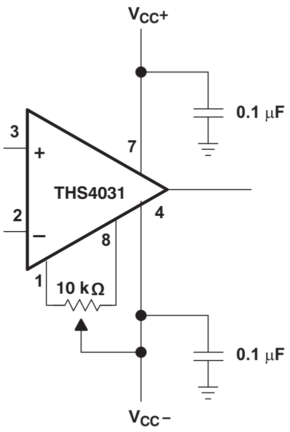


Figure 57. Offset Nulling Schematic

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This application report is intended as a guide for using an analog multiplexer to multiplex several input signals to a high-performance driver amplifier which subsequently drives a single high-resolution, high-speed SAR analog-to-digital converter (ADC). This example uses the ADS8411 and the TS5A3159 or TS5A3359 as the ADC and the multiplexer, respectively. This application uses the THS4031 as the operational amplifier.

9.2 Typical Application

As Figure 58 shows, the evaluation system consists of the ADC (ADS8411), a driving operational amplifier (THS4031), the multiplexer (TS5A3159), an AC source, a DC source, and two driving operational amplifiers (two THS4031s or a single THS4032) for the sources to make them a low-impedance source, a passive band-pass filter after the AC source to filter the source noise and distortion.

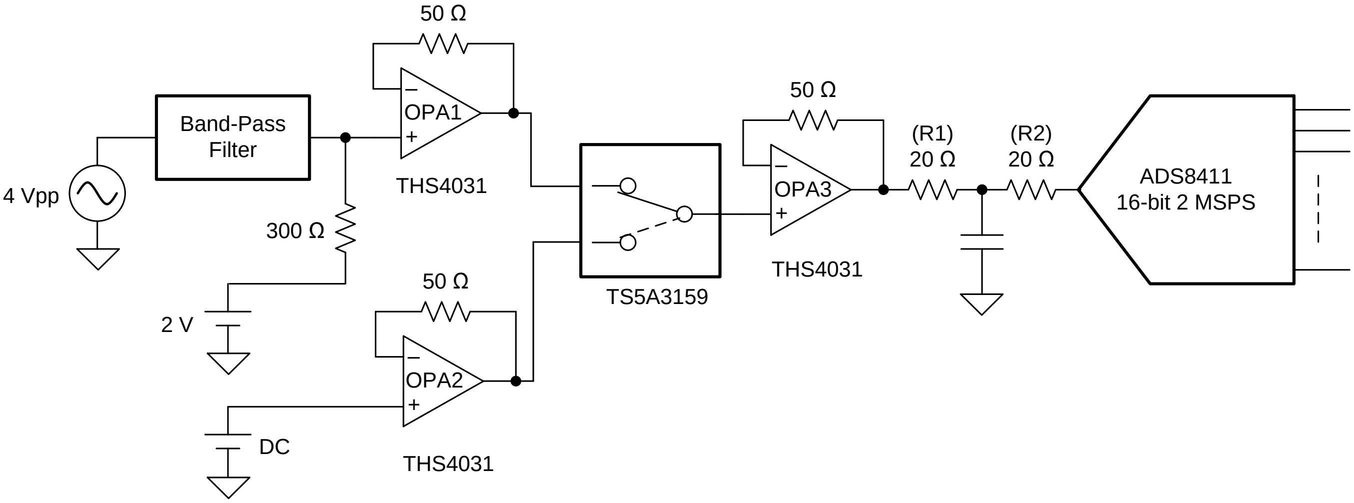


Figure 58. Evaluation Set Up

9.2.1 Design Requirements

Design a multiplexed digitizer system with the dynamic performance as Table 3 lists:

Table 3. Design Specifications

DEVICE SPEED (MSPS)	INPUT FREQUENCY (kHz)	SNR (dB)	THD (dB)	CROSSTALK (dB)
2	20	> 84	< –90	< –110
2	100	> 84	< –90	< –96

9.2.2 Detailed Design Procedure

The ADS8411 is a 16-bit, 2-MSPS analog-to-digital converter (ADC) with a 4-V reference. The device includes a 16-bit capacitor-based SAR ADC with inherent sample and hold. It has a unipolar single-ended input. The device offers a 16-bit parallel interface.

The TS5A3159 is a single-pole, double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON state resistance and an excellent ON resistance matching with the break-before-make feature to prevent signal distortion during the transfer of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes low power. The TS5A3359 is a single-pole, triple-throw (SP3T) version of the same switch.

9.2.2.1 Selection of Multiplexer

Figure 59 shows an equivalent circuit diagram of one of the channels of a multiplexer. C_S is the input capacitance of the channel; C_D is the output capacitance of the channel. R_{ON} is the resistance of the channel when the channel is ON. C_L and R_L are the load capacitance and resistance, respectively. V_{IN} is the input voltage of the source. R_S is the source resistance of the source. V_{OUT} is the output voltage of the multiplexer.

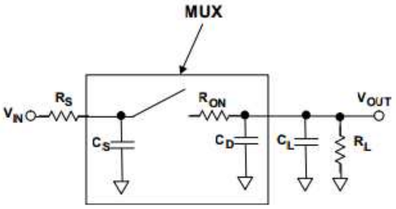


Figure 59. Multiplexer Equivalent Circuit

To improve settling time, the values of R_S, R_{ON}, C_S, C_D, and C_L must be smaller, and the value of R_L must be large.

For TS5A3159:

- $R_S = 1\ \Omega$
- $C_S = C_D = 84$ pF

Considering

- $R_S = 50\ \Omega$
- $C_L = 5$ pF
- $R_L = 10\ k\Omega$
- T_{RC} (time constant) = 8.65 ns

For a 16-bit system, at least 18-bit settling is required. For 18-bit settling, the time required is $(18 \times \ln 2) \times T_{RC} = 108$ ns, which is better than 2 MSPS (500 ns). If the settling time is more than the conversion time of the ADC, the output of the multiplexer does not settle to the required accuracy which results in harmonic distortion.

One more important parameter of a multiplexer is the ON-state resistance variation with voltage. This also affects distortion because R_{ON} and R_L act like a resistor divider circuit and any variation of R_{ON} with voltage affects the output voltage.

9.2.2.2 Signal Source

The input signal source must be a low-noise, low-distortion source with low source resistance. As discussed in the earlier section, RS must be low to improve settling time. If the source is not a low-noise and low-distortion source, a passive band-pass filter can be added to improve the signal quality as shown in Figure 58.

9.2.2.3 Driving Amplifier

The driving operational amplifier (OPA3 in Figure 58) in this application must have good slew rate, bandwidth, low noise, and distortion. The input of the operational amplifier can result in a maximum step of 4 V because of MUX switching. As a result, even if the signal bandwidth is low, the driving amplifier must settle from 0 V to 4 V (or 4 V to 0 V) within one ADC sampling frame. When selecting the operational amplifier, one must ensure that the amplifier settles from 0 V to 4 V (or from 4 V to 0 V) within the ADC sampling time (in this case 500 ns). The amplifier used for driving the ADC is the THS4031. The operational amplifiers (OPA1, OPA2 in Figure 58) used before the MUX is for signal conditioning. These operational amplifiers must have low noise and distortion.

9.2.2.4 Driving Amplifier Bandwidth Restriction

The restriction of bandwidth by an RC filter (after OPA3 in Figure 58) may result in better SNR and THD, but the restriction makes the operational amplifier difficult to settle within the required accuracy. If the output does not settle properly, some residual charge of the previous channel remains in the next sampling and appears as a crosstalk. If the throughput of the ADC is reduced, allowing the output of the operational amplifier to settle properly, the problem becomes smaller. Therefore, using a larger capacitor slows down the settling of the operational amplifier output. Within the ADC sampling frame, the operational amplifier output does not settle to the final level. Figure 60 and Figure 61 show SNR and crosstalk as a function of the filter capacitor.

Figure 62 shows input settling behavior with three different bandwidths. The value of the capacitor changes to change the bandwidth. As the bandwidth increases, the settling time improves (see Equation 3).

$$Bandwidth \cong \frac{1}{2\pi R_1 C_1} \tag{3}$$

9.2.3 Application Curves

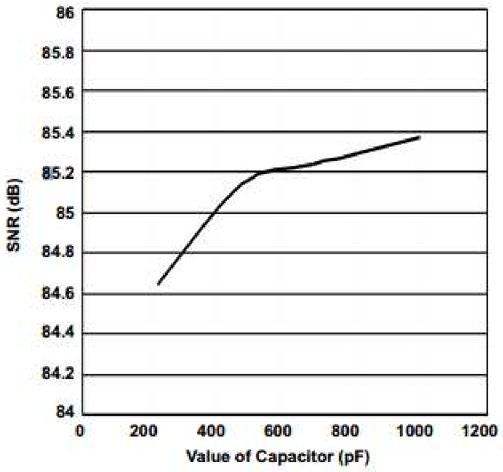


Figure 60. SNR vs Input Bandwidth

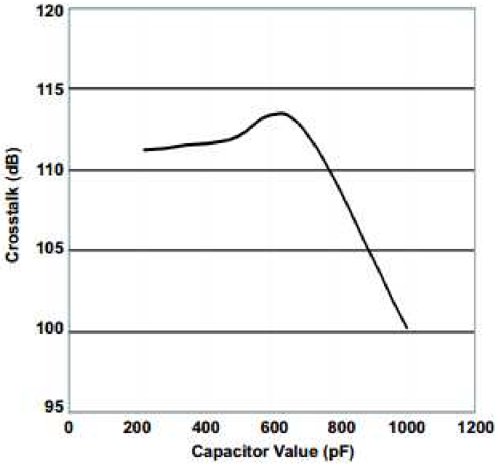


Figure 61. Crosstalk vs Input Bandwidth

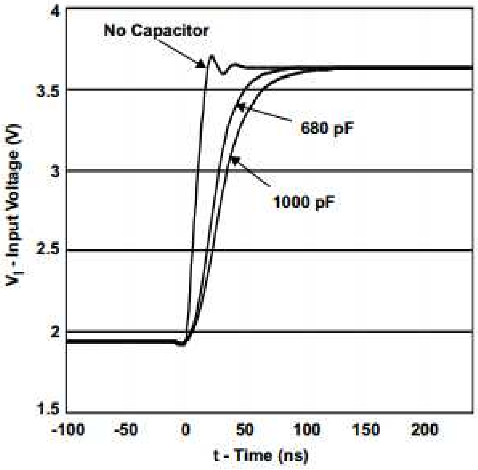


Figure 62. Input Settings With Different Values of Capacitors

10 Power Supply Recommendations

The THS4031 can operate off a single supply or with dual supplies if the input CM voltage range (CMIR) contains the required headroom to either supply rail. Operating from a single supply can have numerous advantages. With the negative supply at ground, the DC errors due to the –PSRR term are minimized. Supplies must be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. TI recommends using a ground plane. In most high-speed devices, removing the ground plane close to device sensitive pins (such as the inputs) is advisable. An optional supply decoupling capacitor across the two power supplies (for split-supply operation) improves second harmonic distortion performance.

11 Layout

11.1 Layout Guidelines

In order to achieve the levels of high-frequency performance of the THS403x, it is essential that proper printed-circuit board (PCB) high-frequency design techniques be followed. A general set of guidelines is shown below. In addition, a THS403x evaluation board is available to use as a guide for layout or for evaluating the performance of the device.

- Ground planes: TI highly recommends using a ground plane on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power-supply decoupling: Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor must always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor must be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer must strive for distances of less than 0.1 inch between the device power pins and the ceramic capacitors.
- Sockets: TI does not recommend sockets for high-speed operational amplifiers. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs andcompact part placements: Optimum high-frequency performance is achieved when stray series inductance is minimized. To realize this, the circuit layout must be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention must be paid to the inverting input of the amplifier. The length must be kept as short as possible. This helps minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components: TI recommends using surface-mount passive components for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing stray inductance and capacitance. If leaded components are used, TI recommends that the lead lengths are kept as short as possible.

11.2 Layout Example

An evaluation board is available for the THS4031 and THS4032. This board is configured for very low parasitic capacitance to realize the full performance of the amplifier. Figure 63 shows the a schematic of the evaluation board. The circuitry is designed so that the amplifier can be used in an inverting or noninverting configuration. For more information, see *THS4031 EVM User's Guide* or the *THS4032 EVM User's Guide*. To order the evaluation board, contact your local TI sales office or distributor.

Layout Example (continued)

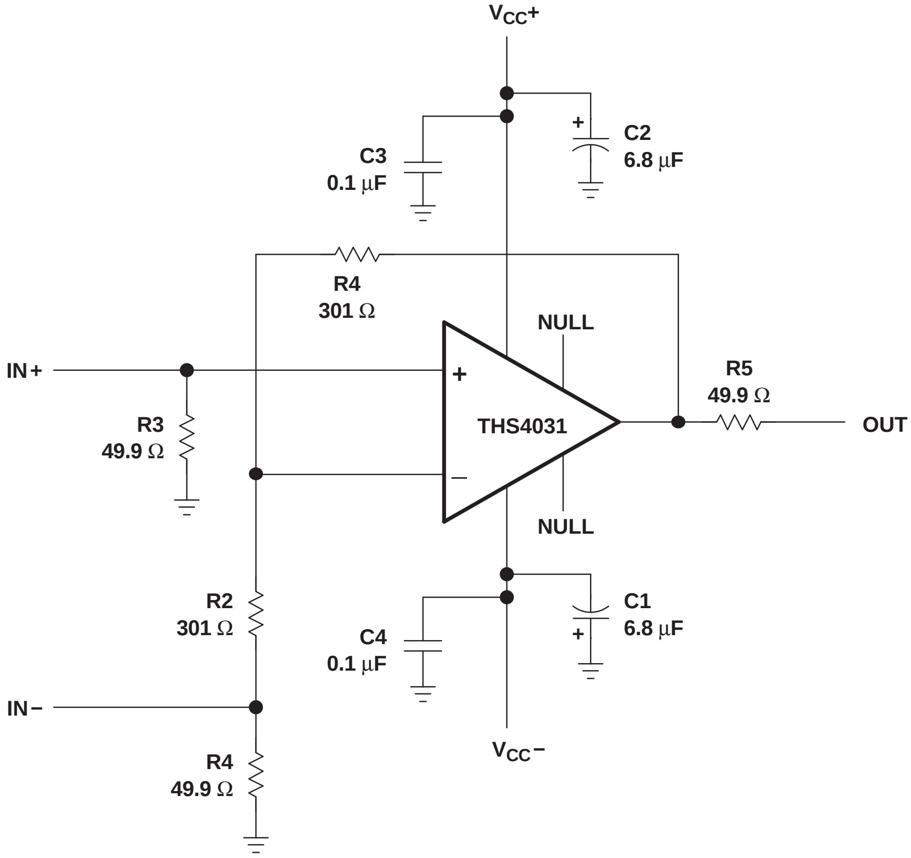


Figure 63. THS4031 Evaluation Board

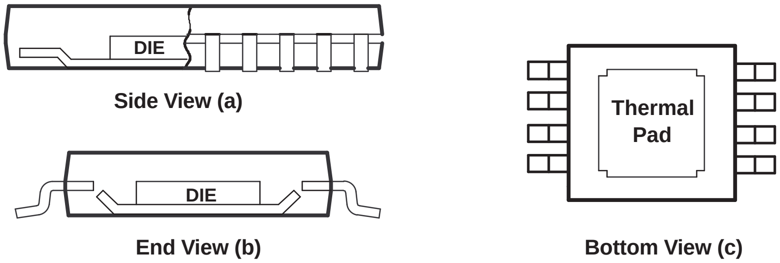
11.3 General PowerPAD™ Design Considerations

The THS403x is available in a thermally-enhanced DGN package, which is a member of the PowerPAD™ family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 64(a) and Figure 64(b)]. This arrangement results in the leadframe exposed as a thermal pad on the underside of the package [see Figure 64(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD™ package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into a ground plane or other heat-dissipating device.

The PowerPAD™ package represents a breakthrough in combining the small area and ease of assembly of surface mount with the heretofore awkward mechanical methods of heat sinking.

General PowerPAD™ Design Considerations (continued)



A. The thermal pad is electrically isolated from all pins in the package.

Figure 64. Views of Thermally-Enhanced DGN Package

Although there are many ways to properly heat sink this device, the following steps show the recommended approach.

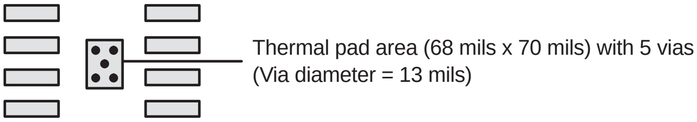


Figure 65. PowerPAD™ PCB Etch and Via Pattern

1. Prepare the PCB with a top-side etch pattern as shown in Figure 65. There must be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes must be 13 mils (0.3302 mm) in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS403xDGN device. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal-resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS403xDGN package must connect to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask must leave the pins of the package and the thermal pad area with the five holes exposed. The bottom-side solder mask must cover the five holes of the thermal pad area, which prevents solder from pulling away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and to all the device pins.
8. With these preparatory steps in place, the THS403xDGN device is placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

The actual thermal performance achieved with the THS403xDGN in the PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches (7.62 cm × 7.62 cm), then the expected thermal coefficient, $R_{\theta JA}$, is approximately 58.4°C/W. For a given $R_{\theta JA}$, the maximum power dissipation is calculated by Equation 4:

$$P_D = \left(\frac{T_{MAX} - T_A}{R_{\theta JA}} \right)$$

where

General PowerPAD™ Design Considerations (continued)

- P_D = Maximum power dissipation of THS403x device (watts)
- T_{MAX} = Absolute maximum operating junction temperature (125°C)
- T_A = Free-ambient air temperature (°C)
- $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$
  - $R_{\theta JC}$ = Thermal coefficient from junction to case
  - $R_{\theta CA}$ = Thermal coefficient from case to ambient air (°C/W) (4)

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments technical brief *PowerPAD™ Thermally-Enhanced Package*. This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office (see *PowerPAD™ Thermally-Enhanced Package* when ordering).

The next thing to be considered is package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer must never forget about the quiescent heat generated within the device, especially multiamplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. When using V_{CC} = ±5 V, heat is generally not a problem, even with SOIC packages. When using V_{CC} = ±15 V, the SOIC package is severely limited in the amount of heat the package dissipates. The other key factor is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device must always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, $R_{\theta JA}$ decreases and the heat dissipation capability increases. For the dual amplifier package (THS4032), the sum of the RMS output currents and voltages must be used to choose the proper package.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For development support, see these related devices:

- *THS4051 70-MHz High-Speed Amplifier*
- *THS4052 70-MHz High-Speed Amplifier*
- *THS4081 175-MHz Low Power High-Speed Amplifier*
- *THS4082 175-MHz Low Power High-Speed Amplifier*
- *ADS8411 16-Bit, 2 MSPS ADC With P8/P16 Parallel Output, Internal Clock and Internal Reference*
- *TS5A3159 1-Ω SPDT Analog Switch*
- *TS5A3359 1-Ω SP3T Analog Switch 5-V/3.3-V Single-Channel 3:1 Multiplexer/Demultiplexer*
- *THS4031 Single Low-Noise Pre-Amp EVM Module*
- *THS4032 Dual Low-Noise Pre-Amp EVM Module*

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments,*Noise Analysis for High-Speed Op Amps*
- Texas Instruments,*PowerPAD™ Thermally-Enhanced Package*
- Texas Instruments,*THS4031 EVM User's Guide*
- Texas Instruments, *THS4032 EVM User's Guide*

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
THS4031	Click here	Click here	Click here	Click here	Click here
THS4032	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9959501Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9959501Q2A THS4031MFKB	Samples
5962-9959501QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9959501QPA THS4031M	Samples
THS4031CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4031C	Samples
THS4031CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM		ACM	Samples
THS4031CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM		ACM	Samples
THS4031CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4031C	Samples
THS4031ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4031I	Samples
THS4031IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4031I	Samples
THS4031IDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM		ACN	Samples
THS4031IDGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM		ACN	Samples
THS4031IDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM		ACN	Samples
THS4031IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4031I	Samples
THS4031MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9959501Q2A THS4031MFKB	Samples
THS4031MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	THS4031MJG	Samples
THS4031MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9959501QPA THS4031M	Samples
THS4032CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4032C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4032CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ABD	Samples
THS4032CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4032C	Samples
THS4032ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4032I	Samples
THS4032IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4032I	Samples
THS4032IDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ABG	Samples
THS4032IDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ABG	Samples
THS4032IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4032I	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF THS4031, THS4031M, THS4032 :

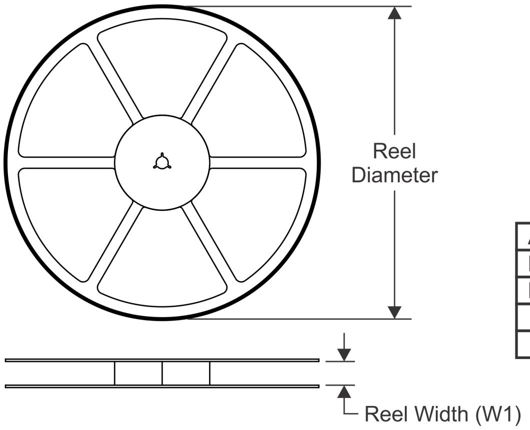
- Catalog: THS4031
- Enhanced Product: THS4032-EP
- Military: THS4031M

NOTE: Qualified Version Definitions:

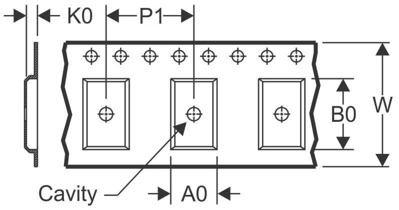
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

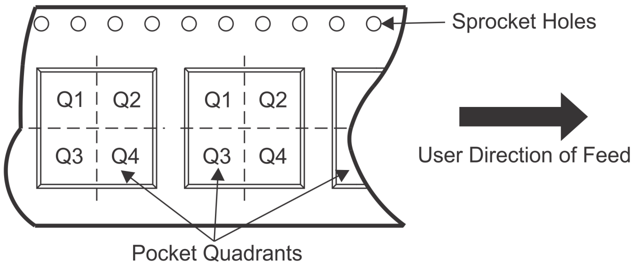


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

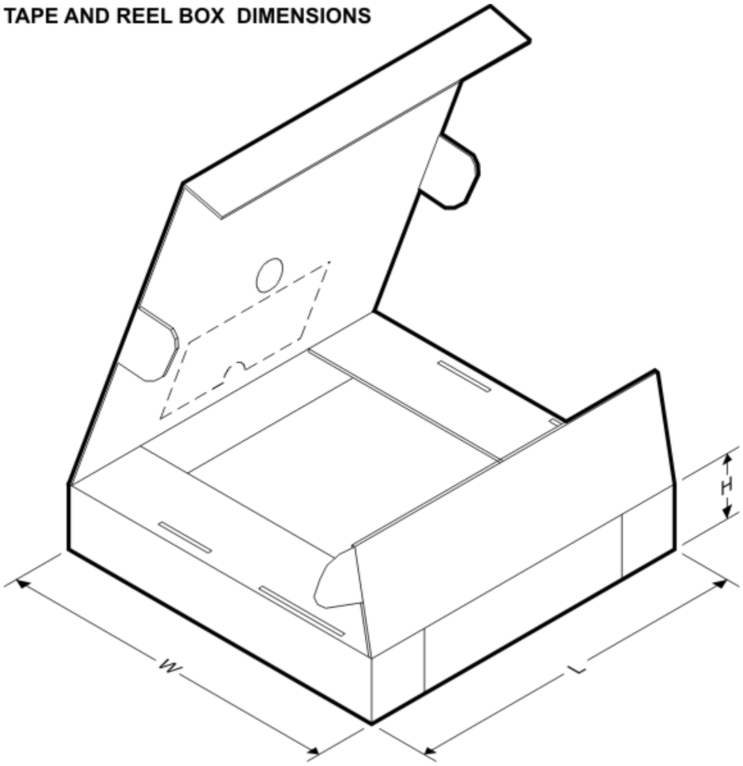
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4031CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4031CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4031IDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4031IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4032CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4032IDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4032IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

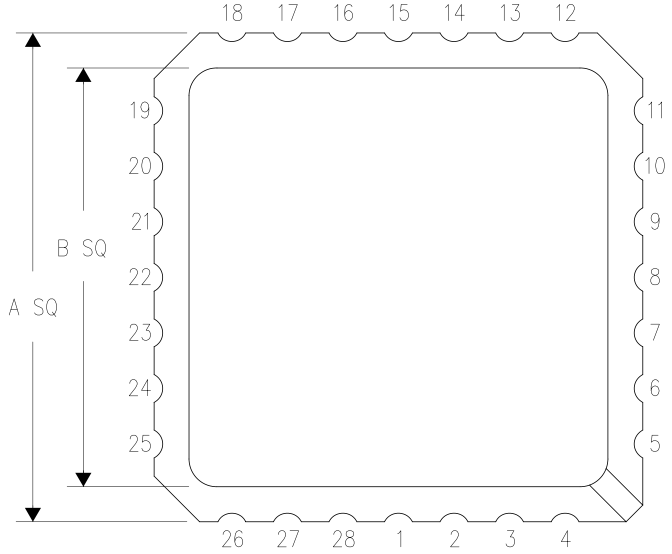


*All dimensions are nominal

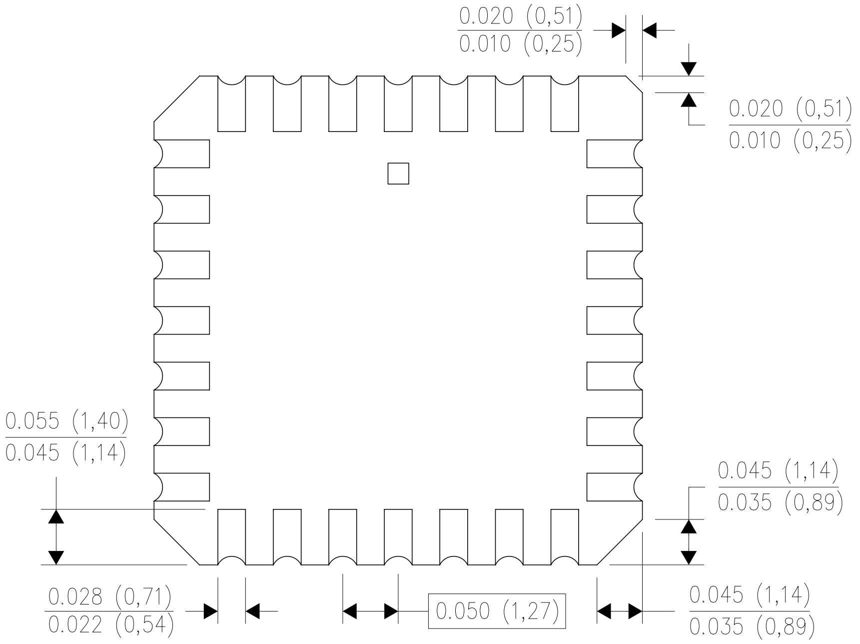
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4031CDGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
THS4031CDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4031IDGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
THS4031IDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4032CDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4032IDGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
THS4032IDR	SOIC	D	8	2500	350.0	350.0	43.0

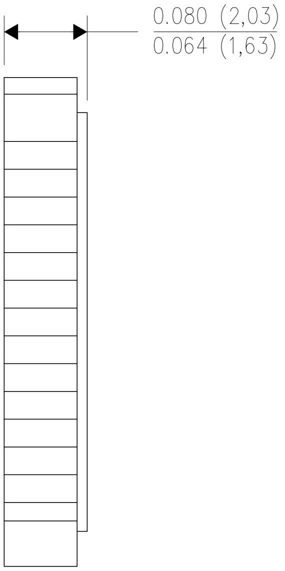
FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

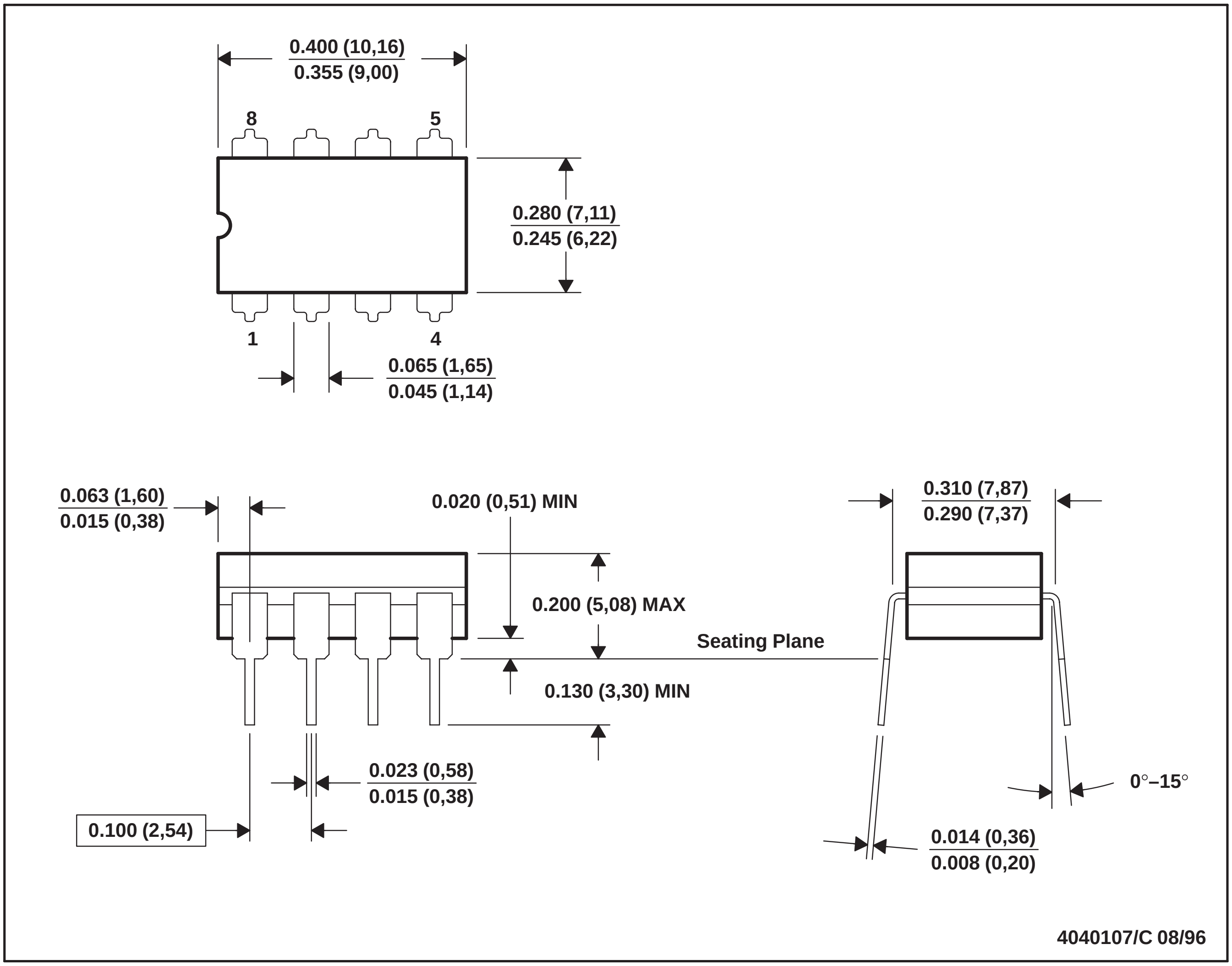




4040140/D 01/11

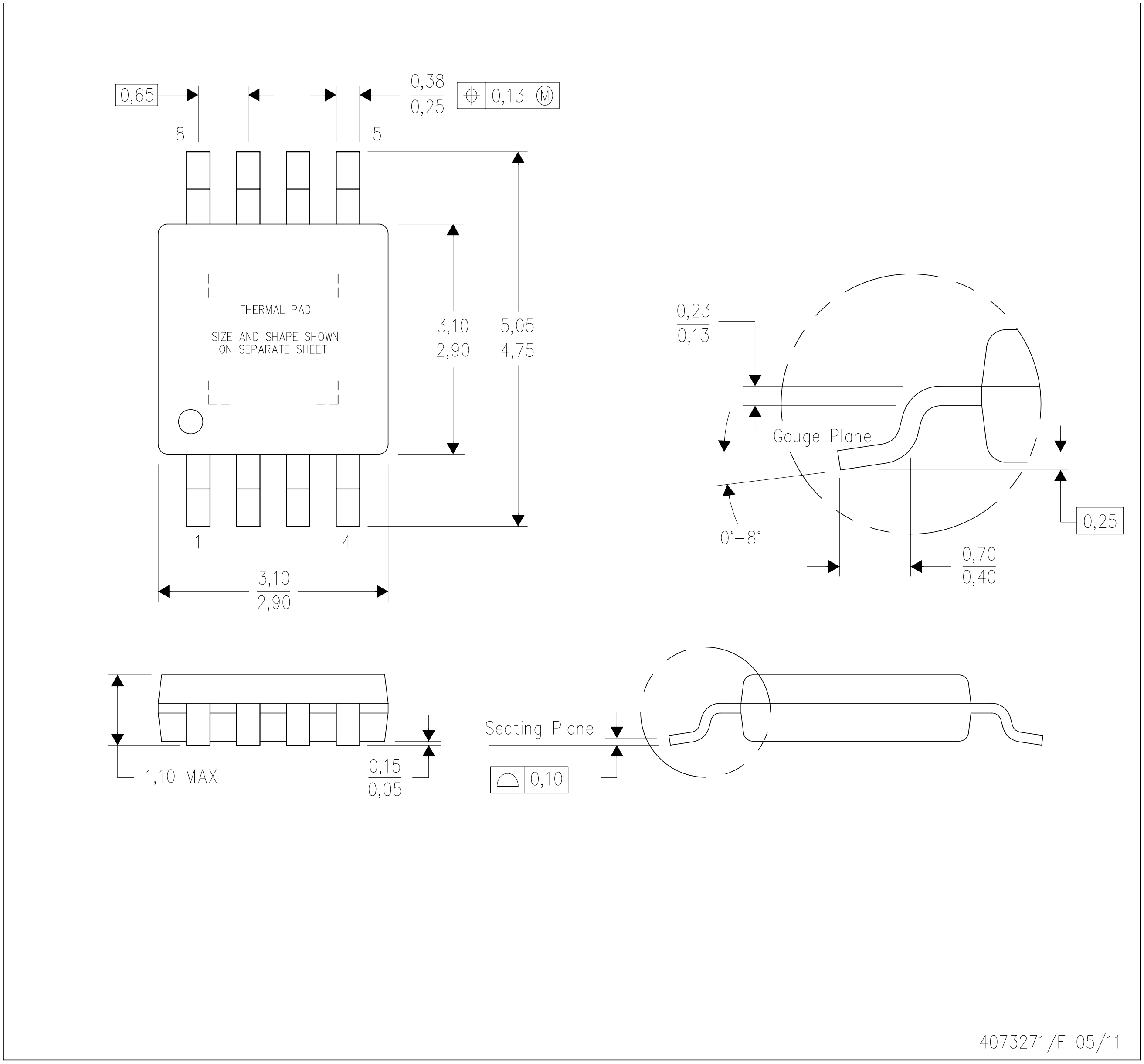
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

JG (R-GDIP-T8) CERAMIC DUAL-IN-LINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

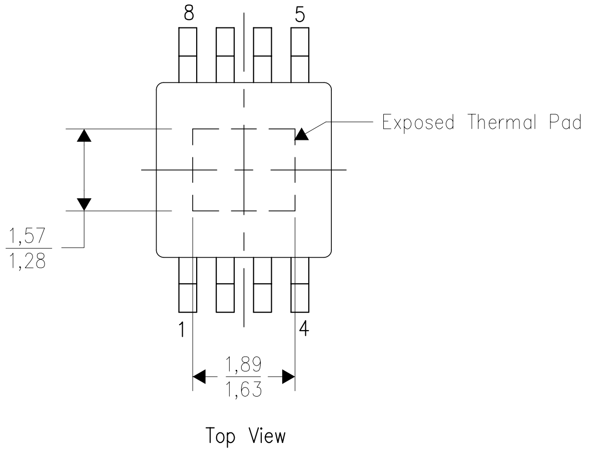
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

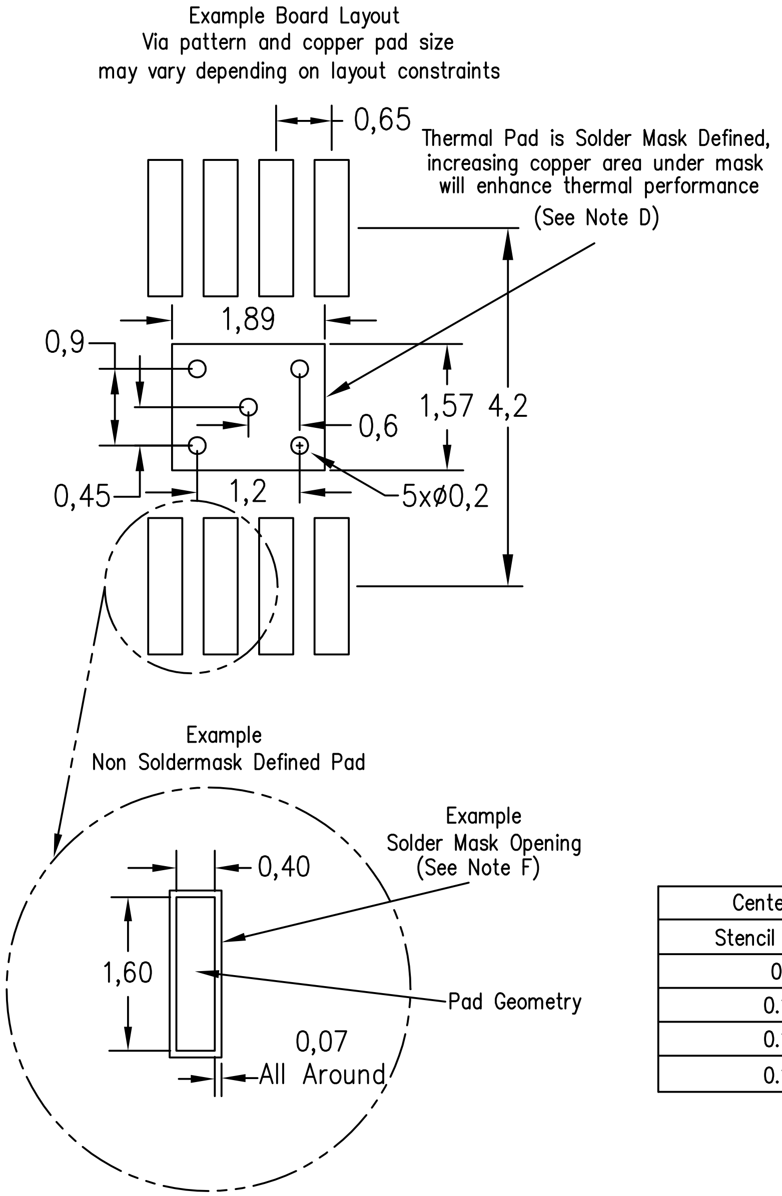
Exposed Thermal Pad Dimensions

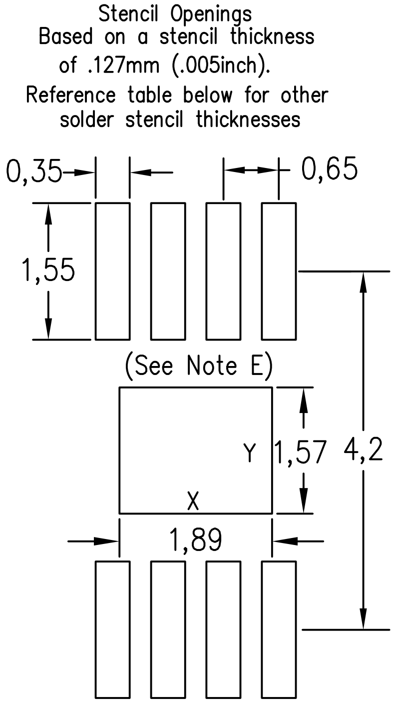
4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737-2/F 02/13

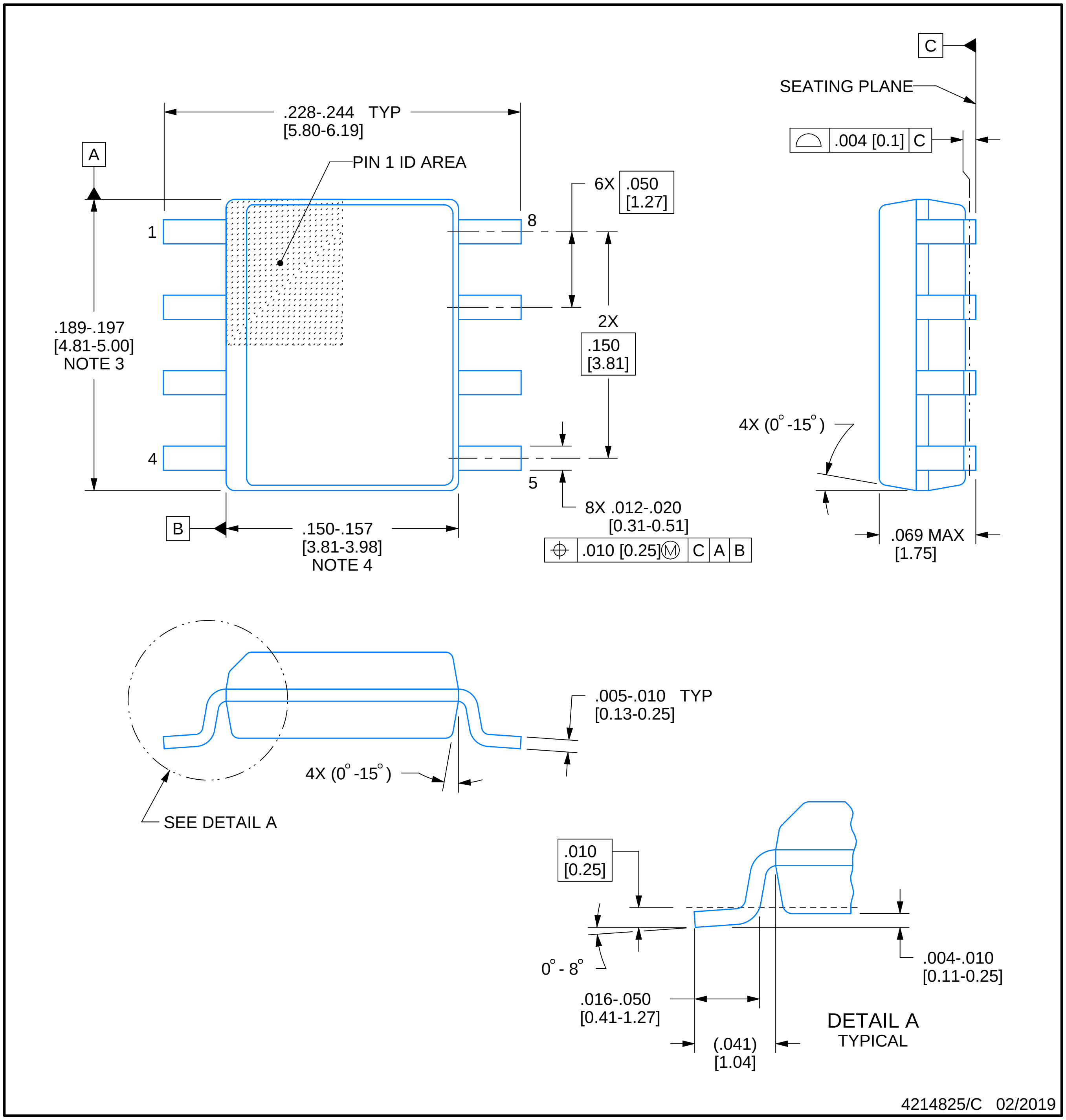
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

PACKAGE OUTLINE

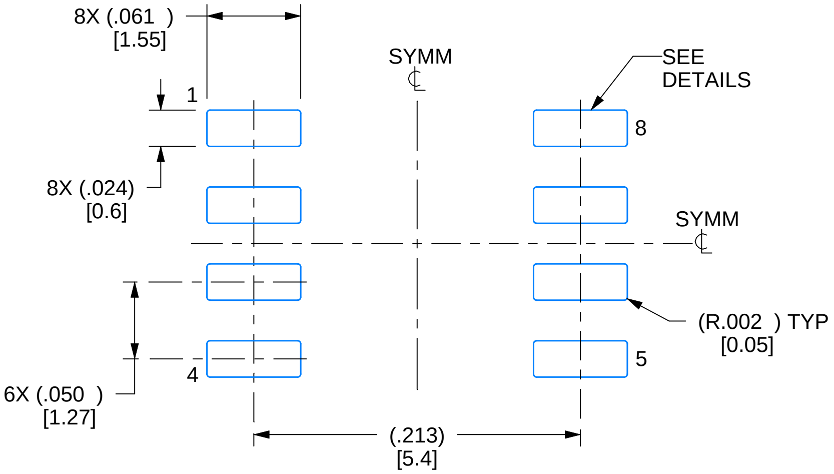
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

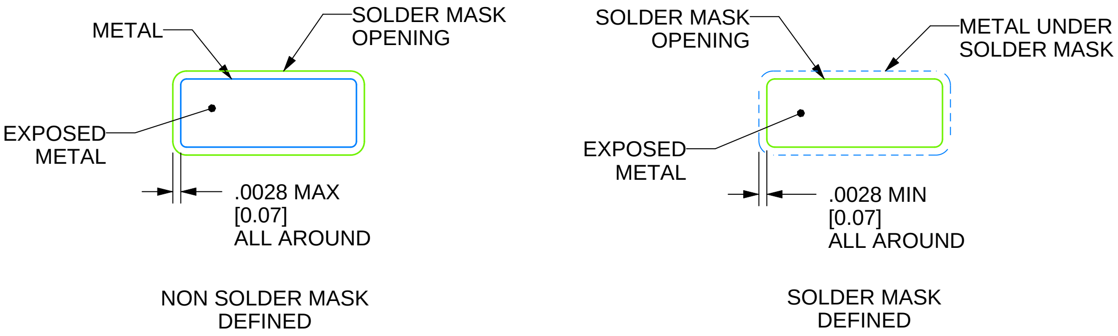


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

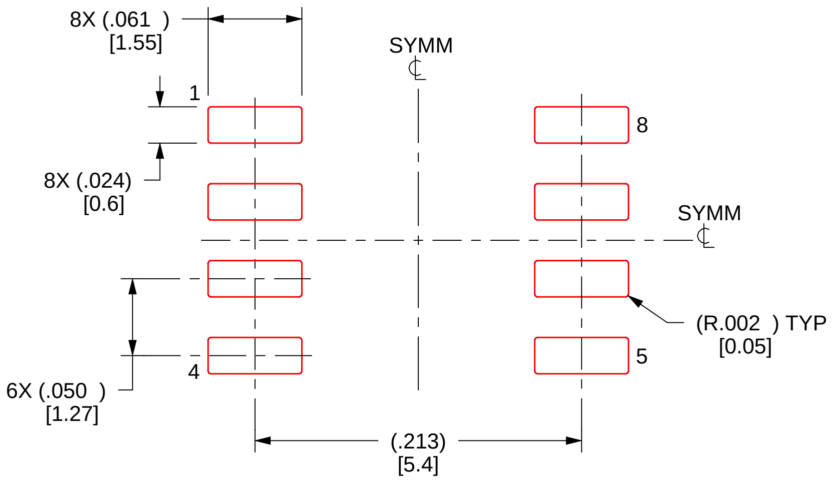


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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