THE DATASHEET OF

LMH6703MFX/NOPB

LMH6703 1.2 GHz, Low Distortion Op Amp with Shutdown

1 Features

- −3-dB bandwidth (V_{OUT} = 0.5 V_{PP}, A_V = 2) 1.2 GHz
- 2nd/3rd Harmonics (20 MHz, SOT-23) −69/−90 dBc
- Low Noise: 2.3 nV/√Hz
- Fast Slew Rate: 4500 V/µs
- Supply Current: 11 mA
- Output Current: 90 mA
- Low Differential Gain and Phase 0.01%/0.02°

2 Applications

- RGB Video Driver
- High Resolution Projectors
- Flash A/D Driver
- D/A Transimpedance Buffer
- Wide Dynamic Range IF Amp
- Radar/Communication Receivers
- DDS Post-Amps
- Line Driver

3 Description

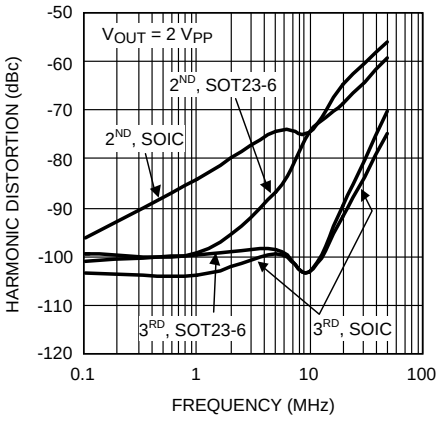
The LMH™6703 is a very wideband, DC coupled monolithic operational amplifier designed specifically for ultra high resolution video systems as well as wide dynamic range systems requiring exceptional signal fidelity. Benefitting from current feedback architecture, the LMH6703 offers a practical gain range of ±1 to ±10 while providing stable operation without external compensation, even at unity gain. At a gain of 2, the LMH6703 supports ultra high resolution video systems with a 750-MHz, 2 V_{PP}, −3-dB Bandwidth. With 12-bit distortion levels through 10 MHz (R_L = 100 Ω), and a 2.3-nV/√Hz input referred noise, the LMH6703 is the ideal driver or buffer for high speed flash A/D and D/A converters. Wide dynamic range systems such as radar and communication receivers requiring a wideband amplifier offering exceptional signal purity will find the LMH6703 low input referred noise and low harmonic distortion an attractive solution.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6703	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Harmonic Distortion vs Frequency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E — **Page**

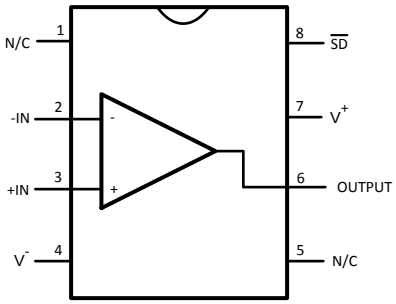
- Added *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Updated maximum value of Input Bias Current (non-inverting) from ±20 to –20 in *Electrical Characteristics* ... 5
- Updated boldface maximum value (temperature extreme) of Input Bias Current (non-inverting) from ±23 to –23 in *Electrical Characteristics* ... 5

Changes from Revision C (March 2013) to Revision D — **Page**

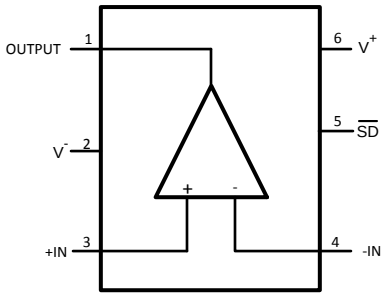
- Changed layout of National Data Sheet to TI format ... 14

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



D Package
6-Pin SOT-23
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	D	DBV		
- IN	2	4	I	Inverting input voltage
+ IN	3	3	I	Non-inverting input voltage
N/C	1, 5	—	—	No connection
OUT	6	1	O	Output
V -	4	2	I	Negative supply
V +	7	6	I	Positive supply
$\overline{SD}$	8	5	I	Shutdown (active low)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S				±6.75	V
I_{OUT}			See (2)		
	Common mode input voltage		V^-	V^+	V
	Maximum junction temperature			150	°C
	Storage temperature		−65	150	°C
	Soldering Information	Infrared or convection (20 sec.)		235	°C
		Wave soldering (10 sec.)		260	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum output current (I_{OUT}) is determined by device power dissipation limitations.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model (MM), per JEDEC specification JESD22-C101, all pins(2)	±200	

(1) Human body model: 1.5 kΩ in series with 100 pF. JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 2000-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) Machine model: 0 Ω in series with 200 pF. JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 200-V MM is possible with the necessary precautions. Pins listed as ±200 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Operating temperature	–40		85	°C
Supply voltage	±4		±6	V

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see *Electrical Characteristics* .

6.4 Thermal Information

THERMAL METRIC(1)		LMH6703		UNIT
		DBV (SOT-23)	D (SOIC)	
		6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	182	133	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	139	79	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40	73	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28	28	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40	73	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

at T_J = 25°C, A_V = 2, V_S = ±5 V, R_L = 100 Ω, R_F = 560 Ω, $\overline{SD}$ = Floating (unless otherwise noted)(1)
Boldface limits apply at the temperature extremes.

PARAMETER		CONDITIONS	MIN (2)	TYP (3)	MAX (2)	UNIT
FREQUENCY DOMAIN PERFORMANCE						
SSBW	–3-dB bandwidth	V_{OUT} = 0.5 V_{PP}, A_V = +1		1800		MHz
		V_{OUT} = 0.5 V_{PP}, A_V = +2		1200		
LSBW		V_{OUT} = 2 V_{PP}		750		
		V_{OUT} = 4 V_{PP}		500		
GF	0.1-dB gain flatness	V_{OUT} = 0.5 V_{PP}		150		MHz
		V_{OUT} = 2 V_{PP}		150		
DG	Differential gain	R_L = 150 Ω, 4.43 MHz		0.01%		
DP	Differential phase	R_L = 150 Ω, 4.43 MHz		0.02		deg
TIME DOMAIN RESPONSE						
t_r	Rise time	2-V step, 10% to 90%		0.5		ns
		6-V step, 10% to 90%		1.05		ns
t_f	Fall time	2-V step, 10% to 90%		0.5		ns
		6-V step, 10% to 90%		1.05		ns
SR	Slew rate	4-V step, 10% to 90% (4)		4200		V/µs
		6-V step, 10% to 90% (4)		4500		
t_s	Settling time	2-V step, V_{OUT} within 0.1%		10		ns
DISTORTION AND NOISE RESPONSE						
HD2	2nd harmonic distortion	2 V_{PP}, 5 MHz, SOT-23-6		−87		dBc
		2 V_{PP}, 20 MHz, SOT-23-6		−69		
		2 V_{PP}, 50 MHz, SOT-23-6		−60		
HD3	3rd harmonic distortion	2 V_{PP}, 5 MHz, SOT-23-6		−100		dBc
		2 V_{PP}, 20 MHz, SOT-23-6		−90		
		2 V_{PP}, 50 MHz, SOT-23-6		−70		
IMD	3rd order intermodulation products	50 MHz, P_O = 5 dBm/ tone		−80		dBc
e_n	Input referred voltage noise	>1 MHz		2.3		nV/√Hz
i_n	Input referred noise current	Inverting Pin >1 MHz		18.5		pA/√Hz
	Input referred noise current	Non-Inverting Pin >1 MHz		3		pA/√Hz
u						
V_{OS}	Input offset voltage			±1.5	±7 **±9**	mV
TCV_{OS}	Input offset voltage average drift	(5)		22		µV/°C
I_B	Input bias current	Non-Inverting (6)		−7	–20 **–23**	µA
		Inverting (6)		−2	±35 **±44**	
TCI_B	Input bias current average drift	Non-Inverting (5)		+30		nA/°C
		Inverting (5)		−70		

(1) Electrical Characteristics values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. Parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
(3) Typical numbers are the most likely parametric norm.
(4) Slew rate is the average of the rising and falling edges.
(5) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(6) Negative input current implies current flowing out of the device.

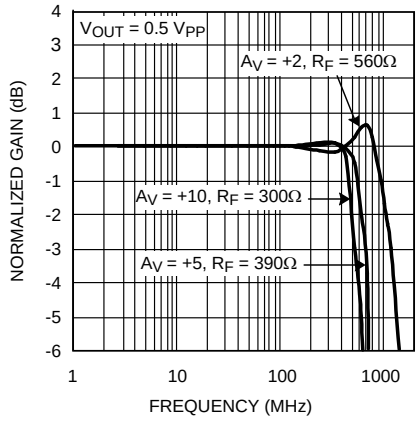
Electrical Characteristics (continued)

at T_J = 25°C, A_V = 2, V_S = ±5 V, R_L = 100 Ω, R_F = 560 Ω, $\overline{SD}$ = Floating (unless otherwise noted)(1)
Boldface limits apply at the temperature extremes.

PARAMETER		CONDITIONS	MIN (2)	TYP (3)	MAX (2)	UNIT
V_O	Output voltage range	R_L = ∞	**±3.3**	±3.45		V
		R_L = 100 Ω	±3.2 **±3.14**	±3.4		
PSRR	Power supply rejection ratio	V_S = ± 4.0 V to ±6.0 V	48 **46**	52		dB
CMRR	Common mode rejection ratio	V_{CM} = −1.0 V to +1.0 V	45 **44**	47		dB
I_S	Supply current (enabled)	$\overline{SD}$ = 2 V, R_L = ∞		11	12.5 **15.0**	mA
	Supply current (disabled)	$\overline{SD}$ = 0.8 V, R_L = ∞		0.2	0.900 **0.935**	mA
MISCELLANEOUS PERFORMANCE						
R_{IN+}	Non-inverting input resistance			1		MΩ
R_{IN-}	Inverting input resistance	Output Impedance of Input Buffer		30		Ω
C_{IN}	Non-inverting input capacitance			0.8		pF
R_O	Output resistance	Closed Loop		0.05		Ω
CMVR	Input common mode voltage range	CMRR ≥ 40 dB	±1.9			V
I_O	Linear output current	V_{IN} = 0 V, V_{OUT} ≤ ±80 mV	±55	±90		mA
ENABLE/DISABLE PERFORMANCE (DISABLED LOW)						
T_{ON}	Enable time			10		ns
T_{OFF}	Disable time			10		ns
	Output glitch			50		mV_{PP}
V_{IH}	Enable voltage	$\overline{SD}$ ≥ V_{IH}	2.0			V
V_{IL}	Disable voltage	$\overline{SD}$ ≤ V_{IL}			0.8	V
I_{IH}	Disable pin bias current, high	$\overline{SD}$ = V^+ (6)		−7	±70	µA
I_{IL}	Disable pin bias current, low	$\overline{SD}$ = 0 V (6)	−50	−240	−400	µA
I_{OZ}	Disabled output leakage current	V_{OUT} = ±1.8 V		0.07	±25 **±40**	µA

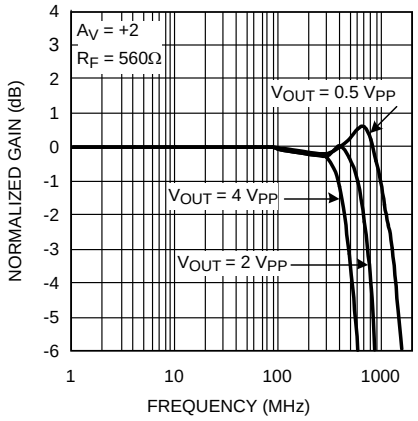
7 Typical Characteristics

at A_V = 2, R_L = 100 Ω, V_S = ±5 V, R_F = 560 Ω, T_A = 25°C, SOT-23-6 (unless otherwise noted)



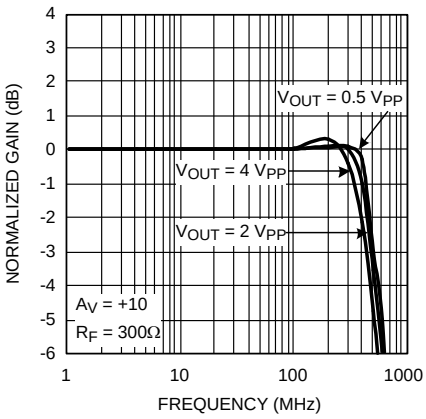
(SOT-23)

Figure 1. Small Signal Non-Inverting Frequency Response



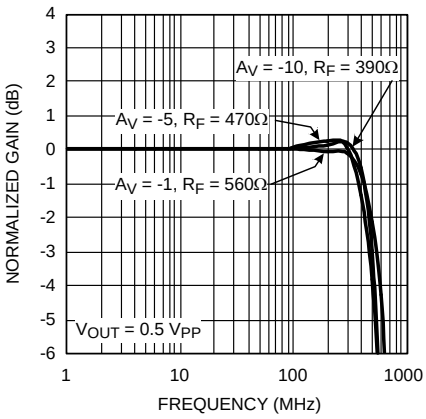
(SOT-23)

Figure 2. Large Signal Frequency Response



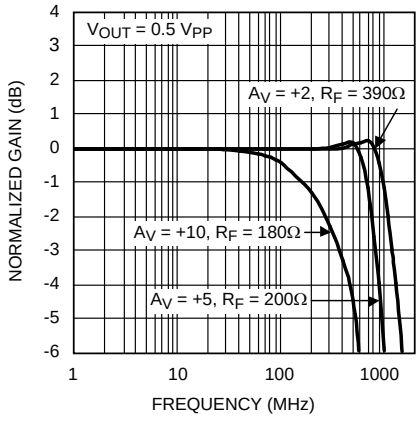
(SOT-23)

Figure 3. Large Signal Frequency Response



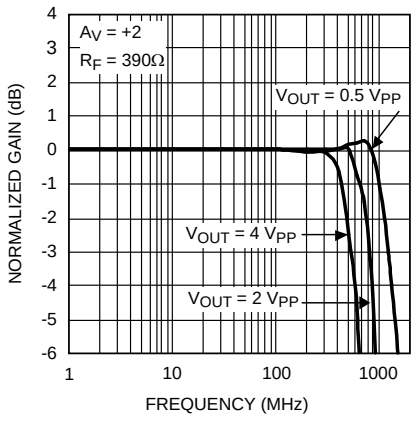
(SOT-23)

Figure 4. Small Signal Inverting Frequency Response



(SOIC)

Figure 5. Small Signal Non-Inverting Frequency Response



(SOIC)

Figure 6. Large Signal Frequency Response

Typical Characteristics (continued)

at A_V = 2, R_L = 100 Ω, V_S = ±5 V, R_F = 560 Ω, T_A = 25°C, SOT-23-6 (unless otherwise noted)

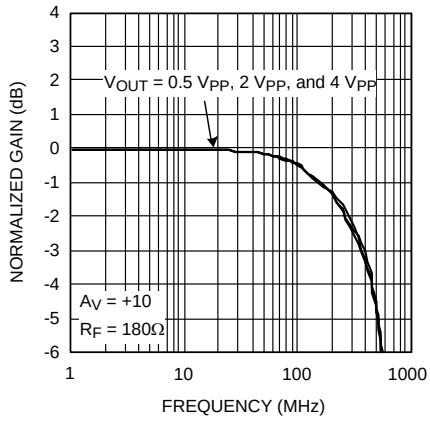


Figure 7. Large Signal Frequency Response

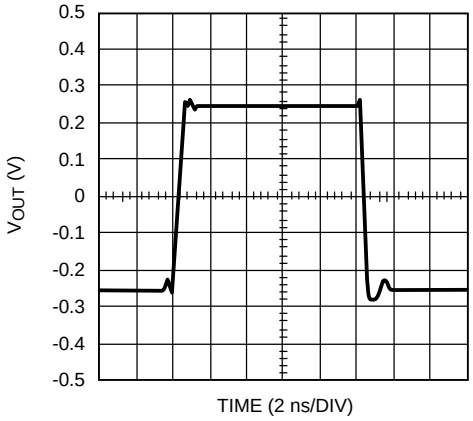


Figure 8. Small Signal Pulse Response

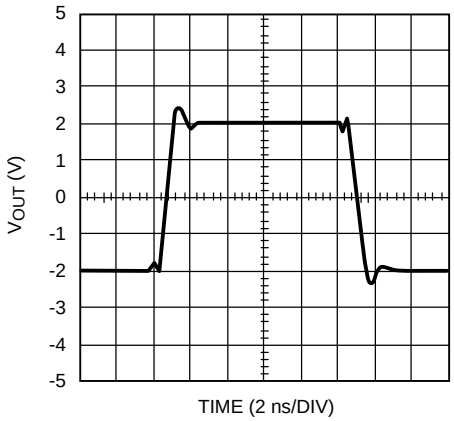


Figure 9. Large Signal Pulse Response

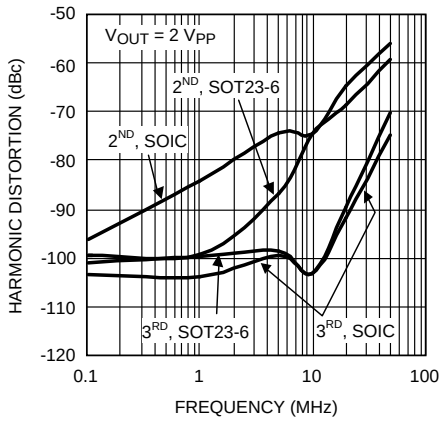


Figure 10. Harmonic Distortion vs Frequency

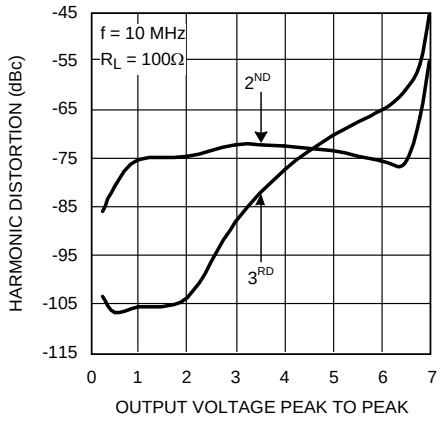


Figure 11. Harmonic Distortion vs Output Voltage

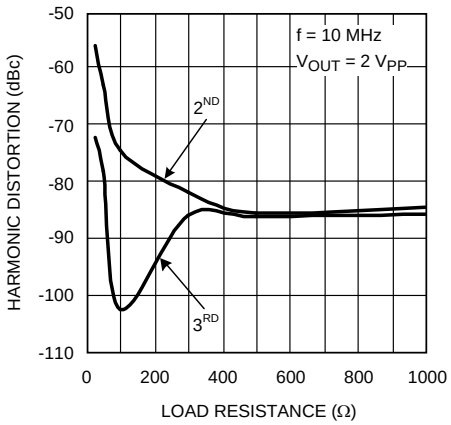


Figure 12. Harmonic Distortion vs. Load

Typical Characteristics (continued)

at A_V = 2, R_L = 100 Ω, V_S = ±5 V, R_F = 560 Ω, T_A = 25°C, SOT-23-6 (unless otherwise noted)

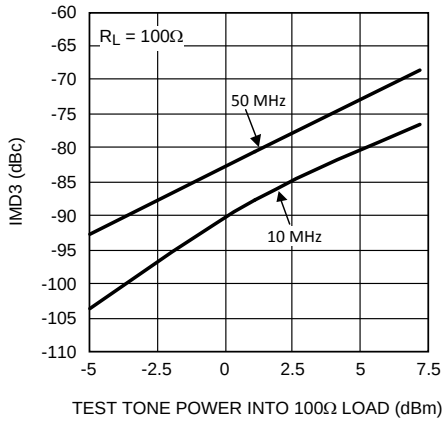


Figure 13. 2-Tone 3rd Order Intermodulation

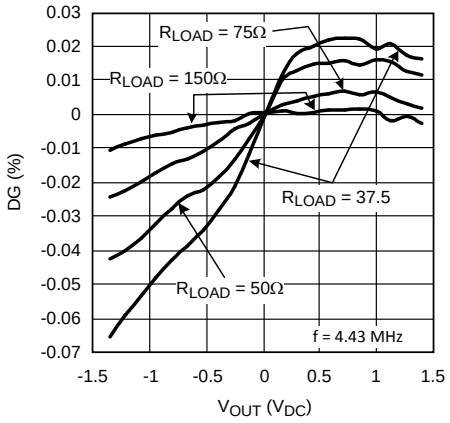


Figure 14. Differential Gain

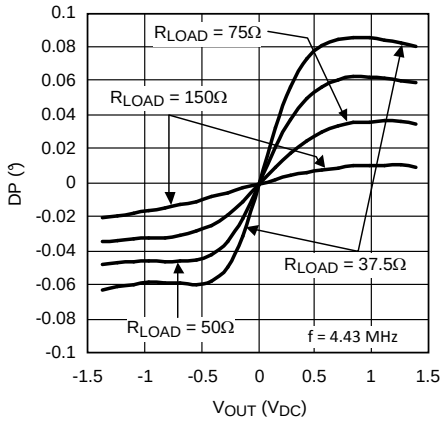


Figure 15. Differential Phase

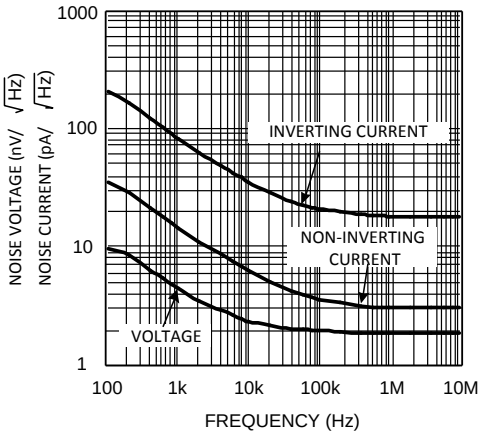


Figure 16. Noise

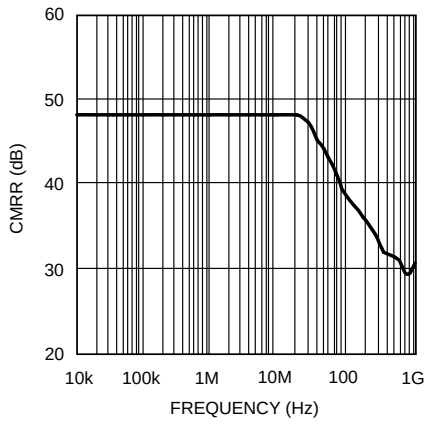


Figure 17. CMRR vs Frequency

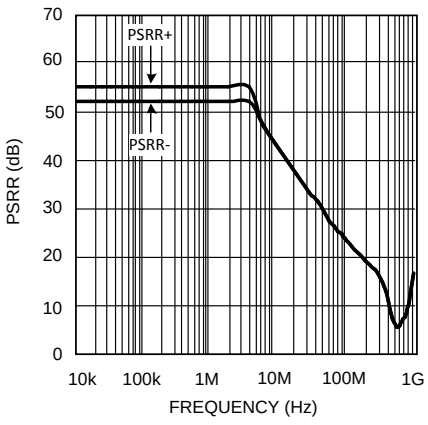


Figure 18. PSRR vs Frequency

Typical Characteristics (continued)

at A_V = 2, R_L = 100 Ω, V_S = ±5 V, R_F = 560 Ω, T_A = 25°C, SOT-23-6 (unless otherwise noted)

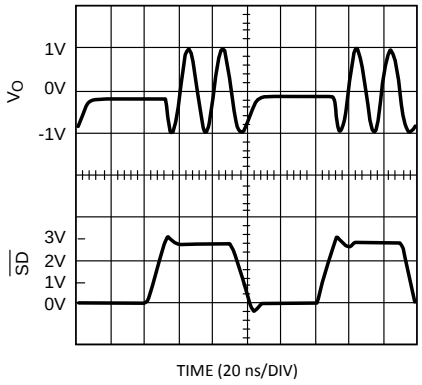


Figure 19. Disable Timing

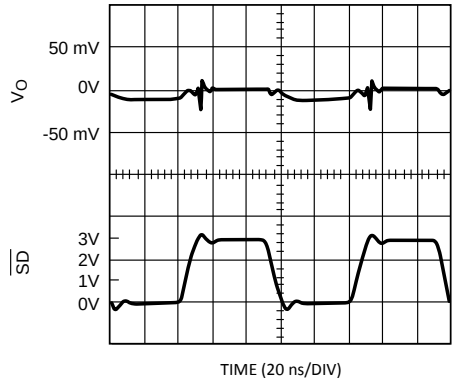
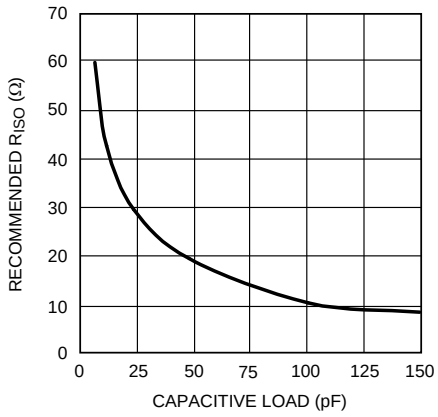


Figure 20. Disable Output Glitch



(See *Application and Implementation*)

Figure 21. R_{ISO} vs C_{LOAD}

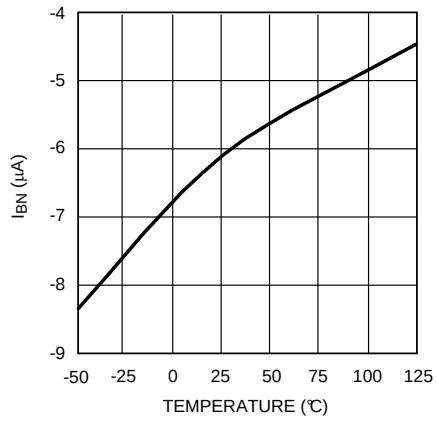


Figure 22. Non-Inverting Input Bias vs Temperature

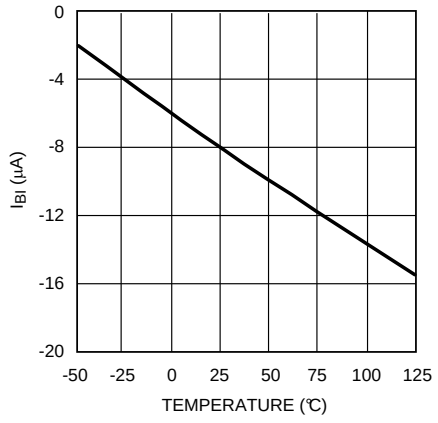


Figure 23. Inverting Input Bias vs Temperature

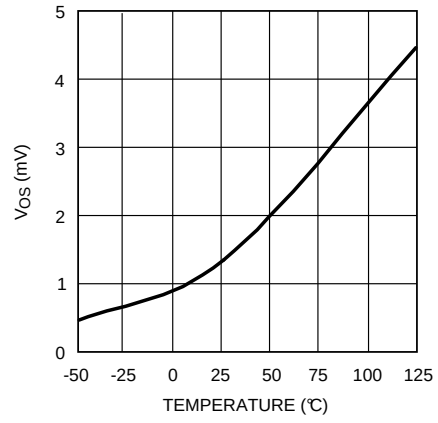


Figure 24. Input Offset vs Temperature

Typical Characteristics (continued)

at A_V = 2, R_L = 100 Ω, V_S = ±5 V, R_F = 560 Ω, T_A = 25°C, SOT-23-6 (unless otherwise noted)

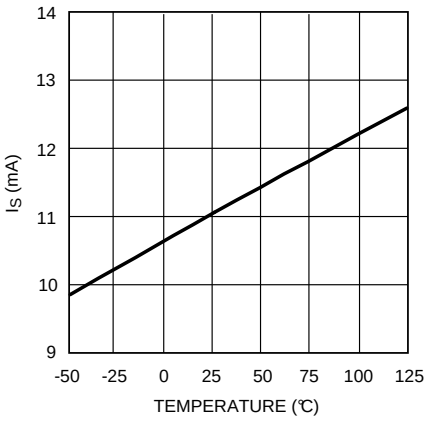


Figure 25. Supply Current vs Temperature

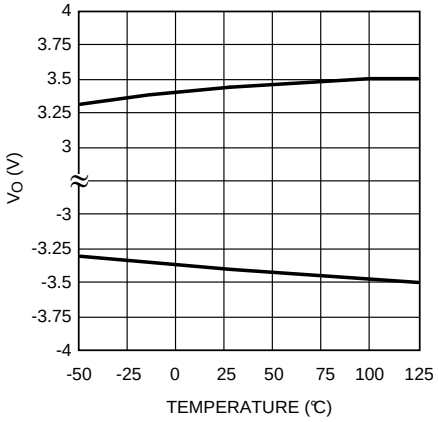


Figure 26. Voltage Swing vs Temperature

8 Detailed Description

8.1 Overview

The LMH6703 has been optimized for exceptionally low harmonic distortion while driving very demanding resistive or capacitive loads. Generally, when used as the input amplifier to very high speed flash ADCs, the distortions introduced by the converter will dominate over the low LMH6703 distortions shown in *Typical Characteristics*.

8.2 Feature Description

The LMH6703 is a high speed current feedback amplifier, optimized for excellent bandwidth, gain flatness, and low distortion. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The LMH6703 in the SOT-23-6 package is optimized for use with a 560-Ω feedback resistor. The LMH6703 in the SOIC package is optimized for use with a 390-Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 (SNOA366) discusses this in detail along with the occasions where a different R_F might be advantageous.

8.3 Device Functional Modes

8.3.1 Feedback Resistor Selection

One of the key benefits of a current feedback operational amplifier is the ability to maintain optimum frequency response independent of gain by using appropriate values for the feedback resistor (R_F). The Electrical Characteristics and Typical Characteristics plots specify an R_F of 560 Ω (390 Ω for the SOIC package), a gain of 2 V/V, and ±5-V power supplies (unless otherwise specified). Generally, lowering R_F from it's recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below it's recommended value will cause overshoot, ringing and, eventually, oscillation.

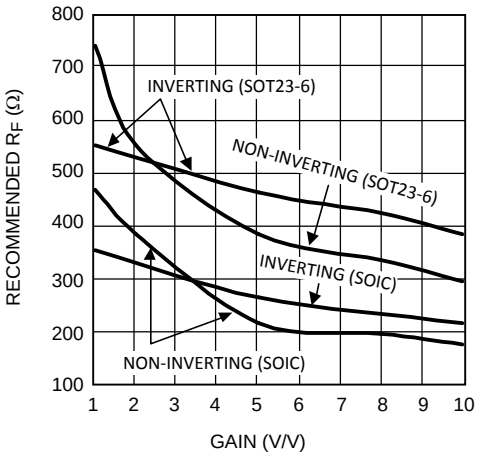


Figure 27. Recommended R_F vs. Gain

Since a current feedback amplifier is dependant on the value of R_F to provide frequency compensation and since the value of R_F can be used to optimize the frequency response, different packages use different R_F values. As shown in Figure 27, the SOT-23-6 and the SOIC package use different values for the feedback resistor, R_F. Since each application is slightly different, it is worth some experimentation to find the optimal R_F for a given circuit. In general, a value of R_F that produces ≈0.1 dB of peaking is the best compromise between stability and maximum bandwidth. Note that it is not possible to use a current feedback amplifier with the output shorted directly to the inverting input. The buffer configuration of the LMH6703 requires a 560 Ω (390 Ω for SOIC package) feedback resistor for stable operation.

Device Functional Modes (continued)

The LMH6703 was optimized for high speed operation. As shown in Figure 27, the suggested value for R_F decreases for higher gains. Due to the output impedance of the input buffer, there is a practical limit for how small R_F can go, based on the lowest practical value of R_G. This limitation applies to both inverting and non inverting configurations. For the LMH6703 the input resistance of the inverting input is approximately 30Ω and 20Ω is a practical (but not hard and fast) lower limit for R_G. The LMH6703 begins to operate in a gain bandwidth limited fashion in the region when R_G is nearly equal to the input buffer impedance. Note that the amplifier will operate with R_G values well below 20 Ω, however results may be substantially different than predicted from ideal models. In particular the voltage potential between the Inverting and Non-Inverting inputs cannot be expected to remain small.

Inverting gain applications that require impedance matched inputs may limit gain flexibility somewhat (especially if maximum bandwidth is required). The impedance seen by the source is R_G || R_T (R_T is optional). The value of R_G is R_F /Gain. Thus for a SOT-23 in a gain of —5V/V, an R_F of 460 Ω is optimum and R_G is 92 Ω. Without a termination resistor, R_T, the input impedance would equal R_G, 92 Ω. Using an R_T of 109Ω will set the input resistance to match a 50-Ω source. Note that source impedances greater then R_G cannot be matched in the inverting configuration.

For more information see Application Note OA-13 (SNOA366) which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The value for the inverting input impedance for the LMH6703 is approximately 30 Ω. The LMH6703 is designed for optimum performance at gains of 1 to 10 V/V and −1 to −9 V/V. Higher gain configurations are still useful, however, the bandwidth will fall as gain is increased, much like a typical voltage feedback amplifier.

The LMH6703 data sheet shows both SOT-23-6 and SOIC data in the Electrical Characteristic section to aid in selecting the right package. The Typical Characteristics section shows SOT-23-6 package plots only.

8.3.2 DC Accuracy and Noise

Example below shows the output offset computation equation for the non-inverting configuration (see Figure 29) using the typical bias current and offset specifications for A_V = 2:

Output Offset : $V_O = (I_{BN} \times R_{IN} \pm V_{OS}) (1 + R_F/R_G) \pm I_{BI} \times R_F$

Where R_{IN} is the equivalent input impedance on the non-inverting input.

Example computation for A_V = 2, R_F = 560 Ω, R_{IN} = 25 Ω:

$V_O = (7\ \mu A \times 25\ \Omega \pm 1.5\ mV) (1 + 560/560) \pm 2\ \mu A \times 560 \approx -3.7\ mV$ to 4.5 mV

A good design, however, should include a worst case calculation using Min/Max numbers in the data sheet tables, in order to ensure "worst case" operation.

Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA-07 (SNOA365). The two input bias currents are physically unrelated in both magnitude and polarity for the current feedback topology. It is not possible, therefore, to cancel their effects by matching the source impedance for the two inputs (as is commonly done for matched input bias current devices).

The total output noise is computed in a similar fashion to the output offset voltage. Using the input noise voltage and the two input noise currents, the output noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. See Application Note OA-12 (SNOA375) for a full discussion of noise calculations for current feedback amplifiers.

Device Functional Modes (continued)

8.3.3 Enable/Disable

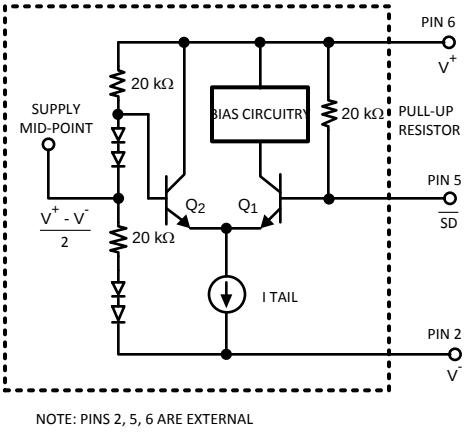


Figure 28. $\overline{SD}$ Pin Simplified Schematic (SOT-23 Pinout Shown)

For 5-V supplies only, the LMH6703 has a TTL logic compatible disable function. Apply a logic low (< 0.8 V) to the $\overline{SD}$ pin and the LMH6703 is disabled. Apply a logic high (> 2.0 V), or let the pin float and the LMH6703 is enabled. Voltage, not current, at the Shutdown pin ($\overline{SD}$) determines the enable/disable state. Care must be exercised to prevent the shutdown pin voltage from going more than 0.8 V below the midpoint of the supply voltages (0V with split supplies, $V^+/2$ with single supply biasing). Doing so could cause transistor Q1 to Zener resulting in damage to the disable circuit (See Figure 28). The core amplifier is unaffected by this, but the shutdown operation could become permanently slower as a result.

Disabled, the LMH6703 inputs and output become high impedances. While disabled the LMH6703 quiescent current is approximately 200 µA. Because of the pull up resistor on the shutdown circuit, the I_{CC} and I_{EE} currents (positive and negative supply currents respectively) are not balanced in the disabled state. The positive supply current (I_{CC}) is approximately 300 µA while the negative supply current (I_{EE}) is only 200 µA. The remaining I_{EE} current of 100 µA flows through the shutdown pin.

The disable function can be used to create analog switches or multiplexers. Implement a single analog switch with one LMH6703 positioned between an input and output. Create an analog multiplexer with several LMH6703s and tie the outputs together.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

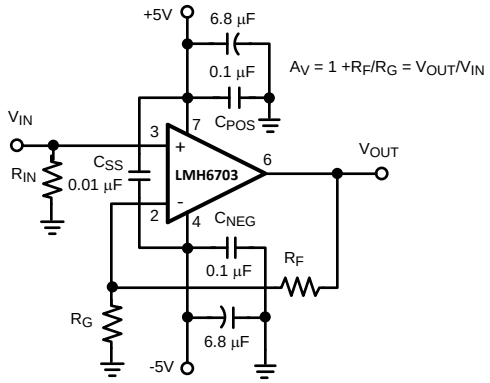


Figure 29. Recommended Non-Inverting Gain Circuit (SOIC Pinout Shown)

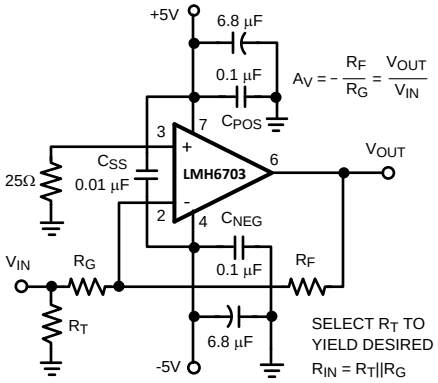


Figure 30. Recommended Inverting Gain Circuit (SOIC Pinout Shown)

9.1.1 Capacitive Load Drive

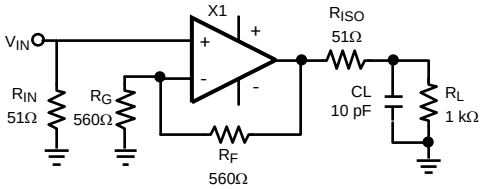


Figure 31. Decoupling Capacitive Loads

Typical Application (continued)

Capacitive output loading applications will benefit from the use of a series output resistor R_{ISO}. Figure 31 shows the use of a series output resistor, R_{ISO}, to stabilize the amplifier output under capacitive loading. Capacitive loads from 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Figure 21 gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This produces a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{ISO} can be reduced slightly from the recommended values.

9.1.2 Video Performance

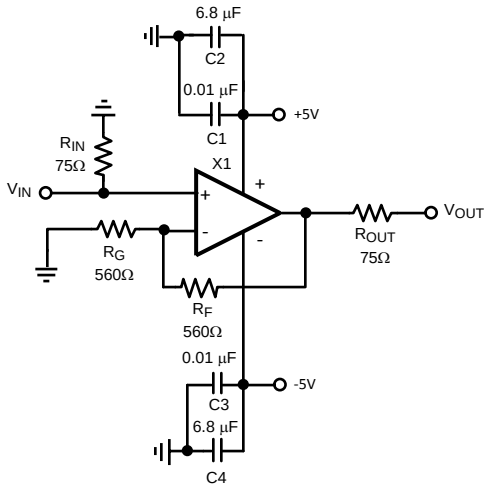


Figure 32. Typical Video Application

The LMH6703 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. NTSC and PAL performance is nearly flawless with DG of 0.01% and DP of 0.02°. Best performance will be obtained with back terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitance from the amplifier output stage. Figure 32 shows a typical configuration for driving 75Ω cable. The amplifier is configured for a gain of two compensating for the 6 dB loss due to R_{OUT}.

10 Power Supply Recommendations

The LMH6703 can operate off a single supply or with dual supplies as long as the input CM voltage range (CMIR) has the required headroom to either supply rail. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

11 Layout

11.1 Layout Guidelines

Whenever questions about layout arise, use the evaluation board (see Table 1) as a guide. The LMH730216 is the evaluation board for SOT-23-6 samples and the LMH730227 is the evaluation board for SOIC samples.

To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. Components in the feedback path should be placed as close to the device as possible to minimize parasitic capacitance. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends.

Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each voltage rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located further from the device, the smaller ceramic bypass capacitors should be placed as close to the device as possible. In Figure 29 and Figure 30, C_{SS} is optional, but is recommended for best second order harmonic distortion.

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations. See *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers*, Application Note OA-15 (SNOA367). The evaluation board(s) is a good example of high frequency layout techniques as a reference.

General high-speed, signal-path layout suggestions include:

- Continuous ground planes are preferred for signal routing, as shown in Figure 33 and Figure 34, with matched impedance traces for longer runs. However, open up both ground and power planes around the capacitive sensitive input and output device pins.
- Use good, high-frequency decoupling capacitors (0.1 µF) on the ground plane at the device power pins as shown in Figure 33. Higher value capacitors (2.2 µF) are required, but may be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply-decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- When using differential signal routing over any appreciable distance, use microstrip layout techniques with matched impedance traces.
- The input summing junction is very sensitive to parasitic capacitance. Connect any Rf, and Rg elements into the summing junction with minimal trace length to the device pin side of the resistor, as shown in Figure 34. The other side of these elements can have more trace length if needed to the source or to ground.

Table 1. Evaluation Boards

DEVICE	PACKAGE	EVALUATION BOARD PART NUMBER
LMH6703MF	SOT-23-6	LMH730216
LMH6703MA	SOIC	LMH730227

11.2 Layout Example

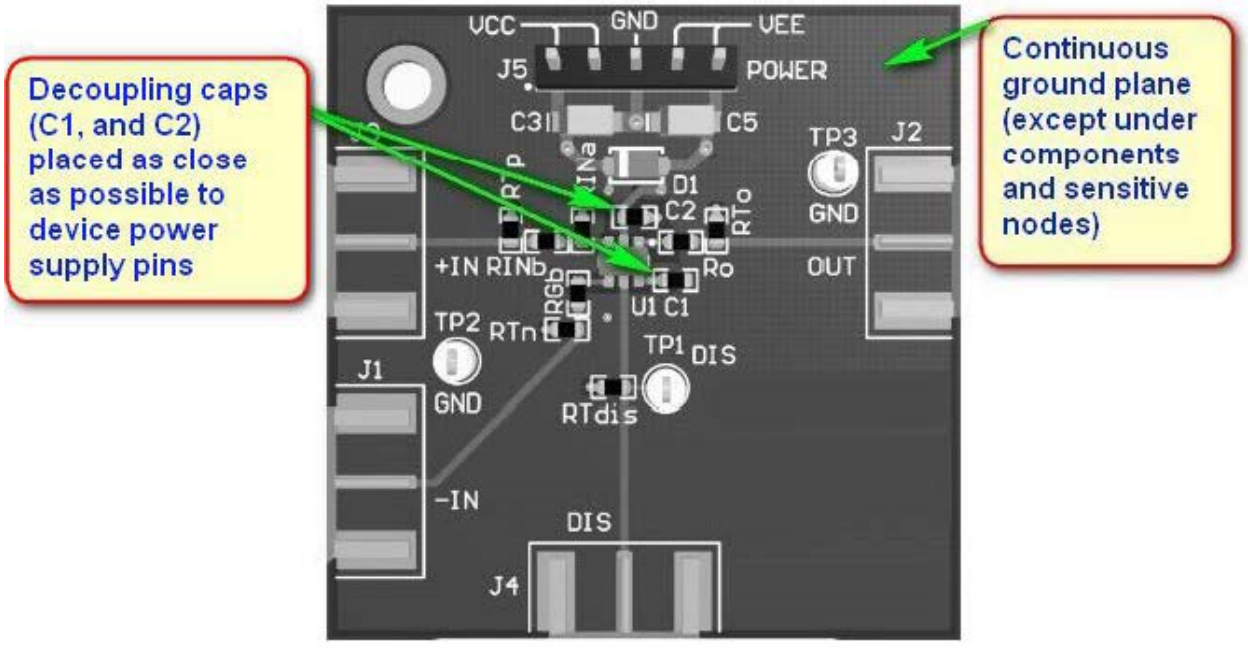


Figure 33. Evaluation Board Layer 1

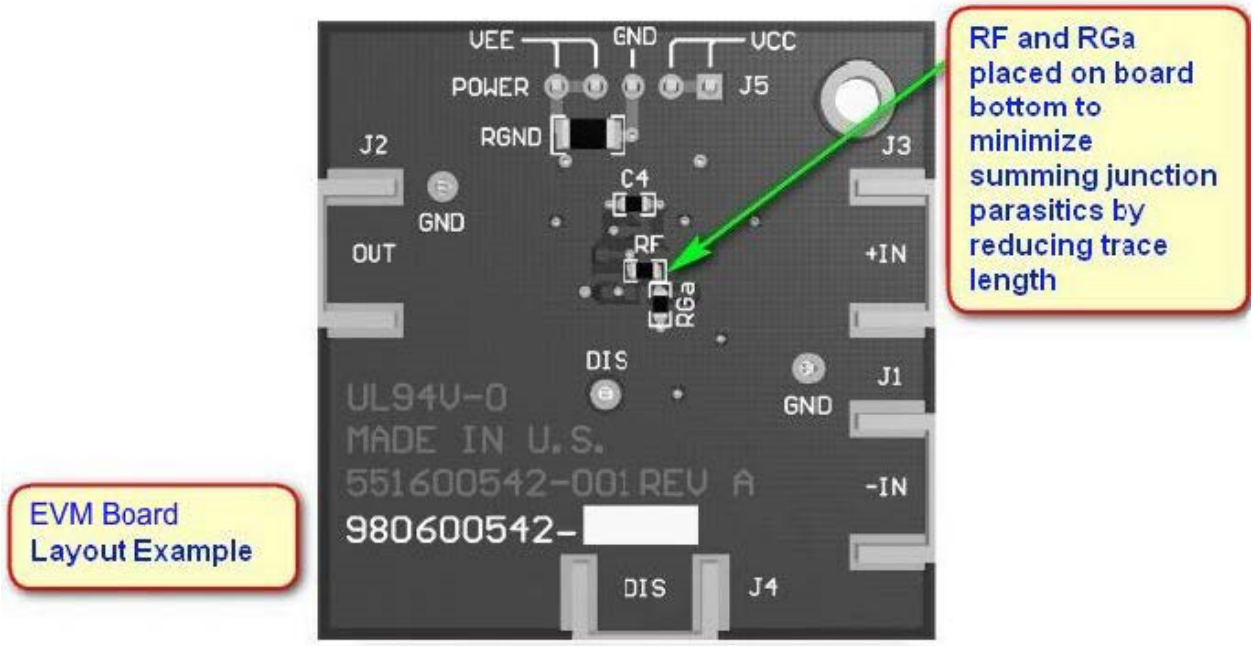


Figure 34. Evaluation Board Layer 2

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Absolute Maximum Ratings for Soldering (SNOA549)
- Current Feedback Op Amp Applications Circuit Guide, Application Note OA--07 (SNOA365)
- Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers, Application Note OA-15 (SNOA367)
- Noise Analysis for Comlinear Amplifiers, Application Note OA-12 (SNOA375)
- Semiconductor and IC Package Thermal Metrics (SPRA953)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

LMH, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6703MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH67 03MA	Samples
LMH6703MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH67 03MA	Samples
LMH6703MF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	AR1A	Samples
LMH6703MFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	AR1A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

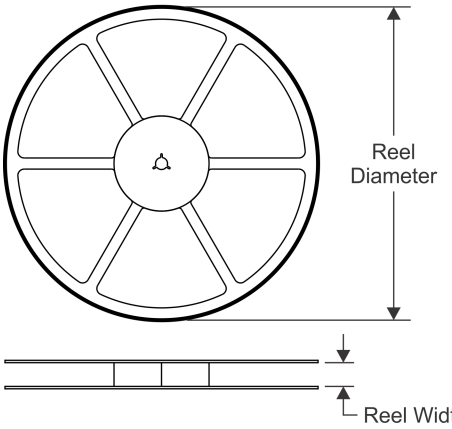
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

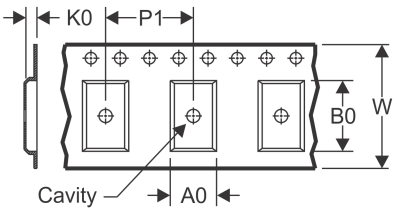
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

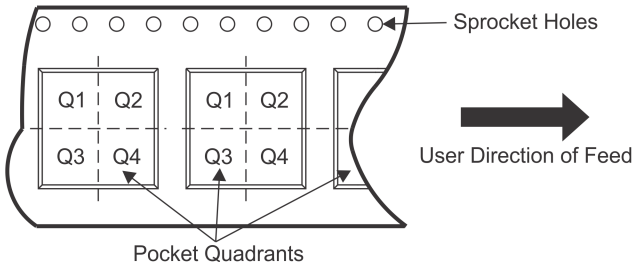


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

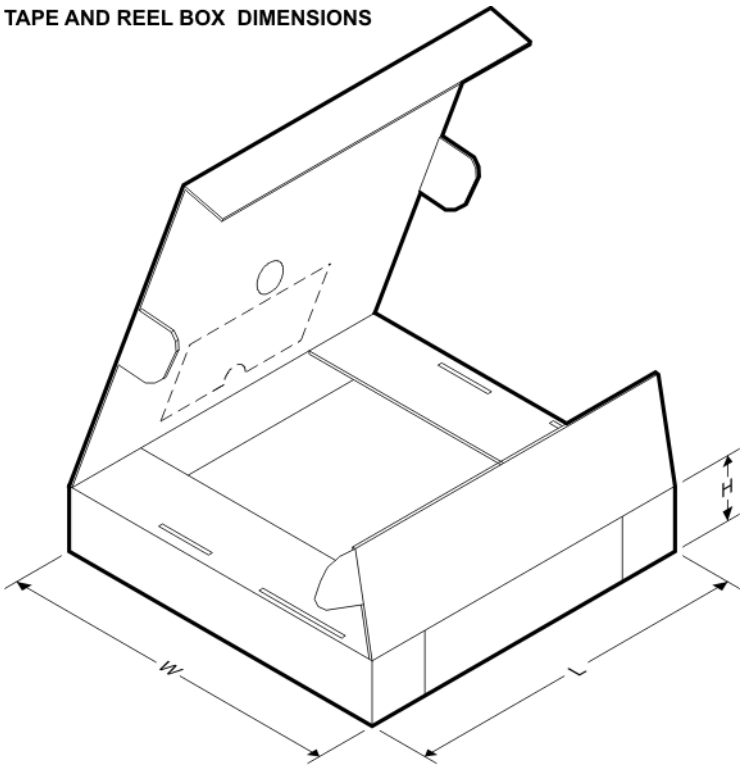
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6703MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6703MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6703MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

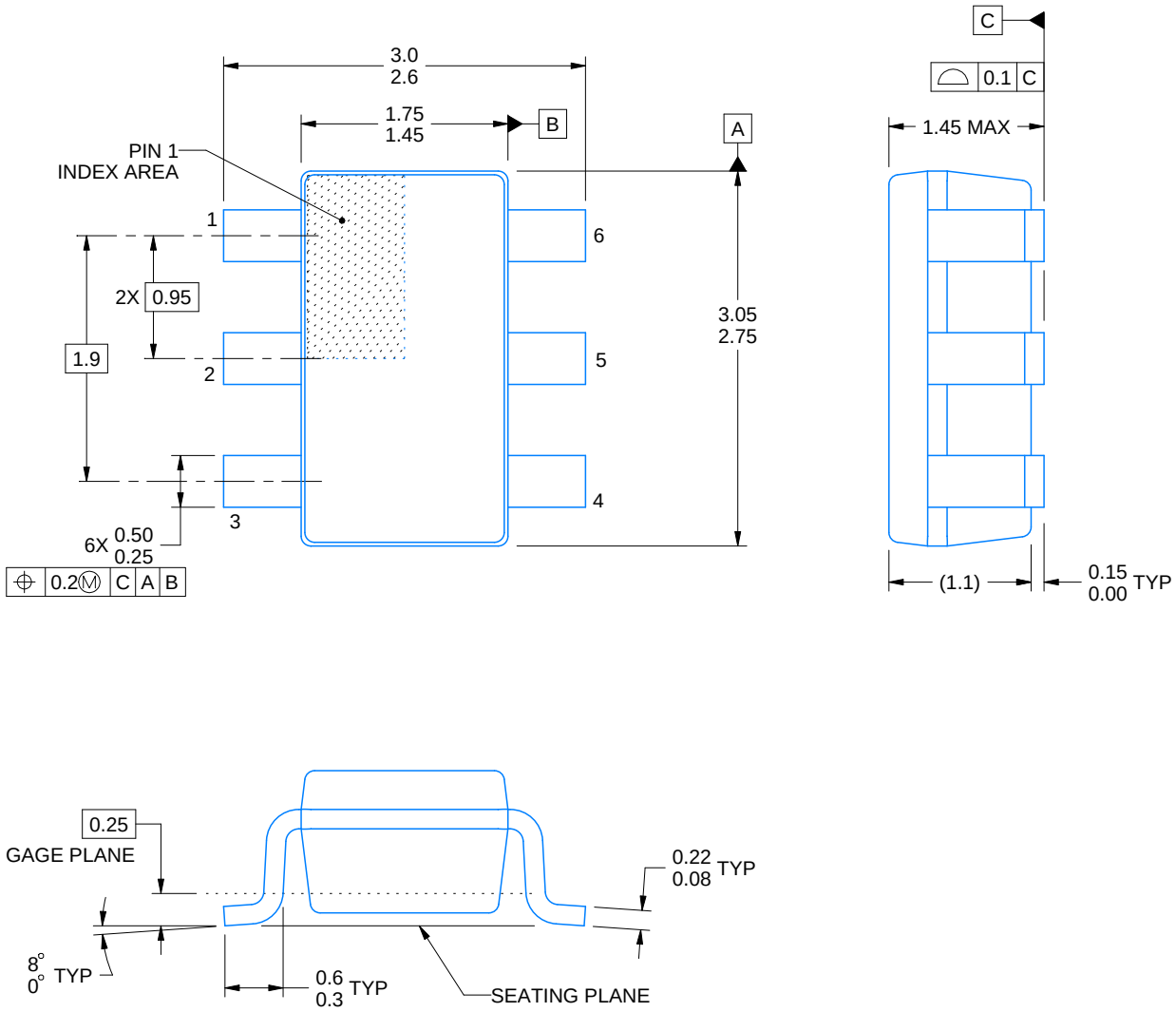
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6703MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6703MF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LMH6703MFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

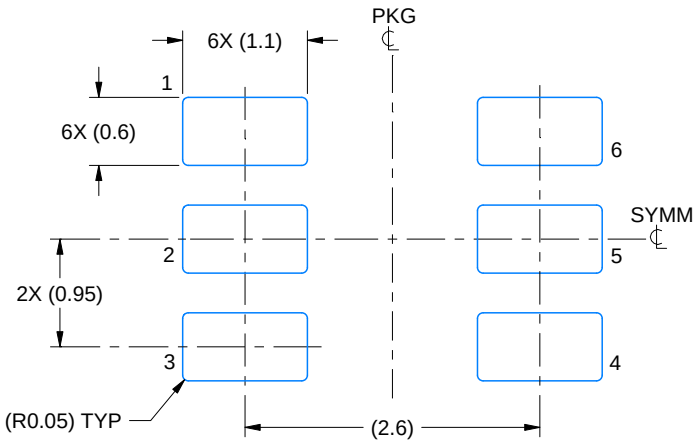
SMALL OUTLINE TRANSISTOR



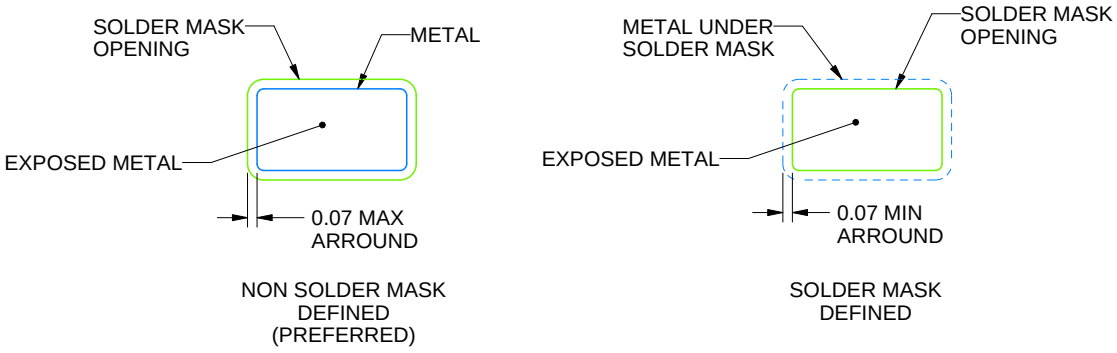
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

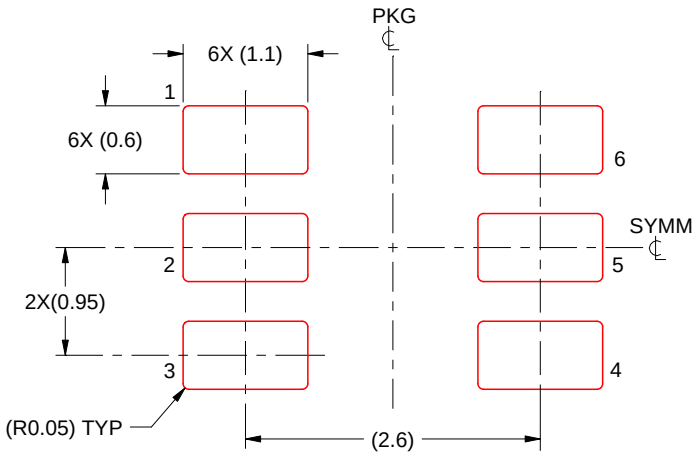


SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

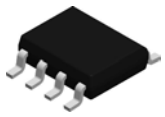


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

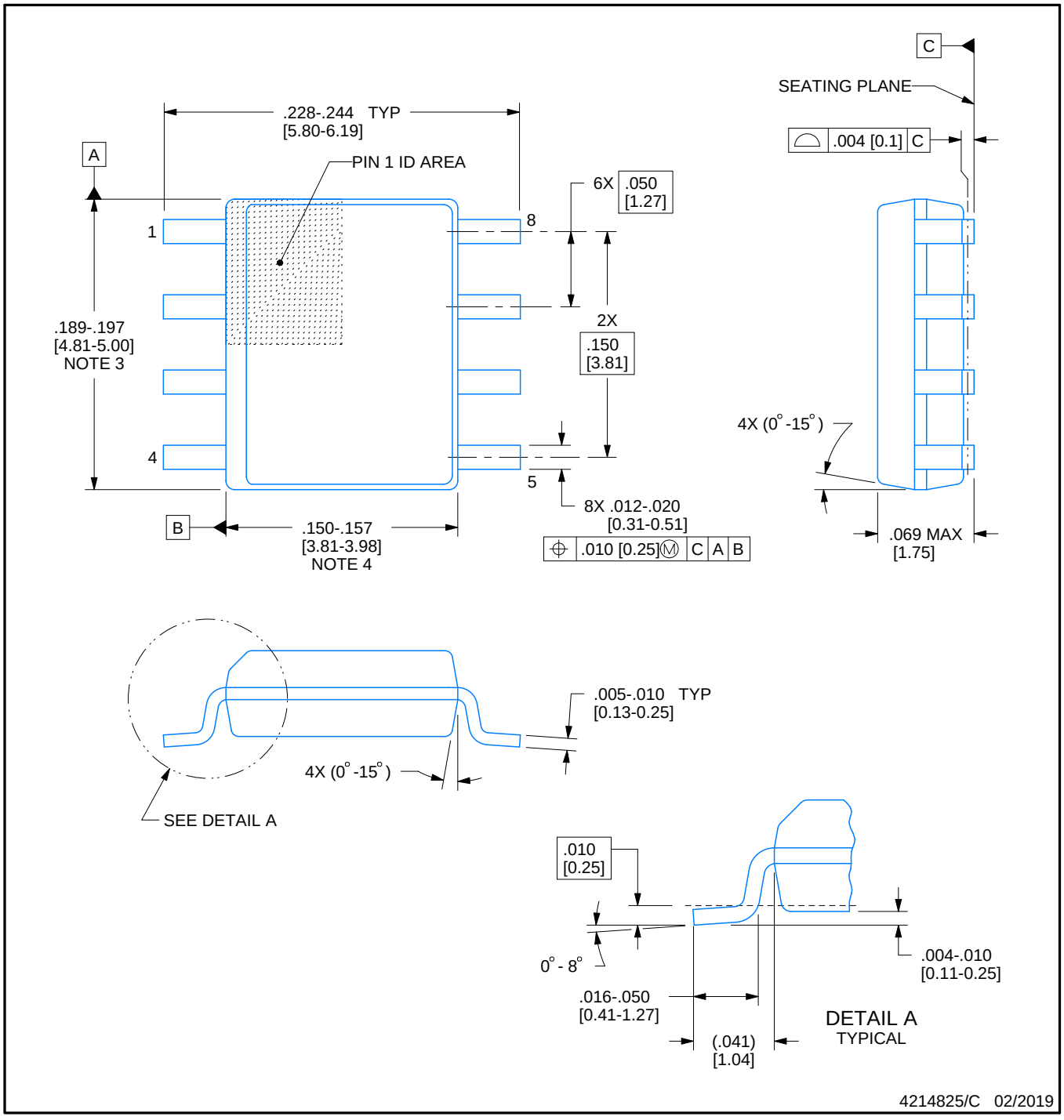


PACKAGE OUTLINE

D0008A

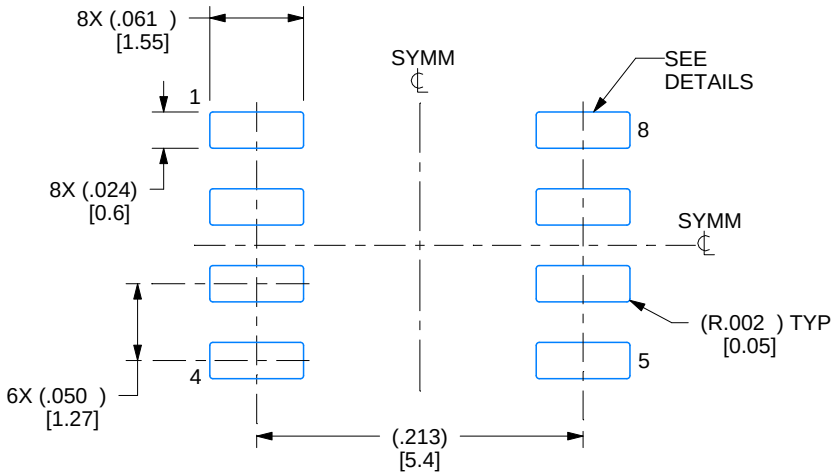
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

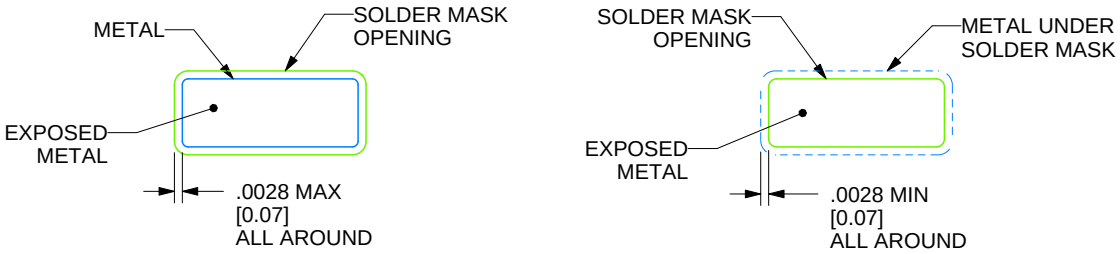


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

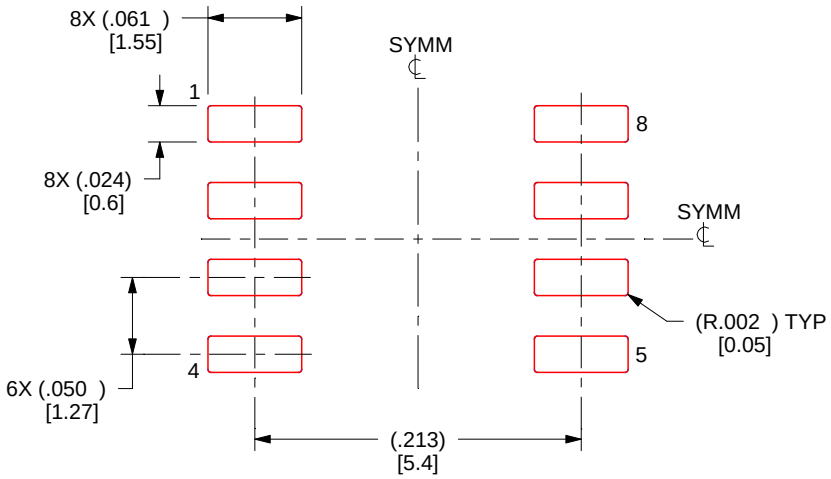
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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