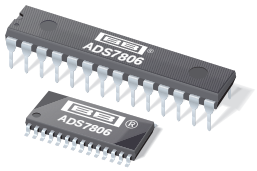
# THE DATASHEET OF

# ADS7806UB

www.win-source.net 0086-755-83957316

# ADS7806



SBAS021B – NOVEMBER 1992 – REVISED SEPTEMBER 2003

# Low-Power 12-Bit Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

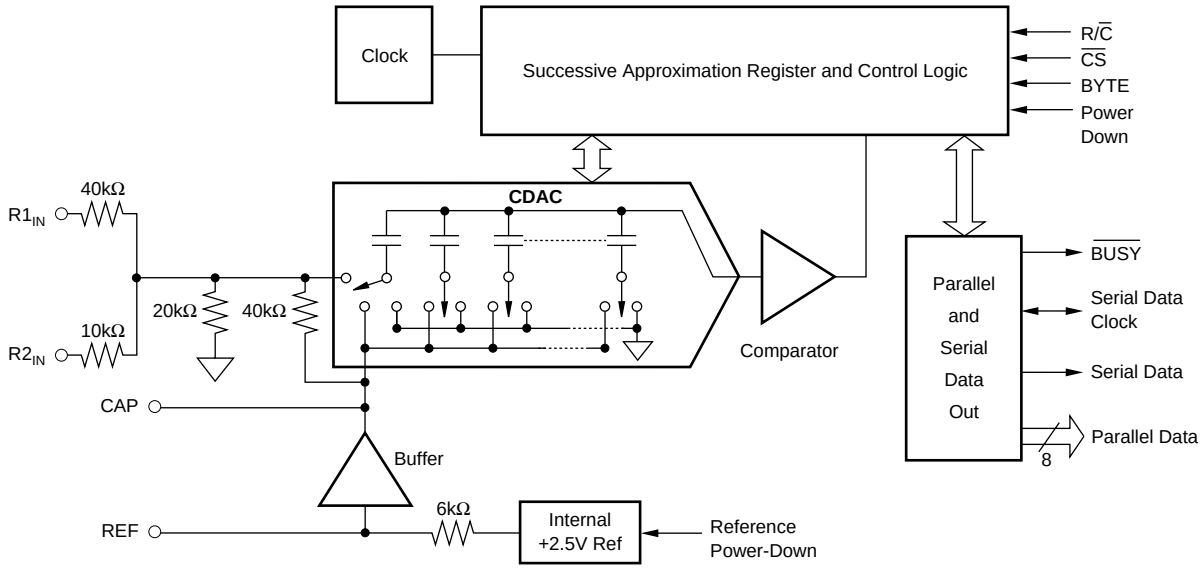
- **POWER DISSIPATION: 35mW max**
- **POWER-DOWN MODE: 50μW**
- **ACQUISITION AND CONVERSION: 25μs max**
- **±1/2 LSB MAX INL AND DNL**
- **72dB MIN SINAD WITH 1kHz INPUT**
- **INPUT RANGES: ±10V, 0V to +5V, and 0V TO +4V**
- **SINGLE +5V SUPPLY OPERATION**
- **PARALLEL AND SERIAL DATA OUTPUT**
- **PIN-COMPATIBLE WITH THE 16-BIT ADS7807**
- **USES INTERNAL OR EXTERNAL REFERENCE**
- **0.3" DIP-28 AND SO-28**

## DESCRIPTION

The ADS7806 is a low-power, 12-bit, sampling Analog-to-Digital (A/D) converter using state of the art CMOS structures. It contains a complete 12-bit, capacitor-based, Successive Approximation Register (SAR) A/D converter with sample-and-hold, clock, reference, and a microprocessor interface with parallel and serial output drivers.

The ADS7806 can acquire and convert to full 12-bit accuracy in 25μs max, while consuming only 35mW max. Laser trimmed scaling resistors provide standard industrial input ranges of ±10V and 0V to +5V. In addition, a 0V to +4V range allows development of complete single-supply systems.

The ADS7806 is available in a 0.3" DIP-28 and SO-28, both fully specified for operation over the industrial –40°C to +85°C temperature range.

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## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Analog Inputs: $R1_{IN}$ | ±12V |
| $R2_{IN}$ | ±5.5V |
| CAP | $V_{ANA}$ + 0.3V to AGND2 – 0.3V |
| REF | Indefinite Short to AGND2, Momentary Short to $V_{ANA}$ |
| Ground Voltage Differences: DGND, AGND1, and AGND2 | ±0.3V |
| $V_{ANA}$ | 7V |
| $V_{DIG}$ to $V_{ANA}$ | +0.3V |
| $V_{DIG}$ | 7V |
| Digital Inputs | –0.3V to $V_{DIG}$ + 0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (DB) | PACKAGE-LEAD | PACKAGE DESIGNATOR[1] | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---|---|---|---|---|---|---|---|---|
| ADS7806P | ±0.9 | 70 | DIP-28 | NT | –40°C to +85°C | ADS7806P | ADS7806P | Tubes, 13 |
| ADS7806PB | ±0.45 | 72 | " | " | " | ADS7806PB | ADS7806PB | Tubes, 13 |
| ADS7806U | ±0.9 | 70 | SO-28 | DW | –40°C to +85°C | ADS7806U | ADS7806U | Tubes, 28 |
| " | " | " | " | " | " | ADS7806U | ADS7806U/1K | Tape and Reel, 1000 |
| ADS7806UB | ±0.45 | 72 | " | " | " | ADS7806UB | ADS7806UB | Tubes, 28 |
| " | " | " | " | " | " | ADS7806UB | ADS7806UB/1K | Tape and Reel, 1000 |

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

# ELECTRICAL CHARACTERISTICS

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, and using internal reference and fixed resistors (see Figure 7b), unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7806P, U | | | ADS7806PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 12 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Ranges | | | | ±10, 0 to +5, 0 to +4 | | | | V |
| Impedance | | | | (See Table I) | | | | |
| Capacitance | | | 35 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Time | | | | 20 | | | * | µs |
| Complete Cycle | Acquire and Convert | | | 25 | | | * | µs |
| Throughput Rate | | 40 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | ±0.15 | ±0.9 | | * | ±0.45 | LSB[1] |
| Differential Linearity Error | | | ±0.15 | ±0.9 | | * | ±0.45 | LSB |
| No Missing Codes | | | Tested | | | * | | Bits |
| Transition Noise[2] | | | 0.1 | | | * | | LSB |
| Gain Error | | | ±0.2 | | | ±0.1 | | % |
| Full-Scale Error[3,4] | | | | ±0.5 | | | ±0.25 | % |
| Full-Scale Error Drift | | | ±7 | | | ±5 | | ppm/°C |
| Full-Scale Error[3,4] | Ext. 2.5000V Ref | | | ±0.5 | | | ±0.25 | % |
| Full-Scale Error Drift | Ext. 2.5000V Ref | | ±0.5 | | | * | | ppm/°C |
| Bipolar Zero Error[3] | ±10V Range | | | ±10 | | | * | mV |
| Bipolar Zero Error Drift | ±10V Range | | ±0.5 | | | * | | ppm/°C |
| Unipolar Zero Error[3] | 0V to 5V, 0V to 4V Ranges | | | ±3 | | | * | mV |
| Unipolar Zero Error Drift | 0V to 5V, 0V to 4V Ranges | | ±0.5 | | | * | | ppm/°C |
| Recovery Time to Rated Accuracy from Power-Down[5] | 2.2µF Capacitor to CAP | | 1 | | | * | | ms |
| Power-Supply Sensitivity ($V_{DIG}$ = $V_{ANA}$ = $V_S$) | +4.75V < $V_S$ < +5.25V | | | ±0.5 | | | * | LSB |

# ELECTRICAL CHARACTERISTICS (Cont.)

At $T_A$ = –40°C to +85°C, $f_S$ = 40kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, and using internal reference and fixed resistors (see Figure 7b), unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7806P, U | | | ADS7806PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 1kHz, ±10V | 80 | 90 | | * | * | | dB(6) |
| Total Harmonic Distortion | $f_{IN}$ = 1kHz, ±10V | | –90 | –80 | | * | * | dB |
| Signal-to-(Noise + Distortion) | $f_{IN}$ = 1kHz, ±10V | 70 | 73 | | 72 | * | | dB |
| Signal-to-Noise | $f_{IN}$ = 1kHz, ±10V | 70 | 73 | | 72 | * | | dB |
| Usable Bandwidth(7) | | | 130 | | | * | | kHz |
| Full-Power Bandwidth (–3dB) | | | 600 | | | * | | kHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 40 | | | * | | ns |
| Aperture Jitter | | | 20 | | | * | | ps |
| Transient Response | FS Step | | | 5 | | | * | µs |
| Over-Voltage Recovery(8) | | | 750 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | No Load | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer.) | | | 1 | | | * | | µA |
| Internal Reference Drift | | | 8 | | | * | | ppm/°C |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | External 2.5000V Ref | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | Parallel 12-bits in 2-bytes; Serial Binary Two's Complement or Straight Binary | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$(9) | | +2.0 | | $V_D$ +0.3V | * | | * | V |
| $I_{IL}$ | $V_{IL}$ = 0V | | | ±10 | | | * | µA |
| $I_{IH}$ | $V_{IH}$ = 5V | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | | | | | | |
| Data Coding | | | | | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +4 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | * | pF |
| **DIGITAL TIMING** | | | | | | | | |
| Bus Access Time | $R_L$ = 3.3kΩ, $C_L$ = 50pF | | | 83 | | | * | ns |
| Bus Relinquish Time | $R_L$ = 3.3kΩ, $C_L$ = 10pF | | | 83 | | | * | ns |
| **POWER SUPPLIES** | | | | | | | | |
| Specified Performance | | | | | | | | |
| $V_{DIG}$ | Must be ≤ $V_{ANA}$ | +4.75 | +5 | +5.25 | * | * | * | V |
| $V_{ANA}$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| $I_{DIG}$ | | | 0.6 | | | * | | mA |
| $I_{ANA}$ | | | 5.0 | | | * | | mA |
| Power Dissipation | $V_{ANA}$ = $V_{DIG}$ = 5V, $f_S$ = 40kHz | | 28 | 35 | | * | * | mW |
| | REFD HIGH | | 23 | | | * | | mW |
| | PWRD and REFD HIGH | | 50 | | | * | | µW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | * | | * | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| DIP | | | 75 | | | * | | °C/W |
| SO | | | 75 | | | * | | °C/W |

* Specifications same as ADS7806 P, U.

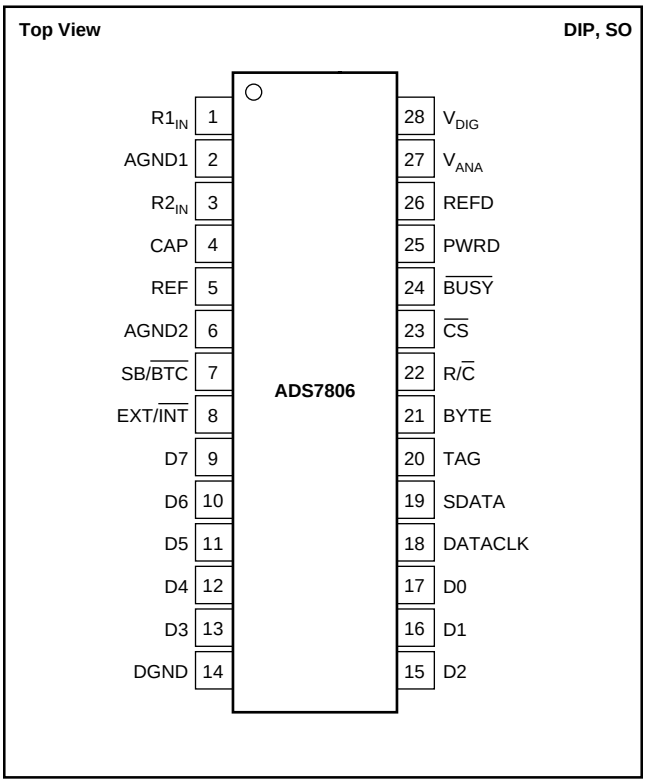
NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 4.88mV. (2) Typical rms noise at worst-case transition. (3) As measured with fixed resistors, see Figure 7b. Adjustable to zero with external potentiometer. (4) Full-scale error is the worst case of –Full-Scale or +Full-Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) This is the time delay after the ADS7806 is brought out of Power-Down mode until all internal settling occurs and the analog input is acquired to rated accuracy. A Convert command after this delay will yield accurate results. (6) All specifications in dB are referred to a full-scale input. (7) Usable bandwidth defined as full-scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (8) Recovers to specified performance after 2 • FS input overvoltage. (9) The minimum $V_{IH}$ level for the DATACLK signal is 3V.

## PIN DESCRIPTIONS

| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $R1_{IN}$ | | Analog Input. See Figure 7. |
| 2 | AGND1 | | Analog Sense Ground |
| 3 | $R2_{IN}$ | | Analog Input. See Figure 7. |
| 4 | CAP | | Reference Buffer Output. 2.2µF tantalum capacitor to ground. |
| 5 | REF | | Reference Input/Output. 2.2µF tantalum capacitor to ground. |
| 6 | AGND2 | | Analog Ground |
| 7 | SB/$\overline{BTC}$ | I | Selects Straight Binary or Binary Two's Complement for Output Data Format. |
| 8 | EXT/$\overline{INT}$ | I | External/Internal data clock select. |
| 9 | D7 | O | Data Bit 3 if BYTE is HIGH. Data bit 11 (MSB) if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. Leave unconnected when using serial output. |
| 10 | D6 | O | Data Bit 2 if BYTE is HIGH. Data bit 10 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 11 | D5 | O | Data Bit 1 if BYTE is HIGH. Data bit 9 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 12 | D4 | O | Data Bit 0 (LSB) if BYTE is HIGH. Data bit 8 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 13 | D3 | O | LOW if BYTE is HIGH. Data bit 7 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 14 | DGND | | Digital Ground |
| 15 | D2 | O | LOW if BYTE is HIGH. Data bit 6 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 16 | D1 | O | LOW if BYTE is HIGH. Data bit 5 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 17 | D0 | O | LOW if BYTE is HIGH. Data bit 4 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. |
| 18 | DATACLK | I/O | Data Clock Output when EXT/$\overline{INT}$ is LOW. Data clock input when EXT/$\overline{INT}$ is HIGH. |
| 19 | SDATA | O | Serial Output Synchronized to DATACLK |
| 20 | TAG | I | Serial Input When Using an External Data Clock |
| 21 | BYTE | I | Selects 8 most significant bits (LOW) or 4 least significant bits (HIGH) on parallel output pins. |
| 22 | R/$\overline{C}$ | I | With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output. |
| 23 | $\overline{CS}$ | I | Internally OR'ed with R/$\overline{C}$. If R/$\overline{C}$ is LOW, a falling edge on $\overline{CS}$ initiates a new conversion. If EXT/$\overline{INT}$ is LOW, this same falling edge will start the transmission of serial data results from the previous conversion. |
| 24 | $\overline{BUSY}$ | O | At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated. |
| 25 | PWRD | I | PWRD HIGH shuts down all analog circuitry except the reference. Digital circuitry remains active. |
| 26 | REFD | I | REFD HIGH shuts down the internal reference. External reference will be required for conversions. |
| 27 | $V_{ANA}$ | | Analog Supply. Nominally +5V. Decouple with 0.1µF ceramic and 10µF tantalum capacitors. |
| 28 | $V_{DIG}$ | | Digital Supply. Nominally +5V. Connect directly to pin 27. Must be ≤ $V_{ANA}$. |

## PIN CONFIGURATION

**Top View** **DIP, SO**



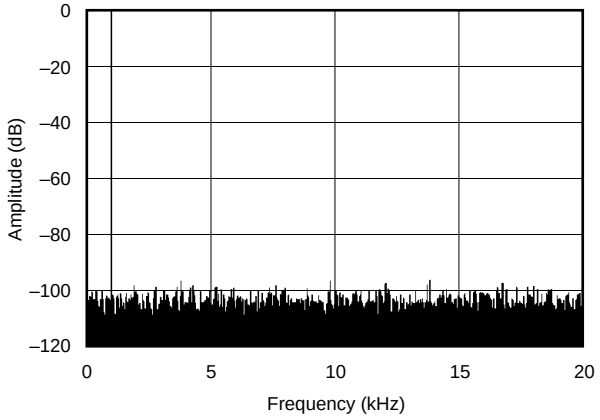

| ANALOG INPUT RANGE | CONNECT $R1_{IN}$ VIA 200Ω TO | CONNECT $R2_{IN}$ VIA 100Ω TO | IMPEDANCE |
|---|---|---|---|
| ±10V | $V_{IN}$ | CAP | 45.7kΩ |
| 0V to 5V | AGND | $V_{IN}$ | 20.0kΩ |
| 0V to 4V | $V_{IN}$ | $V_{IN}$ | 21.4kΩ |

TABLE I. Input Range Connections. See Figure 7.

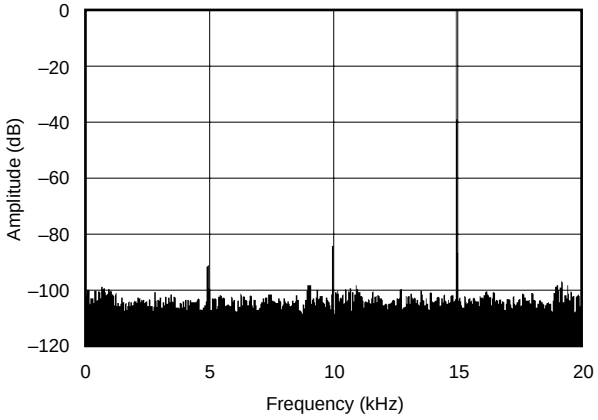
# TYPICAL CHARACTERISTICS

$T_A$ = +25°C, $f_S$ = 40kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, and using internal reference and fixed resistors (see Figure 7b), unless otherwise specified.

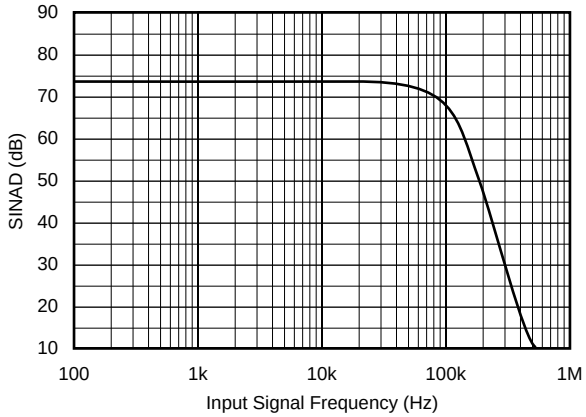
FREQUENCY SPECTRUM
(8192 Point FFT; $f_{IN}$ = 1kHz, 0dB)



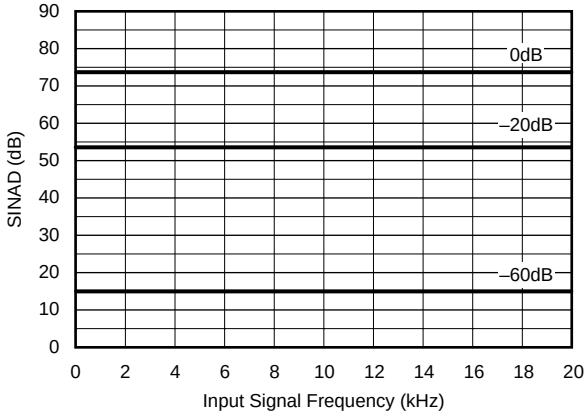

FREQUENCY SPECTRUM
(8192 Point FFT; $f_{IN}$ = 15kHz, 0dB)



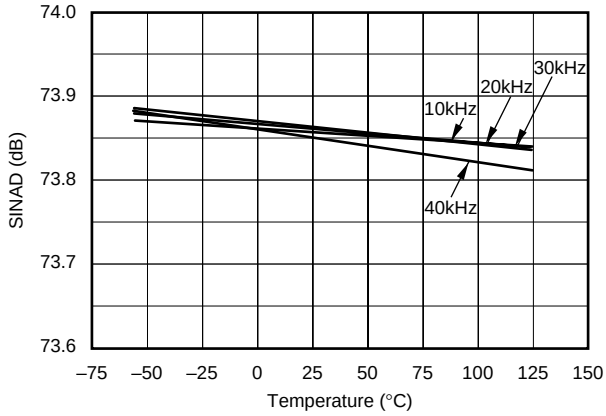

SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY ($f_{IN}$ = 0dB)



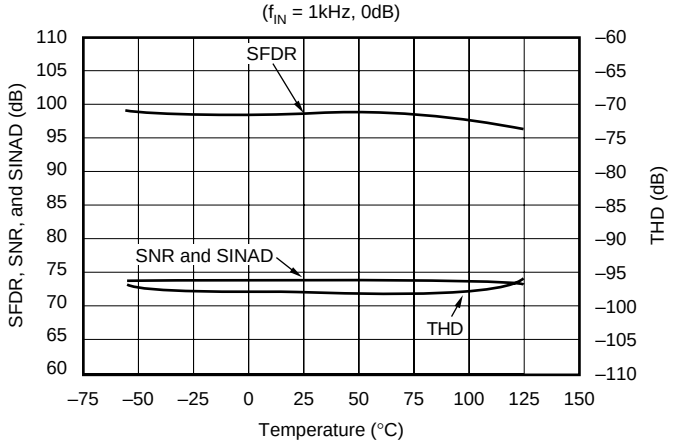

SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY AND INPUT AMPLITUDE




SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE
($f_{IN}$ = 1kHz, 0dB; $f_S$ = 10kHz to 40kHz)

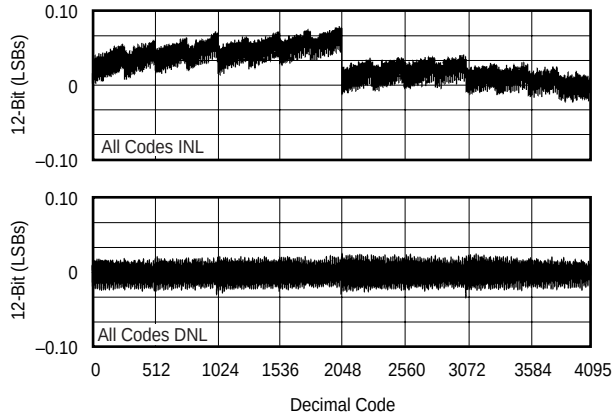



AC PARAMETERS vs TEMPERATURE
($f_{IN}$ = 1kHz, 0dB)

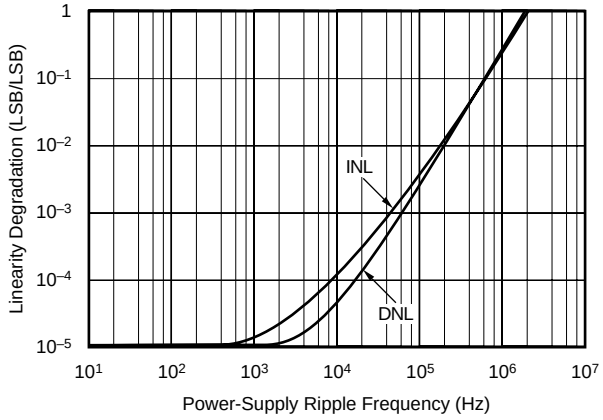


# TYPICAL CHARACTERISTICS (Cont.)

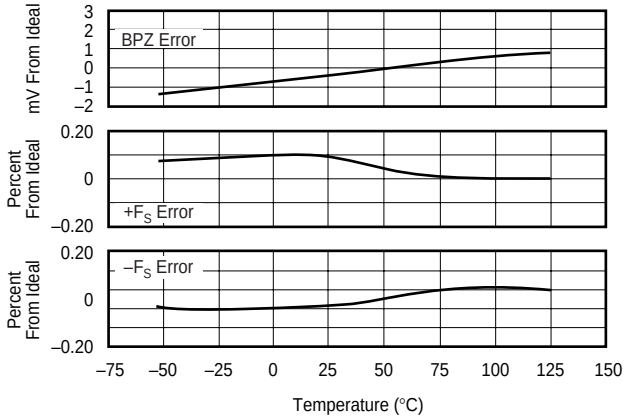
$T_A$ = +25°C, $f_S$ = 40kHz, $V_{DIG}$ = $V_{ANA}$ = +5V, and using internal reference and fixed resistors (see Figure 7b), unless otherwise specified.



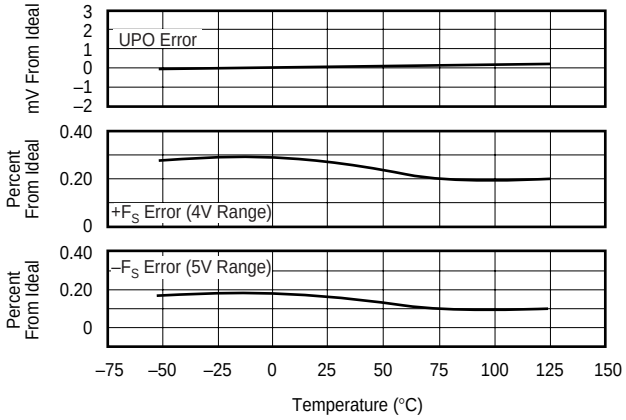

POWER-SUPPLY RIPPLE SENSITIVITY
INL/DNL DEGRADATION PER LSB OF P-P RIPPLE



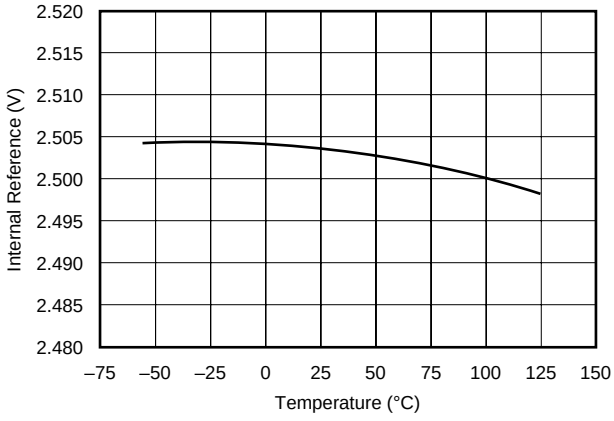

ENDPOINT ERRORS (20V Bipolar Range)



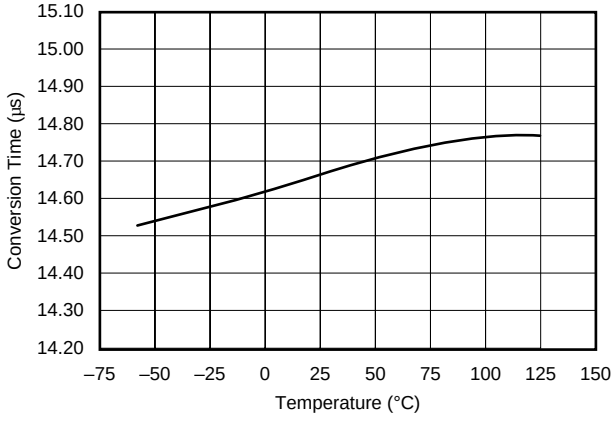

ENDPOINT ERRORS (Unipolar Ranges)




INTERNAL REFERENCE VOLTAGE vs TEMPERATURE




CONVERSION TIME vs TEMPERATURE



# BASIC OPERATION

### PARALLEL OUTPUT

Figure 1a shows a basic circuit to operate the ADS7806 with a ±10V input range and parallel output. Taking R/$\overline{C}$ (pin 22) LOW for 40ns (12µs max) will initiate a conversion. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until the conversion is completed and the output register is updated. If BYTE (pin 21) is LOW, the eight Most Significant Bits (MSBs) will be valid when $\overline{BUSY}$ rises; if BYTE is HIGH, the four Least Significant Bits (LSBs) will be valid when $\overline{BUSY}$ rises. Data will be output in Binary Two's Complement (BTC) format. $\overline{BUSY}$ going HIGH can be used to latch the data. After the first byte has been read, BYTE can be toggled allowing the remaining byte to be read. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the Calibration section).

### SERIAL OUTPUT

Figure 1b shows a basic circuit to operate the ADS7806 with a ±10V input range and serial output. Taking R/$\overline{C}$ (pin 22) LOW for 40ns (12µs max) will initiate a conversion and output valid data from the previous conversion on SDATA (pin 19) synchronized to 12 clock pulses output on DATACLK (pin 18). $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until the conversion is completed and the serial data has been transmitted. Data will be output in BTC format, MSB first, and will be valid on both the rising and falling edges of the data clock. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

# STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 23) and R/$\overline{C}$ (pin 22) LOW for a minimum of 40ns immediately puts the sample-and-hold of the ADS7806 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH, or a new conversion will be initiated without sufficient time to acquire a new signal.

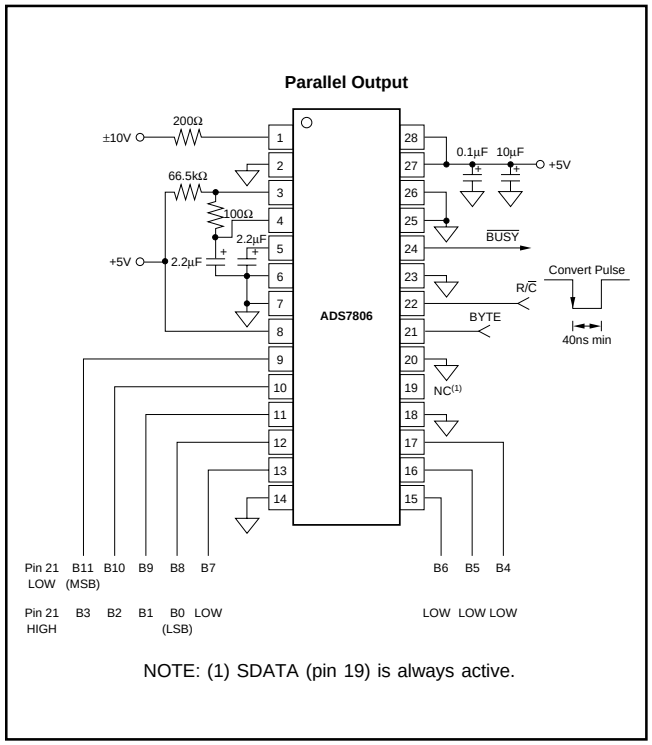



FIGURE 1a. Basic ±10V Operation, both Parallel and Serial Output.

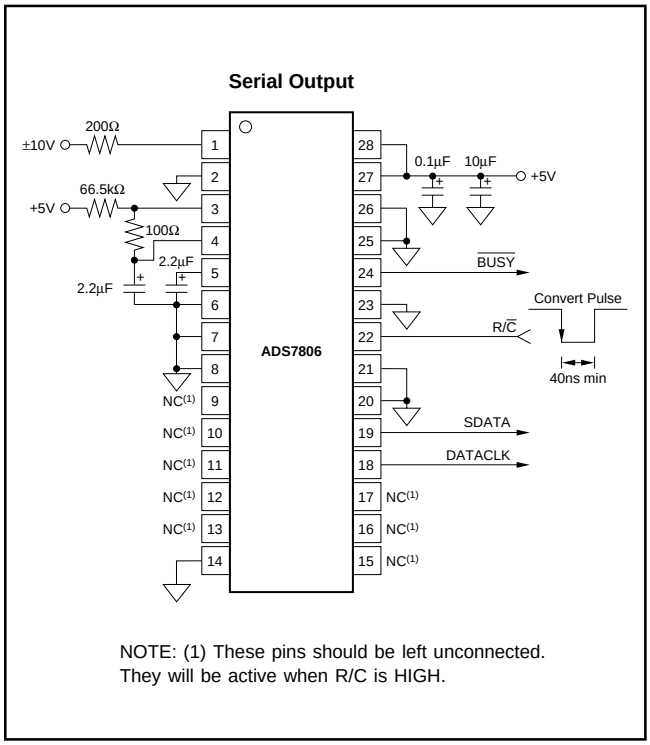



FIGURE 1b. Basic ±10V Operation with Serial Output.

The ADS7806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal. Refer to Tables II and III for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states, and Figures 2 through 6 for timing diagrams.

| $\overline{CS}$ | R/$\overline{C}$ | $\overline{BUSY}$ | OPERATION |
|---|---|---|---|
| 1 | X | X | None. Databus is in Hi-Z state. |
| ↓ | 0 | 1 | Initiates conversion 'n'. Databus remains in Hi-Z state. |
| 0 | ↓ | 1 | Initiates conversion 'n'. Databus enters Hi-Z state. |
| 0 | 1 | ↑ | Conversion 'n' completed. Valid data from conversion 'n' on the databus. |
| ↓ | 1 | 1 | Enables databus with valid data from conversion 'n'. |
| ↓ | 1 | 0 | Enables databus with valid data from conversion 'n – 1'(1). Conversion 'n' in progress. |
| 0 | ↑ | 0 | Enables databus with valid data from conversion 'n – 1'(1). Conversion 'n' in progress. |
| 0 | 0 | ↑ | New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH. |
| X | X | 0 | New convert commands ignored. Conversion 'n' in progress. |

NOTE: (1) See Figures 2 and 3 for constraints on data valid from conversion 'n – 1'.

TABLE II. Control Functions When Using Parallel Output (DATACLK tied LOW, EXT/$\overline{INT}$ tied HIGH).

$\overline{CS}$ and R/$\overline{C}$ are internally OR'ed and level triggered. There is no requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input. If EXT/$\overline{INT}$ (pin 8) is LOW when initiating conversion 'n', serial data from conversion 'n – 1' will be output on SDATA (pin 19) following the start of conversion 'n'. See Internal Data Clock in the Reading Data section.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. The parallel output and the serial output (only when using an external data clock), however, will be affected whenever R/$\overline{C}$ goes HIGH. Refer to the Reading Data section.

# READING DATA

The ADS7806 outputs serial or parallel data in Straight Binary (SB) or Binary Two's Complement data output format. If SB/BTC (pin 7) is HIGH, the output will be in SB format, and if LOW, the output will be in BTC format. Refer to Table IV for ideal output codes.

The parallel output can be read without affecting the internal output registers; however, reading the data through the serial port will shift the internal output registers one bit per data clock pulse. As a result, data can be read on the parallel port

| $\overline{CS}$ | R/$\overline{C}$ | $\overline{BUSY}$ | EXT/$\overline{INT}$ | DATACLK | OPERATION |
|---|---|---|---|---|---|
| ↓ | 0 | 1 | 0 | Output | Initiates conversion 'n'. Valid data from conversion 'n – 1' clocked out on SDATA. |
| 0 | ↓ | 1 | 0 | Output | Initiates conversion 'n'. Valid data from conversion 'n – 1' clocked out on SDATA. |
| ↓ | 0 | 1 | 1 | Input | Initiates conversion 'n'. Internal clock still runs conversion process. |
| 0 | ↓ | 1 | 1 | Input | Initiates conversion "n". Internal clock still runs conversion process. |
| ↓ | 1 | 1 | 1 | Input | Conversion 'n' completed. Valid data from conversion 'n' clocked out on SDATA synchronized to external data clock. |
| ↓ | 1 | 0 | 1 | Input | Valid data from conversion 'n – 1' output on SDATA synchronized to external data clock. Conversion 'n' in progress. |
| 0 | ↑ | 0 | 1 | Input | Valid data from conversion 'n – 1' output on SDATA synchronized to external data clock. Conversion 'n' in progress. |
| 0 | 0 | ↑ | X | X | New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH. |
| X | X | 0 | X | X | New convert commands ignored. Conversion "n" in progress. |

NOTE: (1) See Figures 4, 5, and 6 for constraints on data valid from conversion 'n – 1'.

TABLE III. Control Functions When Using Serial Output.

| DESCRIPTION | ANALOG INPUT | | | DIGITAL OUTPUT | | | |
|---|---|---|---|---|---|---|---|
| | | | | BINARY TWO'S COMPLEMENT (SB/$\overline{BTC}$ LOW) | | STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH) | |
| Full-Scale Range<br>Least Significant Bit (LSB) | ±10<br>4.88mV | 0V to 5V<br>1.22mV | 0V to 4V<br>976µV | BINARY CODE | HEX CODE | BINARY CODE | HEX CODE |
| +Full-Scale (FS – 1LSB) | 9.99512V | 4.99878V | 3.999024V | 0111 1111 1111 1111 | 7FF | 1111 1111 1111 1111 | FFF |
| Midscale | 0V | 2.5V | 2V | 0000 0000 0000 0000 | 000 | 1000 0000 0000 0000 | 800 |
| One LSB Below Midscale | –4.88mV | 2.49878V | 1.999024V | 1111 1111 1111 1111 | FFF | 0111 1111 1111 1111 | 7FF |
| –Full-Scale | –10V | 0V | 0V | 1000 0000 0000 0000 | 800 | 0000 0000 0000 0000 | 000 |

TABLE IV. Output Codes and Ideal Input Voltages.

prior to reading the same data on the serial port, but data cannot be read through the serial port prior to reading the same data on the parallel port.

## PARALLEL OUTPUT

To use the parallel output, tie EXT/$\overline{INT}$ (pin 8) HIGH and DATACLK (pin 18) LOW. SDATA (pin 19) should be left unconnected. The parallel output will be active when R/$\overline{C}$ (pin 22) is HIGH and $\overline{CS}$ (pin 23) is LOW. Any other combination of $\overline{CS}$ and R/C will tri-state the parallel output. Valid conversion data can be read in two 8-bit bytes on D7-D0 (pins 9-13 and 15-17). When BYTE (pin 21) is LOW, the eight most significant bits will be valid with the MSB on D7. When BYTE is HIGH, the four least significant bits will be valid with the LSB on D4. BYTE can be toggled to read both bytes within one conversion cycle.

Upon initial power up, the parallel output will contain indeterminate data.

## PARALLEL OUTPUT (AFTER A CONVERSION)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) will go HIGH. Valid data from conversion 'n' will be available on D7-D0 (pins 9-13 and 15-17). $\overline{BUSY}$ going high can be used to latch the data. Refer to Table V and Figures 2 and 3 for timing constraints.

## PARALLEL OUTPUT (DURING A CONVERSION)

After conversion 'n' has been initiated, valid data from conversion 'n – 1' can be read and will be valid up to 12µs after the start of conversion 'n'. Do not attempt to read data beyond 12µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 24) goes HIGH; this may result in reading invalid data. Refer to Table V and Figures 2 and 3 for timing constraints.

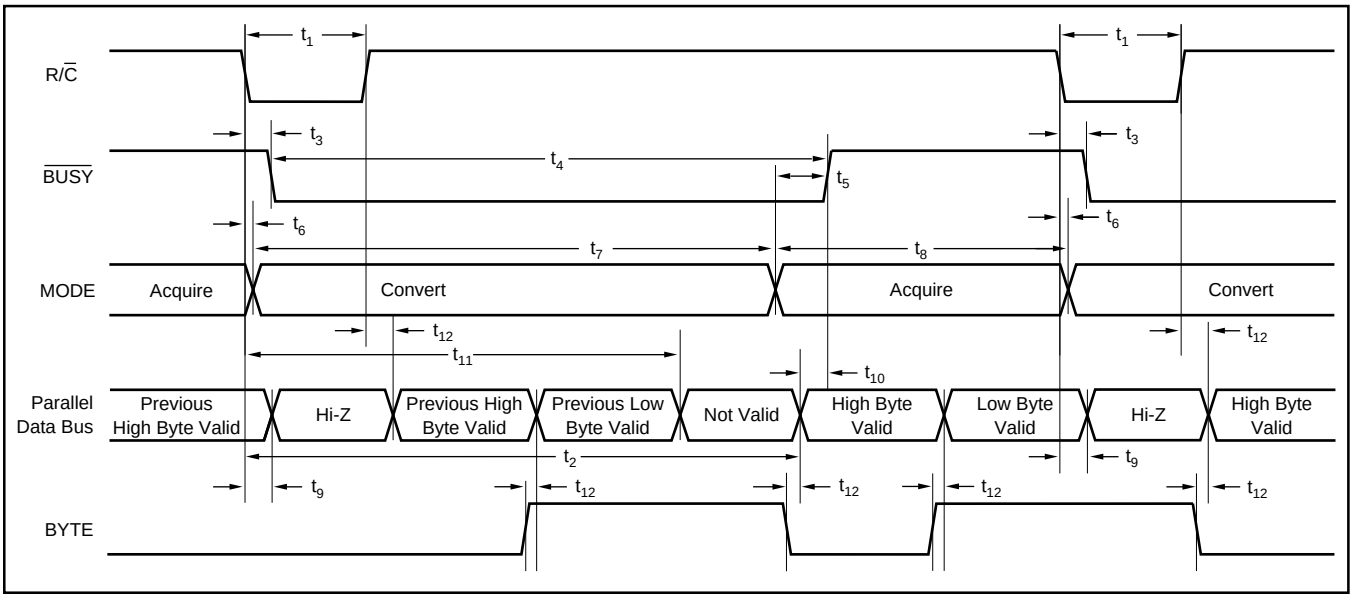



FIGURE 2. Conversion Timing with Parallel Output ($\overline{CS}$ and DATACLK tied LOW, EXT/$\overline{INT}$ tied HIGH).

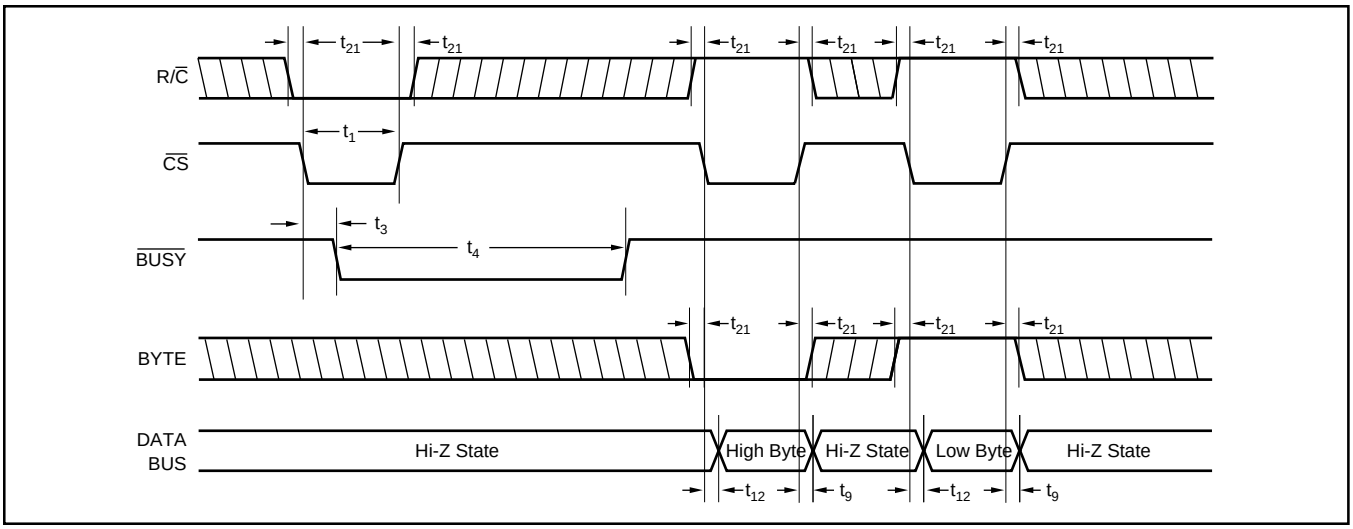



FIGURE 3. Using $\overline{CS}$ to Control Conversion and Read Timing with Parallel Outputs.

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_1$ | Convert Pulse Width | 0.04 | | 12 | µs |
| $t_2$ | Data Valid Delay after R/$\overline{C}$ LOW | | 14.7 | 20 | µs |
| $t_3$ | $\overline{BUSY}$ Delay from Start of Conversion | | | 85 | ns |
| $t_4$ | $\overline{BUSY}$ LOW | | 14.7 | 20 | µs |
| $t_5$ | $\overline{BUSY}$ Delay after End of Conversion | | 90 | | ns |
| $t_6$ | Aperture Delay | | 40 | | ns |
| $t_7$ | Conversion Time | | 14.7 | 20 | µs |
| $t_8$ | Acquisition Time | | | 5 | µs |
| $t_9$ | Bus Relinquish Time | 10 | | 83 | ns |
| $t_{10}$ | $\overline{BUSY}$ Delay after Data Valid | 20 | 60 | | ns |
| $t_{11}$ | Previous Data Valid after Start of Conversion | 12 | 14.7 | | µs |
| $t_{12}$ | Bus Access Time and $\overline{BUSY}$ Delay | | | 83 | ns |
| $t_{13}$ | Start of Conversion to DATACLK Delay | | 1.4 | | µs |
| $t_{14}$ | DATACLK Period | | 1.1 | | µs |
| $t_{15}$ | Data Valid to DATACLK HIGH Delay | 20 | 75 | | ns |
| $t_{16}$ | Data Valid after DATACLK LOW Delay | 400 | 600 | | ns |
| $t_{17}$ | External DATACLK Period | 100 | | | ns |
| $t_{18}$ | External DATACLK LOW | 40 | | | ns |
| $t_{19}$ | External DATACLK HIGH | 50 | | | ns |
| $t_{20}$ | $\overline{CS}$ and R/$\overline{C}$ to External DATACLK Setup Time | 25 | | | ns |
| $t_{21}$ | R/$\overline{C}$ to $\overline{CS}$ Setup Time | 10 | | | ns |
| $t_{22}$ | Valid Data after DATACLK HIGH | 25 | | | ns |
| $t_7 + t_8$ | Throughput Time | | | 25 | µs |

TABLE V. Conversion and Data Timing. $T_A$ = –40°C to +85°C.

## SERIAL OUTPUT

Data can be clocked out with the internal data clock or an external data clock. When using serial output, be careful with the parallel outputs, D7-D0 (pins 9-13 and 15-17), as these pins will come out of Hi-Z state whenever $\overline{CS}$ (pin 23) is LOW and R/$\overline{C}$ (pin 22) is HIGH. The serial output can not be tri-stated and is always active.

## INTERNAL DATA CLOCK

### (During A Conversion)

To use the internal data clock, tie EXT/$\overline{INT}$ (pin 8) LOW. The combination of R/$\overline{C}$ (pin 22) and $\overline{CS}$ (pin 23) LOW will initiate conversion ‘n’ and activate the internal data clock (typically a 900kHz clock rate). The ADS7806 will output 12 bits of valid data, MSB first, from conversion ‘n – 1’ on SDATA (pin 19), synchronized to 12 clock pulses output on DATACLK (pin 18). The data will be valid on both the rising and falling edges of the internal data clock. The rising edge of $\overline{BUSY}$ (pin 24) can be used to latch the data. After the 12th clock pulse, DATACLK will remain LOW until the next conversion is initiated, while SDATA will go to whatever logic level was input on TAG (pin 20) during the first clock pulse. Refer to Table VI and Figure 4.

## EXTERNAL DATA CLOCK

To use an external data clock, tie EXT/$\overline{INT}$ (pin 8) HIGH. The external data clock is not a conversion clock; it can only be used as a data clock. To enable the output mode of the ADS7806, $\overline{CS}$ (pin 23) must be LOW and R/$\overline{C}$ (pin 22) must be HIGH. DATACLK must be HIGH for 20% to 70% of the total data clock period; the clock rate can be between DC and 10MHz. Serial data from conversion ‘n’ can be output on SDATA (pin 19) after conversion ‘n’ is completed or during conversion ‘n + 1’.

An obvious way to simplify control of the converter is to tie $\overline{CS}$ LOW and use R/$\overline{C}$ to initiate conversions. While this is perfectly acceptable, there is a possible problem when using an external data clock. At an indeterminate point from 12µs after the start of conversion ‘n’ until $\overline{BUSY}$ rises, the internal logic will shift the results of conversion ‘n’ into the output register. If $\overline{CS}$ is LOW, R/$\overline{C}$ is HIGH, and the external clock is HIGH at this point, data will be lost. So, with $\overline{CS}$ LOW, either R/$\overline{C}$ and/or DATACLK must be LOW during this period to avoid losing valid data.

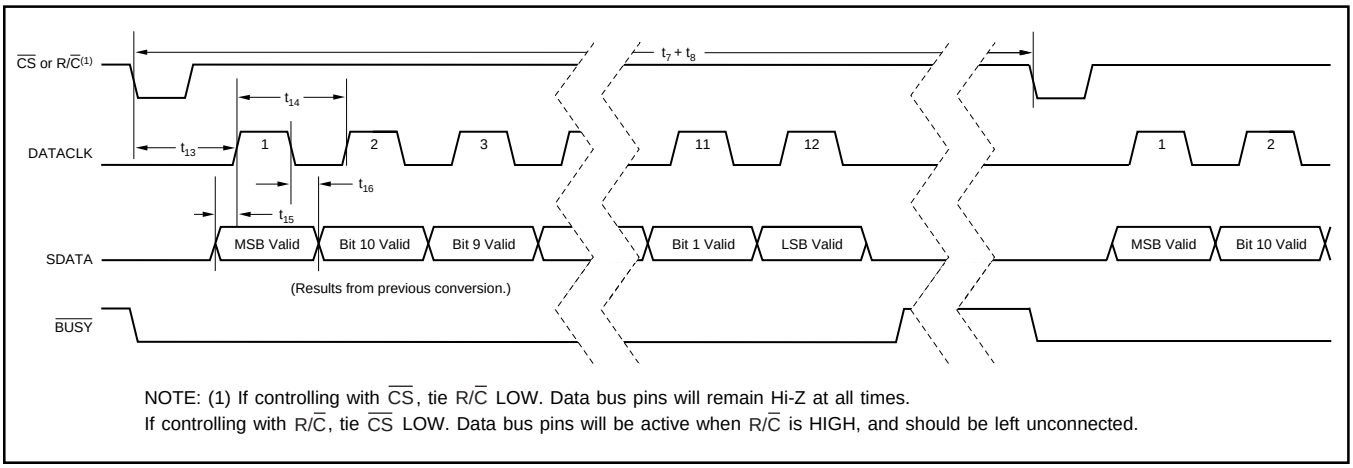



FIGURE 4. Serial Data Timing Using Internal Data Clock (TAG tied LOW).

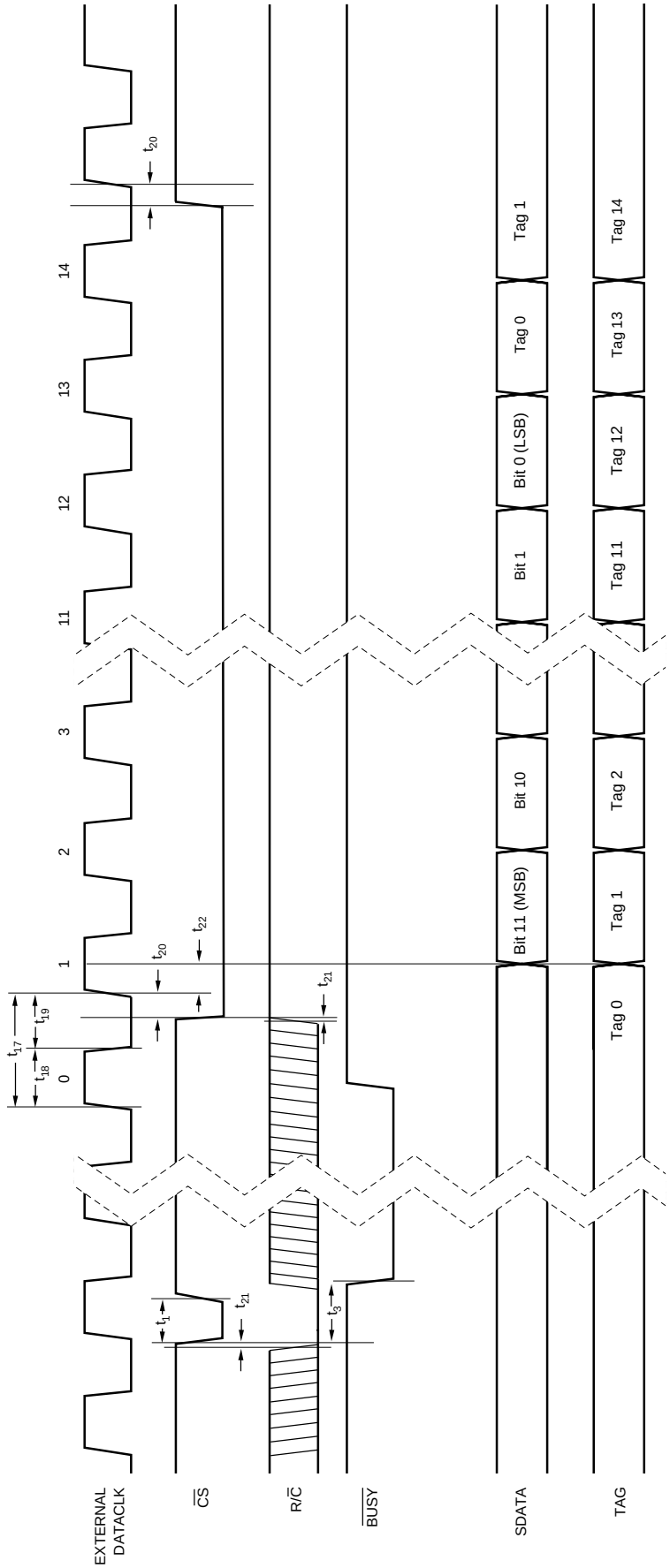



FIGURE 5. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ Tied HIGH) Read after Conversion.

### EXTERNAL DATA CLOCK

### (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) will go HIGH. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, valid data from conversion 'n' will be output on SDATA (pin 19) synchronized to the external data clock input on DATACLK (pin 18). The MSB will be valid on the first falling edge and the second rising edge of the external data clock. The LSB will be valid on the 12th falling edge and 13th rising edge of the data clock. TAG (pin 20) will input a bit of data for every external clock pulse. The first bit input on TAG will be valid on SDATA on the 13th falling edge and the 14th rising edge of DATACLK; the second input bit will be valid on the 14th falling edge and the 15th rising edge, etc. With a continuous data clock, TAG data will be output on SDATA until the internal output registers are updated with the results from the next conversion. Refer to Table V and Figure 5.

### EXTERNAL DATA CLOCK

### (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n – 1' can be read and will be valid up to 12µs after the start of conversion 'n'. Do not attempt to clock out data from 12µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 24) rises; this will result in data loss. NOTE: For the best possible performance when using an external data clock, data should not be clocked out during a conversion. The switching noise of the asynchronous data clock can cause digital feedthrough degrading the converter's performance. Refer to Table VI and Figure 6.

### TAG FEATURE

TAG (pin 20) inputs serial data synchronized to the external or internal data clock.

When using an external data clock, the serial bit stream input on TAG will follow the LSB output on SDATA until the internal output register is updated with new conversion results. See Table VI and Figures 5 and 6.

The logic level input on TAG for the first rising edge of the internal data clock will be valid on SDATA after all 12 bits of valid data have been output.

# INPUT RANGES

The ADS7806 offers three input ranges: standard ±10V, 0V-5V, and a 0V-4V range for complete, single-supply systems. See Figures 7a and 7b for the necessary circuit connections for implementing each input range and optional offset and gain adjust circuitry. Offset and full-scale error(1) specifications are tested with the fixed resistors, see Figure 7b. Adjustments for offset and gain are described in the Calibration section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the Calibration section).

The input impedance, summarized in Table II, results from the combination of the internal resistor network (see the front page of this data sheet) and the external resistors used for

NOTE: (1) Full-scale error includes offset and gain errors measured at both +FS and –FS.

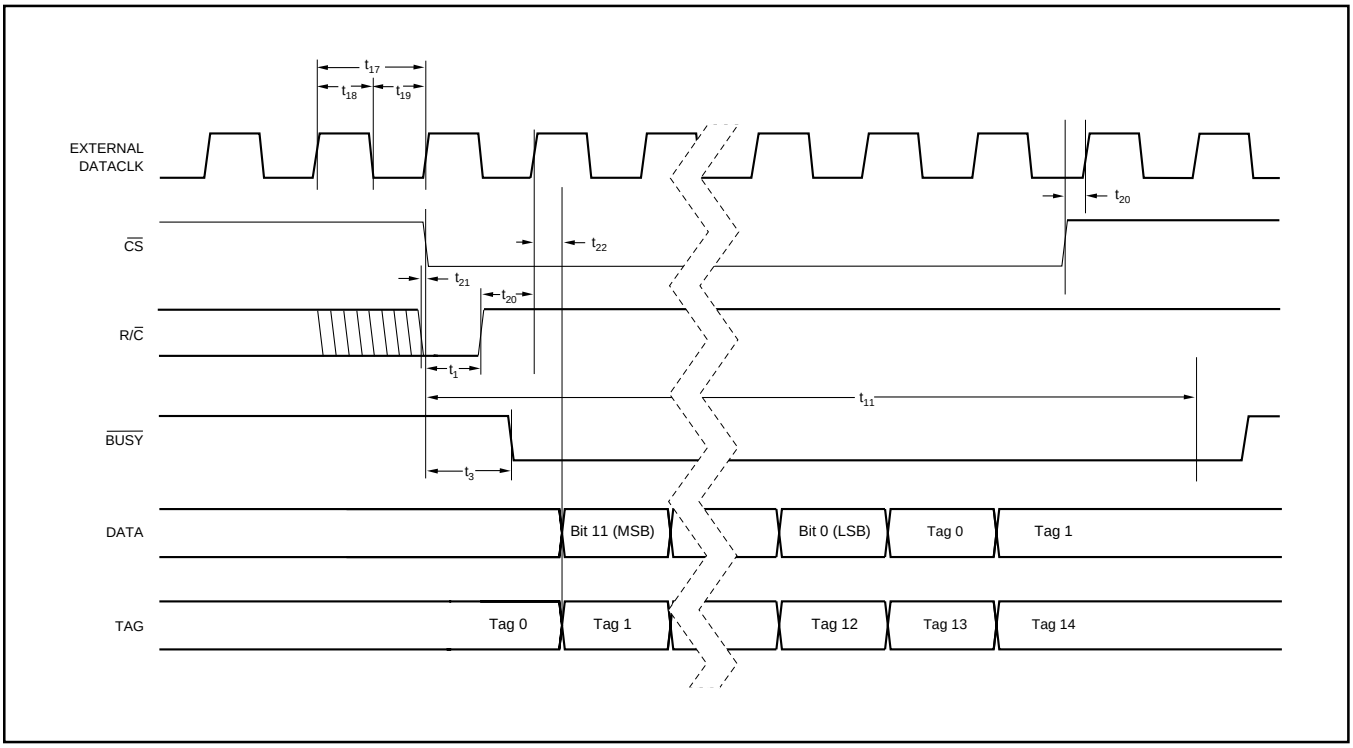



FIGURE 6. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ tied HIGH) Read During a Conversion.

each input range (see Figure 8). The input resistor divider network provides inherent over-voltage protection to at least ±12V on $R1_{IN}$ and ±5.5V on $R2_{IN}$.

Analog inputs above or below the expected range will yield either positive full-scale or negative full-scale digital outputs, respectively. There will be no wrapping or folding over for analog inputs outside the nominal range.

# CALIBRATION

## HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7806 in hardware, install the resistors shown in Figure 7a. Table VI lists the hardware trim ranges relative to the input for each input range.

## SOFTWARE CALIBRATION

To calibrate the offset and gain in software, no external resistors are required. However, to get the data sheet specifications for offset and gain, the resistors shown in Figure 7b are necessary. See the No Calibration section for more details on the external resistors. Refer to Table VII for the range of offset and gain errors with and without the external resistors.

| INPUT RANGE | OFFSET ADJUST RANGE (mV) | GAIN ADJUST RANGE (mV) |
|---|---|---|
| ±10V | ±15 | ±60 |
| 0 to 5V | ±4 | ±30 |
| 0 to 4V | ±3 | ±30 |

TABLE VI. Offset and Gain Adjust Ranges for Hardware Calibration (see Figure 7a).

## NO CALIBRATION

Figure 7b shows circuit connections. Note that the actual voltage dropped across the external resistors is at least two orders of magnitude lower than the voltage dropped across the internal resistor divider network. This should be consid-

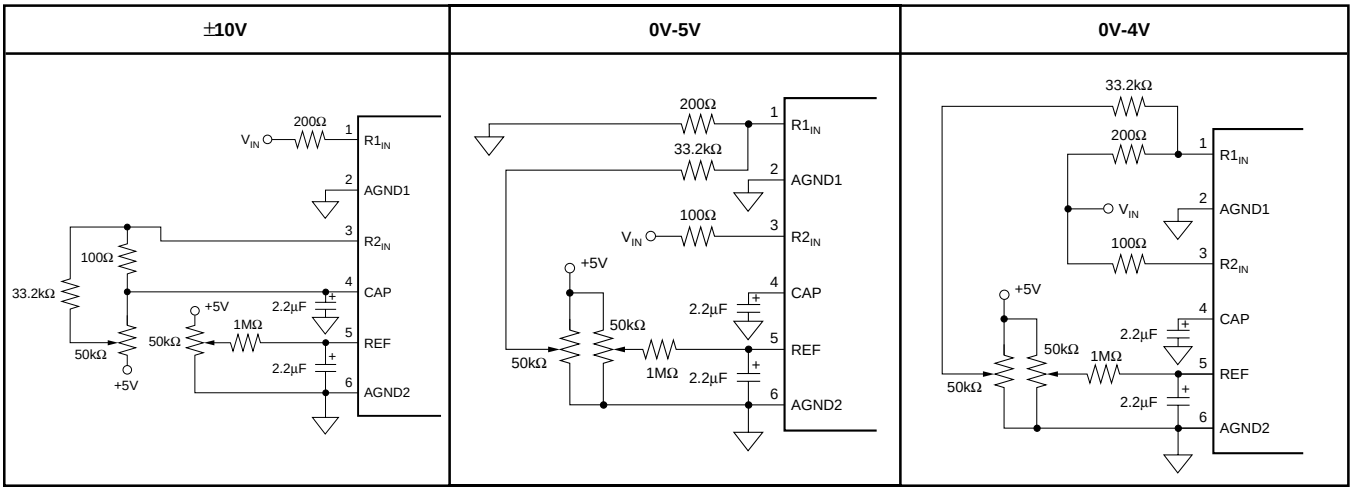



FIGURE 7a. Circuit Diagrams (With Hardware Trim).

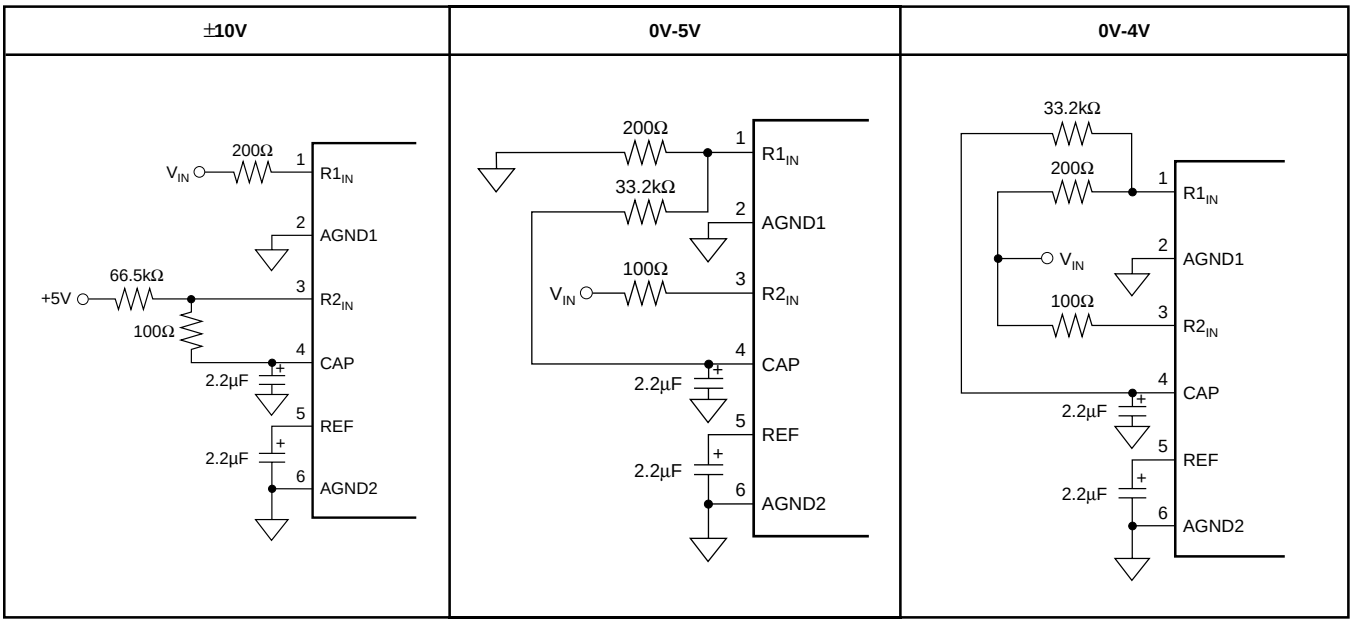



FIGURE 7b. Circuit Diagrams (Without Hardware Trim).

ered when choosing the accuracy and drift specifications of the external resistors. In most applications, 1% metal-film resistors will be sufficient.

The external resistors, see Figure 7b, may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. Not using the external resistors will result in offset and gain errors in addition to those listed in the electrical characteristics section. Offset refers to the equivalent voltage of the digital output when converting with the input grounded. A positive gain error occurs when the equivalent output voltage of the digital output is larger than the analog input. Refer to Table VII for nominal ranges of gain and offset errors with and without the external resistors. Refer to Figure 8 for typical shifts in the transfer functions which occur when the external resistors are removed.

To further analyze the effects of removing any combination of the external resistors, consider Figure 9. The combination of the external and the internal resistors form a voltage divider which reduces the input signal to a 0.3125V to 2.8125V input range at the Capacitor Digital-to-Analog Converter (CDAC). The internal resistors are laser trimmed to high relative accuracy to meet full specifications. The actual input impedance of the internal resistor network looking into pin 1 or pin 3, however, is only accurate to ±20% due to process variations. This should be taken into account when determining the effects of removing the external resistors.

# REFERENCE

The ADS7806 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed; REFD (pin 26)

| INPUT RANGE (V) | OFFSET ERROR | | | GAIN ERROR | | |
|---|---|---|---|---|---|---|
| | WITH RESISTORS | WITHOUT RESISTORS | | WITH RESISTORS | WITHOUT RESISTORS | |
| | RANGE (mV) | RANGE (mV) | TYP (mV) | RANGE (% FS) | RANGE (% FS) | TYP |
| ±10 | –10 ≤ BPZ ≤ 10 | 0 ≤ BPZ ≤ 35 | +15 | –0.4 ≤ G ≤ 0.4<br>0.15 ≤ G(1) ≤ 0.15 | –0.3 ≤ G ≤ 0.5<br>–0.1 ≤ G(1) ≤ 0.2 | +0.05<br>+0.05 |
| 0 to 5 | –3 ≤ UPO ≤ 3 | –12 ≤ UPO ≤ –3 | –7.5 | –0.4 ≤ G ≤ 0.4<br>0.15 ≤ G(1) ≤ 0.15 | –1.0 ≤ G ≤ 0.1<br>–0.55 ≤ G(1) ≤ –0.05 | –0.2<br>–0.2 |
| 0 to 4 | –3 ≤ UPO ≤ 3 | –10.5 ≤ UPO ≤ –1.5 | –6 | –0.4 ≤ G ≤ 0.4<br>–0.15 ≤ G(1) ≤ 0.15 | –1.0 ≤ G ≤ 0.1<br>–0.55 ≤ G(1) ≤ –0.05 | –0.2<br>–0.2 |
| NOTE: (1) High Grade. | | | | | | |

TABLE VII. Range of Offset and Gain Errors With and Without External Resistors

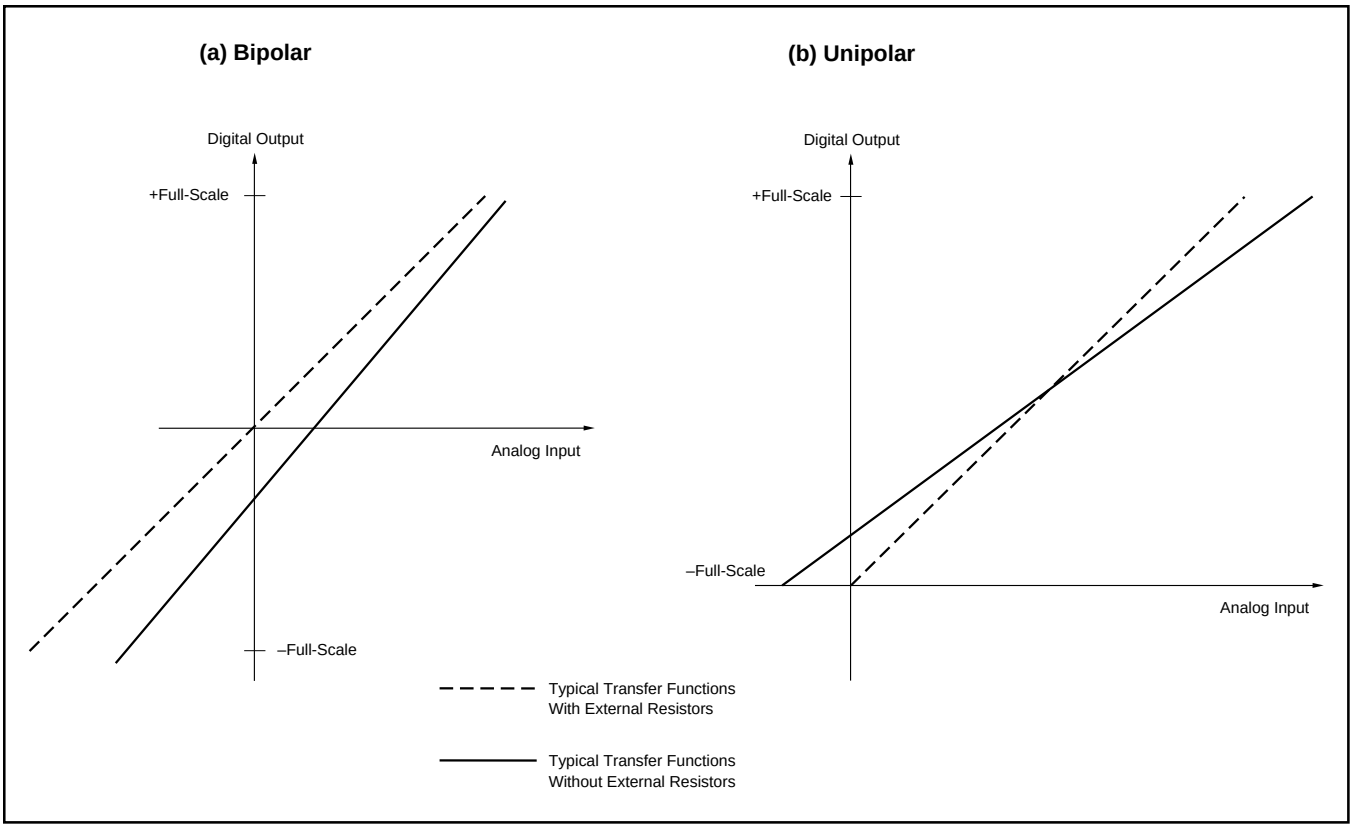



FIGURE 8. Typical Transfer Functions With and Without External Resistors.

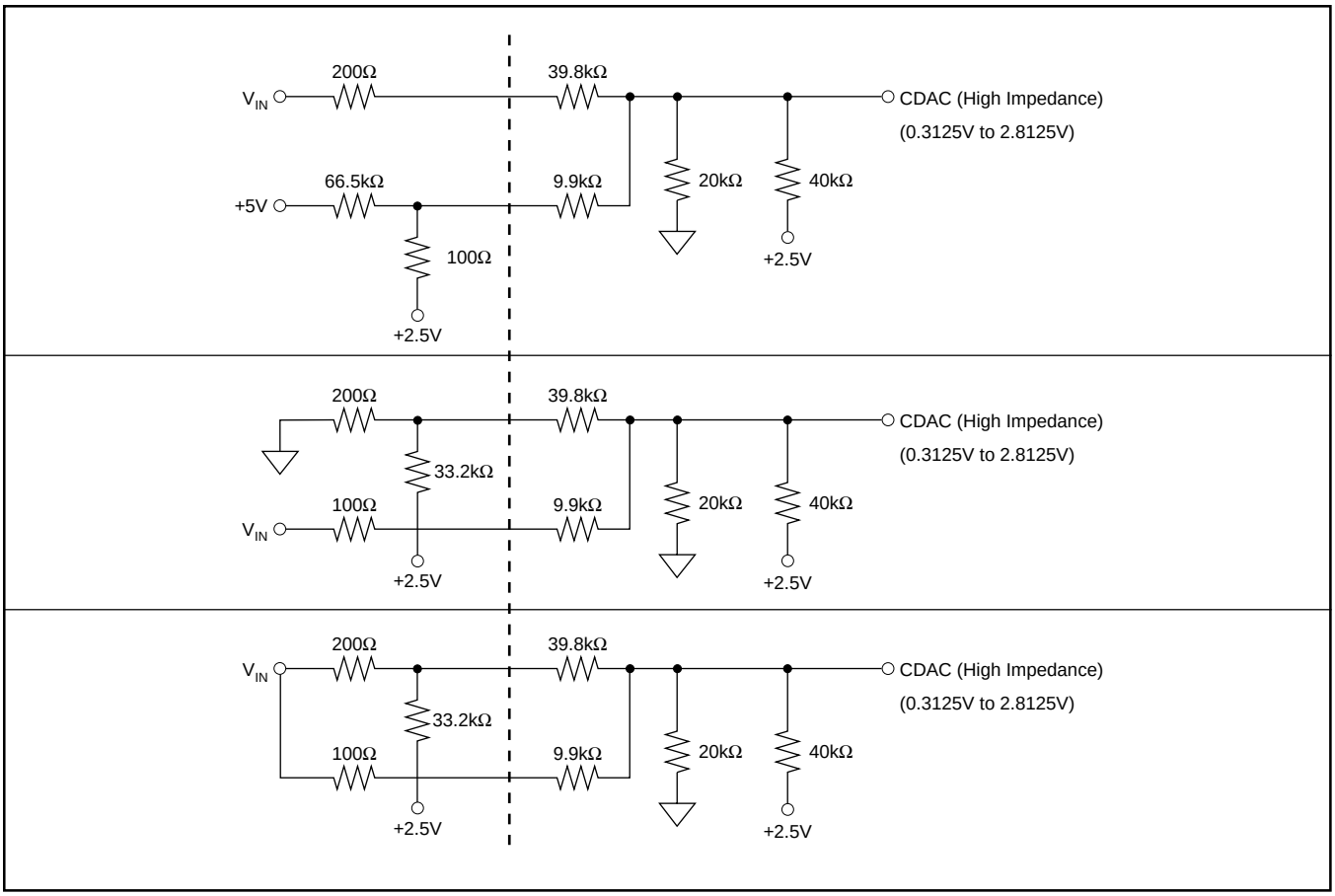



FIGURE 9. Circuit Diagrams Showing External and Internal Resistors.

tied HIGH will power-down the internal reference reducing the overall power consumption of the ADS7806 by approximately 5mW.

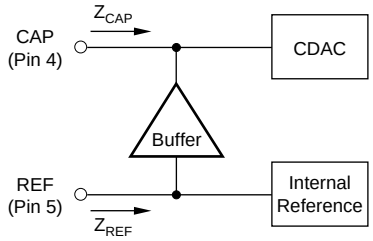
The internal reference has approximately an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full-scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

The ADS7806 also has an internal buffer for the reference voltage. Figure 10 shows characteristic impedances at the input and output of the buffer with all combinations of power-down and reference down.

## REF

REF (pin 5) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF tantalum capacitor should be connected as close as possible to the REF pin from ground. This capacitor and the output resistance of REF create a low-pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference, degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads, as shown in Figure 10.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full-scale range and the LSB size of the converter which can improve the SNR.




| | PWRD 0 REFD 0 | PWRD 0 REFD 1 | PWRD 1 REFD 0 | PWRD 1 REFD 1 |
|---|---|---|---|---|
| $Z_{CAP}$ (Ω) | 1 | 1 | 200 | 200 |
| $Z_{REF}$ (Ω) | 6k | 100M | 6k | 100M |

FIGURE 10. Characteristic Impedances of Internal Buffer.

## CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF tantalum capacitor should be placed as close as possible to the CAP pin from ground to provide optimum switching currents for the CDAC throughout the conversion

cycle. This capacitor also provides compensation for the output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance. See Figures 10 and 11.

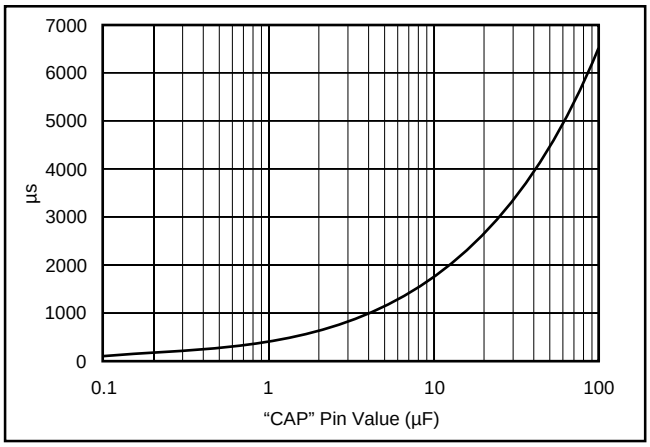



FIGURE 11. Power-Down to Power-Up Time vs Capacitor Value on CAP.

The output of the buffer is capable of driving up to 1mA of current to a DC load. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

# REFERENCE AND POWER-DOWN

The ADS7806 has analog power-down and reference power down capabilities via PWRD (pin 25) and REFD (pin 26), respectively. PWRD and REFD HIGH will power-down all analog circuitry maintaining data from the previous conversion in the internal registers, provided that the data has not already been shifted out through the serial port. Typical power consumption in this mode is 50µW. Power recovery is typically 1ms, using a 2.2µF capacitor connected to CAP. Figure 11 shows power-down to power-up recovery time relative to the capacitor value on CAP. With +5V applied to $V_{DIG}$, the digital circuitry of the ADS7806 remains active at all times, regardless of PWRD and REFD states.

### PWRD

PWRD HIGH will power-down all of the analog circuitry except for the reference. Data from the previous conversion will be maintained in the internal registers and can still be read. With PWRD HIGH, a convert command yields meaningless data.

### REFD

REFD HIGH will power-down the internal 2.5V reference. All other analog circuitry, including the reference buffer, will be active. REFD should be HIGH when using an external reference to minimize power consumption and the loading effects on the external reference. See Figure 10 for the characteristic impedance of the reference buffer's input for both REFD HIGH and LOW. The internal reference consumes approximately 5mW.

# LAYOUT

### POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical characteristics, the ADS7806 uses 90% of its power for the analog circuitry. The ADS7806 should be considered as an analog component.

The +5V power for the A/D converter should be separate from the +5V used for the system's digital logic. Connecting $V_{DIG}$ (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. When using either a filtered digital supply or a regulated analog supply, both $V_{DIG}$ and $V_{ANA}$ should be tied to the same +5V source.

### GROUNDING

Three ground pins are present on the ADS7806. $D_{GND}$ is the digital supply ground. $A_{GND2}$ is the analog supply ground. $A_{GND1}$ is the ground to which all analog signals internal to the A/D converter are referenced. $A_{GND1}$ is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D converter should be tied to an analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

### SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The amount of charge injection due to the sampling FET switch

on the ADS7806 is approximately 5% to 10% of the amount on similar A/D converters with the charge redistribution Digital-to-Analog Converter (DAC) CDAC architecture. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the drive capability on the signal conditioning preceding the A/D converter. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7806.

The resistive front end of the ADS7806 also provides a specified ±25V over-voltage protection. In most cases, this eliminates the need for external over-voltage protection circuitry.

### INTERMEDIATE LATCHES

The ADS7806 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D converter from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7806 has an internal LSB size of 610µV. Transients from fast switching signals on the parallel port, even when the A/D converter is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance. The effects of this phenomenon will be more obvious when using the pin-compatible ADS7807 or any of the other 16-bit converters in the ADS Family. This is due to the smaller internal LSB size of 38µV.

## APPLICATIONS INFORMATION

### QSPI™ INTERFACING

Figure 12 shows a simple interface between the ADS7806 and any QSPI equipped microcontroller. This interface assumes that the convert pulse does not originate from the microcontroller and that the ADS7806 is the only serial peripheral.

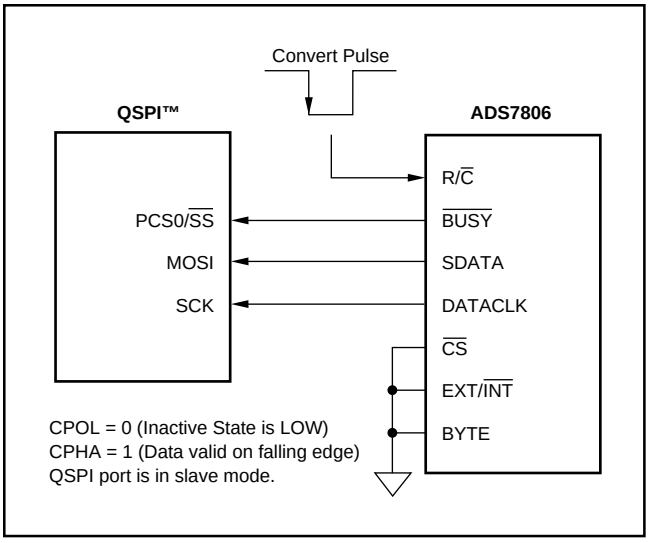



FIGURE 12. QSPI Interface to the ADS7806.

Before enabling the QSPI interface, the microcontroller must be configured to monitor the slave-select line. When a transition from LOW to HIGH occurs on Slave Select ($\overline{SS}$) from $\overline{BUSY}$ (indicating the end of the current conversion), the port can be enabled. If this is not done, the microcontroller and the A/D converter may be "out-of-sync."

Figure 13 shows another interface between the ADS7806 and a QSPI equipped microcontroller. The interface allows the microcontroller to give the convert pulses while also allowing multiple peripherals to be connected to the serial bus. This interface and the following discussion assume a master clock for the QSPI interface of 16.78MHz. Notice that the serial data input of the microcontroller is tied to the MSB (D7) of the ADS7806 instead of the serial output (SDATA). Using D7 instead of the serial port offers tri-state capability which allows other peripherals to be connected to the MISO pin. When communication is desired with those peripherals, PCS0 and PCS1 should be left HIGH; that will keep D7 tri-stated and prevent a conversion from taking place.

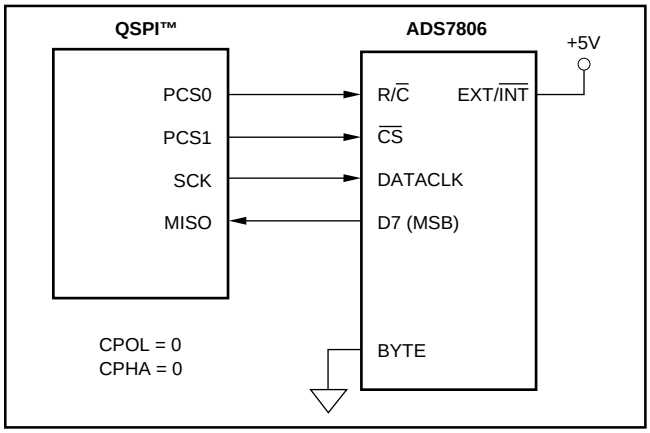



FIGURE 13. QSPI Interface to the ADS7806. Processor Initiates Conversions.

In this configuration, the QSPI interface is actually set to do two different serial transfers. The first, an 8-bit transfer, causes PCS0 (R/$\overline{C}$) and PCS1 ($\overline{CS}$) to go LOW, starting a conversion. The second, a 12-bit transfer, causes only PCS1 ($\overline{CS}$) to go LOW. This is when the valid data will be transferred.

For both transfers, the DT register (delay after transfer) is used to cause a 19µs delay. The interface is also set up to wrap to the beginning of the queue. In this manner, the QSPI is a state machine which generates the appropriate timing for the ADS7806. This timing is thus locked to the crystal-based timing of the microcontroller and not interrupt driven. So, this interface is appropriate for both AC and DC measurements.

For the fastest conversion rate, the baud rate should be set to 2 (4.19MHz SCK), DT set to 10, the first serial transfer set to eight bits, the second set to 12 bits, and DSCK disabled (in the command control byte). This will allow for a 23kHz maximum conversion rate. For slower rates, DT should be increased. Do not slow SCK as this may increase the chance of affecting the conversion results or accidently initiating a second conversion during the first 8-bit transfer.

In addition, CPOL and CPHA should be set to zero (SCK normally LOW and data captured on the rising edge). The command control byte for the 8-bit transfer should be set to $20_H$ and for the 12-bit transfer to $61_H$.

## SPI™ INTERFACE

The SPI interface is generally only capable of 8-bit data transfers. For some microcontrollers with SPI interfaces, it might be possible to receive data in a similar manner as shown for the QSPI interface in Figure 12. The microcontroller will need to fetch the eight most significant bits before the contents are overwritten by the least significant bits.

A modified version of the QSPI interface, see Figure 13, might be possible. For most microcontrollers with SPI interface, the automatic generation of the start-of-conversion pulse will be impossible and will have to be done with software. This will limit the interface to 'DC' applications due to the insufficient jitter performance of the convert pulse tself.

## DSP56000 INTERFACING

The DSP56000 serial interface has an SPI compatibility mode with some enhancements. Figure 14 shows an interface between the ADS7806 and the DSP56000 which is very similar to the QSPI interface seen in Figure 12. As mentioned in the QSPI section, the DSP56000 must be programmed to enable the interface when a LOW-to-HIGH transition on SC1 is observed ($\overline{BUSY}$ going HIGH at the end of conversion).

The DSP56000 can also provide the convert pulse by including a monostable multi-vibrator as seen in Figure 15. The receive and transmit sections of the interface are decoupled (asynchronous mode) and the transmit section is set to generate a word length frame sync every other transmit frame (frame rate divider set to two). The prescale modulus should be set to five.

SPI is a registered trademark of Motorola.

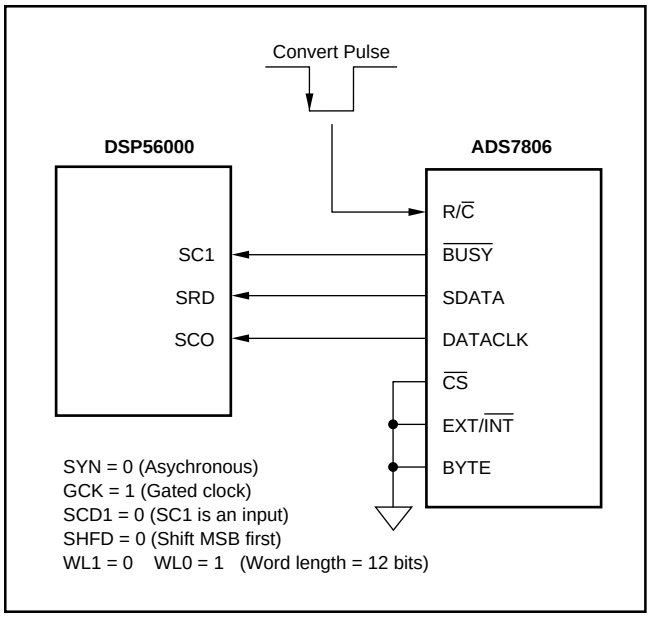



FIGURE 14. DSP56000 Interface to the ADS7806.

The monostable multi-vibrator in this circuit will provide varying pulse widths for the convert pulse. The pulse width will be determined by the external R and C values used with the multi-vibrator. The 74HCT123N data sheet shows that the pulse width is (0.7)RC. Choosing a pulse width as close to the minimum value specified in this data sheet will offer the best performance. See the Starting A Conversion section of this data sheet for details on the conversion pulse width.

The maximum conversion rate for a 20.48MHz DSP56000 is 35.6kHz. If a slower oscillator can be tolerated on the DSP56000, a conversion rate of 40kHz can be achieved by using a 19.2MHz clock and a prescale modulus of four.

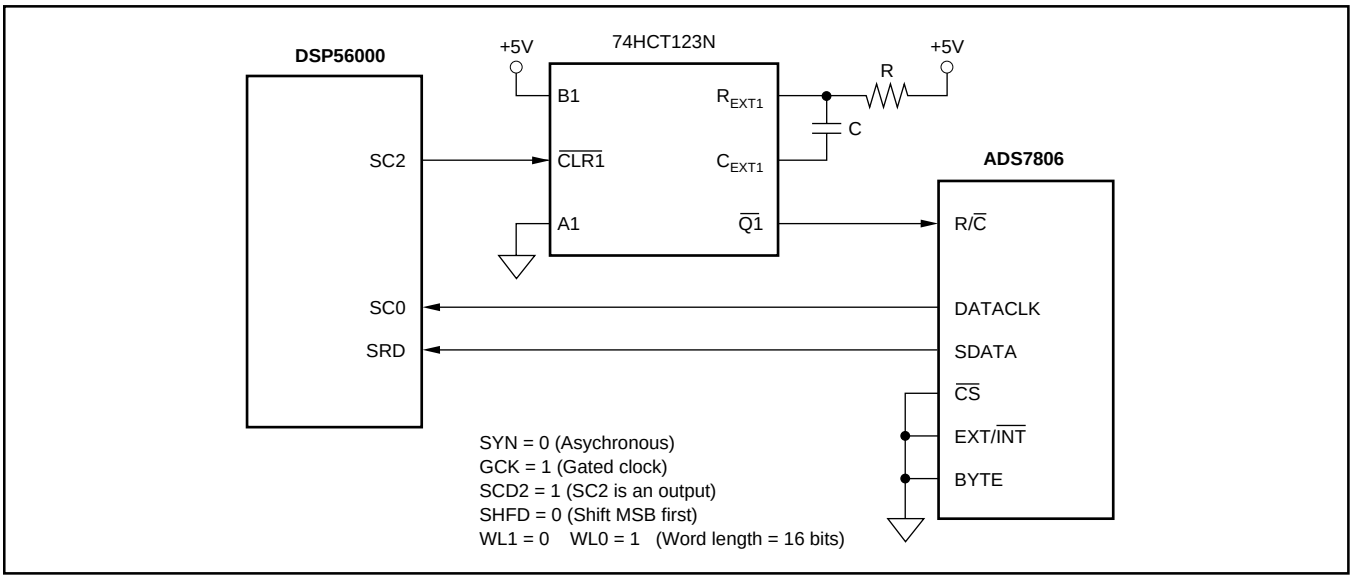



FIGURE 15. DSP56000 Interface to the ADS7806. Processor initiates conversions.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS7806U | LIFEBUY | SOIC | DW | 28 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7806U | |
| ADS7806UB | ACTIVE | SOIC | DW | 28 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7806U B | Samples |
| ADS7806UG4 | LIFEBUY | SOIC | DW | 28 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7806U | |

(1) The marketing status values are defined as follows:
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**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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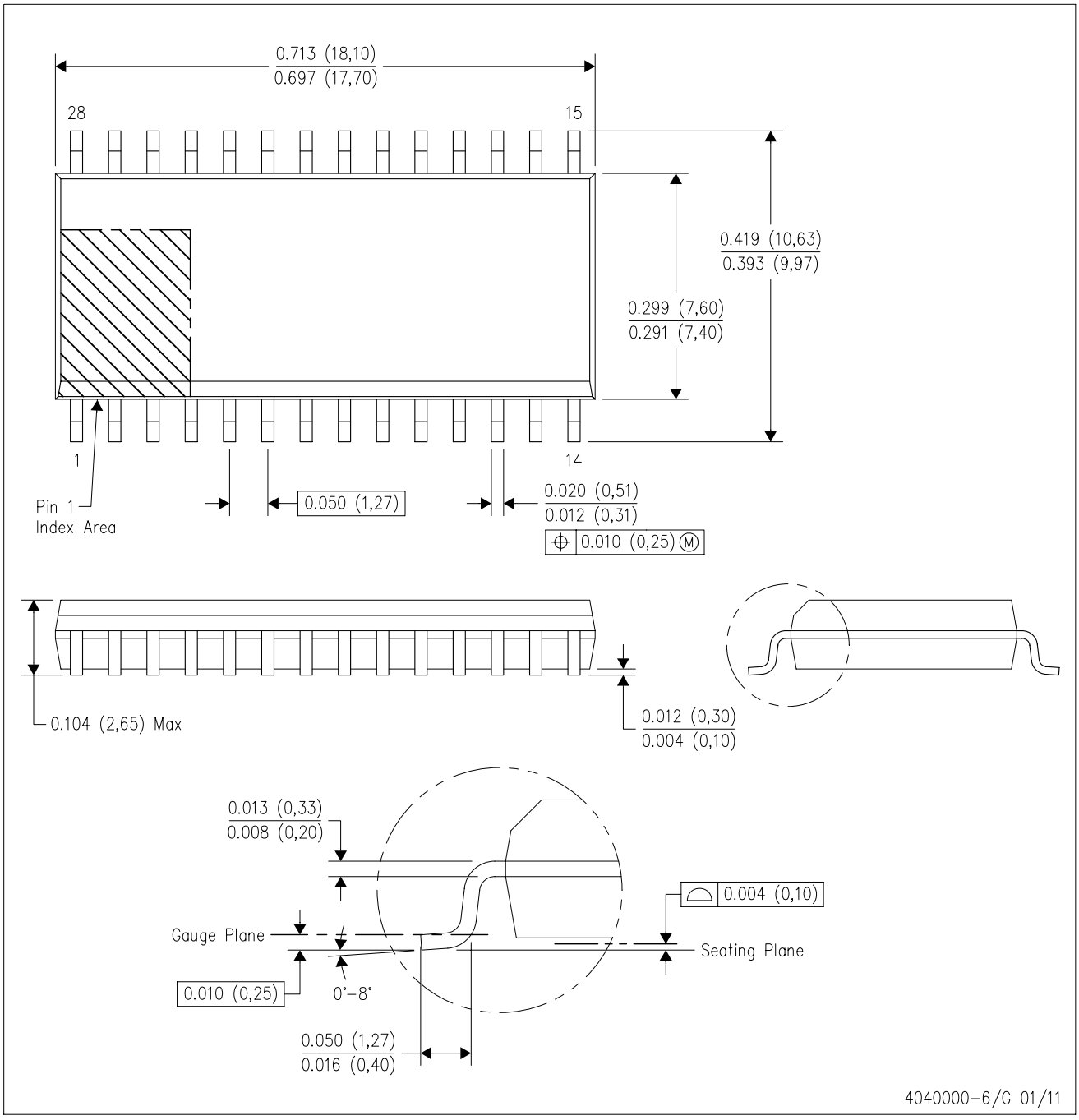
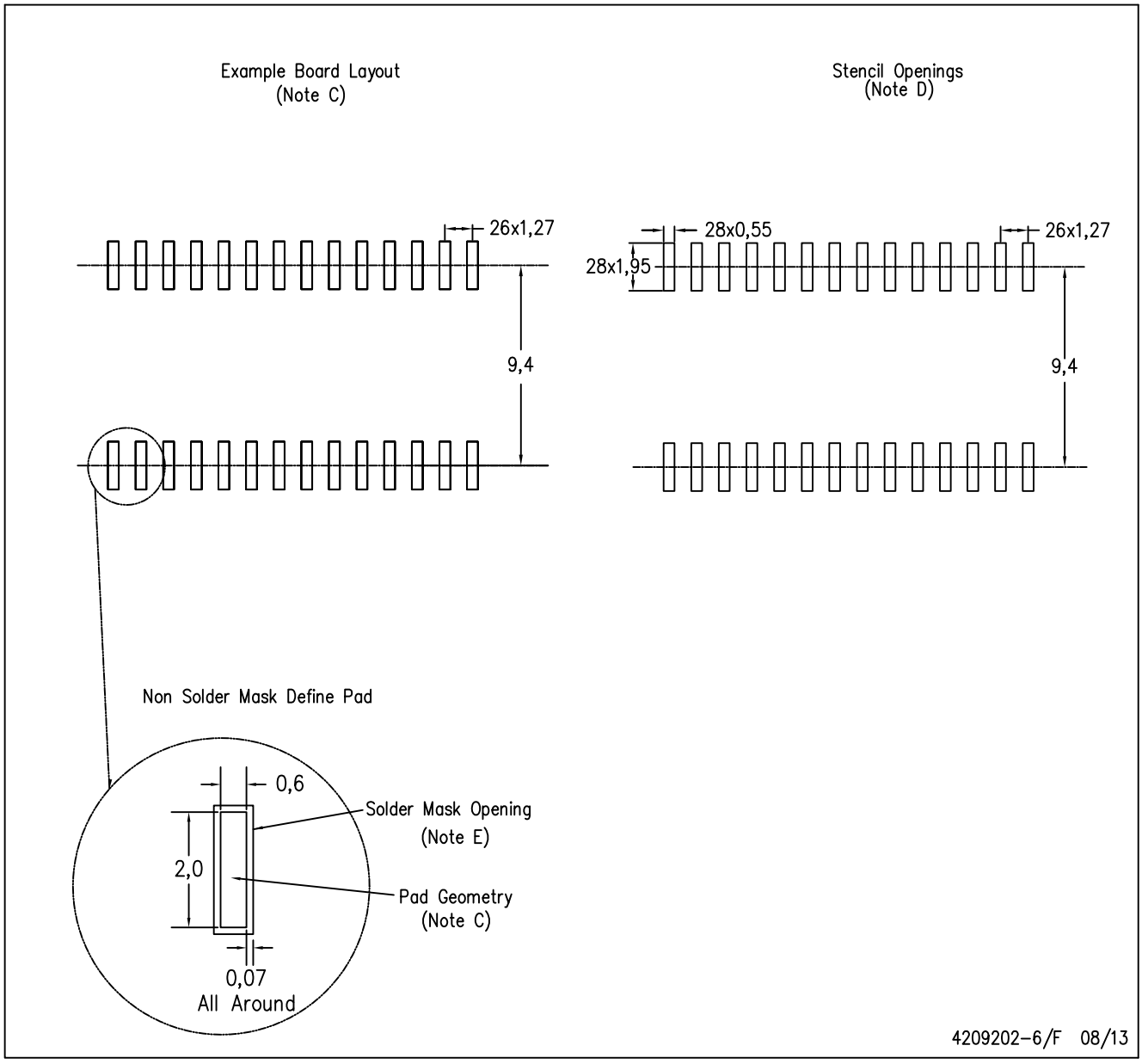
DW (R–PDSO–G28) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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