



THE DATASHEET OF PIC16C62B-04I/SP



MOSFET

Metall Oxide Semiconductor Field Effect Transistor

CoolMOS E6

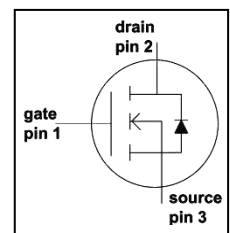
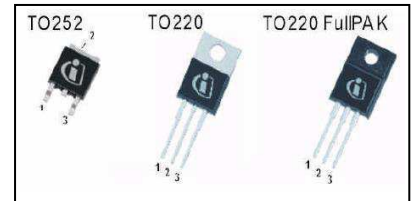
650V CoolMOS™ E6 Power Transistor
IPx65R600E6

Data Sheet

Rev. 2.4
Final

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ DE series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter, and cooler.



Features

- Extremely low losses due to very low FoM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive, Pb-free plating, Halogen free mold compound
- Fully qualified according to JEDEC for Industrial Applications

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages e.g. PC Silverbox, Adapter, LCD & PDP TV, Lightning, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.



Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j, max}$	700	V
$R_{DS(on), max}$	0.6	Ω
Q_G, typ	23	nC
$I_D, pulse$	18	A
$E_{oss} @ 400V$	2	μJ
Body diode di/dt	500	A/ μs

Type / Ordering Code	Package	Marking	Related links
IPD65R600E6	PG-TO252	65E6600	IFX CoolMOS Webpage IFX Design tools
IPP65R600E6	PG-TO220		
IPA65R600E6	PG-TO220 FullPAK		

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2 Maximum ratings

At $T_j = 25^\circ\text{C}$, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	–	–	7.3	A	$T_C = 25^\circ\text{C}$
		–	–	4.6		$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D, pulse}$	–	–	18		$T_C = 25^\circ\text{C}$
Averlanche energy, single pulse	E_{AS}	–	–	142	mJ	$I_D = 1.3\text{A}; V_{DD} = 50\text{V};$ $T_C = 25^\circ\text{C}$ (see Table 21)
Averlanche energy, repetitive	E_{AR}	–	–	0.21		$I_D = 1.3\text{A}, V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}	–	–	1.3	A	
MOSFET dv/dt ruggedness	dv/dt	–	–	50	V/ns	$V_{DS} = 0 \dots 480\text{V}$
Gate source voltage	V_{GS}	-20	–	20	V	static
		-30		30		AC ($f > 1\text{Hz}$)
Power dissipation for Non FullPAK	P_{tot}	–	–	63	W	$T_C = 25^\circ\text{C}$
Power dissipation for FullPAK	P_{tot}	–	–	28	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-55	–	150	°C	
Mounting torque TO-220		–	–	60	Ncm	M3 and M3.5 screws
Mounting torque TO-220 FullPAK		–	–	50		M2.5 Screws
Continous diode forward current	I_S	–	–	6.3	A	$T_C = 25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S, pulsed}$	–	–	18	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	–	–	15	V/ns	$V_{DS} = 0 \dots 480\text{V}, I_{SD} \leq I_D,$
Maximum diode commutation speed ³⁾	di/dt			500	A/ μs	$T_C = 125^\circ\text{C}$ (see table 22)

1) Limited by $T_{j, max}$. Maximum duty cycle $D=0.75$

2) Pulse width t_p limited by $T_{j, max}$

3) Identical low side and high side switch with identical R_θ

3 Thermal characteristics

Table 3 Thermal characteristics TO-220 (IPP65R600E6)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	–	–	2.0	°C/W	leaded
Thermal resistance, junction-ambient	R_{thJA}	–	–	62		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	–	–	260	°C	1.6mm (0.063 in.) from case for 10 s

Table 4 Thermal characteristics TO-220 FullPAK (IPA65R600E6)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	–	–	4.5	°C/W	leaded
Thermal resistance, junction-ambient	R_{thJA}	–	–	80		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	–	–	260	°C	1.6mm (0.063 in.) from case for 10 s

Table 5 Thermal characteristics TO-252 (IPD65R600E6)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	–	–	2.0	°C/W	SMD version, device on PCB, minimal footprint
Thermal resistance, junction-ambient	R_{thJA}	–	–	62		
			35			
Soldering temperature, wave- & reflowsoldering only allowed	T_{sold}	–	–	260	°C	Reflow MSL1

1) Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain-source Breakdown voltage	$V_{(BR)DSS}$	650	–	–	V	$V_{GS}=0V, I_D=1.0mA$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5		$V_{DS}=V_{GS}, I_D=0.21mA$
Zero gate Voltage drain current	I_{DSS}	–	–	1	μA	$V_{DS}=600V, V_{GS}=0V,$ $T_f=25^\circ\text{C}$
		–	10	–		$V_{DS}=600V, V_{GS}=0V,$ $T_f=150^\circ\text{C}$
Gate- source leakage current	I_{GSS}	–	–	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain- source on- state resistance	$R_{DS(on)}$	–	0.54	0.6	Ω	$V_{GS}=10V, I_D=2.1A,$ $T_f=25^\circ\text{C}$
		–	1.40	–		$V_{GS}=10V, I_D=2.1A,$ $T_f=150^\circ\text{C}$
Gate resistance	R_G	–	10.5	–	Ω	$f=1\text{MHz}, \text{open drain}$

Table7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	–	440	–	pF	$V_{GS}=0V, V_{DS}=100V,$ $f=1\text{MHz}$
Output capacitance	C_{oss}	–	30	–		
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	–	21	–		
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	–	88	–		
Turn- on delay time	$t_{d(on)}$	–	10	–	ns	$V_{DD}=400V$ $V_{GS}=13V, I_D=3.2A,$ $R_G=6.8\Omega$ (see table 20)
Rise time	t_r	–	8	–		
Turn- off delay time	$t_{d(off)}$	–	64	–		
Fall time	t_f	–	11	–		

1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	–	2.75	–	nC	$V_{DD}=480V, I_D=3.2A,$ $V_{GS}=0$ to 10 V
Gate to drain charge	Q_{GD}	–	12	–		
Gate charge, total	Q_G	–	23	–		
Gate plateau voltage	$V_{plateau}$	–	5.5	–	V	

Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	–	0.9	–	V	$V_{GS}=0V, I_F=3.2A,$ $T_J=25^\circ C$
Reverse recovery time	t_{rr}	–	270	–	ns	$V_R=400V, I_F=3.2A,$ $diF/dt=100A/\mu s$
Reverse recovery charge	Q_{rr}	–	2.0	–	nC	
Peak reverse recovery current	I_{rrm}	–	13	–	A	(see table 22)

5 Electrical characteristics diagrams

Table 10

Power dissipation Non FullPAK	Power dissipation FULLPAK
$P_{tot} = f(T_c)$	$P_{tot} = f(T_c)$

Table 11

Max. transient thermal impedance Non FullPAK	Max. transient thermal impedance Non FullPAK
$Z_{th(jc)} = f(t_p)$; parameter: $D = t_p/T$	$Z_{th(jc)} = f(t_p)$; parameter: $D = t_p/T$

Table 12

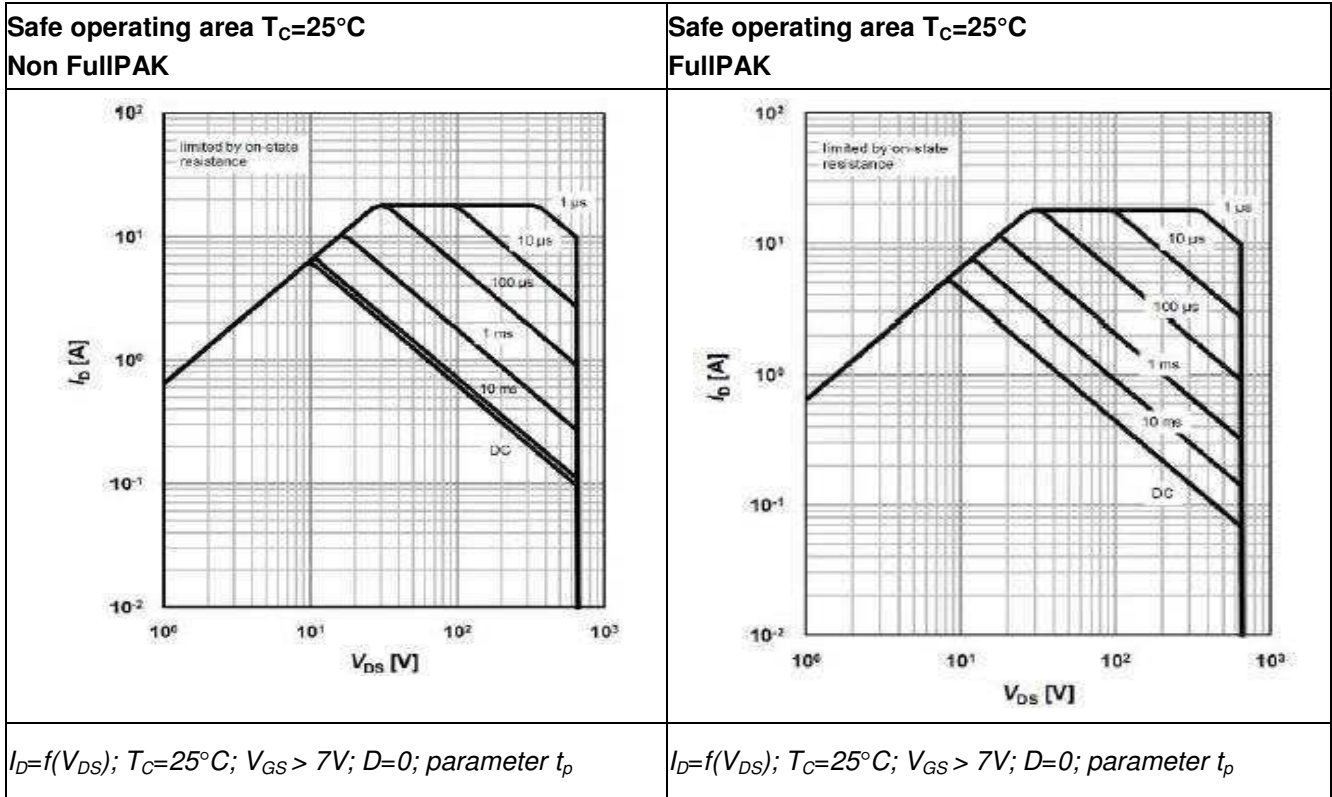


Table 13

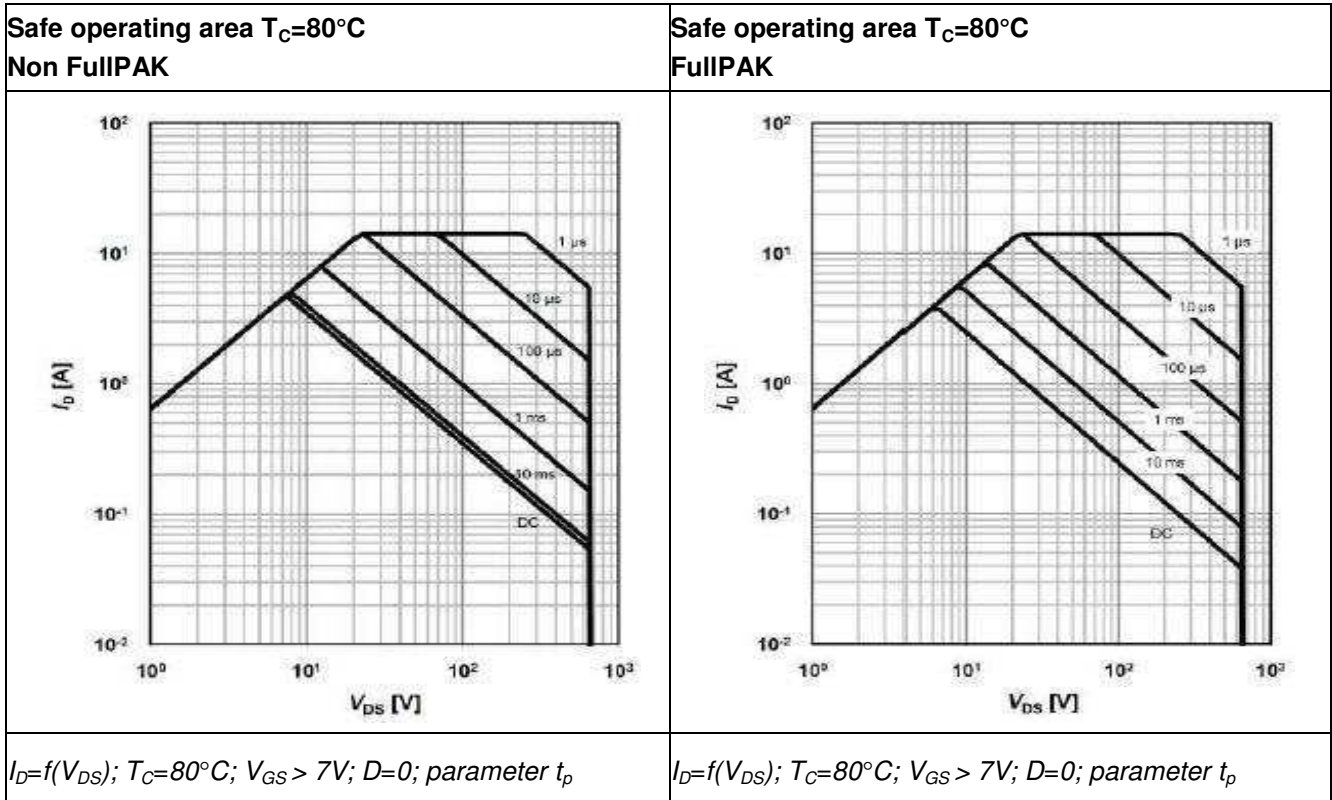


Table 14

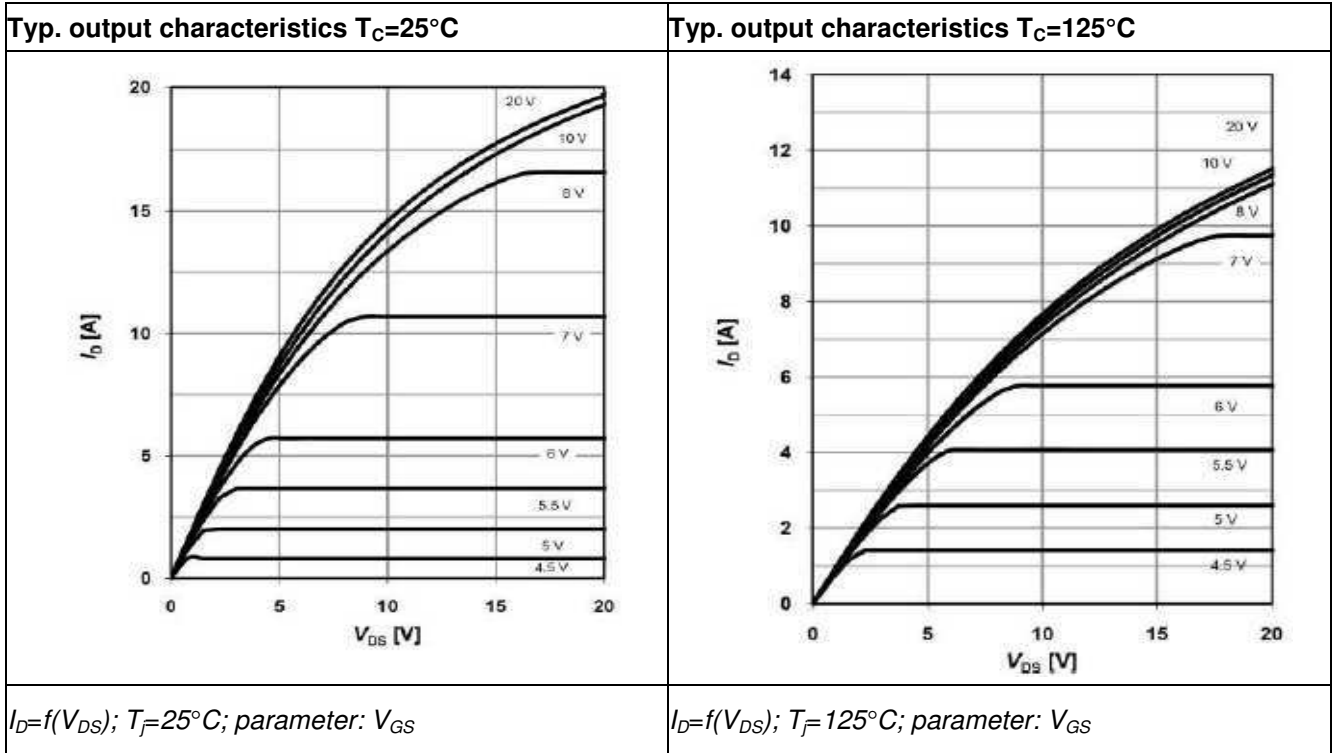


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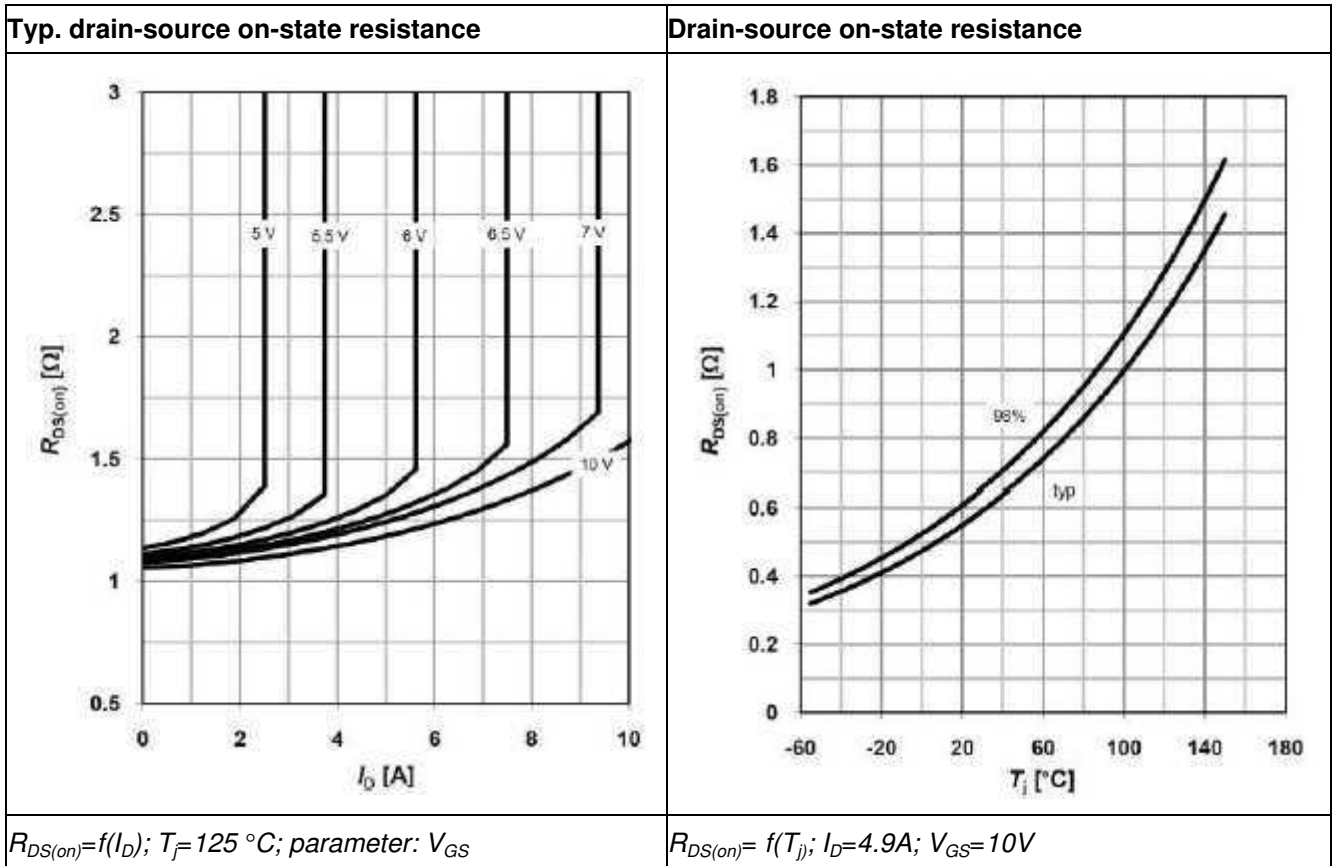


Table 16

Typ. transfer characteristics	Typ. gate charge
$I_D = f(V_{GS}); V_{DS} = 20V$	$V_{GS} = f(Q_{gate}), I_D = 4.9 A \text{ pulsed}$

Table 17

Avalanche energy	Drain-source breakdown voltage
$E_{AS} = f(T_j); I_D = 1.8 A; V_{DD} = 50 V$	$V_{BR(DSS)} = f(T_j); I_D = 1.0 mA$

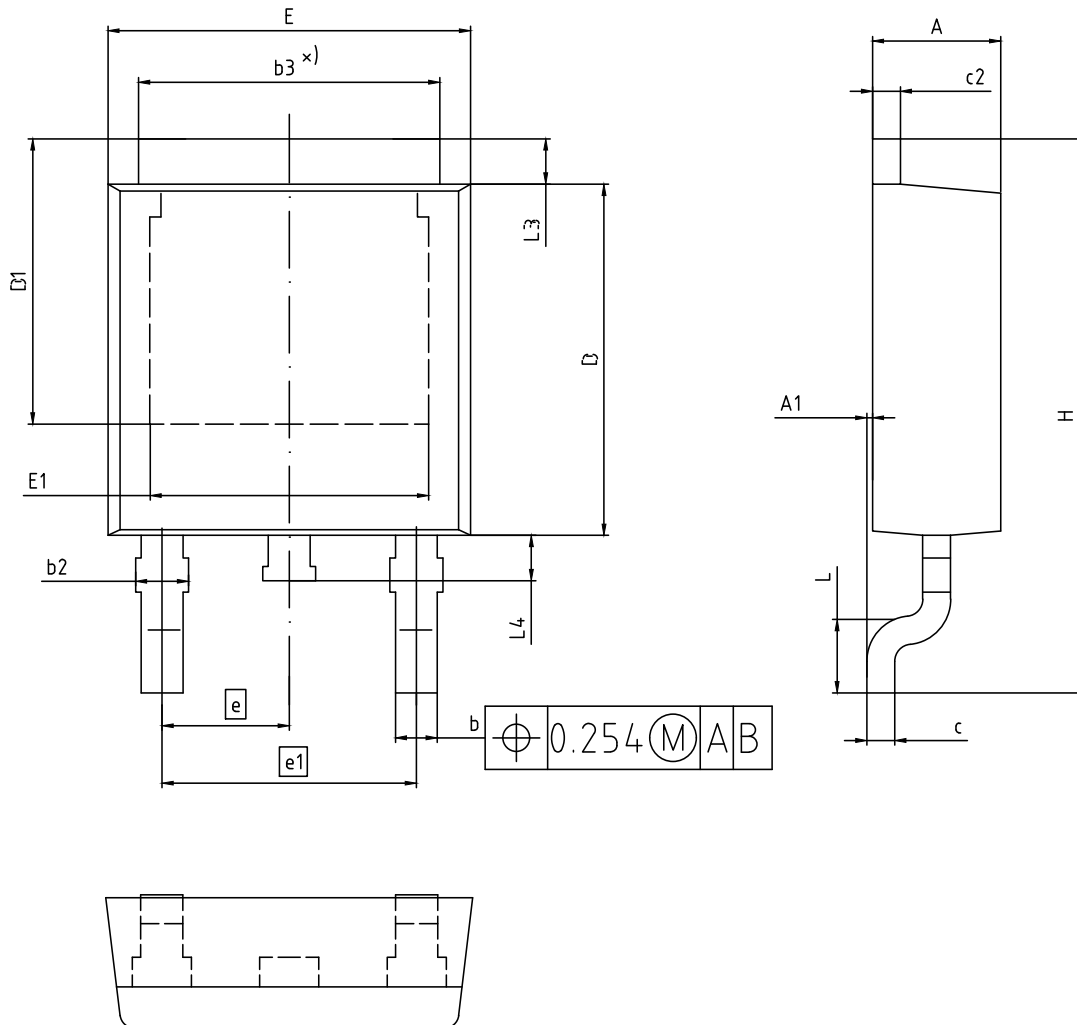
Table 18

Typ. capacitances	Typ. C_{OSS} stored energy
<p>A semi-logarithmic plot showing capacitance C [pF] on the y-axis (log scale from 10⁰ to 10⁵) versus drain-source voltage V_{DS} [V] on the x-axis (linear scale from 0 to 600). Three curves are shown: C_{iss} (input capacitance) is constant at approximately 500 pF; C_{oss} (output capacitance) starts at ~10³ pF at 0V and decreases to ~10¹ pF at 600V; C_{rss} (reverse transfer capacitance) starts at ~10³ pF at 0V, drops sharply to ~10⁰ pF at 100V, and then slightly increases to ~10¹ pF at 600V.</p>	<p>A linear plot showing stored energy E_{oss} [μJ] on the y-axis (linear scale from 0 to 4) versus drain-source voltage V_{DS} [V] on the x-axis (linear scale from 0 to 600). The curve shows that stored energy increases from 0 μJ at 0V to approximately 3.5 μJ at 600V.</p>
<p>$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$</p>	<p>$E_{OSS}=f(V_{DS})$</p>

Table 19

Forward characteristics of reverse diode
<p>A semi-logarithmic plot showing reverse current I_r [A] on the y-axis (log scale from 10⁻¹ to 10²) versus reverse drain-source voltage V_{SD} [V] on the x-axis (linear scale from 0 to 2). Two curves are shown for different temperatures: 125°C and 25°C. Both curves show an exponential-like increase in current with voltage, with the 125°C curve being significantly higher than the 25°C curve.</p>
<p>$I_F=f(V_{SD}); \text{parameter: } T_j$</p>

7 Package outlines

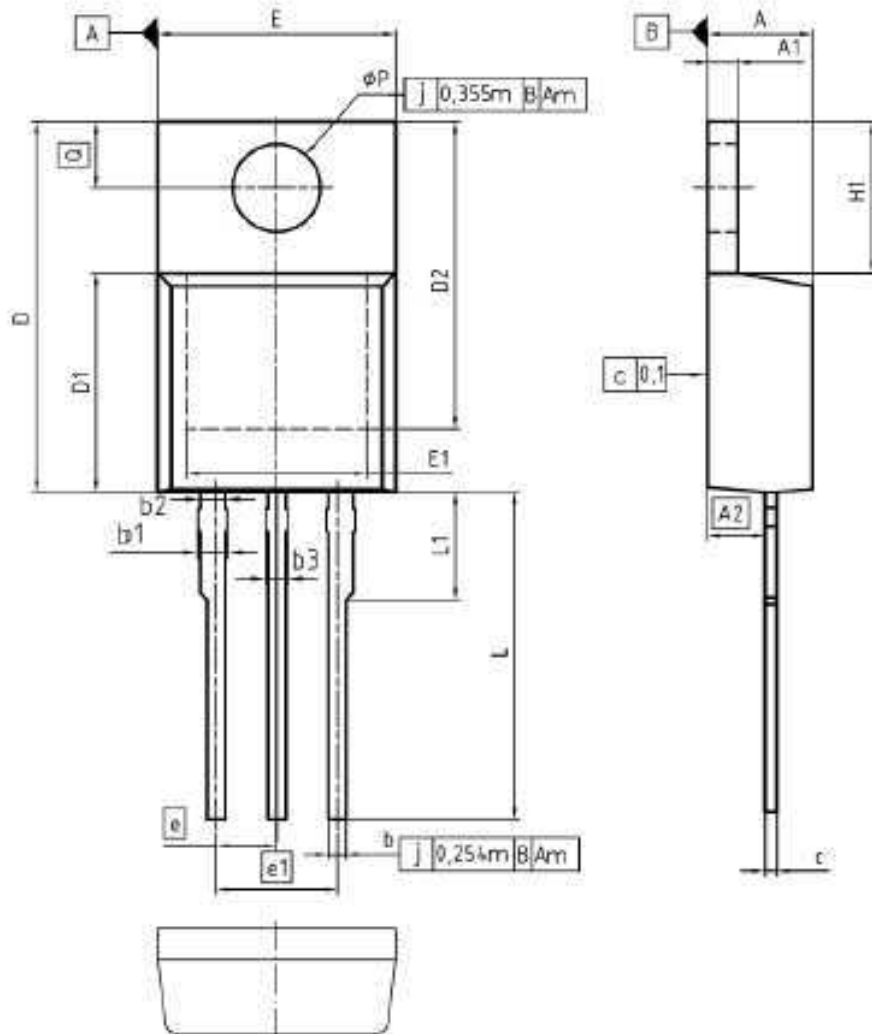


ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b2	0.65	1.15
b3	4.95	5.50
c	0.46	0.61
c2	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L3	0.89	1.27
L4	0.51	1.02

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Figure 1 Outlines TO-252, dimensions in mm



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.00	0.256	0.313
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	6.90	6.90	0.272	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.90	-	0.193
φP	3.60	3.60	0.142	0.153
G	2.60	3.00	0.102	0.118

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Figure 2 Outlines TO220, dimensions in mm/inches

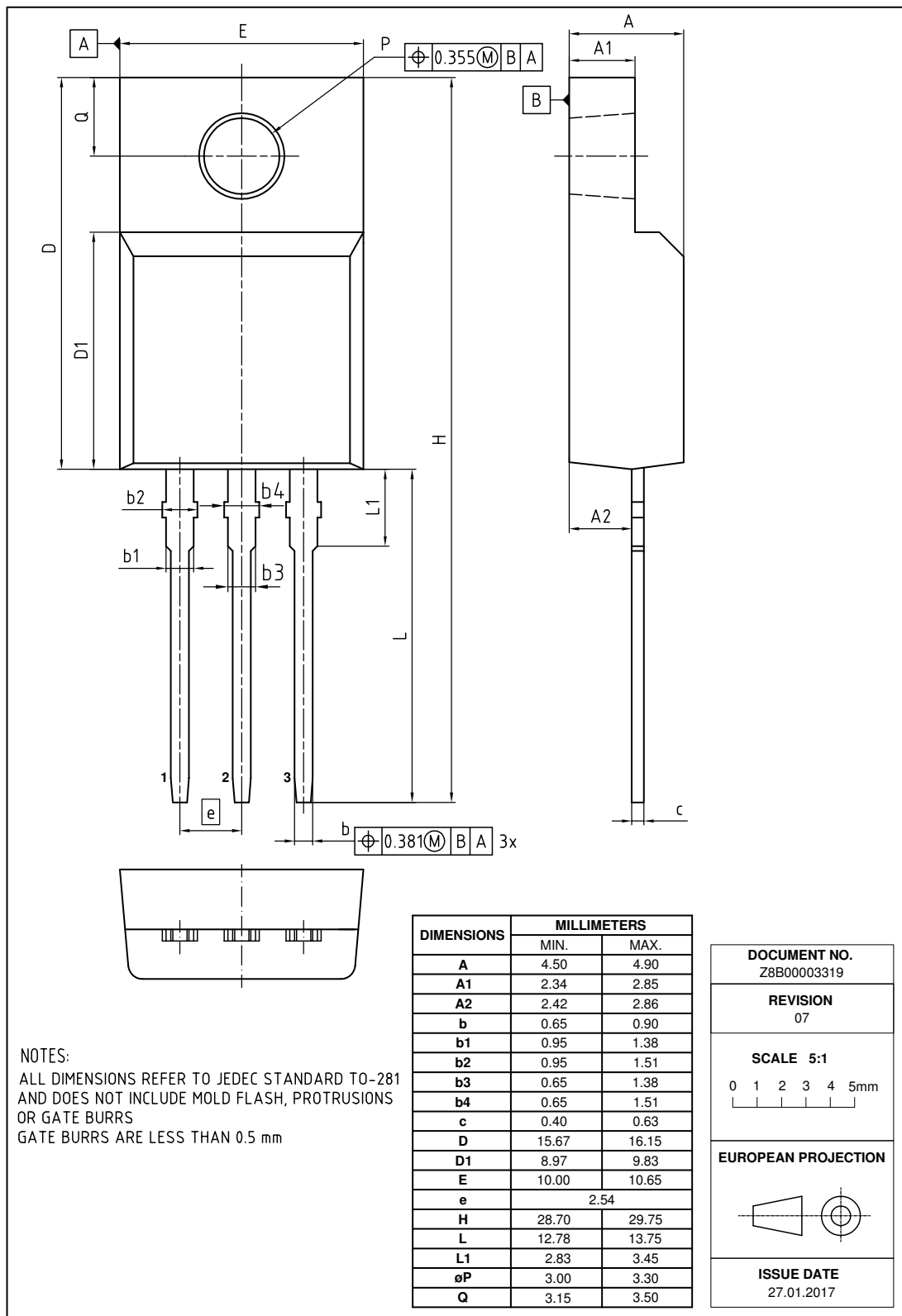


Figure 3 Outlines TO220 FullPAK, dimensions in mm

Revision History

IPx65R600E6

Revision: 2020-05-20, Rev. 2.4

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.2	2016-08-04	Revised TO220 Full PAK package drawing on page 16
2.3	2018-03-04	Outline PG-TO-220 FullPAK update
2.4	2020-05-20	Update of the package outlines TO-252

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