THE DATASHEET OF

ADP124ARHZ-3.3-R7

5.5 V Input, 500 mA, Low Quiescent Current, CMOS Linear Regulators

Data Sheet

ADP124/ADP125

FEATURES

- Input voltage supply range: 2.3 V to 5.5 V
- 500 mA maximum output current
- Fixed and adjustable output voltage versions
- 1% initial accuracy
- Up to 31 fixed-output voltage options available from 1.75 V to 3.3 V
- Adjustable-output voltage range from 0.8 V to 5.0 V
- Very low dropout voltage: 130 mV
- Low quiescent current: 45 µA
- Low shutdown current: <1 µA
- Excellent PSRR performance: 60 dB at 100 kHz
- Excellent load/line transient response
- Optimized for small 1.0 µF ceramic capacitors
- Current limit and thermal overload protection
- Logic controlled enable
- Compact 8-lead exposed paddle MSOP and LFCSP packages

APPLICATIONS

- Digital camera and audio devices
- Portable and battery-powered equipment
- Automatic meter reading (AMR) meters
- GPS and location management units
- Medical instrumentation
- Point of load power

TYPICAL APPLICATION CIRCUITS

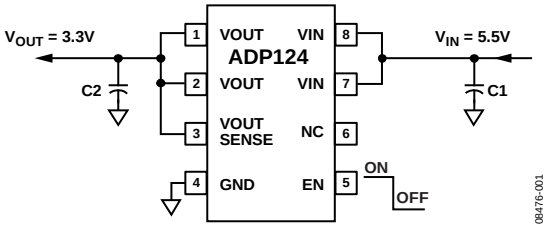

Figure 1. ADP124 with Fixed Output Voltage

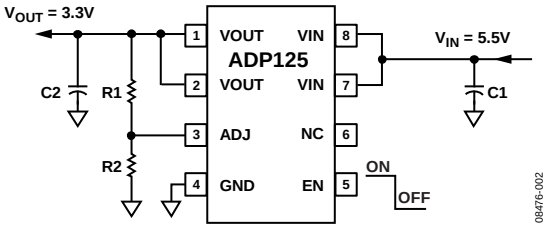

Figure 2. ADP125 with Adjustable Output Voltage

GENERAL DESCRIPTION

The ADP124/ADP125 are low quiescent current, low dropout linear regulators. They are designed to operate from an input voltage between 2.3 V and 5.5 V and to provide up to 500 mA of output current. The low 130 mV dropout voltage at a 500 mA load improves efficiency and allows operation over a wide input voltage range.

The low 210 µA of quiescent current with a 500 mA load makes the ADP124/ADP125 ideal for battery-operated portable equipment.

The ADP124 is capable of 31 fixed-output voltages from 1.75 V to 3.3 V. The ADP125 is the adjustable version of the device and allows the output voltage to be set between 0.8 V and 5.0 V by an external voltage divider.

The ADP124/ADP125 are specifically designed for stable operation with tiny 1 µF ceramic input and output capacitors to meet the requirements of high performance, space constrained applications.

The ADP124/ADP125 have an internal soft start that gives a constant start-up time of 350 µs. Short-circuit protection and thermal overload protection circuits prevent damage in adverse conditions. The ADP124/ADP125 are available in 8-lead exposed paddle MSOP and LFCSP packages. When compared with the standard MSOP and LFCSP packages, the exposed paddle MSOP and LFCSP packages have lower thermal resistance (θ_{JA}). The lower thermal resistance package allows the ADP124/ADP125 to meet the needs of a variety of portable applications while minimizing the rise in junction temperature.

Rev. D

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12/09—Revision 0: Initial Version

SPECIFICATIONS

Unless otherwise noted, V_{IN} = (V_{OUT} + 0.5 V) or 2.3 V, whichever is greater; ADJ connected to VOUT; I_{OUT} = 10 mA; C_{IN} = 1.0 µF; C_{OUT} = 1.0 µF; T_A = 25°C.

Table 1.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}		2.3		5.5	V
OPERATING SUPPLY CURRENT[1]	I_{GND}	I_{OUT} = 0 µA		45		µA
		I_{OUT} = 0 µA, T_J = −40°C to +125°C			105	µA
		I_{OUT} = 1 mA		60		µA
		I_{OUT} = 1 mA, T_J = −40°C to +125°C			120	µA
		I_{OUT} = 250 mA		160		µA
		I_{OUT} = 250 mA, T_J = −40°C to +125°C			210	µA
		I_{OUT} = 500 mA		210		µA
		I_{OUT} = 500 mA, T_J = −40°C to +125°C			280	µA
SHUTDOWN CURRENT	I_{SD}	EN = GND		0.1		µA
		EN = GND, T_J = −40°C to +125°C			1	µA
OUTPUT VOLTAGE ACCURACY[2]	V_{OUT}					
Fixed Output		I_{OUT} = 10 mA	−1		+1	%
		100 µA < I_{OUT} < 500 mA, V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V, T_J = −40°C to +125°C	−2		+1.5	%
Adjustable Output						
		I_{OUT} = 10 mA	0.495	0.500	0.505	V
		100 µA < I_{OUT} < 500 mA, V_{IN} = 2.3 V to 5.5 V, T_J = −40°C to +125°C	0.485	0.500	0.515	V
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = V_{IN} = 2.3 V to 5.5 V, T_J = −40°C to +125°C	−0.05		+0.05	%/V
LOAD REGULATION[3]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 1 mA to 500 mA		0.0005		%/mA
		I_{OUT} = 1 mA to 500 mA, T_J = −40°C to +125°C			0.001	%/mA
ADJ INPUT BIAS CURRENT	ADJ_{I-BIAS}	2.3 V ≤ V_{IN} ≤ 5.5 V, ADJ connected to VOUT		15		nA
DROPOUT VOLTAGE[4]	$V_{DROPOUT}$					
		I_{OUT} = 10 mA, V_{OUT} > 2.3 V		3		mV
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			5	mV
		I_{OUT} = 250 mA, V_{OUT} > 2.3 V		65		mV
		I_{OUT} = 250 mA, T_J = −40°C to +125°C			120	mV
		I_{OUT} = 500 mA, V_{OUT} > 2.3V		130		mV
		I_{OUT} = 500 mA, T_J = −40°C to +125°C			230	mV
START-UP TIME[5]	$t_{START-UP}$	V_{OUT} = 3.0 V		350		µs
CURRENT LIMIT THRESHOLD[6]	I_{LIMIT}		550	750	1000	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
EN INPUT						
EN Input Logic High	V_{IH}	2.3 V ≤ V_{IN} ≤ 5.5 V	1.2			V
EN Input Logic Low	V_{IL}	2.3 V ≤ V_{IN} ≤ 5.5 V			0.4	V
EN Input Leakage Current	$V_{I-LEAKAGE}$	EN = VIN or GND		0.1		µA
		EN = VIN or GND, T_J = −40°C to +125°C			1	µA
UNDERVOLTAGE LOCKOUT	UVLO					
Input Voltage Rising	$UVLO_{RISE}$	T_J = −40°C to +125°C			2.1	V
Input Voltage Falling	$UVLO_{FALL}$	T_J = −40°C to +125°C	1.5			V
Hysteresis	$UVLO_{HYS}$	T_A = 25°C		125		mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN} = 5.5 V, V_{OUT} = 1.2 V		25		μV rms
		10 Hz to 100 kHz, V_{IN} = 5.5 V, V_{OUT} = 1.8 V		35		μV rms
		10 Hz to 100 kHz, V_{IN} = 5.5 V, V_{OUT} = 2.5 V		45		μV rms
		10 Hz to 100 kHz, V_{IN} = 5.5 V, V_{OUT} = 3.3 V		55		μV rms
		10 Hz to 100 kHz, V_{IN} = 5.5 V, V_{OUT} = 4.2V		65		μV rms
POWER SUPPLY REJECTION RATIO (V_{IN} = V_{OUT} +1V)	PSRR	10 kHz to 100 kHz, V_{OUT} = 1.8 V, 2.5 V, 3.3 V		60		dB

[1] The current from the external resistor divider network in the case of adjustable voltage output (as with the ADP125) should be subtracted from the ground current measured.
[2] Accuracy when VOUT is connected directly to ADJ. When VOUT voltage is set by external feedback resistors, absolute accuracy in adjust mode depends on the tolerances of the resistors used.
[3] Based on an endpoint calculation using 1 mA and 500 mA loads.
[4] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages greater than 2.3 V.
[5] Start-up time is defined as the time between the rising edge of EN to VOUT being at 90% of its nominal value.
[6] Current limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.3 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.3 V, or 2.97 V.

RECOMMENDED CAPACITOR SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum Input and Output Capacitance[1]	CAP_{MIN}	T_A = −40°C to +125°C	0.70			μF
Capacitor ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		1	Ω

[1] The minimum input and output capacitance should be greater than 0.70 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with this LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +6.5 V
ADJ to GND	−0.3 V to +6.5 V
EN to GND	−0.3 V to +6.5 V
VOUT to GND	−0.3 V to VIN
Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	−40°C to +85°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP124/ADP125 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J will remain within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be limited.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications in which high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 inch × 3 inch circuit board. Refer to JESD 51-7 for detailed information on the board construction.

Ψ_{JB} is the junction-to-board thermal characterization parameter and is measured in °C/W. The Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The *Guidelines for Reporting and Using Package Thermal Information: JESD51-12* states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package—factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

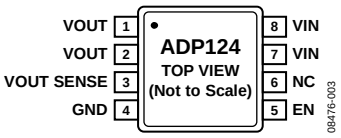
Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
8-Lead MSOP	102.8	31.8	°C/W
8-Lead LFCSP	68.9	44.1	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

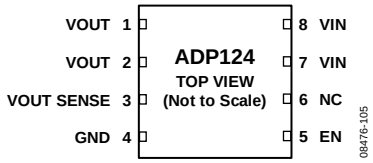


NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD MUST BE CONNECTED TO GROUND.

Figure 3. ADP124 Fixed Output MSOP Pin Configuration

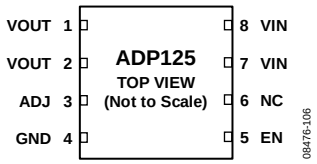
NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD MUST BE CONNECTED TO GROUND.

Figure 5. ADP125 Adjustable Output MSOP Pin Configuration



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD MUST BE CONNECTED TO GROUND.

Figure 4. ADP124 Fixed Output LFCSP Pin Configuration



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD MUST BE CONNECTED TO GROUND.

Figure 6. ADP125 Adjustable Output LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic		Description
	ADP124	ADP125	
1	VOUT	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 1 µF or greater capacitor.
2	VOUT	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 1 µF or greater capacitor.
3	VOUT SENSE	N/A	Feedback Node for the Error Amplifier. Connect to VOUT.
	N/A	ADJ	Feedback Node for the Error Amplifier. Connect the midpoint of an external divider from VOUT to GND to this pin to set the output voltage.
4	GND	GND	Ground.
5	EN	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
6	NC	NC	No Connect. This pin is not connected internally.
7	VIN	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
8	VIN	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
	EPAD	EPAD	The exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8 V, V_{OUT} = 3.3V, I_{OUT} = 10 mA, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, T_A = 25°C, unless otherwise noted.

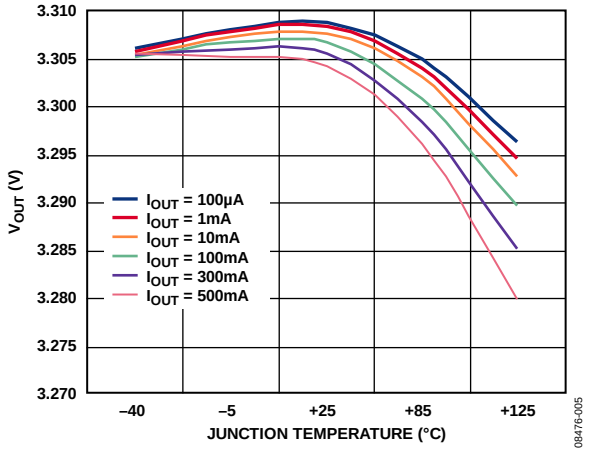


Figure 7. Output Voltage vs. Junction Temperature

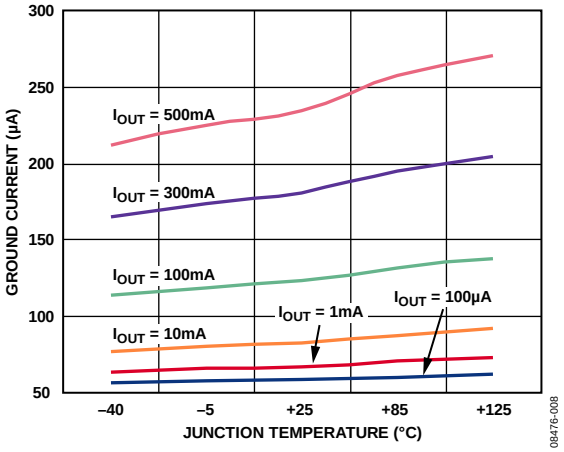


Figure 10. Ground Current vs. Junction Temperature

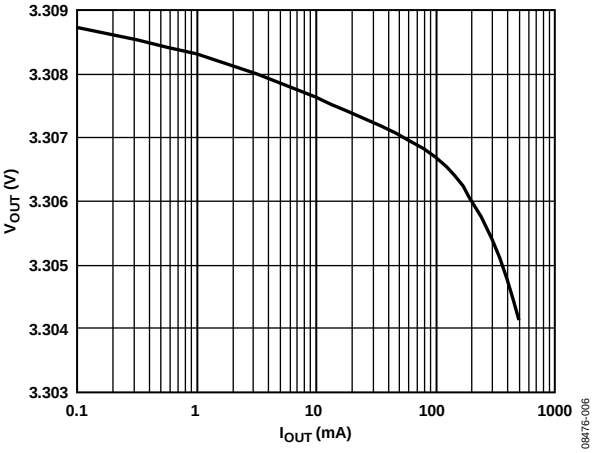


Figure 8. Output Voltage vs. Load Current

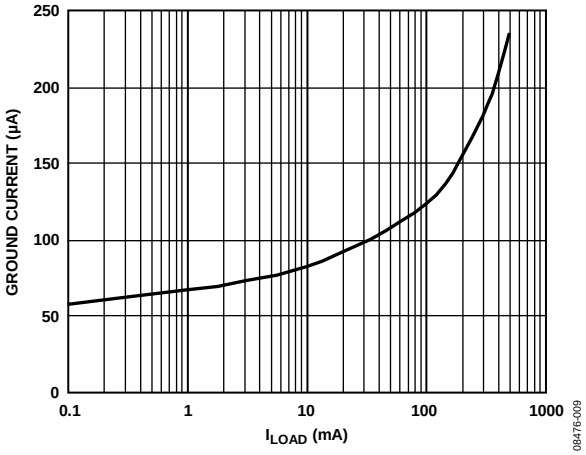


Figure 11. Ground Current vs. Load Current

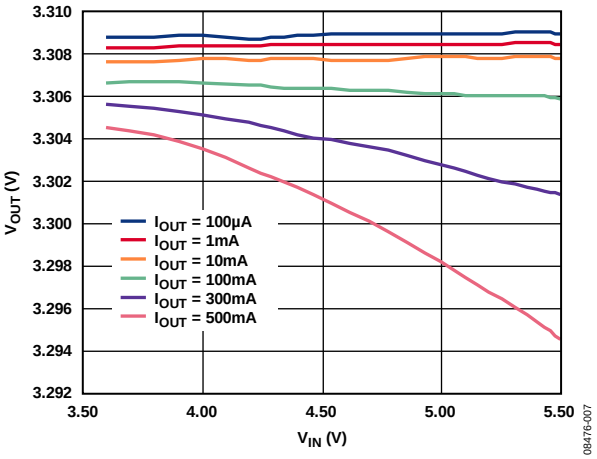


Figure 9. Output Voltage vs. Input Voltage

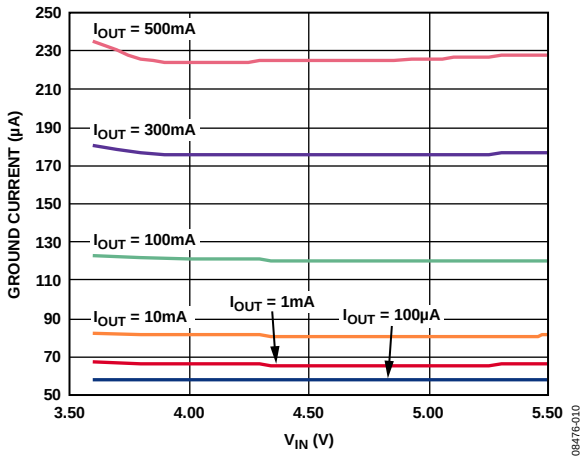


Figure 12. Ground Current vs. Input Voltage

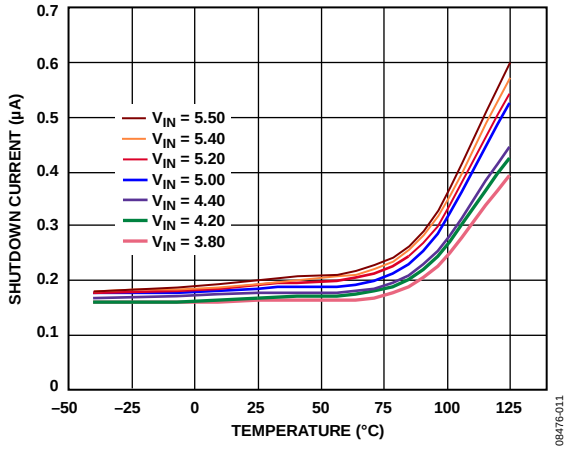


Figure 13. Shutdown Current vs. Temperature at Various Input Voltages

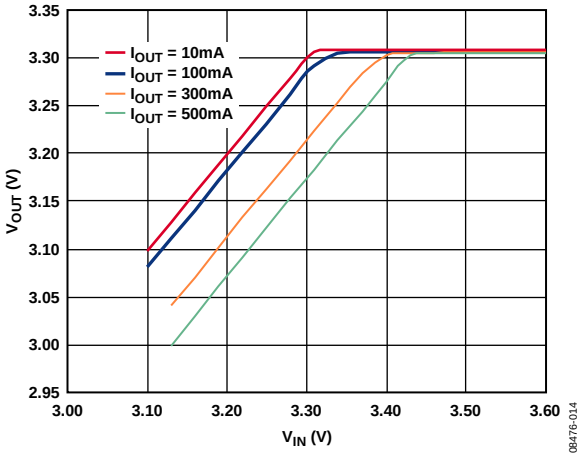


Figure 16. Output Voltage vs. Input Voltage (in Dropout)

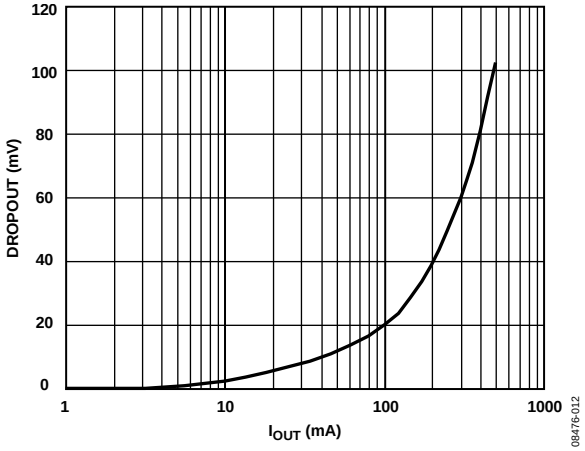


Figure 14. Dropout Voltage vs. Load Current

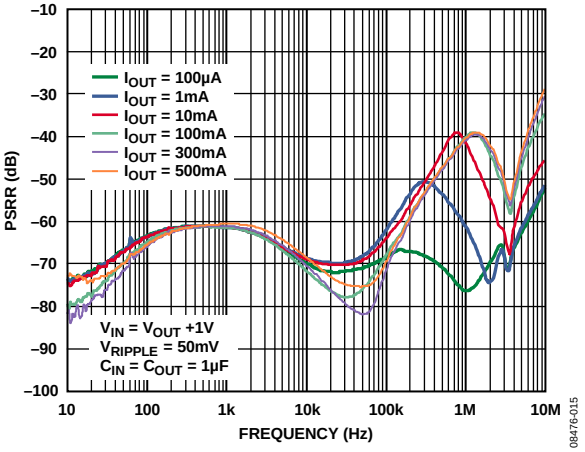


Figure 17. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 2.8 V, V_{IN} = 3.8 V

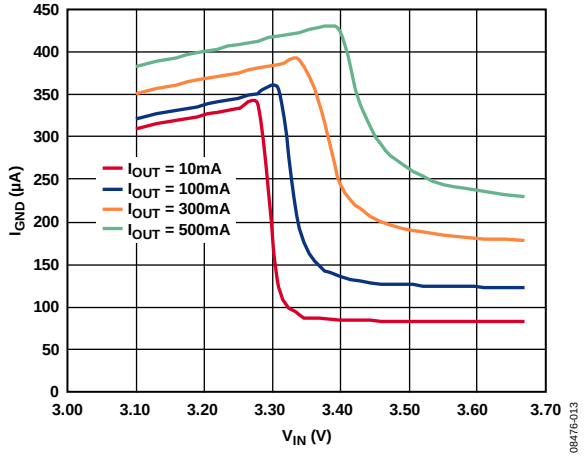


Figure 15. Ground Current vs. Input Voltage (in Dropout)

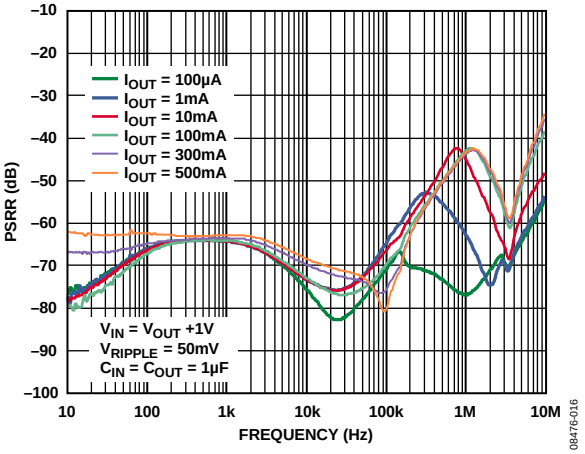


Figure 18. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 3.3 V, V_{IN} = 4.3 V

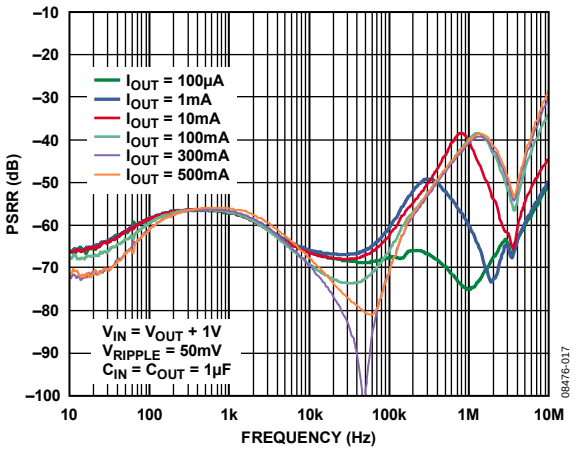


Figure 19. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 4.2 V, V_{IN} = 5.2 V

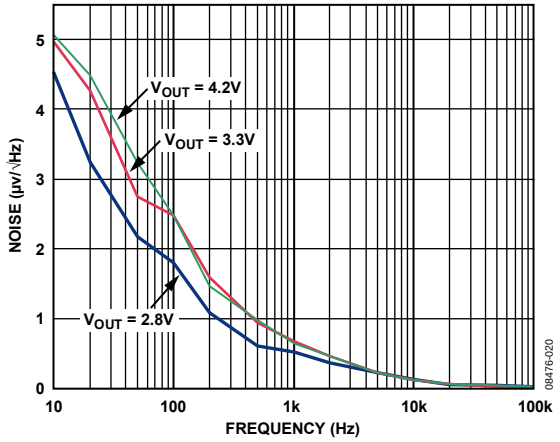


Figure 22. Output Noise Spectrum, V_{IN} = 5 V

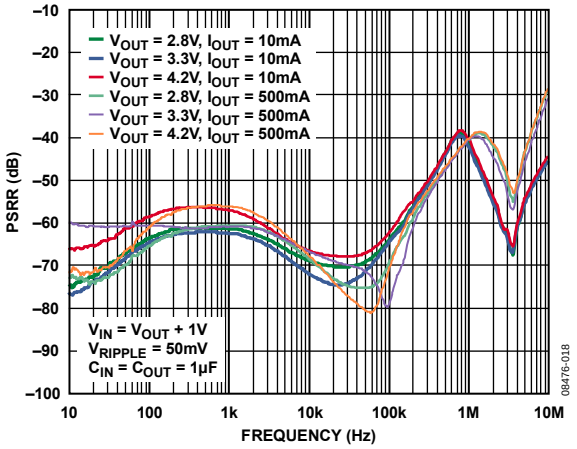


Figure 20. Power Supply Rejection Ratio vs. Frequency, Various Output Voltages and Load Currents

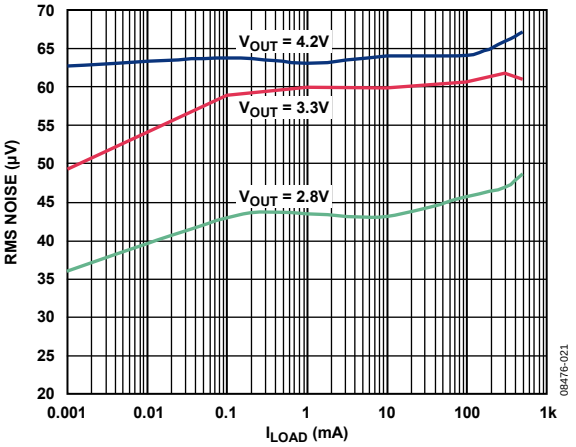


Figure 23. Output Noise vs. Load Current and Output Voltage, V_{IN} = 5 V

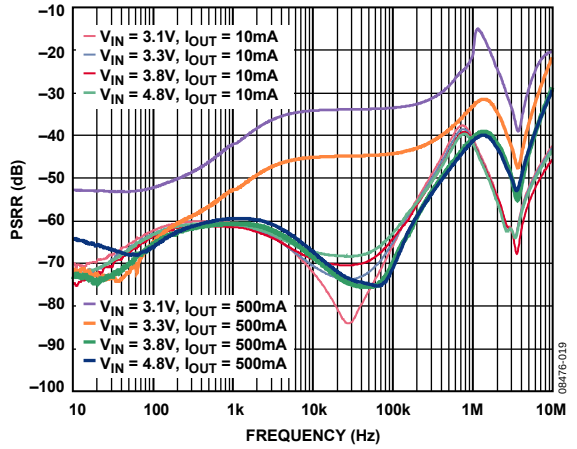


Figure 21. Power Supply Rejection Ratio vs. Headroom Voltage (V_{IN} – V_{OUT}), V_{OUT} = 2.8 V

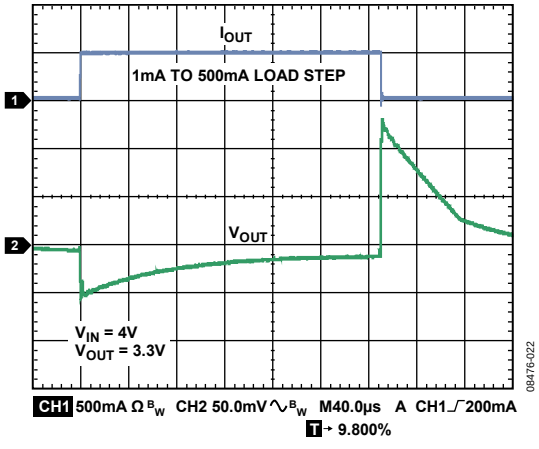


Figure 24. Load Transient Response, C_{OUT} = 1 µF

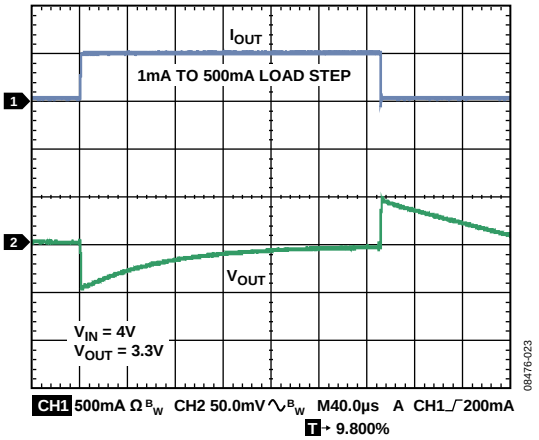


Figure 25. Load Transient Response, C_{OUT} = 4.7 µF

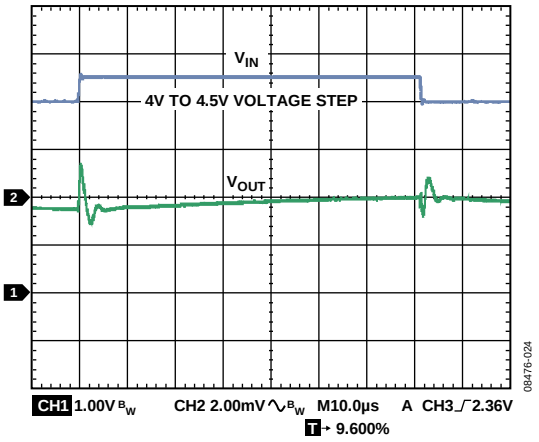


Figure 26. Line Transient Response, Load Current = 1 mA

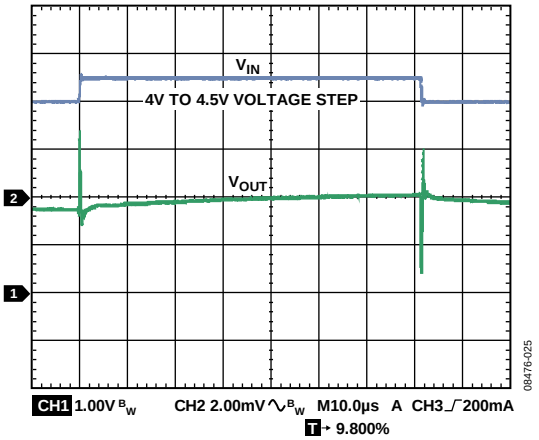


Figure 27. Line Transient Response, Load Current = 500 mA

THEORY OF OPERATION

The ADP124/ADP125 are low quiescent current, low dropout linear regulators that operate from 2.3 V to 5.5 V and can provide up to 500 mA of output current. Drawing a low 210 µA of quiescent current (typical) at full load makes the ADP124/ADP125 ideal for battery-operated portable equipment. Shutdown current consumption is typically 100 nA.

Optimized for use with small 1 µF ceramic capacitors, the ADP124/ADP125 provide excellent transient performance.

Internally, the ADP124/ADP125 consist of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The adjustable ADP125 has an output voltage range of 0.8 V to 5.0 V. The output voltage is set by the ratio of two external resistors, as shown in Figure 2. The device servos the output to maintain the voltage at the ADJ pin at 0.5 V referenced to ground. The current in R1 is then equal to 0.5 V/R2 and the current in R1 is the current in R2 plus the ADJ pin bias current. The ADJ pin bias current, 15 nA at 25°C, flows through R1 into the ADJ pin.

The output voltage can be calculated using the equation:

$$V_{OUT} = 0.5\ V(1 + R1/R2) + (ADJ_{I\text{-}BIAS})(R1)$$

The value of R1 should be less than 200 kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. For example, when R1 and R2 each equal 200 kΩ, the output voltage is 1.0 V. The output voltage error introduced by the ADJ pin bias current is 3 mV or 0.3%, assuming a typical ADJ pin bias current of 15 nA at 25°C.

Note that in shutdown, the output is turned off and the divider current is 0.

The ADP124/ADP125 use the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on; when EN is low, VOUT turns off. For automatic startup, EN can be tied to VIN.

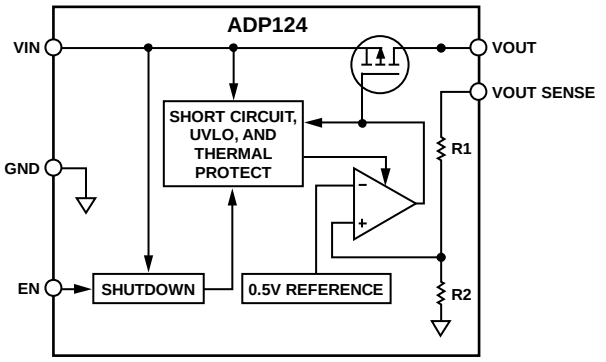


Figure 28. ADP124 Internal Block Diagram (Fixed Output)

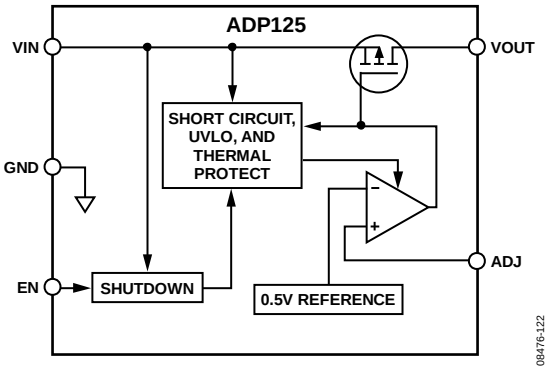


Figure 29. ADP125 Internal Block Diagram (Adjustable Output)

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP124/ADP125 are designed for operation with small, space-saving ceramic capacitors, but these devices can function with most commonly used capacitors as long as care is taken to ensure an appropriate effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 0.70 µF capacitance with an ESR of 1 Ω or less is recommended to ensure stability of the ADP124/ADP125. The transient response to changes in load current is also affected by the output capacitance. Using a larger value of output capacitance improves the transient response of the ADP124/ADP125 to dynamic changes in load current. Figure 30 and Figure 31 show the transient responses for output capacitance values of 1 µF and 4.7 µF, respectively.

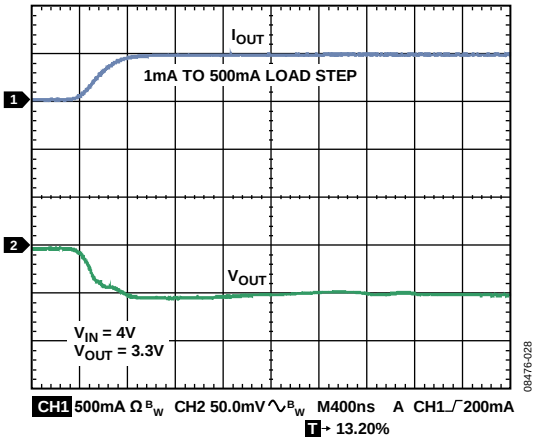


Figure 30. Output Transient Response, C_{OUT} = 1 µF

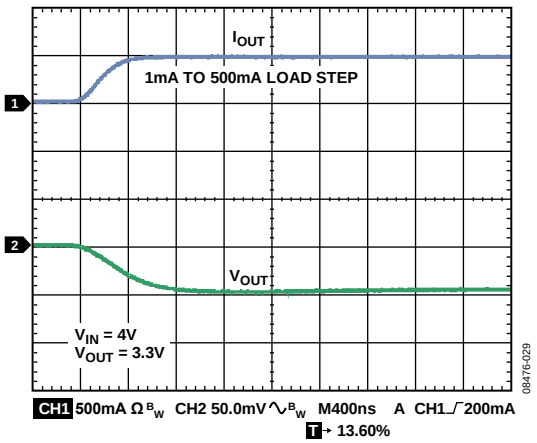


Figure 31. Output Transient Response, C_{OUT} = 4.7 µF

Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN to GND reduces the circuit sensitivity to the printed circuit board (PCB) layout, especially when a long input trace or high source impedance is encountered. If greater than 1 µF of output capacitance is required, the input capacitor should be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP124/ADP125, as long as the capacitor meets the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have an adequate dielectric to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. Using an X5R or X7R dielectric with a voltage rating of 6.3 V or 10 V is recommended. However, using Y5V and Z5U dielectrics are not recommended for any LDO, due to their poor temperature and dc bias characteristics.

Figure 32 depicts the capacitance vs. capacitor voltage bias characteristics of an 0402, 1 µF, 10 V X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and the voltage rating. In general, a capacitor in a larger package or of a higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

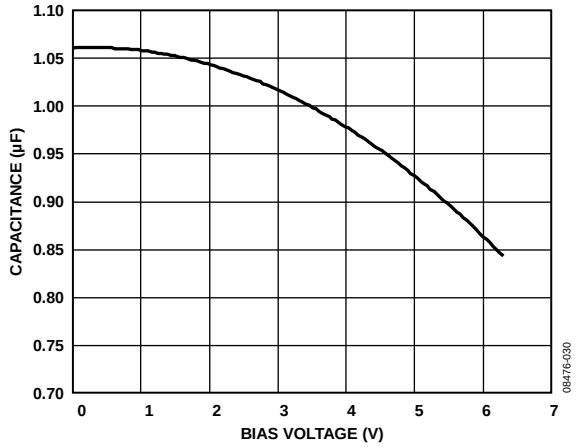


Figure 32. Capacitance vs. Capacitor Voltage Bias Characteristics

Equation 1 can be used to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:

C_{EFF} is the effective capacitance at the operating voltage.
C is the rated capacitance value.
$TEMPCO$ is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C is 0.94 µF at 4.2 V from the graph in Figure 32.

Substituting these values in Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP124/ADP125, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors are evaluated for each application.

UNDERVOLTAGE LOCKOUT

The ADP124/ADP125 have an internal undervoltage lockout circuit that disables all inputs and the output when the input voltage is less than approximately 2 V. This ensures that the ADP124/ADP125 inputs and the output behave in a predictable manner during power-up.

ENABLE FEATURE

The ADP124/ADP125 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 33, when a rising voltage on EN crosses the active threshold, VOUT turns on. Conversely, when a falling voltage on EN crosses the inactive threshold, VOUT turns off.

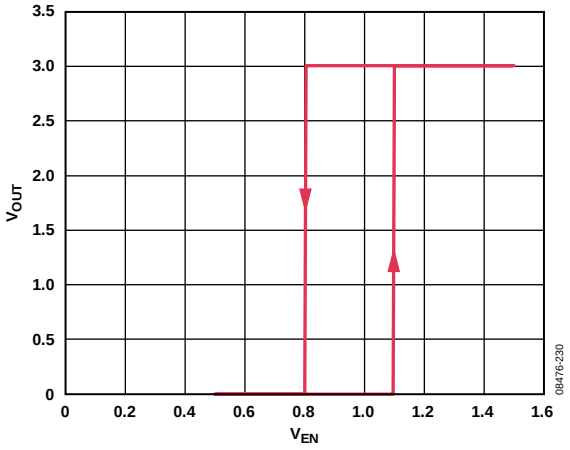


Figure 33. Typical EN Pin Operation

As shown in Figure 33, the EN pin has built-in hysteresis. This prevents on/off oscillations that may occur due to noise on the EN pin as it passes through the threshold points.

The active and inactive thresholds of the EN pin are derived from the VIN voltage. Therefore, these thresholds vary as the input voltage changes. Figure 34 shows typical EN active and inactive thresholds when the VIN voltage varies from 2.3 V to 5.5 V.

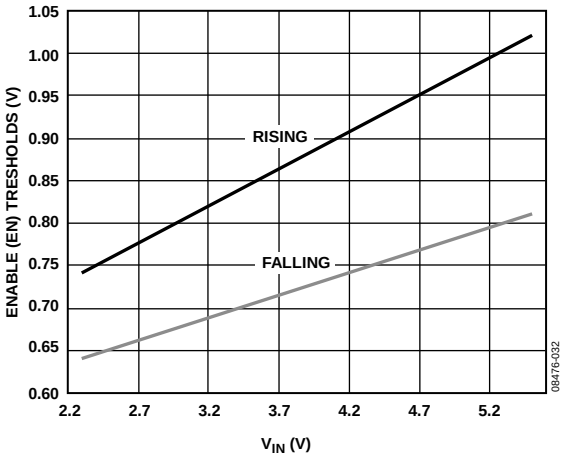


Figure 34. Typical EN Pin Thresholds vs. Input Voltage

The ADP124/ADP125 use an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 2.8 V option is approximately 350 µs from the time the EN active threshold is crossed to when the output reaches 90% of its final value. As shown in Figure 35, the start-up time is dependent on the output voltage setting and increases slightly as the output voltage increases.

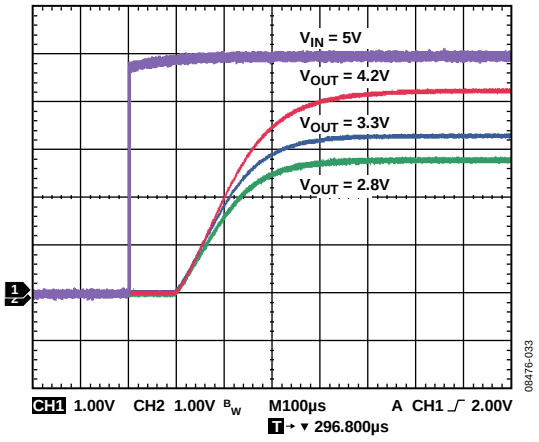


Figure 35. Typical Start-Up Time

CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP124/ADP125 are protected from damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP124/ADP125 are designed to limit the current when the output load reaches 750 mA (typical). When the output load exceeds 750 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C typical. Under extreme conditions (that is, high ambient temperature and power dissipation), when the junction temperature starts to rise above 150°C, the output is turned off, reducing output current to zero. When the junction temperature cools to less than 135°C, the output is turned on again and the output current is restored to its nominal value.

Consider the case where a hard short from VOUT to GND occurs. At first, the ADP124/ADP125 limit the current so that only 750 mA is conducted into the short. If self-heating causes the junction temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. When the junction temperature cools to less than 135°C, the output turns on and conducts 750 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C results in a current oscillation between 750 mA and 0 mA that continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device from damage due to accidental overload conditions. For reliable operation, the device power dissipation must be externally limited so that the junction temperature does not exceed 125°C.

THERMAL CONSIDERATIONS

To guarantee reliable operation, the junction temperature of the ADP124/ADP125 must not exceed 125°C. To ensure that the junction temperature is less than this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The value of θ_{JA} is dependent on the package assembly compounds used and the amount of copper to which the GND pins of the package are soldered on the PCB. Table 6 shows typical θ_{JA} values of the 8-lead MSOP package for various PCB copper sizes. Table 7 shows typical Ψ_{JB} values of the 8-lead MSOP and 8-lead 3 mm × 3 mm LFCSP package.

Table 6. Typical θ_{JA} Values for Specified PCB Copper Sizes

	θ_{JA} (°C/W)	
Copper Size (mm²)	**MSOP**	**LFCSP**
25	108.6	177.8
100	75.5	138.2
500	42.5	79.8
1000	34.7	67.8
6400	26.1	53.5

Table 7. Typical Ψ_{JB} Values

Ψ_{JB} (°C/W)	
MSOP	**LFCSP**
31.7	44.1

The junction temperature of the ADP124/ADP125 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (3)$$

where:
I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are input and output voltages, respectively.

The power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation can be simplified as follows:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 36 through Figure 41 show junction temperature calculations for different ambient temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

In cases where the board temperature is known, the thermal characterization parameter, Ψ_{JB}, can be used to estimate the junction temperature rise. The maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

JUNCTION TEMPERATURE CALCULATIONS

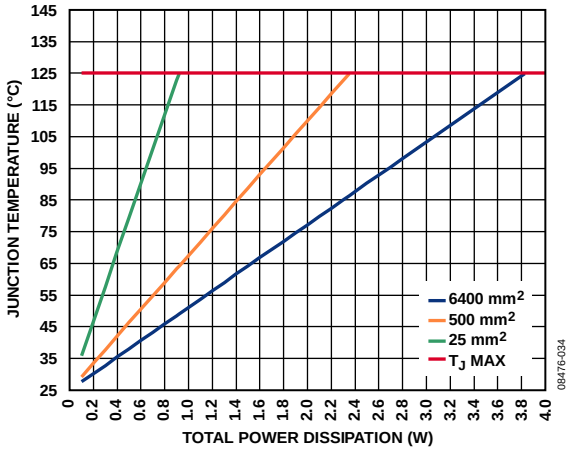


Figure 36. Junction Temperature vs. Power Dissipation and copper area, MSOP, T_A = 25°C

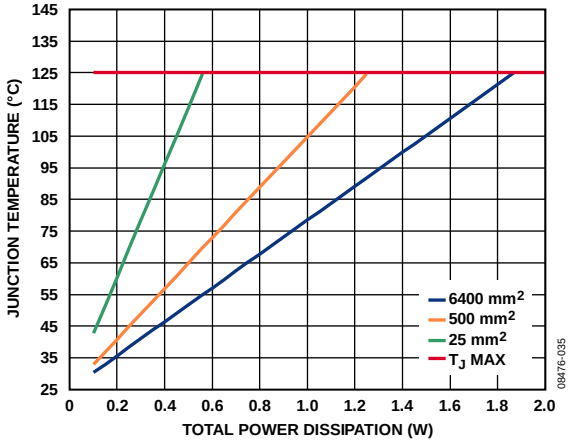


Figure 37. Junction Temperature vs. Power Dissipation and copper area, LFCSP, T_A = 25°C

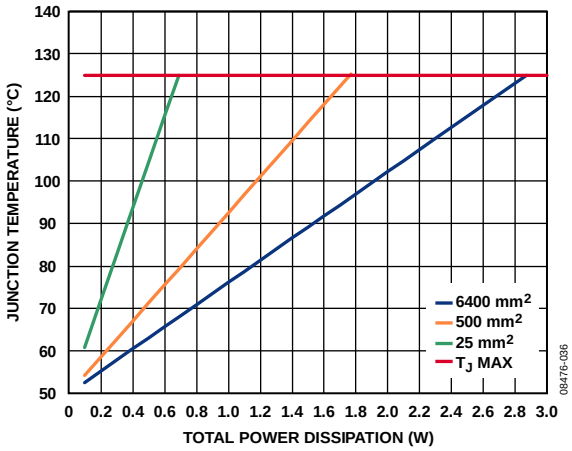


Figure 38. Junction Temperature vs. Power Dissipation and copper area, MSOP, T_A = 50°C

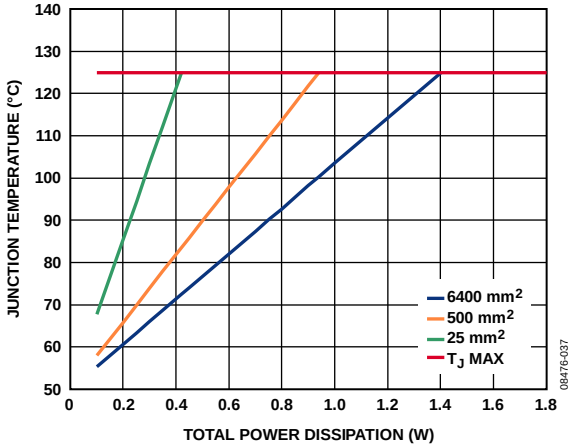


Figure 39. Junction Temperature vs. Power Dissipation and copper area, LFCSP, T_A = 50°C

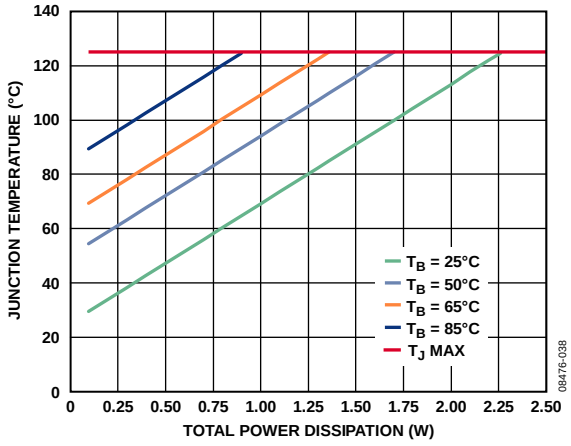


Figure 40. Junction Temperature vs. Power Dissipation, MSOP package at various Board Temperatures

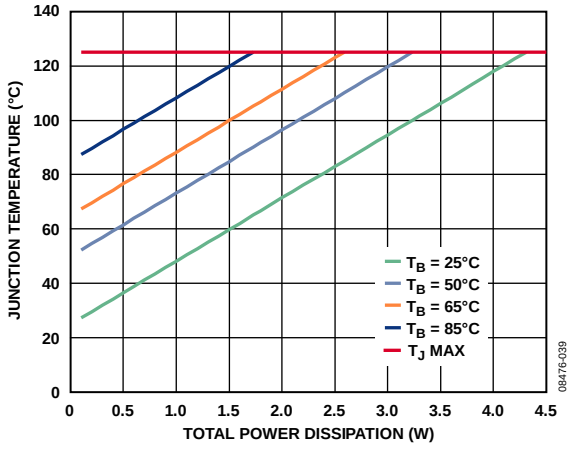


Figure 41. Junction Temperature vs. Power Dissipation, LFCSP package at various Board Temperatures

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP124/ADP125. However, as shown in Table 6, a point of diminishing returns eventually is reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

The input capacitor should be placed as close as possible to the VIN and GND pins, and the output capacitor should be placed as close as possible to the VOUT and GND pins. Use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where the area is limited.

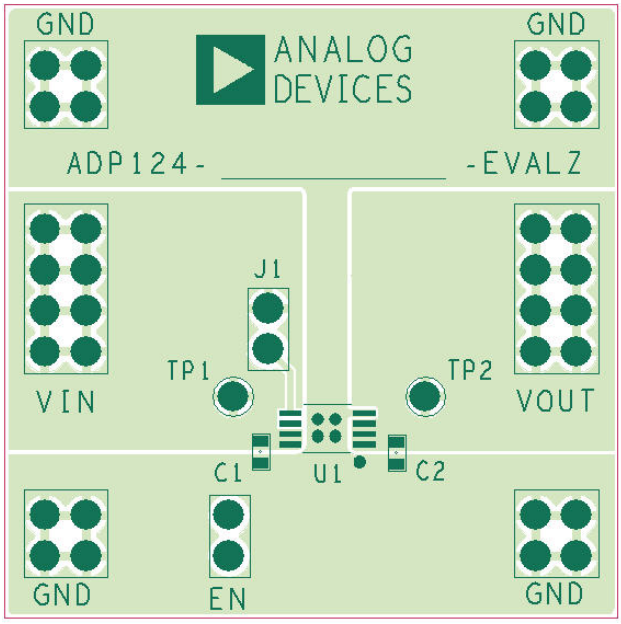


Figure 42. Example ADP124 MSOP PCB Layout

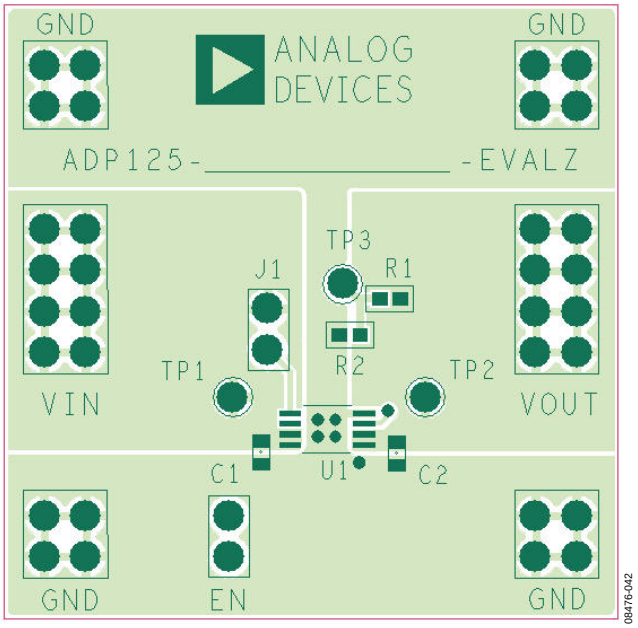


Figure 43. Example ADP125 MSOP PCB Layout

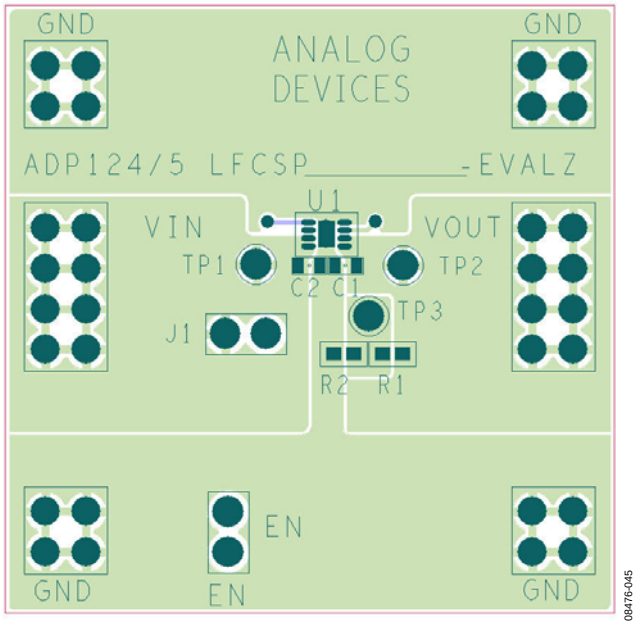
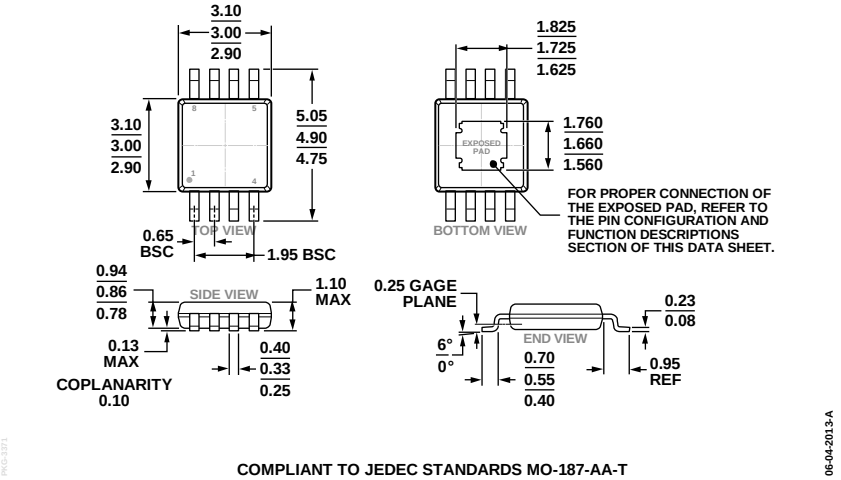


Figure 44. Example ADP124/ADP125 LFCSP PCB Layout

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA-T

Figure 45. 8-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]
(RH-8-1)
Dimensions shown in millimeters

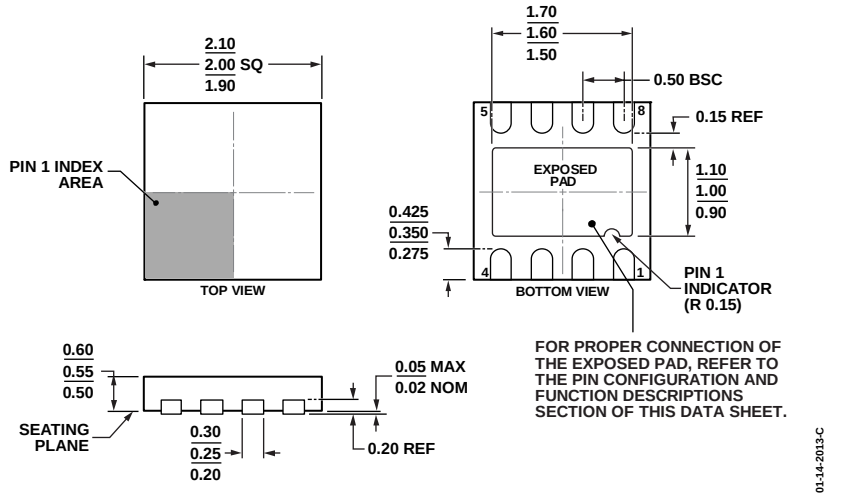


Figure 46. 8-Lead Lead Frame Chip Scale Package [LFCSP_UD]
2 mm × 2 mm Body, Ultra Thin, Dual Lead
(CP-8-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range (T_J)	Output Voltage (V)[2]	Package Description	Package Option	Branding
ADP124ARHZ-1.8-R7	–40°C to +125°C	1.8	8-Lead MINI_SO_EP	RH-8-1	37
ADP124ARHZ-2.5-R7	–40°C to +125°C	2.5	8-Lead MINI_SO_EP	RH-8-1	3T
ADP124ARHZ-2.7-R7	–40°C to +125°C	2.7	8-Lead MINI_SO_EP	RH-8-1	3U
ADP124ARHZ-2.8-R7	–40°C to +125°C	2.8	8-Lead MINI_SO_EP	RH-8-1	3Z
ADP124ARHZ-2.85-R7	–40°C to +125°C	2.85	8-Lead MINI_SO_EP	RH-8-1	40
ADP124ARHZ-2.9-R7	–40°C to +125°C	2.9	8-Lead MINI_SO_EP	RH-8-1	41
ADP124ARHZ-3.0-R7	–40°C to +125°C	3.0	8-Lead MINI_SO_EP	RH-8-1	49
ADP124ARHZ-3.3-R7	–40°C to +125°C	3.3	8-Lead MINI_SO_EP	RH-8-1	4F
ADP124ACPZ-1.8-R7	–40°C to +125°C	1.8	8-Lead LFCSP_UD	CP-8-10	LHH
ADP124ACPZ-2.8-R7	–40°C to +125°C	2.8	8-Lead LFCSP_UD	CP-8-10	LHJ
ADP124ACPZ-2.9-R7	–40°C to +125°C	2.9	8-Lead LFCSP_UD	CP-8-10	LM2
ADP124ACPZ-3.0-R7	–40°C to +125°C	3.0	8-Lead LFCSP_UD	CP-8-10	LHK
ADP124ACPZ-3.3-R7	–40°C to +125°C	3.3	8-Lead LFCSP_UD	CP-8-10	LHL
ADP125ACPZ-R7	–40°C to +125°C	0.8 to 5.0 (Adjustable)	8-Lead LFCSP_UD	CP-8-10	LHM
ADP125ARHZ-R7	–40°C to +125°C	0.8 to 5.0 (Adjustable)	8-Lead MINI_SO_EP	RH-8-1	38
ADP125ARHZ	–40°C to +125°C	0.8 to 5.0 (Adjustable)	8-Lead MINI_SO_EP	RH-8-1	38
ADP125-EVALZ		Adjustable	MSOP Evaluation Board		
ADP125CP-EVALZ		Adjustable	LFCSP Evaluation Board		
ADP124RHZ-REDYKIT			REDYKIT		
ADP124CPZ-REDYKIT			REDYKIT		

[1] Z = RoHS Compliant Part.
[2] Up to 31 fixed-output voltage options from 1.75 V to 3.3 V are available. For additional voltage options, contact a local Analog Devices, Inc., sales or distribution representative.

NOTES

NOTES

D08476-0-12/14(D)

Looking for pricing, stock, or lifecycle information?

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