



**THE DATASHEET OF  
NL17SZ06XV5T2**



# Single Inverter with Open Drain Output

## NL17SZ06

The NL17SZ06 is a single inverter with open drain output in tiny footprint packages.

### Features

- Designed for 1.65 V to 5.5 V  $V_{CC}$  Operation
- 2.1 ns  $t_{PD}$  at  $V_{CC} = 5$  V (typ)
- Input/Output Overvoltage Tolerant up to 5.5 V
- $I_{OFF}$  Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.0 V
- Available in SC-88A, SC-74A, SOT-553, SOT-953 and UDFN6 Packages
- Chip Complexity < 100 FETs
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

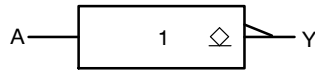
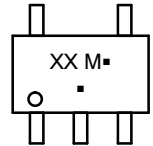


Figure 1. Logic Symbol

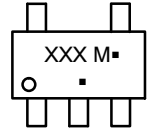
### MARKING DIAGRAMS



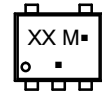
SC-88A  
CASE 419A



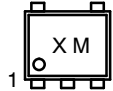
SC-74A  
DBV SUFFIX  
CASE 318BQ



SOT-553  
XV5 SUFFIX  
CASE 463B



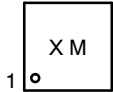
SOT-953  
P5 SUFFIX  
CASE 527AE



UDFN6  
1.45 x 1.0  
CASE 517AQ



UDFN6  
1.0 x 1.0  
CASE 517BX



XX = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.

## NL17SZ06

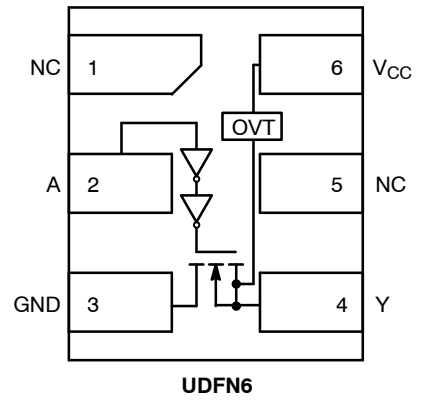
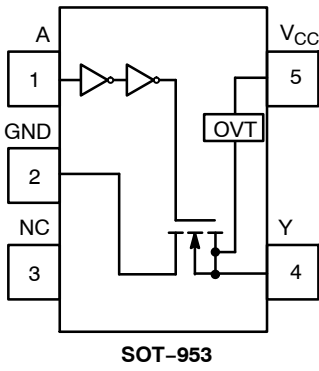
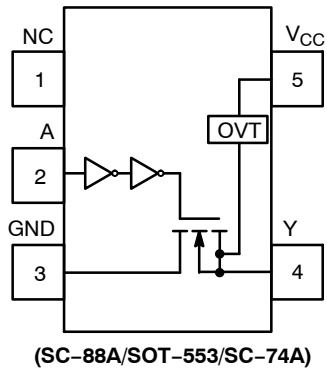


Figure 2. Pinout (Top View)

### PIN ASSIGNMENT (SC-88A/SOT-553/SC-74A)

Pin	Function
1	NC
2	A
3	GND
4	Y
5	V <sub>CC</sub>

### PIN ASSIGNMENT (SOT-953)

Pin	Function
1	A
2	GND
3	NC
4	Y
5	V <sub>CC</sub>

### PIN ASSIGNMENT (UDFN)

Pin	Function
1	NC
2	A
3	GND
4	Y
5	NC
6	V <sub>CC</sub>

### FUNCTION TABLE

A Input	Y Output
L	Z
H	L

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## MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +6.5	V
$V_{IN}$	DC Input Voltage	-0.5 to +6.5	V
$V_{OUT}$	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ( $V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +6.5 -0.5 to +6.5	V
$I_{IK}$	DC Input Diode Current $V_{IN} < GND$	-50	mA
$I_{OK}$	DC Output Diode Current $V_{OUT} < GND$	-50	mA
$I_{OUT}$	DC Output Source/Sink Current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC Supply Current per Supply Pin or Ground Pin	$\pm 100$	mA
$T_{STG}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature, 1 mm from Case for 10 secs	260	$^{\circ}C$
$T_J$	Junction Temperature Under Bias	+150	$^{\circ}C$
$\theta_{JA}$	Thermal Resistance (Note 2)	SC-88A SC-74A SOT-553 SOT-953 UDFN6	377 320 324 254 154 $^{\circ}C/W$
$P_D$	Power Dissipation in Still Air	SC-88A SC-74A SOT-553 SOT-953 UDFN6	332 390 386 491 812 mW
MSL	Moisture Sensitivity	Level 1	-
$F_R$	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
$V_{ESD}$	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)	$\pm 100$	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.
3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

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## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
$V_{CC}$	Positive DC Supply Voltage	1.65	5.5	V
$V_{IN}$	DC Input Voltage	0	5.5	V
$V_{OUT}$	DC Output Voltage	0	$V_{CC}$	V
	Active-Mode (High or Low State)	0	5.5	
	Tri-State Mode (Note 1)	0	5.5	
	Power-Down Mode ( $V_{CC} = 0$ V)	0	5.5	
$T_A$	Operating Temperature Range	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time			ns/V
	$V_{CC} = 1.65$ V to $1.95$ V	0	20	
	$V_{CC} = 2.3$ V to $2.7$ V	0	20	
	$V_{CC} = 3.0$ V to $3.6$ V	0	10	
	$V_{CC} = 4.5$ V to $5.5$ V	0	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Units
				Min	Typ	Max	Min	Max	
$V_{IH}$	High-Level Input Voltage		1.65 to 1.95	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
			2.3 to 5.5	$0.70 \times V_{CC}$	-	-	$0.70 \times V_{CC}$	-	
$V_{IL}$	Low-Level Input Voltage		1.65 to 1.95	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
			2.3 to 5.5	-	-	$0.30 \times V_{CC}$	-	$0.30 \times V_{CC}$	
$V_{OL}$	Low-Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$	1.65 to 5.5	-	-	0.1	-	0.1	V
		$I_{OL} = 100 \mu\text{A}$	1.65	-	0.08	0.24	-	0.24	
		$I_{OL} = 4 \text{ mA}$	2.3	-	0.2	0.3	-	0.3	
		$I_{OL} = 8 \text{ mA}$	2.7	-	0.22	0.4	-	0.4	
		$I_{OL} = 12 \text{ mA}$	3.0	-	0.28	0.4	-	0.4	
		$I_{OL} = 16 \text{ mA}$	3.0	-	0.38	0.55	-	0.55	
		$I_{OL} = 24 \text{ mA}$	4.5	-	0.42	0.55	-	0.55	
$I_{IN}$	Input Leakage Current	$V_{IN} = 5.5$ V or GND	1.65 to 5.5	-	-	$\pm 0.1$	-	$\pm 1.0$	$\mu\text{A}$
$I_{OZ}$	3-State Output Leakage Current	$V_{OUT} = 0$ V to $5.5$ V	1.65 to 5.5	-	-	$\pm 0.5$	-	$\pm 5.0$	$\mu\text{A}$
$I_{OFF}$	Power Off Leakage Current	$V_{IN} = 5.5$ V or $V_{OUT} = 5.5$ V	0	-	-	1.0	-	10	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5	-	-	1.0	-	10	$\mu\text{A}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-55°C ≤ T <sub>A</sub> ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
t <sub>PZL</sub>	Propagation Delay, A to Y (Figures 3 and 4)		1.65 to 1.95	-	6.0	9.0	-	9.5	ns
			2.3 to 2.7	-	3.6	6.1	-	6.5	
			3.0 to 3.6	-	2.7	5.6	-	6.0	
			4.5 to 5.5	-	2.1	4.4	-	4.8	
t <sub>PLZ</sub>	Propagation Delay, A to Y (Figures 3 and 4)		1.65 to 1.95	-	4.0	9.0	-	9.5	ns
			2.3 to 2.7	-	2.8	6.1	-	6.5	
			3.0 to 3.6	-	2.5	5.6	-	6.0	
			4.5 to 5.5	-	2.2	4.4	-	4.8	

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub>	2.5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub>	2.5	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)	10 MHz, V <sub>CC</sub> = 3.3 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub>	9	pF
		10 MHz, V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub>	11	

5. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

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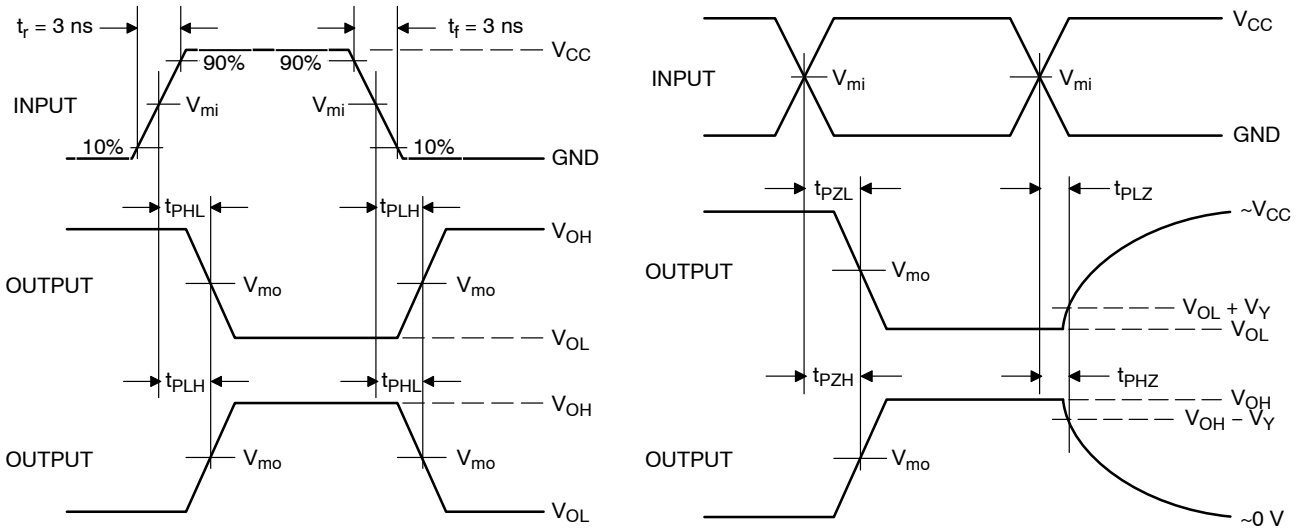


$C_L$  includes probe and jig capacitance  
 $R_T$  is  $Z_{OUT}$  of pulse generator (typically 50  $\Omega$ )  
 $f = 1$  MHz

**Figure 3. Test Circuit**

Test	Switch Position	$C_L$ , pF	$R_L$ , $\Omega$	$R_1$ , $\Omega$
$t_{PLH} / t_{PHL}$	Open	See AC Characteristics Table		
$t_{PLZ} / t_{PZL}$	$2 \times V_{CC}$	50	500	500
$t_{PHZ} / t_{PZH}$	GND	50	500	500

X = Don't Care



**Figure 4. Switching Waveforms**

$V_{CC}$ , V	$V_{mi}$ , V	$V_{mo}$ , V		$V_Y$ , V
		$t_{PLH}, t_{PHL}$	$t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}$	
1.65 to 1.95	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
2.3 to 2.7	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
3.0 to 3.6	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3
4.5 to 5.5	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3

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## DEVICE ORDERING INFORMATION

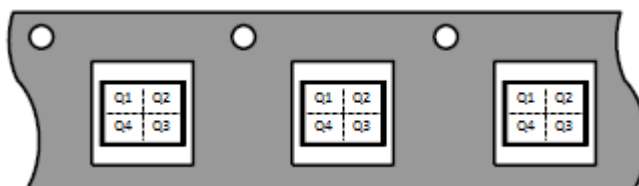
Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping <sup>†</sup>
NL17SZ06DFT2G	SC-88A	LF	Q4	3000 / Tape & Reel
NL17SZ06DFT2G-Q*	SC-88A	LF	Q4	3000 / Tape & Reel
NL17SZ06DBVT1G	SC-74A	AF	Q4	3000 / Tape & Reel
NL17SZ06XV5T2G	SOT-553	LF	Q4	4000 / Tape & Reel
NL17SZ06MU1TCG (Contact <b>onsemi</b> )	UDFN6, 1.45 x 1.0, 0.5P	TBD	Q4	3000 / Tape & Reel
NL17SZ06MU3TCG (Contact <b>onsemi</b> )	UDFN6, 1.0 x 1.0, 0.35P	TBD	Q4	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

### Pin 1 Orientation in Tape and Reel

Direction of Feed



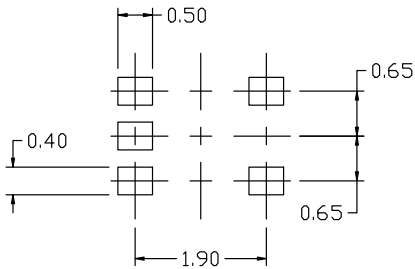
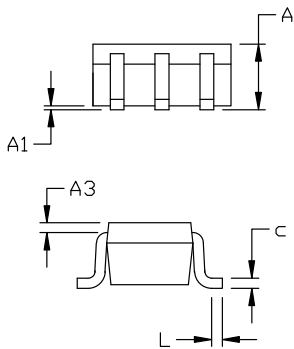
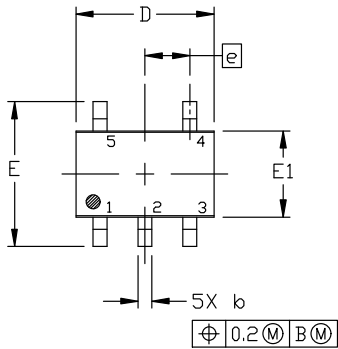
# NL17SZ06

## PACKAGE DIMENSIONS

**SC-88A (SC-70-5/SOT-353)**  
**CASE 419A-02**  
**ISSUE M**

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.



**RECOMMENDED  
MOUNTING FOOTPRINT**

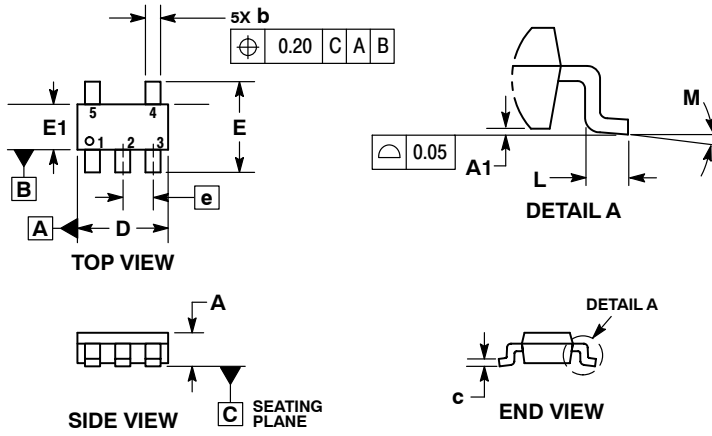
- \* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

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## PACKAGE DIMENSIONS

### SC-74A CASE 318BQ ISSUE B

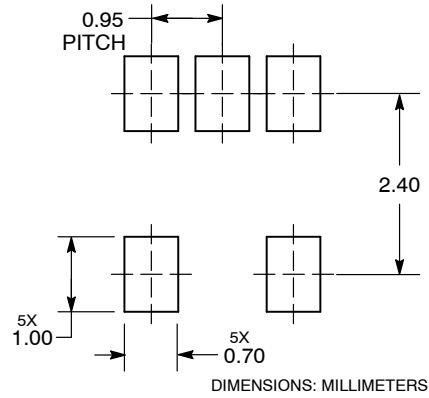


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
A1	0.01	0.10
b	0.25	0.50
c	0.10	0.26
D	2.85	3.15
E	2.50	3.00
E1	1.35	1.65
e	0.95 BSC	
L	0.20	0.60
M	0°	10°

### RECOMMENDED SOLDERING FOOTPRINT\*

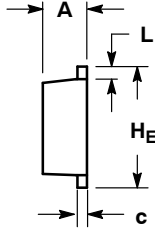
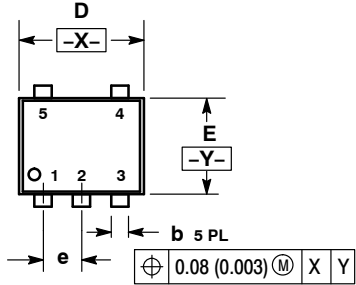


\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NL17SZ06

## PACKAGE DIMENSIONS

SOT-553, 5 LEAD  
CASE 463B  
ISSUE C

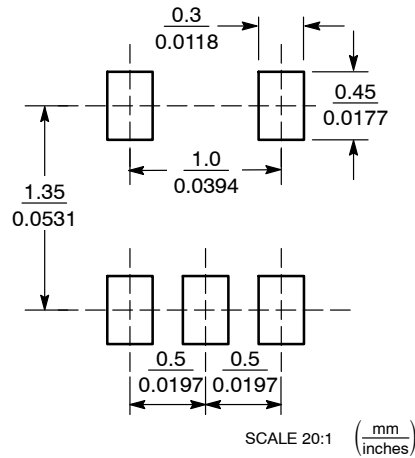


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.15	1.20	1.25	0.045	0.047	0.049
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.55	1.60	1.65	0.061	0.063	0.065

### RECOMMENDED SOLDERING FOOTPRINT\*

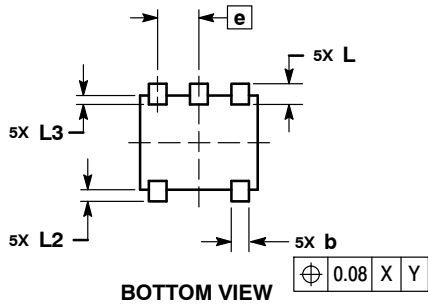
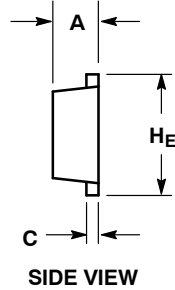
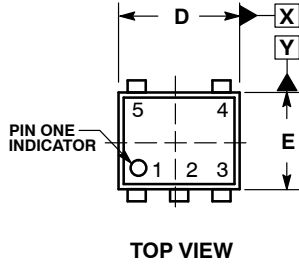


\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NL17SZ06

## PACKAGE DIMENSIONS

**SOT-953**  
CASE 527AE  
ISSUE E

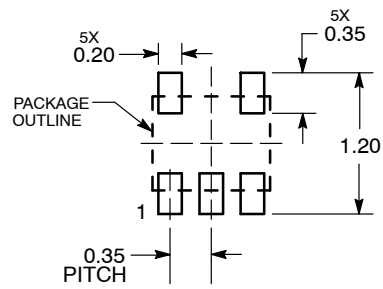


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H <sub>E</sub>	0.95	1.00	1.05
L	0.175 REF		
L2	0.05	0.10	0.15
L3	---	---	0.15

**SOLDERING FOOTPRINT\***



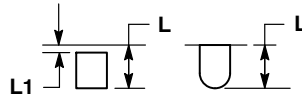
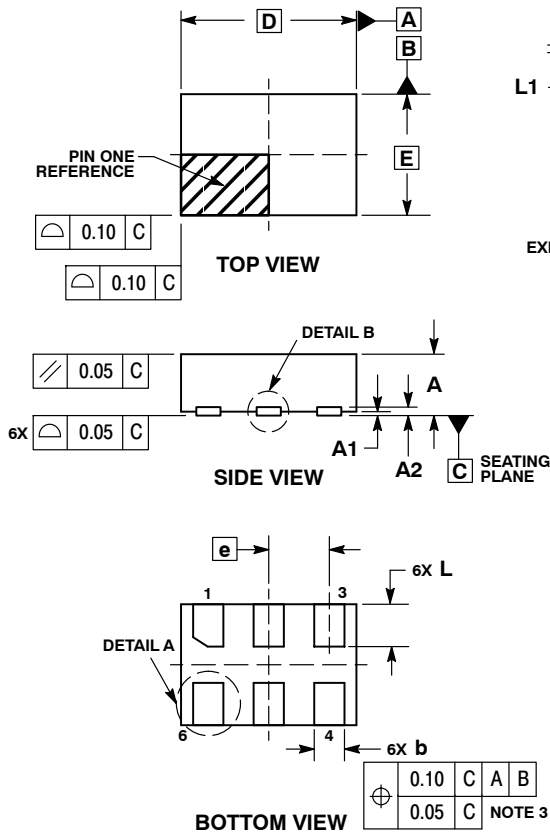
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

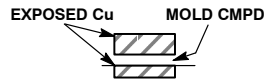
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## PACKAGE DIMENSIONS

UDFN6, 1.45x1.0, 0.5P  
CASE 517AQ  
ISSUE O



**DETAIL A**  
OPTIONAL  
CONSTRUCTIONS



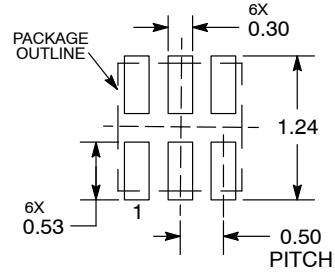
**DETAIL B**  
OPTIONAL  
CONSTRUCTIONS

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07	REF
b	0.20	0.30
D	1.45	BSC
E	1.00	BSC
e	0.50	BSC
L	0.30	0.40
L1	---	0.15

### MOUNTING FOOTPRINT



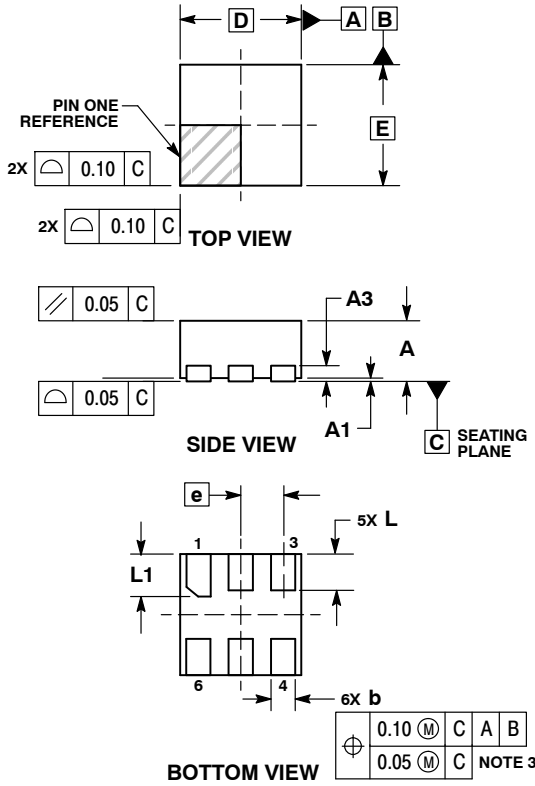
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NL17SZ06

## PACKAGE DIMENSIONS

UDFN6, 1x1, 0.35P  
CASE 517BX  
ISSUE 0

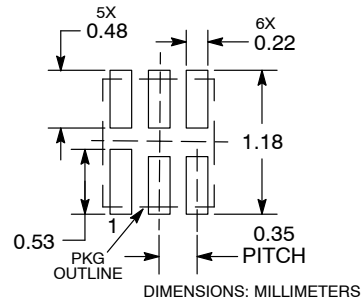


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.12	0.22
D	1.00	BSC
E	1.00	BSC
e	0.35	BSC
L	0.25	0.35
L1	0.30	0.40

**RECOMMENDED SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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