THE DATASHEET OF

SL23EP05SI-1HT

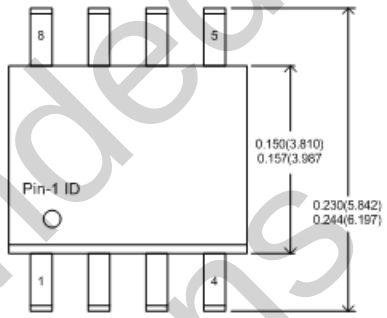
SL23EP05

Not Recommended for New Designs

Low Jitter and Skew 10 to 220 MHz Zero Delay Buffer (ZDB)

Features

- 10 to 220 MHz operating frequency range
- Low output clock jitter:
  - 50 ps-typ cycle-to-cycle jitter
  - 20 ps-typ period jitter
- Low output-to-output skew: 30 ps-typ
- Low product-to-product skew: 60 ps-typ
- Wide 2.5 V to 3.3 V power supply range
- Low power dissipation:
  - 16 mA-max at 66 MHz and VDD = 3.3 V
  - 14 mA-max at 66 MHz and VDD = 2.5 V
- One input drives five outputs organized as 4+1
- SpreadThru™ PLL that allows use of SSCG
- Standard and High-Drive options
- Available in 8 pin SOIC and TSSOP packages
- Available in Commercial and Industrial grades



Ordering Information:
See page 14.

Applications

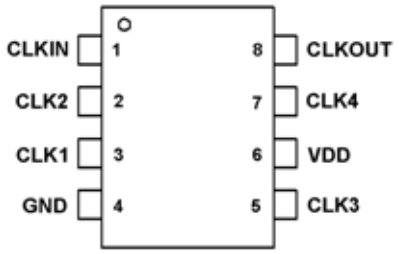
- Printers and MFPs
- Digital Copiers
- PCs and Work Stations
- Routers, Switchers and Servers
- Digital Embedded Systems

Benefits

- Up to five distribution of input clock
- Standard and High-Drive levels to control impedance level, frequency range and EMI
- Low power dissipation, jitter and skew
- Low cost

Pin Assignments

SL23EP05



Patents pending

Description

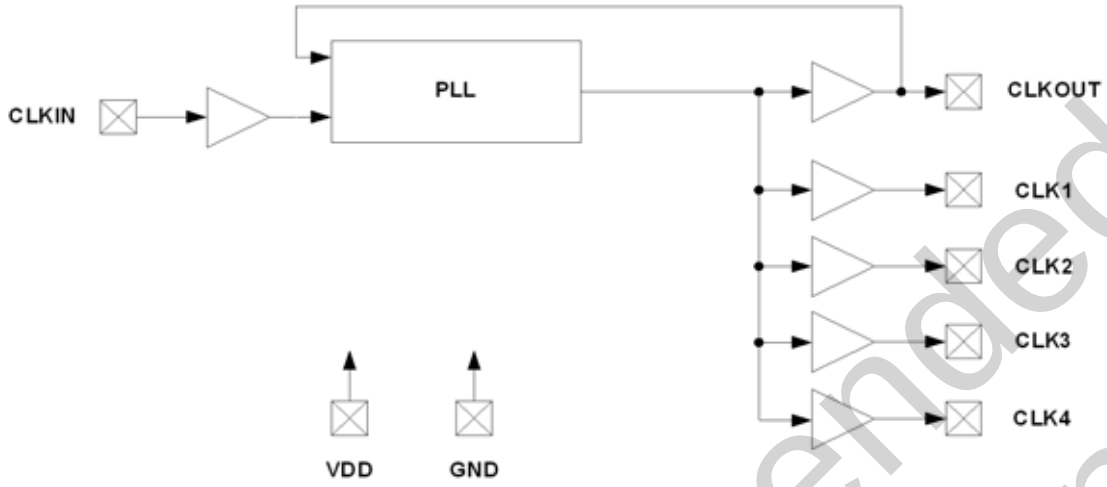
The SL23EP05 is a low skew, low jitter, and low power Zero Delay Buffer (ZDB) designed to produce up to five clock outputs from one reference input clock for high speed clock distribution applications. The product has an on-chip PLL which locks to the input clock at CLKIN and receives its feedback internally from the CLKOUT pin.

The SL23EP05 is available with two drive strength versions called –1 and –1H. The –1 is the standard-drive version and –1H is the high-drive version.

The SL23EP05 high-drive version operates up to 220 MHz and 180 MHz at 3.3 V and 2.5 V power supplies, respectively. The standard drive version –1 operates up to 200 MHz and 167 MHz at 3.3 V and 2.5 V, respectively.

The SL23EP05 enter into Power Down (PD) mode if the input at CLKIN is less then 2.0 MHz or there is no rising edge. In this state all five outputs are tri-stated and the PLL is turned off leading to less than 10 µA of power supply current draw.

Functional Block Diagram



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1. Electrical Specifications

Table 1. DC Electrical Specifications (V_{DD} = 3.3 V)

Unless otherwise stated for both C and I Grades.

Parameter	Symbol	Test Condition	Min	Max	Unit
Supply Voltage	VDD		3.0	3.6	V
Input LOW Voltage	VIL		—	0.8	V
Input HIGH Voltage	VIH		2.0	V_{DD}+0.3	V
Input Leakage Current	IIL	0 < VIN < 0.8 V	—	±10	µA
Input HIGH Current	IIH	VIN = V_{DD}	—	100	µA
Output LOW Voltage	VOL	IOL = 8 mA (Standard Drive)	—	0.4	V
		IOL = 12 mA (High Drive)	—	0.4	V
Output HIGH Voltage	VOH	IOH = –8 mA (Standard Drive)	2.4	—	V
		IOH = –12 mA (High Drive)	2.4	—	V
Power Down Supply Current	IDDPD	CLKIN = 0 MHz (Commercial)	—	10	µA
		CLKIN = 0 MHz (Industrial)	—	25	µA
Power Supply Current	IDD	All Outputs CL = 0, 66-MHz CLKIN	—	16	mA

Table 2. DC Electrical Specifications (V_{DD} = 2.5 V)

Unless otherwise stated for both C and I Grades.

Parameter	Symbol	Test Condition	Min	Max	Unit
Supply Voltage	VDD		2.3	2.7	V
Input LOW Voltage	VIL		—	0.7	V
Input HIGH Voltage	VIH		1.7	V_{DD}+ 0.3	V
Input Leakage Current	IIL	0<VIN < 0.8 V	—	+/-10	µA
Input HIGH Current	IIH	VIN = V_{DD}	—	100	µA
Output LOW Voltage	VOL	IOL = 8 mA (Standard drive)	—	0.5	V
		IOL = 12 mA (High drive)	—	0.5	V
Output HIGH Voltage	VOH	IOH = –8 mA (Standard drive)	V_{DD} – 0.6	—	V
		IOH = –12 mA (High drive)	V_{DD} – 0.6	—	V
Power Down Supply Current	IDDPD	CLKIN = 0 MHz (Commercial)	—	10	µA
		CLKIN = 0 MHz (Industrial)	—	25	µA
Power Supply Current	IDD	All Outputs CL = 0, 66 MHz CLKIN	—	14	mA

Table 3. AC Electrical Specifications (V_{DD} = 3.3 V and 2.5 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Frequency (Input=Output) [1]	FMAX	3.3 V High Drive	10	—	220	MHz
		3.3 V Standard Drive	10	—	200	MHz
		2.5 V High Drive	10	—	180	MHz
		2.5 V Standard Drive	10	—	167	MHz
Input Duty Cycle	INDC	<135 MHz, V_{DD} = 3.3 V	25	—	75	%
		<135 MHz, V_{DD} = 2.5 V	40	—	60	%
Output Duty Cycle [2]	OUTDC	<135 MHz, V_{DD} = 3.3 V	45	—	55	%
		<135 MHz, V_{DD} = 2.5 V	40	—	60	%
Rise, Fall Time (3.3V) Measured at: 0.8 to 2.0 V [2]	tr/f3.3	High drive, CL = 15 pF, >135 MHz	—	—	0.5	ns
		Std drive, CL = 15 pF, <170 MHz	—	—	1.5	ns
		High drive, CL = 30 pF, <100 MHz	—	—	1.5	ns
		Std drive, CL = 30 pF, <100 MHz	—	—	2.5	ns
Rise, Fall Time (2.5) [2] Measured at: 0.6 to 1.8 V	tr/f2.5	High drive, CL = 15 pF, >135 MHz	—	—	1.5	ns
		Std drive, CL = 15 pF, <135 MHz	—	—	2.5	ns
		High drive, CL = 30 pF, <100 MHz	—	—	2.5	ns
Output-to-Output Skew [2]	t1	All outputs CL = 0, 3.3 V supply, 2.5 V power supply, standard drive	—	30	90	ps
		All outputs CL = 0, 2.5 V power supply, high drive	—	40	100	ps
Delay Time, CLKIN Rising Edge to CLKOUT Rising Edge [2]	t2	PLL enabled @ 3.3 V	–100	—	100	ps
		PLL enabled @2.5 V	–200	—	200	ps
Part-to-Part Skew [2]	t3	Measured at V_{DD}/2. Any output to any output, 3.3 V supply	–150	—	150	ps
		Measured at V_{DD}/2. Any output to any output, 2.5 V supply	–300	—	300	ps

Notes:
1. For the given maximum loading conditions. See CL in Operating Conditions Table.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 4. AC Electrical Specifications (V_{DD} = 3.3 V and 2.5 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Lock Time[9]	tPLLOCK	From 90% of V_{DD} to valid clocks presented on all output clock pins	—	—	1.0	ms
Cycle-to-cycle Jitter	CCJ *	3.3 V supply, >66 MHz, <15 pF, Standard Drive	—	50	125	ps
		3.3 V supply, >66 MHz, <30 pF, High Drive	—	70	140	ps
		3.3 V supply, >66 MHz, <30 pF, Standard Drive	—	80	170	ps
		2.5 V supply, >66 MHz, <15 pF, High Drive	—	50	80	ps
		2.5 V supply, >66 MHz, <15 pF, Standard Drive	—	90	200	ps
		2.5 V supply, >66 MHz, <30 pF, High Drive	—	100	250	ps
Peak Period Jitter	PPJ *	3.3 V supply, >100 MHz, <15 pF, Standard Drive	—	30	65	ps
		3.3 V supply, 66–100 MHz, <15 pF, Standard Drive	—	40	75	ps
		3.3 V supply, >66 MHz, <30 pF, High Drive	—	60	120	ps
		3.3 V supply, >66 MHz, <30 pF, Standard Drive	—	70	150	ps
		2.5 V supply, > 100 MHz, <15 pF, High Drive	—	20	45	ps
		2.5 V supply, 66–100 MHz, <15 pF, High Drive	—	20	60	ps
		2.5 V supply, >66 MHz, <15 pF, Standard Drive	—	60	120	ps

***Note:** Typical jitter is measured at 3.3 V or 2.5 V, 30ºC with all outputs driven into the maximum specified load.

Table 5. Operating Conditions

Unless otherwise stated V_{DD} = 2.5 V to 3.3 V and for both C and I Grades.

Parameter	Symbol	Test Condition	Min	Max	Unit
3.3 V Supply Voltage	VDD3.3		3.0	3.6	V
2.5 V Supply Voltage	VDD2.5		2.3	2.7	V
Operating Temperature (Ambient)	TA	Commercial	0	70	°C
		Industrial	–40	85	°C
Load Capacitance	CLOAD	<220 MHz, 3.3 V with High Drive	—	15	pF
		<200 MHz, 3.3 V with Standard Drive	—	15	pF
		<180 MHz, 2.5 V with High Drive	—	15	pF
		<167 MHz, 2.5 V with Standard Drive	—	15	pF
		<200 MHz, 3.3 V with High Drive	—	22	pF
		<180 MHz, 3.3 V with Standard Drive	—	22	pF
		<167 MHz, 2.5 V with High Drive	—	22	pF
		<134 MHz, 2.5 V with Standard Drive	—	22	pF
		<133 MHz, 3.3 V with High Drive	—	30	pF
		<100 MHz, 3.3 V with Standard Drive	—	30	pF
		<80 MHz, 2.5 V with High Drive	—	30	pF
		< 67 MHz, 2.5 V with Standard Drive	—	30	pF
Input Capacitance	CIN	CLKIN pin	—	5	pF
Closed-loop bandwidth	CLBW	3.3 V, (typical)	1-1.5		MHz
		2.5 V, (typical)	0.8		MHz
Output Impedance	ZOUT	3.3 V, (typical), High Drive	29		Ω
		3.3 V, (typical), Standard Drive	41		Ω
		2.5 V, (typical), High Drive	37		Ω
		2.5 V, (typical), Standard Drive	41		Ω

Table 6. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient		Still air	—	110	—	°C/W
		1 m/s air flow	—	100	—	°C/W
		3 m/s air flow	—	80	—	°C/W
Thermal Resistance Junction to Case		Independent of air flow	—	35	—	°C/W

Table 7. Absolute Maximum Rating

Parameter	Test Condition	Min	Max	Unit
Supply voltage, V_{DD}		–0.5	4.6	V
All Inputs and Outputs		–0.5	V_{DD}+0.5	V
Ambient Operating Temperature	In operation, C-Grade	0	70	°C
Ambient Operating Temperature	In operation, I-Grade	–40	85	°C
Storage Temperature	No power is applied	–65	150	°C
Junction Temperature	In operation, power is applied	—	125	°C
Soldering Temperature		—	260	°C
ESD Rating (Human Body Model)	JEDECC22-A114D	–4000	4000	V
ESD Rating (Charge Device Model)	JEDECC22-C101C	–1500	1500	V
ESD Rating (Machine Model)	JEDECC22-A115D	–200	200	V

2. General Description

The SL23EP05 is a low skew, low jitter Zero Delay Buffer with very low operating current.

The product includes an on-chip high performance PLL that locks into the input reference clock and produces five output clock drivers tracking the input reference clock for systems requiring clock distribution.

3. Input and Output Frequency Range

The input and output frequency range is the same. However, it depends on V_{DD} and drive levels as given in the below Table 8.

Table 8. Input/Output Frequency Range

V_{DD} (V)	Drive	Min (MHz)	Max (MHz)
3.3	HIGH	10	220
3.3	STD	10	200
2.5	HIGH	10	180
2.5	STD	10	167

If the input clock frequency is DC (0 to V_{DD}), this is detected by an input frequency detection circuitry and all five clock outputs are forced to Hi-Z. The PLL is shutdown to save power. In this shutdown state, the product draws less than 10 µA supply current.

4. SpreadThru™ Feature

If a Spread Spectrum Clock (SSC) were to be used as an input clock, the SL23EP05 is designed to pass the modulated Spread Spectrum Clock (SSC) signal from its reference input to the output clocks. The same spread characteristics at the input are passed through the PLL and drivers without any degradation in spread percent (%), spread profile and modulation frequency.

5. High and Low-Drive Product Options

The SL23EP05 is offered with High-Drive “–1H” and Standard-Drive “–1” options. These drive options enable the users to control load levels, frequency range and EMI control. Refer to the AC electrical tables for the details.

6. Skew and Zero Delay

All outputs should drive the similar load to achieve output-to-output skew and input-to-output specifications given in the AC electrical tables. However, Zero delay between input and outputs can be adjusted by changing the loading of CLKOUT relative to the banks A and B clocks since CLKOUT is the feedback to the PLL.

7. Power Supply Range (V_{DD})

The SL23EP05 is designed to operate in a wide power supply range from 2.250 V (Min) to 3.360 V (Max). This power supply range complies with 3.3 V+/–10% and 2.5 V+/–10% standard power supply requirements used in most systems. An internal on-chip voltage regulator is used to supply PLL constant power supply of 1.8 V, leading to a consistent and stable PLL electrical performance in terms of skew, and jitter and power dissipation.

8. External Components and Design Considerations

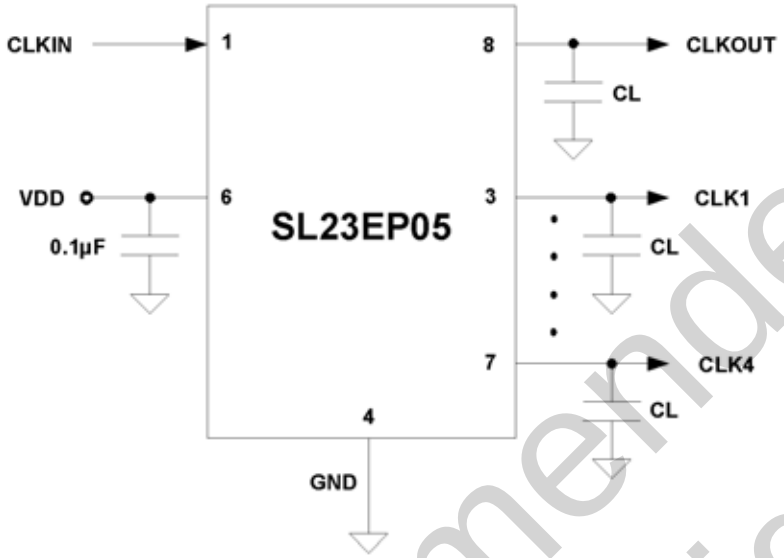

Figure 1. Typical Application Schematic

8.1. Comments and Recommendations

Decoupling Capacitor: A minimum decoupling capacitor of 0.1 µF must be used between VDD and VSS on the pins 6 and 4. Additional capacitors may be necessary depending on the application. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin.

Series Termination Resistor: A series termination resistor is recommended if the distance between the output (SSCLK) and the load is over 1.5 inches. The nominal impedance of the SSCLK output is about 30 Ω. Use 20 Ω resistor in series with the output to terminate 50 Ω trace impedance and place 20 Ω resistor as close to the clock outputs as possible.

Zero Delay and Skew Control: All outputs and CLKIN pins should be loaded with the same load to achieve “Zero Delay” between the CLKIN and the outputs. The CLKOUT pin is connected to CLKIN internally on-chip for internal feedback to PLL, and sees an additional 2 pF load with respect to the clock pins. For applications requiring zero input/output delay, the load at the all output pins including the CLKOUT pin must be the same. If any delay adjustment is required, the capacitance at the CLKOUT pin could be increased or decreased to increase or decrease the delay between clocks and CLKIN.

For minimum pin-to-pin skew, the external load at the clocks must be the same.

8.2. Switching Waveforms

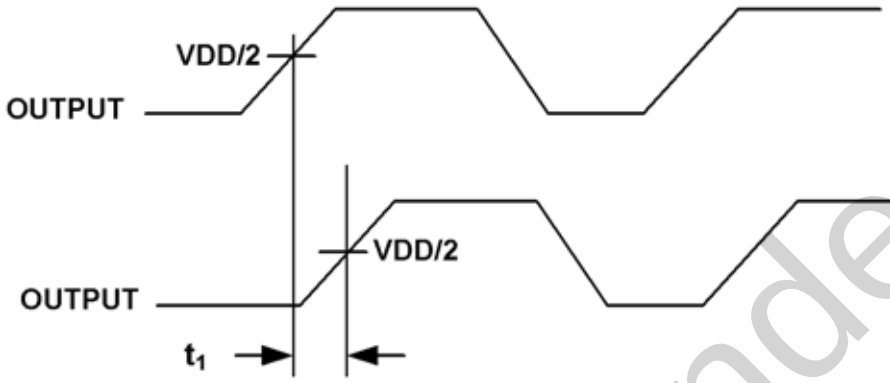

Figure 2. Output to Output Skew

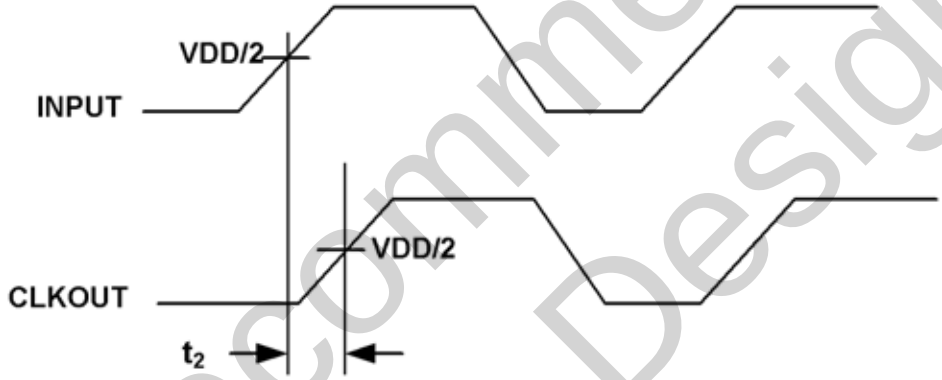

Figure 3. Input to Output Skew

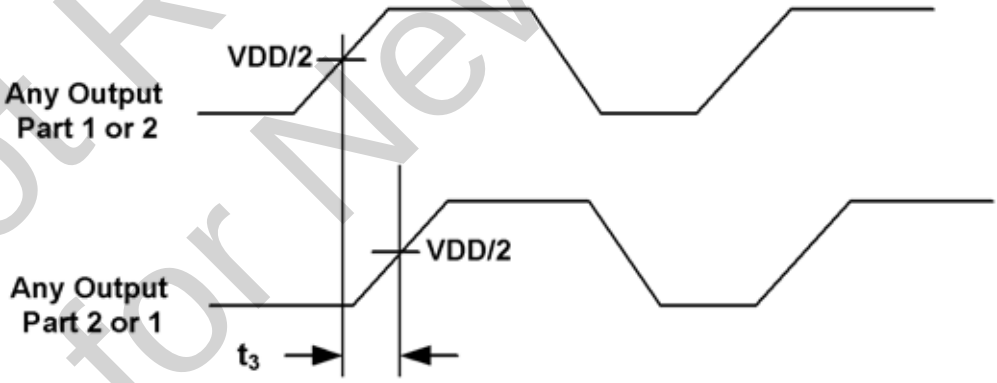

Figure 4. Part-to-Part Skew

9. Pin Descriptions

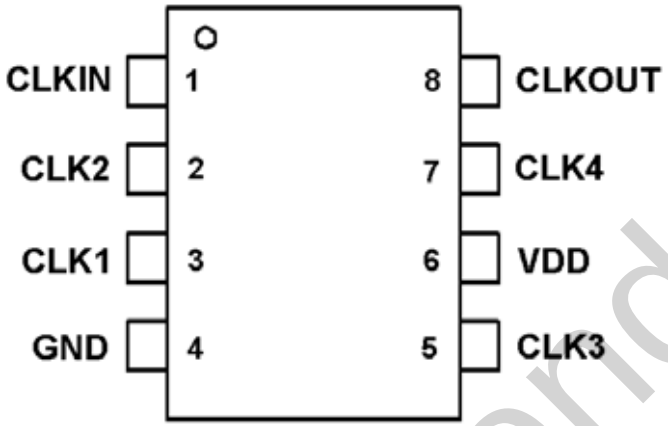

Figure 5. 8-Pin SOIC

Table 9. Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	Reference Frequency Clock Input. Weak pull-down (150 kΩ).
2	CLK2	Output	Buffered Clock Output Weak pull-down (150 kΩ).
3	CLK1	Output	Buffered Clock Output. Weak pull-down (150 kΩ).
4	GND	Power	Power Ground.
5	CLK3	Output	Buffered Clock Output. Weak pull-down (150 kΩ).
6	VDD	Power	3.3 V or 2.5 V Power Supply.
7	CLK4	Output	Buffered Clock Output. Weak pull-down (150 kΩ).
8	CLKOUT	Output	Buffered Clock Output. Used for Internal Feedback to PLL Input. Weak pull-down (150 kΩ).

10. Package Outline and Dimensions

10.1. 8-Lead SOIC (150 mm)

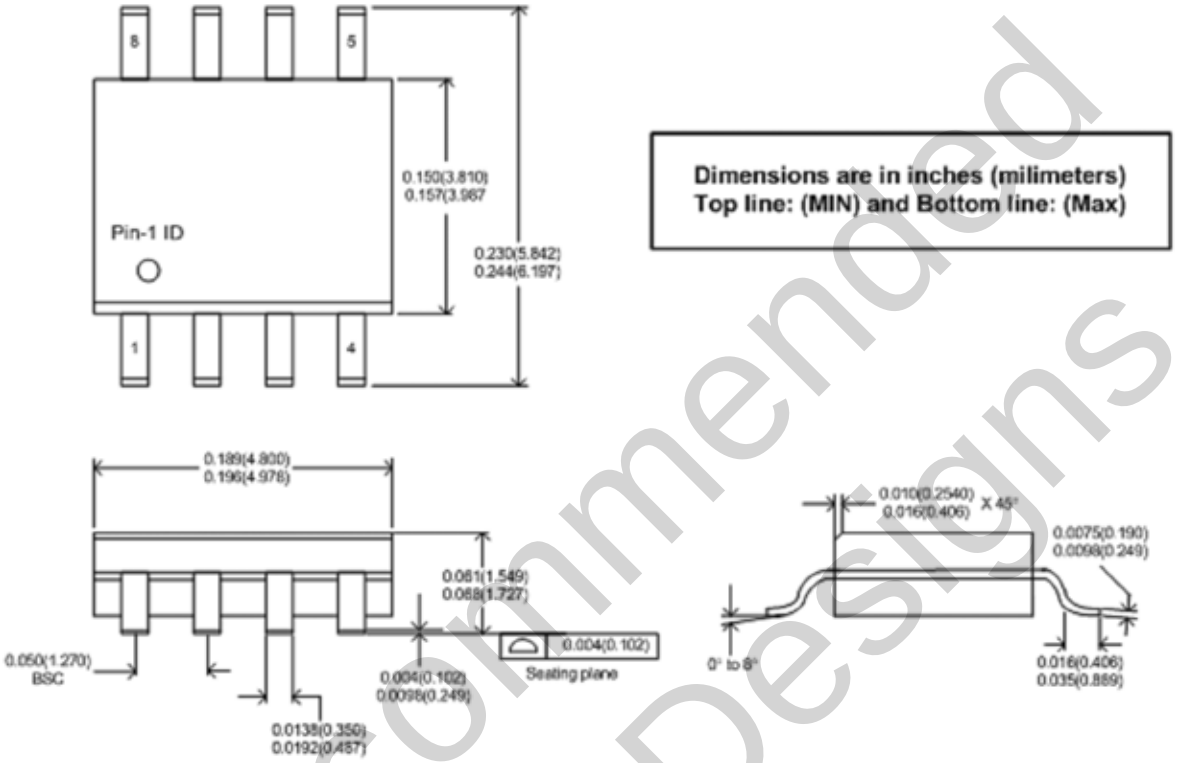

Figure 6. 8-Lead SOIC (150 mm)

11. Ordering Guide

Table 10. Ordering Guide

Ordering Number	Shipping Package	Package	Temperature
SL23EP05SC-1	Tube	8-pin SOIC	0 to 70°C
SL23EP05SC-1T	Tape and Reel	8-pin SOIC	0 to 70°C
SL23EP05SI-1	Tube	8-pin SOIC	–40 to 85°C
SL23EP05SI-1T	Tape & Reel	8-pin SOIC	–40 to 85°C
SL23EP05SC-1H	Tube	8-pin SOIC	0 to 70°C
SL23EP05SC-1HT	Tape & Reel	8-pin SOIC	0 to 70°C
SL23EP05SI-1H	Tube	8-pin SOIC	–40 to 85°C
SL23EP05SI-1HT	Tape & Reel	8-pin SOIC	–40 to 85°C
SL23EP05BSI-1H	Tube	8-pin SOIC	–40 to 85°C
SL23EP05BSI-1HT	Tape & Reel	8-pin SOIC	–40 to 85°C

Notes:
1. The SL23EP05 products are RoHS compliant.
2. Minimum Order Quantity (MOQ) is for production orders. Silicon Labs provides lesser quantities for pre-production samples.

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