



**THE DATASHEET OF  
AS7C31026B-12JCN**



**Revision History****AS7C31026B**

Revision	Details	Date
Rev 1.0	Initial Issue	March. 2004
Rev 1.1	10ns TSOP II not offered due to poor yields	April 2007
Rev 2.0	industrial temp TSOP II not offered due to poor yields - refer to 'C' die option for TSOP II. We can still offer in SOJ industrial temp.	August 2009

Please note modified from the original Alliance Semiconductor datasheet by Alliance Memory

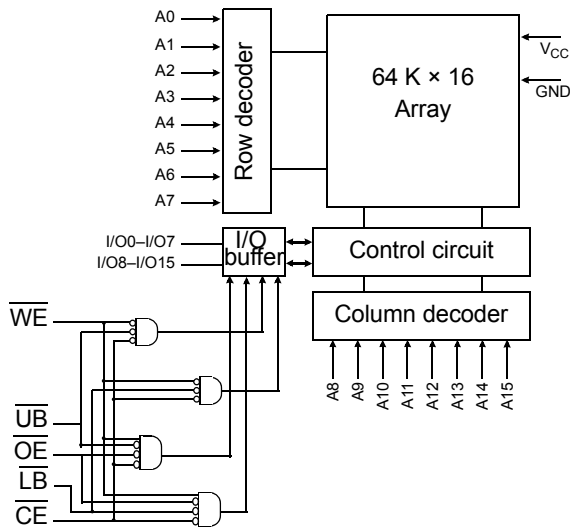


3.3 V 64K X 16 CMOS SRAM

Features

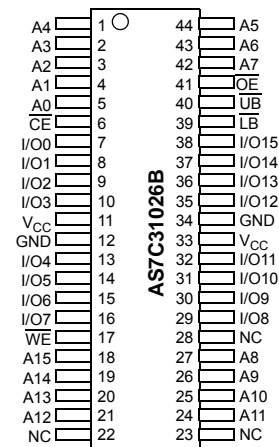
- Industrial and commercial versions
- Organization: 65,536 words × 16 bits
- Center power and ground pins for low noise
- High speed
  - 10/12/15/20 ns address access time
  - 5, 6, 7, 8 ns output enable access time
- Low power consumption: ACTIVE
  - 288 mW / max @ 10 ns
- Low power consumption: STANDBY
  - 18 mW / max CMOS I/O
- 6 T 0.18 u CMOS technology
- Easy memory expansion with  $\overline{CE}$ ,  $\overline{OE}$  inputs
- TTL-compatible, three-state I/O
- JEDEC standard packaging
  - 44-pin 400 mil SOJ
  - 44-pin TSOP 2-400
- ESD protection  $\geq 2000$  volts
- Latch-up current  $\geq 200$  mA

Logic block diagram



Pin arrangement

44-Pin SOJ (400 mil), TSOP 2



Selection guide

	-10	-12	-15	-20	Unit
Maximum address access time	10	12	15	20	ns
Maximum output enable access time	5	6	7	8	ns
Maximum operating current	80	75	70	65	mA
Maximum CMOS standby current	5	5	5	5	mA



## Functional description

The AS7C31026B is a high-performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) device organized as 65,536 words  $\times$  16 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times ( $t_{AA}$ ,  $t_{RC}$ ,  $t_{WC}$ ) of 10/12/15/20 ns with output enable access times ( $t_{OE}$ ) of 5, 6, 7, 8 ns are ideal for high-performance applications.

When  $\overline{CE}$  is high, the device enters standby mode. A write cycle is accomplished by asserting write enable ( $\overline{WE}$ ) and chip enable ( $\overline{CE}$ ). Data on the input pins I/O0 through I/O15 is written on the rising edge of  $\overline{WE}$  (write cycle 1) or  $\overline{CE}$  (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ( $\overline{OE}$ ) or write enable ( $\overline{WE}$ ).

A read cycle is accomplished by asserting output enable ( $\overline{OE}$ ) and chip enable ( $\overline{CE}$ ) with write enable ( $\overline{WE}$ ) high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive or write enable is active, output drivers stay in high-impedance mode.

The device provides multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read.  $\overline{LB}$  controls the lower bits, I/O0 through I/O7, and  $\overline{UB}$  controls the higher bits, I/O8 through I/O15.

All chip inputs and outputs are TTL-compatible, and operation is from a single 3.3 V supply. The device is packaged in common industry standard packages.

## Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on $V_{CC}$ relative to GND	$V_{t1}$	-0.50	+5.0	V
Voltage on any pin relative to GND	$V_{t2}$	-0.50	$V_{CC} + 0.50$	V
Power dissipation	$P_D$	-	1.0	W
Storage temperature (plastic)	$T_{stg}$	-65	+150	$^{\circ}C$
Ambient temperature with VCC applied	$T_{bias}$	-55	+125	$^{\circ}C$
DC current into outputs (low)	$I_{OUT}$	-	20	mA

Note: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0–I/O7	I/O8–I/O15	Mode
H	X	X	X	X	High Z	High Z	Standby ( $I_{SB}$ , $I_{SBI}$ )
L	H	L	L	H	$D_{OUT}$	High Z	Read I/O0–I/O7 ( $I_{CC}$ )
L	H	L	H	L	High Z	$D_{OUT}$	Read I/O8–I/O15 ( $I_{CC}$ )
L	H	L	L	L	$D_{OUT}$	$D_{OUT}$	Read I/O0–I/O15 ( $I_{CC}$ )
L	L	X	L	L	$D_{IN}$	$D_{IN}$	Write I/O0–I/O15 ( $I_{CC}$ )
L	L	X	L	H	$D_{IN}$	High Z	Write I/O0–I/O7 ( $I_{CC}$ )
L	L	X	H	L	High Z	$D_{IN}$	Write I/O8–I/O15 ( $I_{CC}$ )
L	H	H	X	X	High Z	High Z	Output disable ( $I_{CC}$ )
L	X	X	H	H	High Z	High Z	

**Key:** H = high, L = low, X = don't care.



### Recommended operating conditions

Parameter	Symbol	Min	Nominal	Max	Unit	
Supply voltage	$V_{CC}$	3.0	3.3	3.6	V	
Input voltage	$V_{IH}$	2.0	–	$V_{CC} + 0.5$	V	
	$V_{IL}$	-0.5	–	0.8	V	
Ambient operating temperature	commercial	$T_A$	0	–	70	$^{\circ}\text{C}$
	industrial	$T_A$	-40	–	85	$^{\circ}\text{C}$

$V_{IL} = -1.0\text{V}$  for pulse width less than 5ns

$V_{IH} = V_{CC} + 1.5\text{V}$  for pulse width less than 5ns

### DC operating characteristics (over the operating range)<sup>1</sup>

Parameter	Sym	Test conditions	-10		-12		-15		-20		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	$ I_{LI} $	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND to } V_{CC}$	–	1	–	1	–	1	–	1	$\mu\text{A}$
Output leakage current	$ I_{LO} $	$V_{CC} = \text{Max}$ $\overline{\text{CE}} = V_{IH}$ , $V_{OUT} = \text{GND to } V_{CC}$	–	1	–	1	–	1	–	1	$\mu\text{A}$
Operating power supply current	$I_{CC}$	$V_{CC} = \text{Max}$ , $\overline{\text{CE}} \leq V_{IL}$ , $I_{OUT} = 0\text{mA}$ $f = f_{\text{Max}}$	–	80	–	75	–	70	–	65	mA
Standby power supply current	$I_{SB}$	$V_{CC} = \text{Max}$ , $\overline{\text{CE}} \geq V_{IH}$ , $f = f_{\text{Max}}$	–	30	–	25	–	20	–	20	mA
	$I_{SB1}$	$V_{CC} = \text{Max}$ , $\overline{\text{CE}} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$ , $f = 0$	–	5	–	5	–	5	–	5	mA
Output voltage	$V_{OL}$	$I_{OL} = 8\text{ mA}$ , $V_{CC} = \text{Min}$	–	0.4	–	0.4	–	0.4	–	0.4	V
	$V_{OH}$	$I_{OH} = -4\text{ mA}$ , $V_{CC} = \text{Min}$	2.4	–	2.4	–	2.4	–	2.4	–	V

### Capacitance ( $f = 1\text{MHz}$ , $T_a = 25\text{ }^{\circ}\text{C}$ , $V_{CC} = \text{NOMINAL}$ )<sup>2</sup>

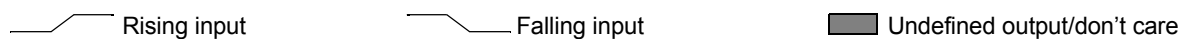
Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	$C_{IN}$	A, $\overline{\text{CE}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ , $\overline{\text{LB}}$ , $\overline{\text{UB}}$	$V_{IN} = 0\text{ V}$	5	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{IN} = V_{OUT} = 0\text{ V}$	7	pF



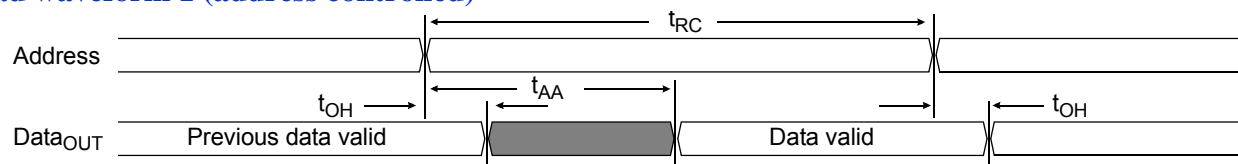
### Read cycle (over the operating range)<sup>3,9</sup>

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	$t_{RC}$	10	–	12	–	15	–	20	–	ns	
Address access time	$t_{AA}$	–	10	–	12	–	15	–	20	ns	3
Chip enable ( $\overline{CE}$ ) access time	$t_{ACE}$	–	10	–	12	–	15	–	20	ns	3
Output enable ( $\overline{OE}$ ) access time	$t_{OE}$	–	5	–	6	–	7	–	8	ns	
Output hold from address change	$t_{OH}$	3	–	3	–	3	–	3	–	ns	5
$\overline{CE}$ low to output in low Z	$t_{CLZ}$	3	–	3	–	3	–	3	–	ns	4, 5
$\overline{CE}$ high to output in high Z	$t_{CHZ}$	–	3	–	3	–	4	–	5	ns	4, 5
$\overline{OE}$ low to output in low Z	$t_{OLZ}$	0	–	0	–	0	–	0	–	ns	4, 5
Byte select access time	$t_{BA}$	–	5	–	6	–	7	–	8	ns	
Byte select Low to low Z	$t_{BLZ}$	0	–	0	–	0	–	0	–	ns	4, 5
Byte select High to high Z	$t_{BHZ}$	–	5	–	6	–	6	–	8	ns	4, 5
$\overline{OE}$ high to output in high Z	$t_{OHZ}$	–	5	–	6	–	7	–	8	ns	4, 5
Power up time	$t_{PU}$	0	–	0	–	0	–	0	–	ns	4, 5
Power down time	$t_{PD}$	–	10	–	12	–	15		20	ns	4, 5

### Key to switching waveforms

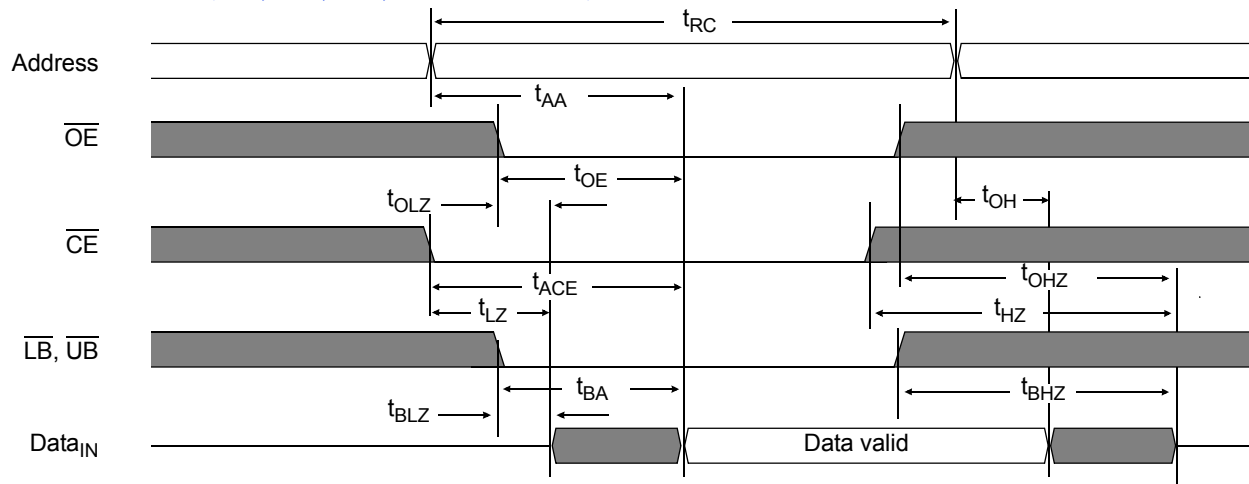


### Read waveform 1 (address controlled)<sup>3,6,7,9</sup>





### Read waveform 2 ( $\overline{OE}$ , $\overline{CE}$ , $\overline{UB}$ , $\overline{LB}$ controlled)<sup>3,6,8,9</sup>

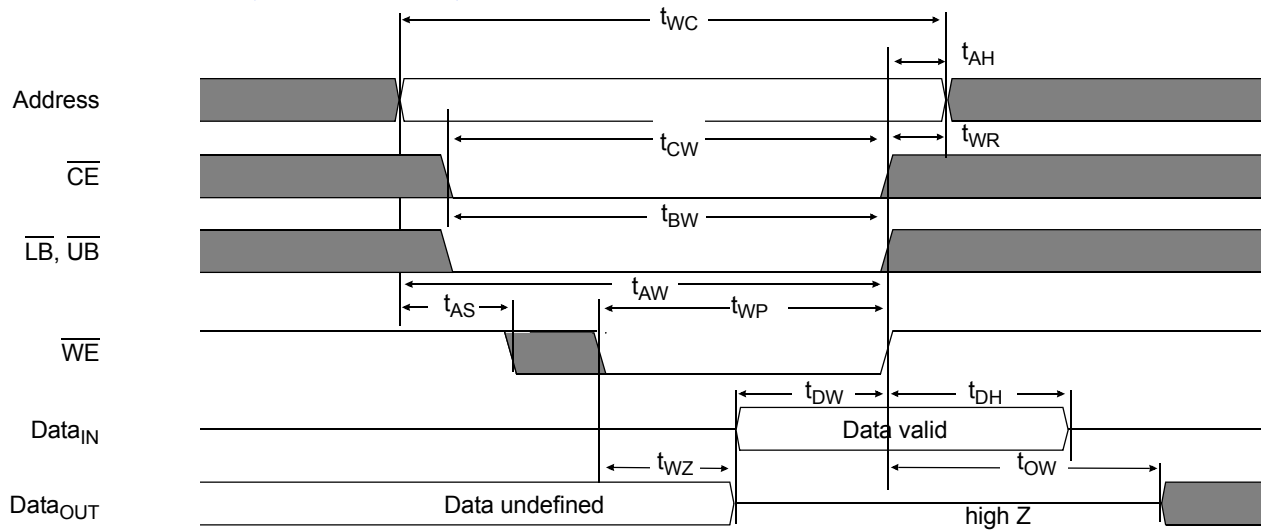


### Write cycle (over the operating range)<sup>11</sup>

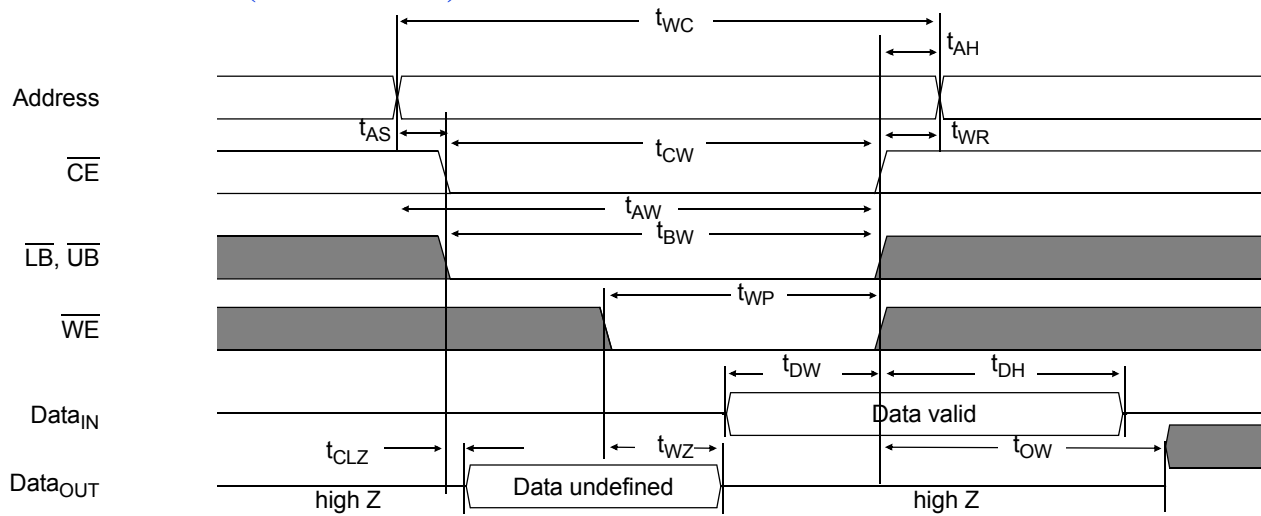
Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	$t_{WC}$	10	–	12	–	15	–	20	–	ns	
Chip enable ( $\overline{CE}$ ) to write end	$t_{CW}$	8	–	9	–	10	–	12	–	ns	
Address setup to write end	$t_{AW}$	8	–	9	–	10	–	12	–	ns	
Address setup time	$t_{AS}$	0	–	0	–	0	–	0	–	ns	
Write pulse width	$t_{WP}$	7	–	8	–	9	–	12	–	ns	
Write recovery time	$t_{WR}$	0	–	0	–	0	–	0	–	ns	
Address hold from end of write	$t_{AH}$	0	–	0	–	0	–	0	–	ns	
Data valid to write end	$t_{DW}$	5	–	6	–	8	–	10	–	ns	
Data hold time	$t_{DH}$	0	–	0	–	0	–	0	–	ns	5
Write enable to output in high Z	$t_{WZ}$	–	5	–	6	–	7	–	8	ns	4, 5
Output active from write end	$t_{OW}$	1	–	1	–	1	–	2	–	ns	4, 5
Byte select low to end of write	$t_{BW}$	7	–	8	–	9	–	9	–	ns	



### Write waveform 1 ( $\overline{\text{WE}}$ controlled)<sup>10,11</sup>



### Write waveform 2 ( $\overline{\text{CE}}$ controlled)<sup>10,11</sup>





## AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.0 V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5

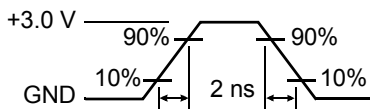


Figure A: Input pulse

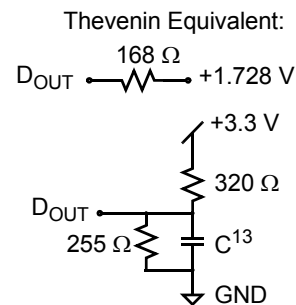


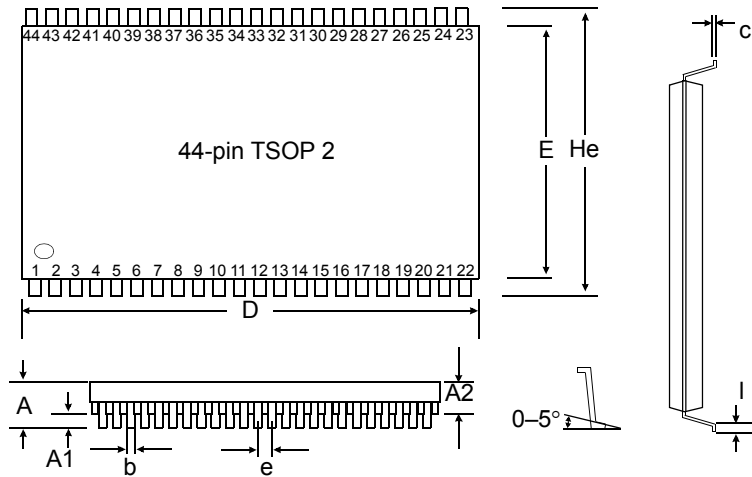
Figure B: 3.3 V Output load

## Notes

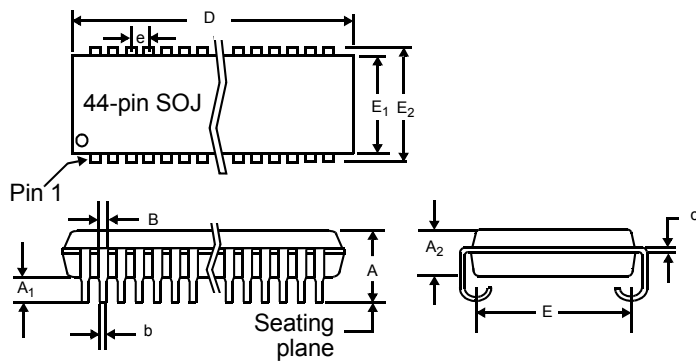
- 1 During  $V_{CC}$  power-up, a pull-up resistor to  $V_{CC}$  on  $\overline{CE}$  is required to meet  $I_{SB}$  specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see *AC Test Conditions*, Figures A and B.
- 4 These parameters are specified with  $C_L = 5$  pF, as in Figures B. Transition is measured  $\pm 500$  mV from steady-state voltage.
- 5 This parameter is guaranteed, but not tested.
- 6  $\overline{WE}$  is high for read cycle.
- 7  $\overline{CE}$  and  $\overline{OE}$  are low for read cycle.
- 8 Address is valid prior to or coincident with  $\overline{CE}$  transition low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 N/A
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 Not applicable.
- 13  $C = 30$  pF, except all high Z and low Z parameters where  $C = 5$  pF.



Package dimensions



	44-pin TSOP 2	
	Min (mm)	Max (mm)
A		1.2
A1	0.05	0.15
A2	0.95	1.05
b	0.30	0.45
c	0.120	0.21
D	18.31	18.52
E	10.06	10.26
He	11.68	11.94
e	0.80 (typical)	
l	0.40	0.60



	44-pin SOJ 400 mil	
	Min (in)	Max (in)
A	0.128	0.148
A1	0.025	–
A2	0.105	0.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370 NOM	
E1	0.395	0.405
E2	0.435	0.445
e	0.050 NOM	



### Ordering codes

Package\Access time	Volt/Temp	10 ns	12 ns	15 ns	20 ns
Plastic SOJ, 400 mil	3.3 V commercial	AS7C31026B-10JCN	AS7C31026B-12JCN	AS7C31026B-15JCN	AS7C31026B-20JCN
	3.3 V industrial	AS7C31026B-10JIN	AS7C31026B-12JIN	AS7C31026B-15JIN	AS7C31026B-20JIN
TSOP 2, 10.2 x 18.4 mm	3.3 V commercial	AS7C31026B-10TCN	AS7C31026B-12TCN	AS7C31026B-15TCN	AS7C31026B-20TCN

### Part numbering system

AS7C	X	1026B	-XX	X	X	X
SRAM prefix	Voltage: 3 = 3.3 V CMOS	Device number	Access time	Package: J = SOJ 400 mil T = TSOP 2, 10.2 x 18.4 mm	Temperature range: C = commercial: 0° C to 70° C I = industrial: -40° C to 85° C	N=Lead Free Part

Please note modified from the original Alliance Semiconductor datasheet by Alliance Memory





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