THE DATASHEET OF

DAC8564ICPWR

www.win-source.net 0086-755-83957316

12-BITS, 125/105/80/65 MSPS ADC WITH DDR LVDS/CMOS OUTPUTS

FEATURES

- **Maximum Sample Rate: 125 MSPS**
- **12-Bit Resolution with No Missing Codes**
- **3.5 dB Coarse Gain and up to 6 dB Programmable Fine Gain for SNR/SFDR Trade-Off**
- **Parallel CMOS and Double Data Rate (DDR) LVDS Output Options**
- **Supports Sine, LVCMOS, LVPECL, LVDS Clock Inputs and Clock Amplitude Down to 400 mV_{PP}**
- **Clock Duty Cycle Stabilizer**
- **Internal Reference with Support for External Reference**
- **No External Decoupling Required for References**
- **Programmable Output Clock Position and Drive Strength to Ease Data Capture**
- **3.3 V Analog and 1.8 V to 3.3 V Digital Supply**
- **32-QFN Package (5 mm × 5 mm)**
- **Pin Compatible 12-Bit Family (ADS612X)**

APPLICATIONS

- **Wireless Communications Infrastructure**
- **Software Defined Radio**
- **Power Amplifier Linearization**
- **802.16d/e**
- **Test and Measurement Instrumentation**
- **High Definition Video**
- **Medical Imaging**
- **Radar Systems**

DESCRIPTION

ADS6125/ADS6124/ADS6123/ADS6122 (ADS612X) is a family of 12-bit A/D converters with sampling frequencies up to 125 MSPS. It combines high performance and low power consumption in a compact 32 QFN package. Using an internal high bandwidth sample and hold and a low jitter clock buffer helps to achieve high SNR and high SFDR even at high input frequencies.

It features coarse and fine gain options that are used to improve SFDR performance at lower full-scale analog input ranges.

The digital data outputs are either parallel CMOS or DDR LVDS (Double Data Rate). Several features exist to ease data capture such as — controls for output clock position and output buffer drive strength, and LVDS current and internal termination programmability.

The output interface type, gain, and other functions are programmed using a 3-wire serial interface. Alternatively, some of these functions are configured using dedicated parallel pins so that the device comes up in the desired state after power-up.

ADS612X includes internal references, while eliminating the traditional reference pins and associated external decoupling. External reference mode is also supported.

The devices are specified over the industrial temperature range (–40°C to 85°C).

ADS612X Performance Summary

		ADS6125	ADS6124	ADS6123	ADS6122
SFDR, dBc	F_{in} = 10 MHz (0 dB gain)	90	91	93	95
	F_{in} = 170 MHz (3.5 dB gain)	78	82	83	84
SINAD, dBFS	F_{in} = 10 MHz (0 dB gain)	71.1	71.3	71.5	71.6
	F_{in} = 170 MHz (3.5 dB gain)	67.6	69.1	69.2	69.8
Power, mW		417	374	318	285

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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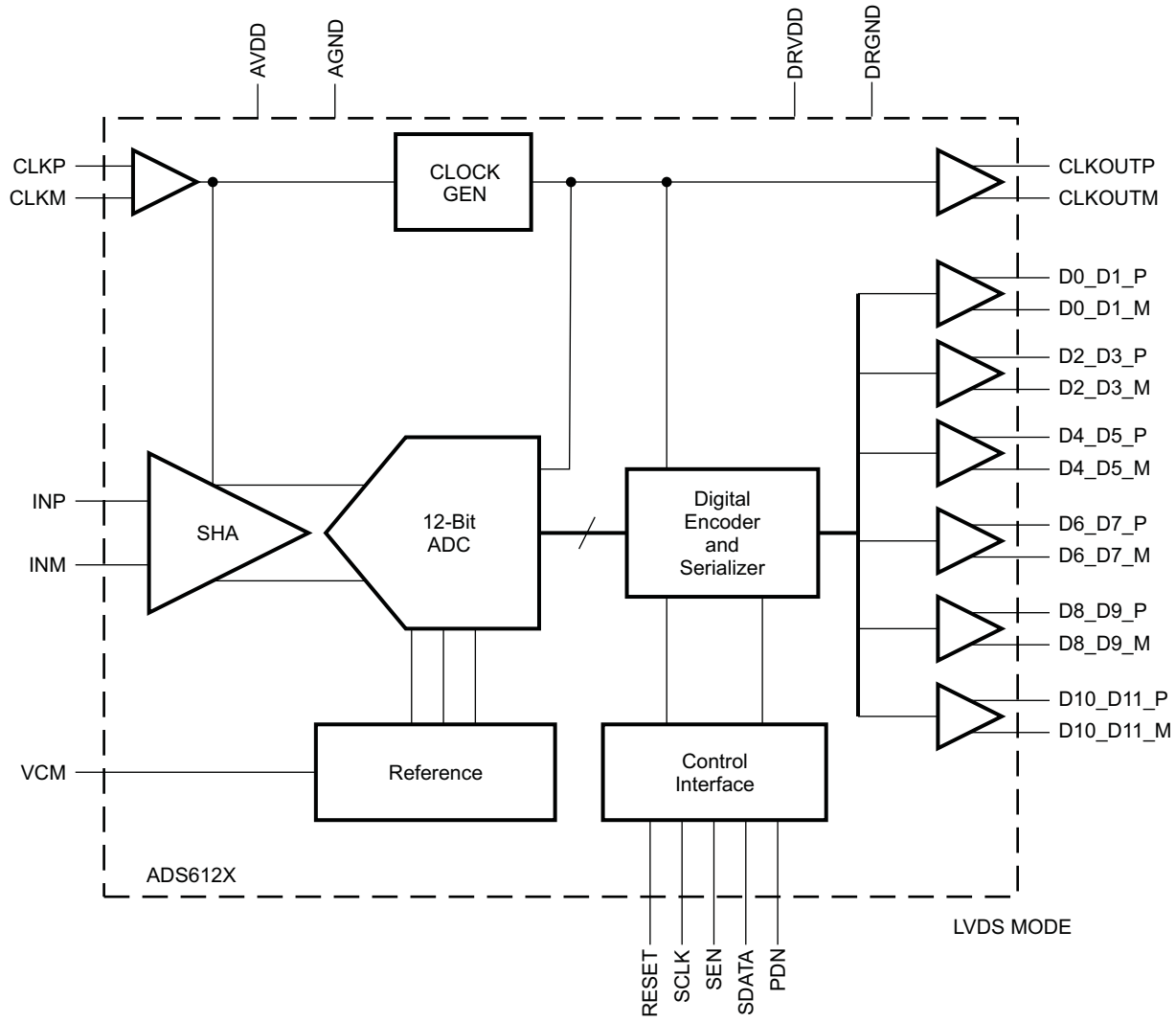
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



ADS61XX FAMILY

	125 MSPS	105 MSPS	80 MSPS	65 MSPS
ADS614X 14 Bits	ADS6145	ADS6144	ADS6143	ADS6142
ADS612X 12 Bits	ADS6125	ADS6124	ADS6123	ADS6122

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PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
ADS6125	QFN-32(2)	RHB	–40°C to 85°C	AZ6125	ADS6125IRHBT	Tape and Reel, small
					ADS6125IRHBR	Tape and Reel, large
ADS6124	QFN-32(2)	RHB	–40°C to 85°C	AZ6124	ADS6124IRHBT	Tape and Reel, small
					ADS6124IRHBR	Tape and Reel, large
ADS6123	QFN-32(2)	RHB	–40°C to 85°C	AZ6123	ADS6123IRHBT	Tape and Reel, small
					ADS6123IRHBR	Tape and Reel, large
ADS6122	QFN-32(2)	RHB	–40°C to 85°C	AZ6122	ADS6122IRHBT	Tape and Reel, small
					ADS6122IRHBR	Tape and Reel, large

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) For thermal pad size on the package, see the mechanical drawings at the end of this data sheet. θ_{JA} = 34 °C/W (0 LFM air flow), θ_{JC} = 30 °C/W when used with 2 oz. copper trace and pad soldered directly to a JEDEC standard four layer 3 in × 3 in (7.62 cm × 7.62 cm) PCB.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
V_I	Supply voltage range, AVDD	–0.3 to 3.9	V
	Supply voltage range, DRVDD	–0.3 to 3.9	V
	Voltage between AGND and DRGND	–0.3 to 0.3	V
	Voltage between AVDD to DRVDD	–0.3 to 3.3	V
	Voltage applied to VCM pin (in external reference mode)	–0.3 to 2	V
	Voltage applied to analog input pins, INP and INM	–0.3 to minimum (3.6, AVDD + 0.3)	V
	Voltage applied to analog input pins, CLKP and CLKM	–0.3 to (AVDD + 0.3)	V
T_A	Operating free-air temperature range	–40 to 85	°C
T_J	Operating junction temperature range	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		3	3.3	3.6	V
DRVDD	Output buffer supply voltage (1)	CMOS Interface	1.65	1.8 to 3.3	3.6	V
		LVDS Interface	3	3.3	3.6	V
ANALOG INPUTS						
	Differential input voltage range			2		V_{pp}
V_{IC}	Input common-mode voltage			1.5 ± 0.1		V
	Voltage applied on VCM in external reference mode		1.45	1.5	1.55	V
CLOCK INPUT						
F_S	Input clock sample rate	ADS6125	1		125	MSPS
		ADS6124	1		105	
		ADS6123	1		80	
		ADS6122	1		65	
	Input clock amplitude differential ($V_{CLKP} - V_{CLKM}$)	Sine wave, ac-Coupled	0.4	1.5		V_{pp}
		LVPECL, ac-Coupled		± 0.8		
		LVDS, ac-Coupled		± 0.35		
		LVCMOS, ac-Coupled		3.3		
	Input Clock duty cycle		35%	50%	65%	
DIGITAL OUTPUTS						
	Output buffer drive strength (2)	For C_{LOAD} ≤ 5 pF and DRVDD ≥ 2.2 V		DEFAULT strength		
		For C_{LOAD} > 5 pF and DRVDD ≥ 2.2 V		MAXIMUM strength		
		For DRVDD < 2.2 V		MAXIMUM strength		
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND	CMOS Interface, maximum buffer strength		10		pF
		LVDS Interface, without internal termination		5		
		LVDS Interface, with internal termination		10		
R_{LOAD}	Differential load resistance (external) between the LVDS output pairs			100		Ω
T_A	Operating free-air temperature		-40		85	°C

(1) For easy migration to next generation, higher sampling speed devices (> 125 MSPS), use 1.8V DRVDD supply.
(2) See *Output Buffer Strength Programmability* in application section

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ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, applies to CMOS and LVDS interfaces, unless otherwise noted.

PARAMETER		ADS6125 F_S = 125 MSPS			ADS6124 F_S = 105 MSPS			ADS6123 F_S = 80 MSPS			ADS6122 F_S = 65 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12			12			12			12		Bits
ANALOG INPUT														
	Differential input voltage range		2			2			2			2		V_{PP}
	Differential input resistance (at dc) see Figure 91		> 1			> 1			> 1			> 1		MΩ
	Differential input capacitance see Figure 92		7			7			7			7		pF
	Analog input bandwidth		450			450			450			450		MHz
	Analog input common mode current (per input pin of each ADC)		180			151			114			92		µA
REFERENCE VOLTAGES														
VREFB	Internal reference bottom voltage		1			1			1			1		V
VREFT	Internal reference top voltage		2			2			2			2		V
ΔV_{REF}	Internal reference error (VREFT–VREFB)	-20	± 5	20	-20	± 5	20	-20	± 5	20	-20	± 5	20	mV
V_{CM}	Common mode output voltage		1.5			1.5			1.5			1.5		V
DC ACCURACY														
	No missing codes		Specified			Specified			Specified			Specified		
E_O	Offset error	-10	± 2	10	-10	± 2	10	-10	± 2	10	-10	± 2	10	mV
	Offset error temperature coefficient		0.05			0.05			0.05			0.05		mV/°C
	There are two sources of gain error – internal reference inaccuracy and channel gain error													
E_{GREF}	Gain error due to internal reference inaccuracy alone, (ΔV_{REF} /2) %	-1	0.25	1	-1	0.25	1	-1	0.25	1	-1	0.25	1	% FS
E_{GCHAN}	Gain error of channel alone (1)	-1	±0.3	1	-1	±0.3	1	-1	±0.3	1	-1	±0.3	1	% FS
	Channel gain error temperature coefficient		0.005			0.005			0.005			0.005		Δ%/°C
DNL	Differential nonlinearity	-0.75	± 0.6	2	-0.75	± 0.6	2	-0.75	± 0.5	2	-0.75	± 0.5	2	LSB
INL	Integral nonlinearity	-2	± 1	2	-2	± 1	2	-2	± 1	2	-2	± 1	2	LSB
POWER SUPPLY														
I_{AVDD}	Analog supply current		123			110			94			84		mA
I_{DRVDD}	Digital supply current, **CMOS** interface DRVDD = 1.8 V No load capacitance, F_{IN}= 2 MHZ (2)		6.1			5.4			4.5			4.0		mA
I_{DRVDD}	Digital supply current, **LVDS** interface DRVDD = 3.3 V With 100 Ω external termination		42			42			42			42		mA
	Total power, **CMOS**		417	625		374	525		318	440		285	400	mW
	Global power down		30	60		30	60		30	60		30	60	mW

(1) This is specified by design and characterization; it is not tested in production.
(2) In CMOS mode, the DRVDD current scales with the sampling frequency and the load capacitance on output pins (see **Figure 84**).

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ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, applies to CMOS and LVDS interfaces, unless otherwise noted.

PARAMETER	TEST CONDITIONS		ADS6125 F_S = 125 MSPS			ADS6124 F_S = 105 MSPS			ADS6123 F_S = 80 MSPS			ADS6122 F_S = 65 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS															
SNR Signal to noise ratio, **CMOS**	Fin = 10 MHz			71.3			71.4			71.6			71.7		dBFS
	Fin = 50 MHz		68.5	71.1			71.1		69	71.4			71.5		
	Fin = 70 MHz			70.9		68.5	71			71.3		69	71.5		
	Fin = 170 MHz	0 dB Gain		69.5			70			70.3			70.6		
		3.5 dB Coarse gain		68.7			69.4			69.7			69.9		
	Fin = 230 MHz	0 dB Gain		68.6			69.2			69.6			69.9		
		3.5 dB Coarse gain		67.9			68.6			69.1			69.4		
SNR Signal to noise ratio, **LVDS**	Fin = 10 MHz			71.5			71.5			71.8			71.8		dBFS
	Fin = 50 MHz		68.5	71.4			71.3		69	71.5			71.6		
	Fin = 70 MHz			71.3		68.5	71.3			71.5		69	71.6		
	Fin = 170 MHz	0 dB Gain		70.3			70.3			70.6			70.7		
		3.5 dB Coarse gain		69.8			69.8			70.1			70.1		
	Fin = 230 MHz	0 dB Gain		69.6			69.6			70			70.1		
		3.5 dB Coarse gain		69			69			69.5			69.6		
SINAD Signal to noise and distortion ratio **CMOS**	Fin = 10 MHz			71.1			71.3			71.5			71.6		dBFS
	Fin = 50 MHz		68	70.3			70.7		68.5	71.3			71.4		
	Fin = 70 MHz			70.4		68	70.9			70.9		68.5	71.4		
	Fin = 170 MHz	0 dB Gain		67.7			69.5			69.6			70.2		
		3.5 dB Coarse gain		67.6			69.1			69.2			69.8		
	Fin = 230 MHz	0 dB Gain		66.6			68			68.9			69.1		
		3.5 dB Coarse gain		66.3			68			68.6			69		
SINAD Signal to noise and distortion ratio **LVDS**	Fin = 10 MHz			71.5			71.5			71.7			71.7		dBFS
	Fin = 50 MHz			70.6			70.7			71.4			71.5		
	Fin = 70 MHz			71			71			71.1			71.5		
	Fin = 170 MHz	0 dB Gain		69.1			69.7			70.1			70.3		
		3.5 dB Coarse gain		69.3			69.5			69.9			70		
	Fin = 230 MHz	0 dB Gain		68.2			68.1			69.4			69.1		
		3.5 dB Coarse gain		68.3			68.3			69.2			69.1		
ENOB Effective number of bits	Fin = 50 MHz		11	11.4					11	11.55					Bits
	Fin = 70 MHz					11	11.5					11	11.56		
SFDR Spurious free dynamic range	Fin = 10 MHz			90			91			93			95		dBc
	Fin = 50 MHz		76	80			83		79	89			89		
	Fin = 70 MHz			84		76	84			84		79	86		
	Fin = 170 MHz	0 dB Gain		76			80			81			82		
		3.5 dB Coarse gain		78			82			83			84		
	Fin = 230 MHz	0 dB Gain		75			77			79			79		
		3.5 dB Coarse gain		76			79			81			82		

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ELECTRICAL CHARACTERISTICS (continued)

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, applies to CMOS and LVDS interfaces, unless otherwise noted.

PARAMETER	TEST CONDITIONS		ADS6125 F_S = 125 MSPS			ADS6124 F_S = 105 MSPS			ADS6123 F_S = 80 MSPS			ADS6122 F_S = 65 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
THD Total harmonic distortion	Fin = 10 MHz			88.5			90			91.5			93		dBc
	Fin = 50 MHz		73	79.5			82.5		76	88			88		
	Fin = 70 MHz			82		73	83			83		76	85		
	Fin = 170 MHz	0 dB Gain		73.5			79			78			80		
		3.5 dB Coarse gain		75			81			79			82		
	Fin = 230 MHz	0 dB Gain		71.5			75.5			76			76		
		3.5 dB Coarse gain		72.5			77.5			78			78.5		
HD2 Second harmonic distortion	Fin = 10 MHz			96			96			97			98		dBc
	Fin = 50 MHz		76	95			96		79	96			96		
	Fin = 70 MHz			91		76	92			93		79	93		
	Fin = 170 MHz	0 dB Gain		81			83			83			86		
		3.5 dB Coarse gain		82			84			84			87		
	Fin = 230 MHz	0 dB Gain		75			79			80			79		
		3.5 dB Coarse gain		76			81			81			81		
HD3 Third harmonic distortion	Fin = 10 MHz			90			91			93			95		dBc
	Fin = 50 MHz		76	80			83		79	89			89		
	Fin = 70 MHz			84		76	84			84		79	86		
	Fin = 170 MHz	0 dB Gain		76			80			81			82		
		3.5 dB Coarse gain		78			82			83			84		
	Fin = 230 MHz	0 dB Gain		75			77			79			79		
		3.5 dB Coarse gain		76			79			81			82		
Worst spur (Other than HD2, HD3)	Fin = 10 MHz			93			94			96			97		dBc
	Fin = 50 MHz			92			90			93			96		
	Fin = 70 MHz			91			90			92			95		
	Fin = 170 MHz			90			89			89			91		
	Fin = 230 MHz			90			88			89			90		
IMD 2-Tone intermodulation distortion	F1 = 185 MHz, F2 = 190 MHz Each tone at -7 dBFS			83			82			84			88		dBFS
Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine wave input			1			1			1			1		clock cycles
PSRR AC Power supply rejection ratio	For 100 mVpp signal on AVDD supply			35			35			35			35		dBc

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DIGITAL CHARACTERISTICS(1)

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1 AVDD = 3.3 V

PARAMETER	TEST CONDITIONS	ADS6125/ADS6124 ADS6123/ADS6122			
		MIN	TYP	MAX	UNIT
DIGITAL INPUTS PDN, SCLK, SEN & SDATA (2)					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current			33		µA
Low-level input current			–33		µA
Input capacitance			4		pF
DIGITAL OUTPUTS CMOS INTERFACE, DRVDD = 1.8 to 3.3 V					
High-level output voltage			DRVDD		V
Low-level output voltage			0		V
Output capacitance	Output capacitance inside the device, from each output to ground		2		pF
DIGITAL OUTPUTS LVDS INTERFACE, DRVDD = 3.3 V, I_O = 3.5 mA, R_L = 100 Ω (3)					
High-level output voltage			1375		mV
Low-level output voltage			1025		mV
Output differential voltage, $\|V_{OD}\|$		225	350		mV
V_{OS} Output offset voltage, single-ended	Common-mode voltage of OUTP, OUTM		1200		mV
Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) All LVDS and CMOS specifications are characterized, but not tested at production.
(2) SCLK & SEN function as digital input pins when they are used for serial interface programming. When used as parallel control pins, analog voltage needs to be applied as per Table 1 & Table 2.
(3) I_O Refers to the LVDS buffer current setting, R_L is the differential load resistance between the LVDS output pair.

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TIMING CHARACTERISTICS – LVDS AND CMOS MODES(1)

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} clock amplitude, C_L = 5 pF(2), I_O = 3.5 mA, R_L = 100 Ω (3), no internal termination, unless otherwise noted.

For timings at lower sampling frequencies, see section Output Timings in the APPLICATION INFORMATION of this data sheet.

PARAMETER		TEST CONDITIONS		ADS6125 F_S = 125 MSPS			ADS6124 F_S = 105 MSPS			ADS6123 F_S = 80 MSPS			ADS6122 F_S = 65 MSPS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_a	Aperture delay			0.7	1.5	2.5	0.7	1.5	2.5	0.7	1.5	2.5	0.7	1.5	2.5	ns
t_j	Aperture jitter				150			150			150			150		fs rms
	Wake-up time (to valid data)	From global power down			15	50		15	50		15	50		15	50	µs
		From standby			15	50		15	50		15	50		15	50	µs
		From output buffer disable	CMOS		100	200		100	200		100	200		100	200	ns
			LVDS		200	500		200	500		200	500		200	500	ns
	Latency				9			9			9			9		clock cycles
DDR LVDS MODE(4), DRVDD = 3.3 V																
t_{su}	Data setup time(5)	Data valid (6) to zero-cross of CLKOUTP		1.7	2.3		2.5	3.1		3.9	4.5		5.4	6.0		ns
t_h	Data hold time(5)	Zero-cross of CLKOUTP to data becoming invalid(6)		0.7	1.7		0.7	1.7		0.7	1.7		0.7	1.7		ns
t_{PDI}	Clock propagation delay	Input clock rising edge zero-cross to output clock rising edge zero-cross		4.3	5.8	7.3	4.3	5.8	7.3	4.3	5.8	7.3	4.3	5.8	7.3	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP-CLKOUTM) 10 ≤ Fs ≤ 125 MSPS		40%	47%	55%	40%	47%	55%	40%	47%	55%	40%	47%	55%	
t_r t_f	Data rise time, Data fall time	Rise time measured from –50 mV to 50 mV Fall time measured from 50 mV to –50 mV 1 ≤ Fs ≤ 125 MSPS		70	100	170	70	100	170	70	100	170	70	100	170	ps
$t_{CLKRISE}$ $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –50 mV to 50 mV Fall time measured from 50 mV to –50 mV 1 ≤ Fs ≤ 125 MSPS		70	100	170	70	100	170	70	100	170	70	100	170	ps
PARALLEL CMOS MODE, DRVDD = 2.5 V to 3.3 V, default output buffer drive strength (7)																
t_{su}	Data setup time(5)	Data valid(8) to 50% of CLKOUT rising edge		2.9	4.4		3.6	5.1		5.1	6.6		6.5	8.0		ns
t_h	Data hold time(5)	50% of CLKOUT Rising edge to data becoming invalid(8)		1.3	2.7		2.1	3.5		3.6	5.0		5.1	6.5		ns
t_{PDI}	Clock propagation delay	Input clock rising edge zero-cross to 50% of CLKOUT rising edge		5	6.5	7.9	5	6.5	7.9	5	6.5	7.9	5	6.5	7.9	ns

(1) Timing parameters are specified by design and characterization and not tested in production.
(2) C_L is the Effective external single-ended load capacitance between each output pin and ground.
(3) I_O Refers to the LVDS buffer current setting; R_L is the differential load resistance between the LVDS output pair.
(4) Measurements are done with a transmission line of 100 Ω characteristic impedance between the device and the load.
(5) Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) Data valid refers to logic high of +100 mV and logic low of –100 mV.
(7) For DRVDD < 2.2V, it is recommended to use external clock for data capture and NOT the device output clock signal (CLKOUT). See *Parallel CMOS interface* in application section.
(8) Data valid refers to logic high of 2V (1.7V) and logic low of 0.8 V (0.7V) for DRVDD = 3.3V (2.5V).

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TIMING CHARACTERISTICS – LVDS AND CMOS MODES (continued)

For timings at lower sampling frequencies, see section Output Timings in the APPLICATION INFORMATION of this data sheet.

PARAMETER		TEST CONDITIONS	ADS6125 F_S = 125 MSPS			ADS6124 F_S = 105 MSPS			ADS6123 F_S = 80 MSPS			ADS6122 F_S = 65 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Output clock duty cycle	Duty cycle of output clock (CLKOUT) 10 ≤ Fs ≤ 125 MSPS	45%	50%	55%	45%	50%	55%	45%	50%	55%	45%	50%	55%	
t_r t_f	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD 1 ≤ Fs ≤ 125 MSPS	0.8	1.5	2.4	0.8	1.5	2.4	0.8	1.5	2.4	0.8	1.5	2.4	ns
$t_{CLKRISE}$ $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD 1 ≤ Fs ≤ 125 MSPS	0.8	1.5	2.4	0.8	1.5	2.4	0.8	1.5	2.4	0.8	1.5	2.4	ns

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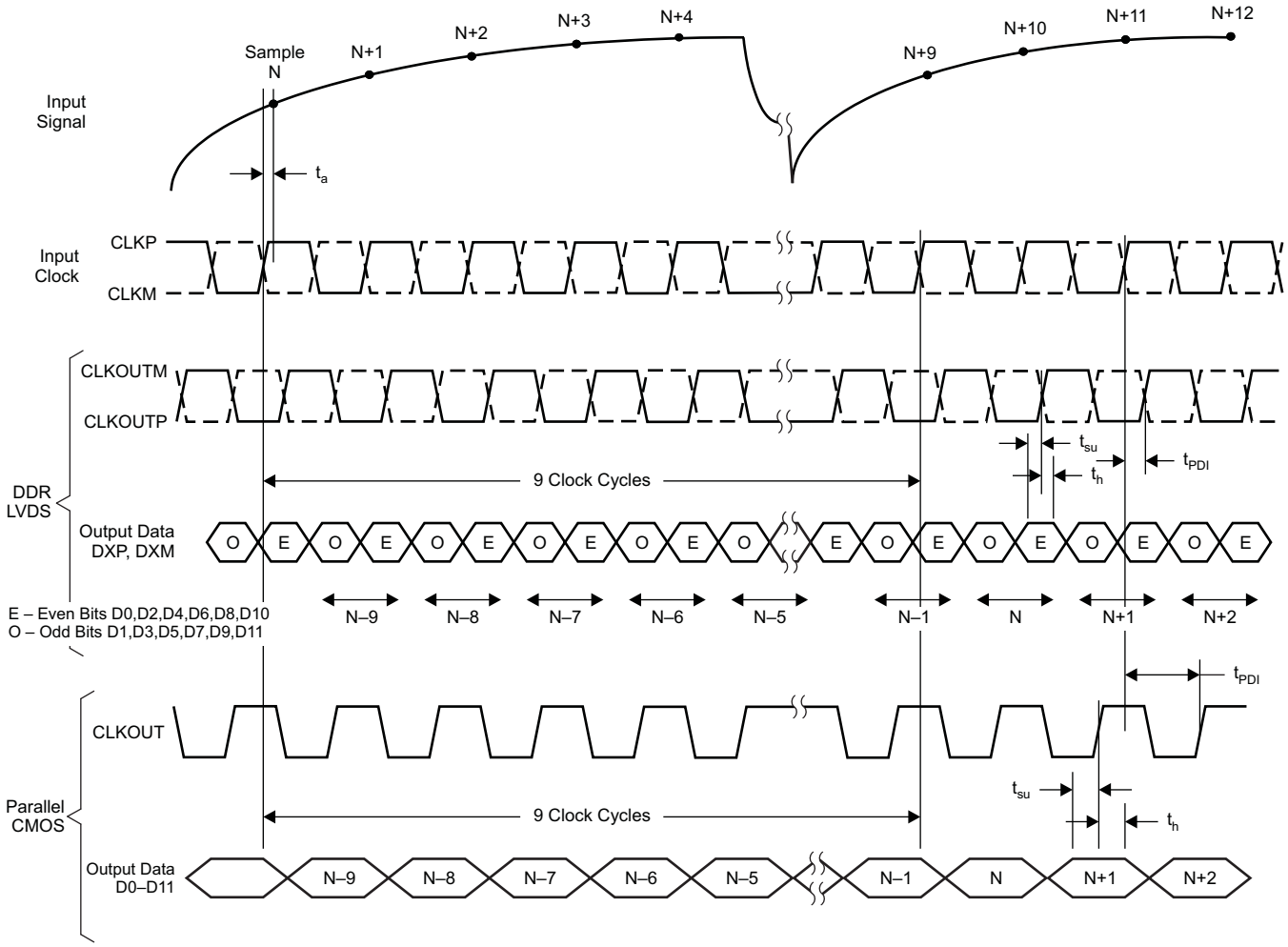
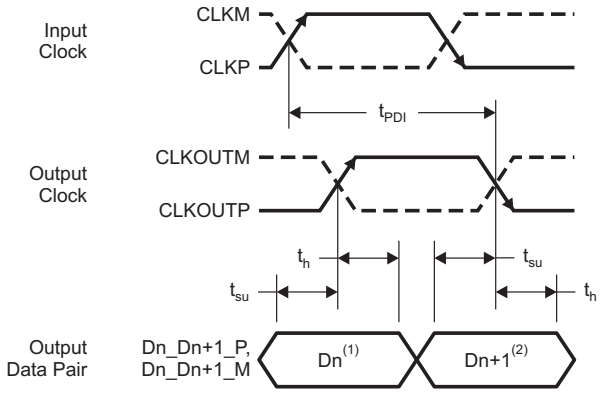
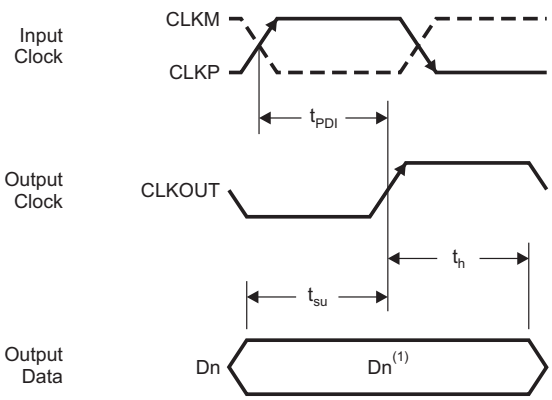


Figure 1. Latency



(1)Dn – Bits D0, D2, D4, D6, D8, D10
(2)Dn+1 – Bits D1, D3, D5, D7, D9, D11

Figure 2. LVDS Mode Timing



(1)Dn – Bits D0–D11

Figure 3. CMOS Mode Timing

DEVICE PROGRAMMING MODES

ADS612X has several features that can be easily configured using either parallel interface control or serial interface programming.

USING SERIAL INTERFACE PROGRAMMING ONLY

To program using the serial interface, the internal registers must first be reset to their default values, and the RESET pin must be kept **low**. In this mode, SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of ADC. The registers are reset either by applying a pulse on the RESET pin, or by a **high** setting on the <RST> bit (D4 in register 0x00). The Serial Interface section describes register programming and register reset in more detail.

USING PARALLEL INTERFACE CONTROL ONLY

To control the device using parallel interface, keep RESET tied to **high** (AVDD). Now, SEN, SCLK, SDATA and PDN function as parallel interface control pins. These pins can be used to directly control certain modes of the ADC by connecting them to the correct voltage levels (as described in Table 1 to Table 3). There is no need to apply a reset pulse.

Frequently used functions are controlled in this mode — standby, selection between LVDS/CMOS output format, internal/external reference and 2s complement/straight binary output format. Table 1,Table 2, and Table 3 describe the modes controlled by the parallel pins.

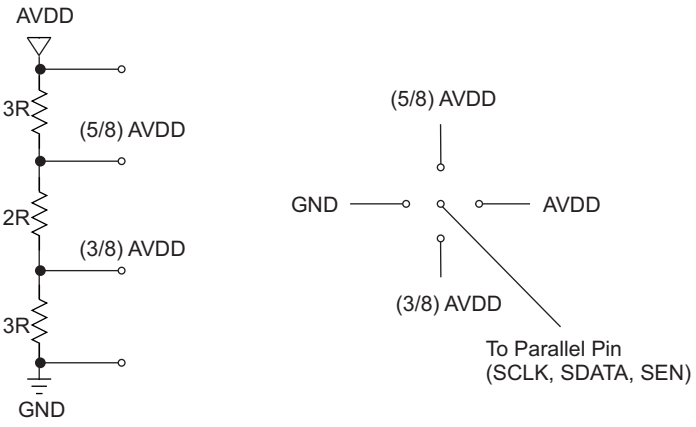


Figure 4. Simple Scheme to Configure Parallel Pins

DESCRIPTION OF PARALLEL PINS

Table 1. SCLK Control Pin

SCLK	DESCRIPTION
0	Internal reference and 0 dB gain (Full-scale = 2 V_{PP})
(3/8) AVDD	External reference and 0 dB gain (Full-scale = 2 V_{PP})
(5/8) AVDD	External reference and 3.5 dB coarse gain (Full-scale = 1.34 V_{PP})
AVDD	Internal reference and 3.5 dB coarse gain (Full-scale = 1.34 V_{PP})

Table 2. SEN Control Pin

SEN	DESCRIPTION
0	2s Complement format and DDR LVDS interface
(3/8) AVDD	Straight binary format and DDR LVDS interface
(5/8) AVDD	Straight binary and parallel CMOS interface
AVDD	2s Complement format and parallel CMOS interface

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Table 3. SDATA, PDN Control Pins

SDATA	PDN	DESCRIPTION
Low	Low	Normal operation
Low	High (AVDD)	Standby - only the ADC is powered down
High (AVDD)	Low	Output buffers are powered down, fast wake-up time
High (AVDD)	High (AVDD)	Global power down. ADC, internal reference and output buffers are powered down, slow wake-up time

SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed through the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock), SDATA (Serial Interface Data) and RESET. After device power-up, the internal registers must be reset to their default values by applying a high-going pulse on RESET (of width greater than 10 ns).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. If the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data is loaded in multiples of 16-bit words within a single active SEN pulse.

The first 5 bits form the register address and the remaining 11 bits form the register data.

The interface can work with SCLK frequency from 20 MHz down to very low speeds (few Hertz) and also with non-50% SCLK duty cycle.

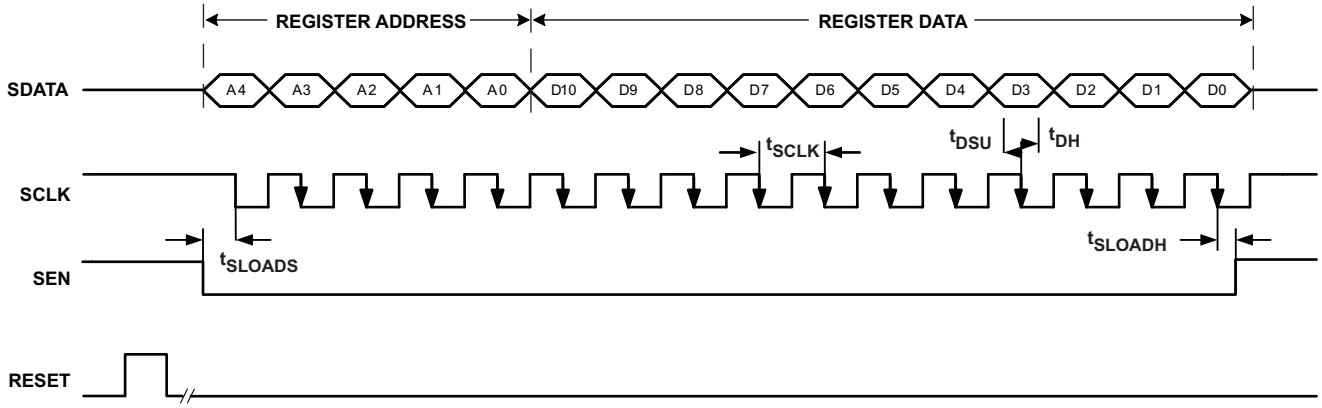

Figure 5. Serial Interface Timing Diagram

REGISTER INITIALIZATION

After power-up, the internal registers *must* be reset to their default values. This is done in one of two ways:

1. Either through hardware reset by applying a high-going pulse on RESET pin (of width greater than 10 ns) as shown in Figure 5.

   OR

2. By applying software reset. Using the serial interface, set the <RST> bit (D4 in register 0x00) to **high**. This initializes the internal registers to their default values and then self-resets the <RST> bit to **low**. In this case the RESET pin is kept **low**.

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SERIAL INTERFACE TIMING

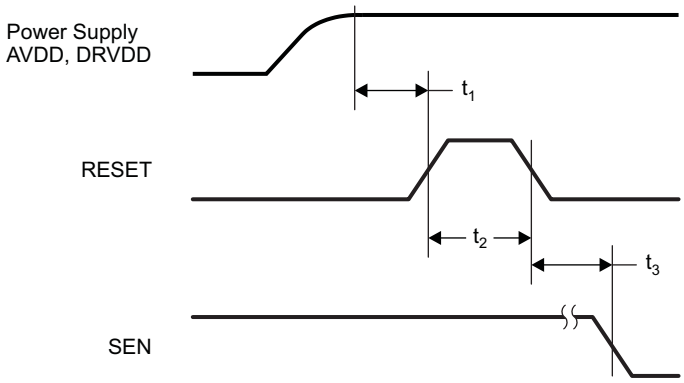
Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK Frequency = $1/t_{SCLK}$	> DC		20	MHz
t_{SLOADS}	SEN to SCLK Setup time	25			ns
t_{SLOADH}	SCLK to SEN Hold time	25			ns
t_{DSU}	SDATA Setup time	25			ns
t_{DH}	SDATA Hold time	25			ns

RESET TIMING

Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active	5			ms
t_2	Reset pulse width	Pulse width of active RESET signal	10			ns
t_3	Register write delay	Delay from RESET disable to SEN active	25			ns
t_{PO}	Power-up time	Delay from power-up of AVDD and DRVDD to output stable		6.5		ms



NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET has to be tied permanently HIGH.

Figure 6. Reset Timing Diagram

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SERIAL REGISTER MAP

Table 4 provides a summary of all the modes that can be programmed through the serial interface.

Table 4. Summary of Functions Supported by Serial Interface(1)(2)

REGISTER ADDRESS IN HEX	REGISTER FUNCTIONS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00	**<PDN OBUF>** Output buffers powered down	**<COARSE GAIN>** Coarse gain	**<LVDS CMOS>** LVDS or CMOS output interface	0	0	**<REF>** Internal or external Reference	**<RST>** Software Reset	0	**<PDN CLKOUT>** Output clock buffer powered down	0	**<STBY>** ADC Power down
04	**<DATAOUT POSN>** Output data position control	**<CLKOUT EDGE>** Output Clock edge control	**<CLKOUT POSN>** Output Clock position control	0	0	0	0	0	0	0	0
09	Bit-wise or Byte-wise control	0	0	0	0	0	0	0	0	0	0
0A	**<DATA FORMAT>** 2s complement or straight binary	0	0	**<TEST PATTERNS>**			0	0	0	0	0
0B	**<CUSTOM LOW>** Custom Pattern lower 7bits							0	0	0	0
0C	**<FINE GAIN>** Fine Gain 0 to 6dB			0	0	0	**<CUSTOM HIGH>** Custom Pattern upper 5 bits				
0E	0	LVDS Termination LVDS Internal Termination control for output data and clock						**<LVDS CURRENT>** LVDS Current control		**<CURRENT DOUBLE>** LVDS current double	
0F	0	0	0	**<DRIVE STRENGTH>** CMOS output buffer drive strength control				0	0	0	0

(1) The unused bits in each register (shown by blank cells in above table) must be programmed as '0'.
(2) Multiple functions in a register can be programmed in a single write operation.

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DESCRIPTION OF SERIAL REGISTERS

Each register function is explained in detail below.

Table 5.

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00	<PDN OBUF> Output buffers powered down	<COARSE GAIN> Coarse gain	<LVDS CMOS> LVDS or CMOS output interface	0	0	<REF> Internal or external reference	<RST> Software Reset	0	<PDN CLKOUT> Output clock buffer powered down	0	<STBY> ADC Power down

D0	<STBY> Power down modes
0	Normal operation
1	Device enters standby mode where only ADC is powered down.

D2	<PDN CLKOUT> Power down modes
0	Output clock is active (on CLKOUT) pin
1	Output clock buffer is powered down and becomes tri-stated. Data outputs are unaffected.

D4	<RST>
1	Software reset applied - resets all internal registers and the bit self-clears to 0.

D5	<REF> Reference selection
0	Internal reference enabled
1	External reference enabled

D8	<LVDS CMOS> Output Interface selection
0	Parallel CMOS interface
1	DDR LVDS interface

D9	<COARSE GAIN> Gain programming
0	0 dB Coarse gain
1	3.5 dB Coarse gain

D10	<PDN OBUF> Power down modes
0	Output data and clock buffers enabled
1	Output data and clock buffers disabled

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Table 6.

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
04	<DATAOUT POSN> Output data position control	<CLKOUT EDGE> Output Clock edge control	<CLKOUT POSN> Output Clock position control	0	0	0	0	0	0	0	0

D8	<CLKOUT POSN> Output clock position control
0	Default output clock position after reset. The setup/hold timings for this clock position are specified in the timing specifications table.
1	Output clock shifted (delayed) by 400 ps

D9	<CLKOUT EDGE>
0	Use rising edge to capture data
1	Use falling edge to capture data

D10	<DATAOUT_POSN>
0	Default position (after reset)
1	Data transition delayed by half clock cycle with respect to default position

Table 7.

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
09	Bit-wise or Byte-wise control	0	0	0	0	0	0	0	0	0	0

D10	Bit-wise or byte-wise selection (DDR LVDS mode only)
0	Bit-wise sequence - Even data bits (D0, D2, D4..D12) are output at rising edge of CLKOUTP and odd data bits (D1, D3, D5..D13) at falling edge of CLKOUTP
1	Byte-wise sequence - Lower 7 data bits (D0-D7) are output at rising edge of CLKOUTP and upper 7 data bits (D8-D13) at falling edge of CLKOUTP

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Table 8.

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0A	<DF> 2s complement or straight binary	0	0	<TEST PATTERNS>			0	0	0	0	0

D7-D5	Test Patterns
000	Normal operation - <D13:D0> = ADC output
001	All zeros - <D13:D0> = 0x0000
010	All ones - <D13:D0> = 0x3FFF
011	Toggle pattern - <D13:D0> toggles between 0x2AAA and 0x1555
100	Digital ramp - <D13:D0> increments from 0x0000 to 0x3FFF by one code every cycle
101	Custom pattern - <D13:D0> = contents of CUSTOM PATTERN registers
110	Unused
111	Unused

D10	<DATA FORMAT>
0	2s Complement
1	Straight binary

Table 9.

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0B	<CUSTOM LOW> Lower 7bits of custom pattern							0	0	0	0

Table 10.

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0C	<FINE GAIN> Fine Gain 0 to 6dB			0	0	0	<CUSTOM HIGH> Upper 5 bits of custom pattern				

Reg 0B D10-D4	**<CUSTOM LOW>** - Specifies lower 7 bits of custom pattern
Reg 0C D4-D0	**<CUSTOM HIGH>** - Specifies upper 5 bits of custom pattern

D10-D8	<FINE GAIN> Gain programming
000	0 dB Gain
001	1 dB Gain
010	2 dB Gain
011	3 dB Gain
100	4 dB Gain
101	5 dB Gain
110	6 dB Gain
111	Unused

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Table 11.

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0E	0	<LVDS TERMINATION> LVDS Internal Termination control for output data and clock						<LVDS CURRENT> LVDS Current control		<CURRENT DOUBLE> LVDS current double	

D1-D0	**<CURRENT DOUBLE>** LVDS current programming
D0	**LVDS Data buffer current control**
0	Default current, set by <LVDS_CURR>
1	2x LVDS Current set by <LVDS_CURR>
D1	**LVDS Clock buffer current control**
0	Default current, set by <LVDS_CURR>
1	2x LVDS Current set by <LVDS_CURR>
D3-D2	**<LVDS CURRENT>** LVDS current programming
00	3.5 mA
01	2.5 mA
10	4.5 mA
11	1.75 mA
D9-D4	LVDS internal termination
D9-D7	**<DATA TERM>** Internal termination for LVDS output data bits
000	No internal termination
001	300 Ω
010	185 Ω
011	115 Ω
100	150 Ω
101	100 Ω
110	80 Ω
111	65 Ω
D6-D4	**<CLKOUT TERM>** Internal termination for LVDS output clock
000	No internal termination
001	300 Ω
010	185 Ω
011	115 Ω
100	150 Ω
101	100 Ω
110	80 Ω
111	65 Ω

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Table 12.

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0F	0	0	0	<DRIVE STRENGTH> CMOS output buffer drive strength control				0	0	0	0

D7-D4	<DRIVE STRENGTH> Output buffer drive strength controls
0101	WEAKER than default drive
0000	DEFAULT drive strength
1111	STRONGER than default drive strength (recommended for load capacitances > 5 pF)
1010	MAXIMUM drive strength (recommended for load capacitances > 5 pF)
Other combinations	Do not use

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PIN CONFIGURATION (CMOS MODE)

RHB PACKAGE
(TOP VIEW)

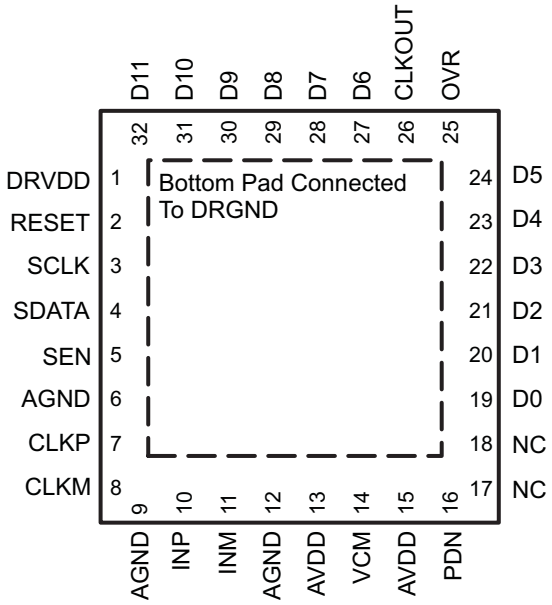

Figure 7. CMOS Mode Pinout

Table 13. Pin Assignments – CMOS Mode

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	I	13, 15	2
AGND	Analog ground	I	6, 9, 12	3
CLKP, CLKM	Differential clock input	I	7, 8	2
INP, INM	Differential analog input	I	10, 11	2
VCM	Internal reference mode – common-mode voltage output. External reference mode – reference input. The voltage forced on this pin sets the internal references.	I/O	14	1
RESET	Serial interface RESET input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin, or by using the software reset option. See the *SERIAL INTERFACE* section. In parallel interface mode, the user has to tie the RESET pin permanently HIGH. (SCLK, SDATA and SEN are used as parallel pin controls in this mode) The pin has an internal 100-kΩ pull-down resistor.	I	2	1
SCLK	This pin functions as serial interface clock input when RESET is low. When RESET is tied high, it controls the coarse gain and internal/external reference selection. Tie SCLK to ***low*** for internal reference and 0 dB gain and ***high*** for internal reference and 3.5 dB gain. See Table 1. The pin has an internal 100-kΩ pull-down resistor.	I	3	1
SDATA	This pin functions as serial interface data input when RESET is ***low***. It controls various power down modes along with PDN pin when RESET is tied ***high***. See Table 3 for detailed information. The pin has an internal 100 kΩ pull-down resistor.	I	4	1
SEN	This pin functions as serial interface enable input when RESET is ***low***. When RESET is high, it controls output interface type and data formats. See Table 2 for detailed information. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	5	1
PDN	Global power down control pin	I	16	1

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Table 13. Pin Assignments – CMOS Mode (continued)

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
CLKOUT	CMOS Output clock	O	26	1
D0	CMOS Output data D0	O	19	1
D1	CMOS Output data D1	O	20	1
D2	CMOS Output data D2	O	21	1
D3	CMOS Output data D3	O	22	1
D4	CMOS Output data D4	O	23	1
D5	CMOS Output data D5	O	24	1
D6	CMOS Output data D6	O	27	1
D7	CMOS Output data D7	O	28	1
D8	CMOS Output data D8	O	29	1
D9	CMOS Output data D9	O	30	1
D10	CMOS Output data D10	O	31	1
D11	CMOS Output data D11	O	32	1
OVR	Indicates over-voltage on analog inputs (for differential input greater than full-scale), CMOS level	O	25	1
DRVDD	Digital supply	I	1	1
DRGND	Digital ground. Connect the pad to the ground plane. See *Board Design Considerations* in application information section.	I	PAD	1
NC	Do not connect		17,18	2

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PIN CONFIGURATION (LVDS MODE)

RHB PACKAGE
(TOP VIEW)

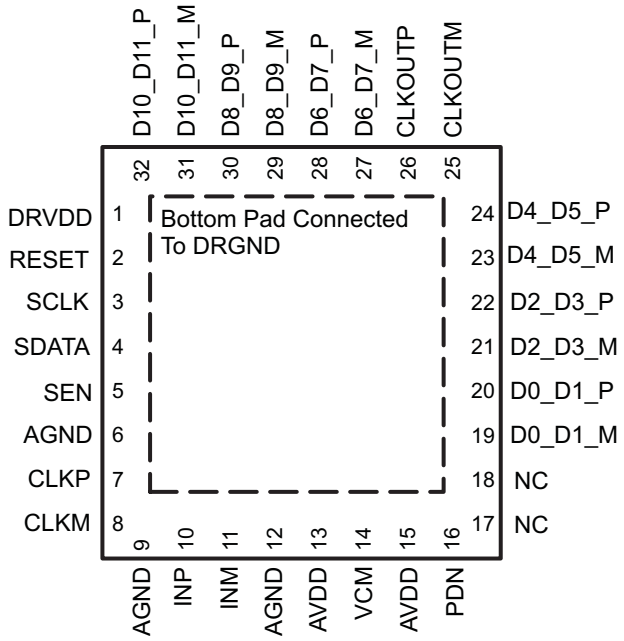

Figure 8. LVDS Mode Pinout

Table 14. Pin Assignments – LVDS Mode

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	I	13, 15	2
AGND	Analog ground	I	6, 9, 12	3
CLKP, CLKM	Differential clock input	I	7, 8	2
INP, INM	Differential analog input	I	10, 11	2
VCM	Internal reference mode – common-mode voltage output. External reference mode – reference input. The voltage forced on this pin sets the internal references.	I/O	14	1
RESET	Serial interface RESET input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin, or by using the software reset option. See the *SERIAL INTERFACE* section. In parallel interface mode, the user has to tie the RESET pin permanently HIGH. (SCLK, SDATA and SEN are used as parallel pin controls in this mode) The pin has an internal 100-kΩ pull-down resistor.	I	2	1
SCLK	This pin functions as serial interface clock input when RESET is low. When RESET is tied high, it controls the coarse gain and internal/external reference selection. Tie SCLK to ***low*** for internal reference and 0 dB gain and ***high*** for internal reference and 3.5 dB gain. See Table 1. The pin has an internal 100-kΩ pull-down resistor.	I	3	1
SDATA	This pin functions as serial interface data input when RESET is ***low***. It controls various power down modes along with PDN pin when RESET is tied ***high***. See Table 3 for detailed information. The pin has an internal 100 kΩ pull-down resistor.	I	4	1
SEN	This pin functions as serial interface enable input when RESET is ***low***. When RESET is high, it controls output interface type and data formats. See Table 2 for detailed information. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	5	1
PDN	Global power down control pin	I	16	1

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Table 14. Pin Assignments – LVDS Mode (continued)

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
CLKOUTP	Differential output clock, true	O	26	1
CLKOUTM	Differential output clock, complement	O	25	1
D0_D1_P	Differential output data D0 and D1 multiplexed, true	O	20	1
D0_D1_M	Differential output data D0 and D1 multiplexed, complement.	O	19	1
D2_D3_P	Differential output data D2 and D3 multiplexed, true	O	22	1
D2_D3_M	Differential output data D2 and D3 multiplexed, complement	O	21	1
D4_D5_P	Differential output data D4 and D5 multiplexed, true	O	24	1
D4_D5_M	Differential output data D4 and D5 multiplexed, complement	O	23	1
D6_D7_P	Differential output data D6 and D7 multiplexed, true	O	28	1
D6_D7_M	Differential output data D6 and D7 multiplexed, complement	O	27	1
D8_D9_P	Differential output data D8 and D9 multiplexed, true	O	30	1
D8_D9_M	Differential output data D8 and D9 multiplexed, complement	O	29	1
D10_D11_P	Differential output data D10 and D11 multiplexed, true	O	32	1
D10_D11_M	Differential output data D10 and D11 multiplexed, complement	O	31	1
DRVDD	Digital supply	I	1	1
DRGND	Digital ground. Connect the pad to the ground plane. See *Board Design Considerations* in application information section.	I	PAD	1
NC	Do not connect		17,18	2

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TYPICAL CHARACTERISTICS - ADS6125 (F_S= 125 MSPS)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

FFT for 20 MHz INPUT SIGNAL

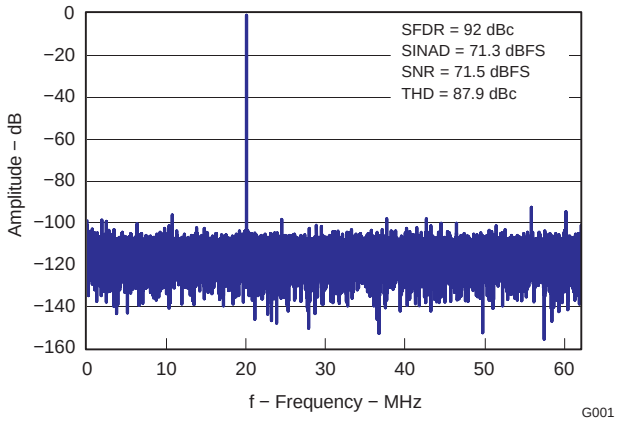

Figure 9.

FFT for 70 MHz INPUT SIGNAL

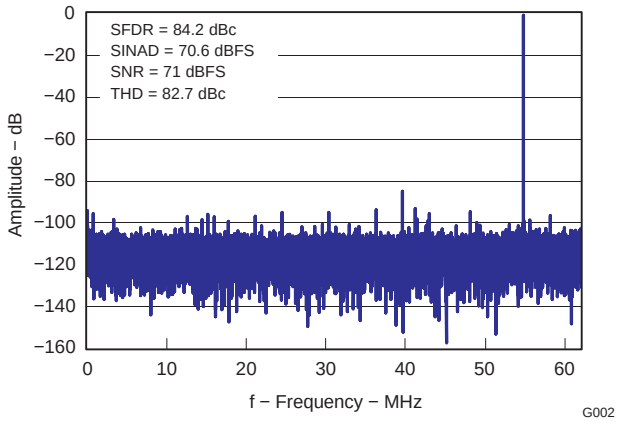

Figure 10.

FFT for 230 MHz INPUT SIGNAL

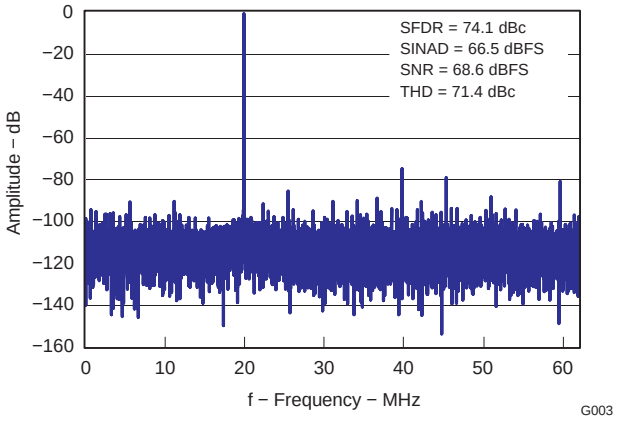

Figure 11.

INTERMODULATION DISTORTION (IMD) vs FREQUENCY

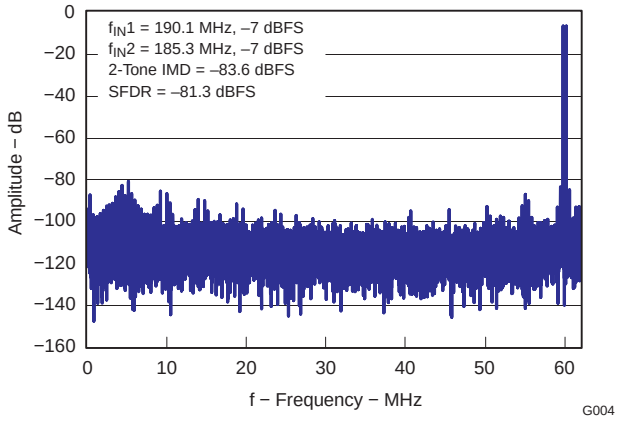

Figure 12.

SFDR vs INPUT FREQUENCY

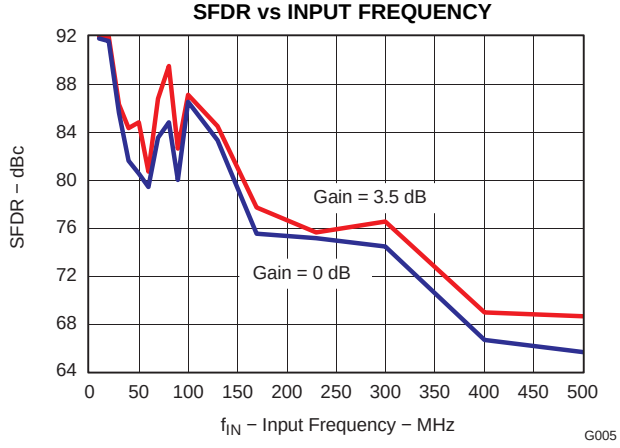

Figure 13.

SNR vs INPUT FREQUENCY

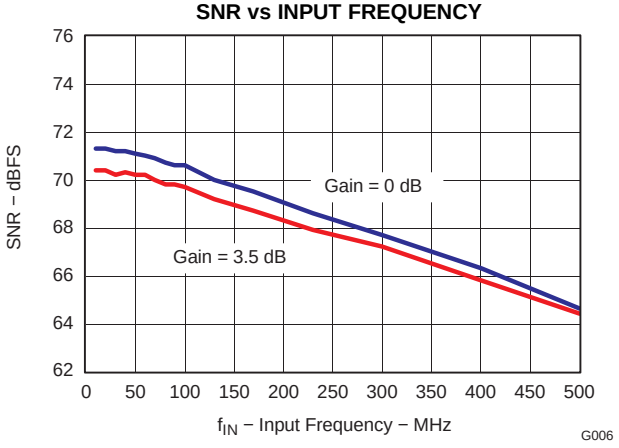

Figure 14.

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TYPICAL CHARACTERISTICS - ADS6125 (F_S= 125 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

SFDR vs INPUT FREQUENCY (LVDS interface)

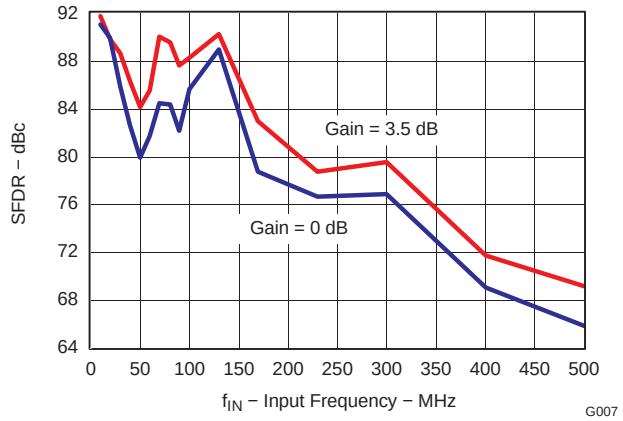

Figure 15.

SNR vs INPUT FREQUENCY (LVDS interface)

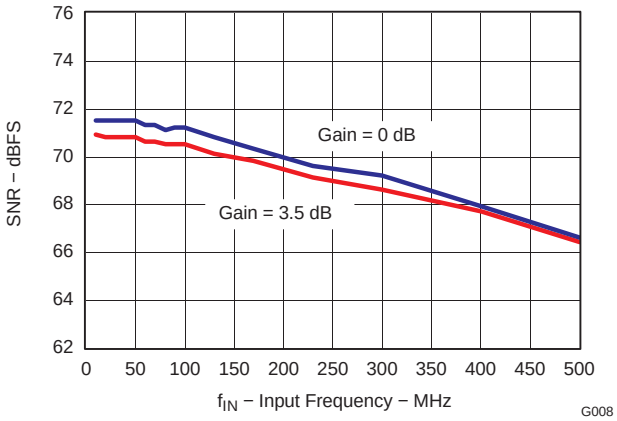

Figure 16.

SFDR vs INPUT FREQUENCY ACROSS GAINS

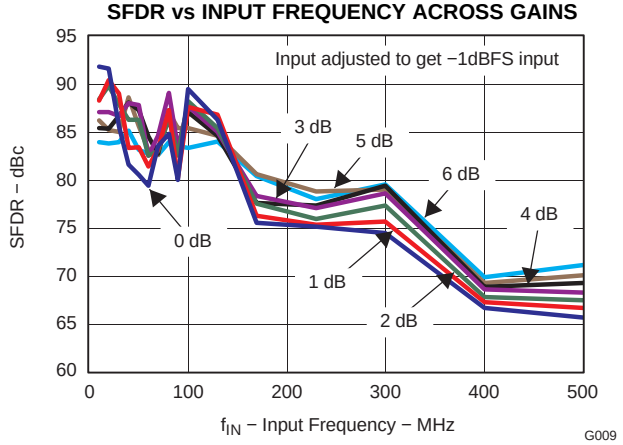

Figure 17.

SINAD vs INPUT FREQUENCY ACROSS GAINS

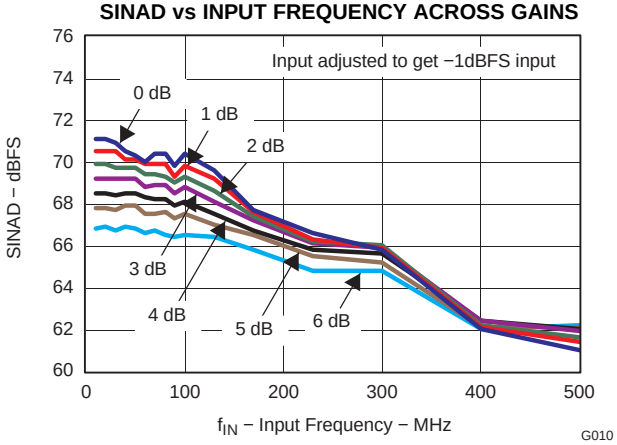

Figure 18.

PERFORMANCE vs AVDD

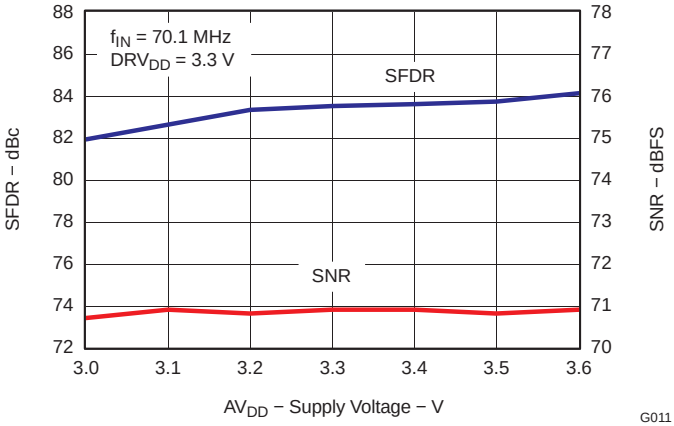

Figure 19.

PERFORMANCE vs DRVDD

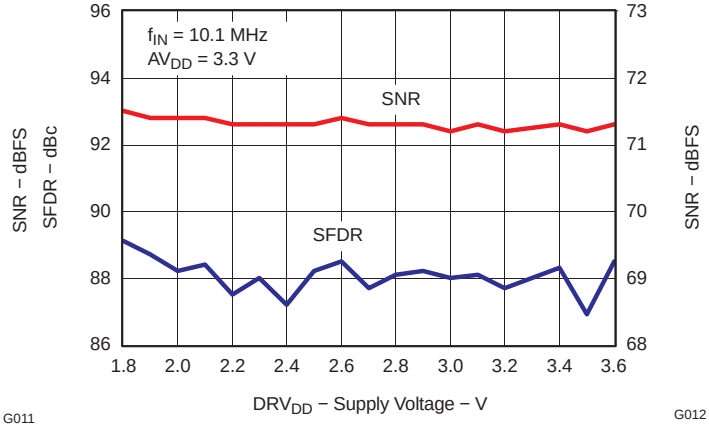

Figure 20.

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TYPICAL CHARACTERISTICS - ADS6125 (F_S= 125 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

PERFORMANCE vs TEMPERATURE

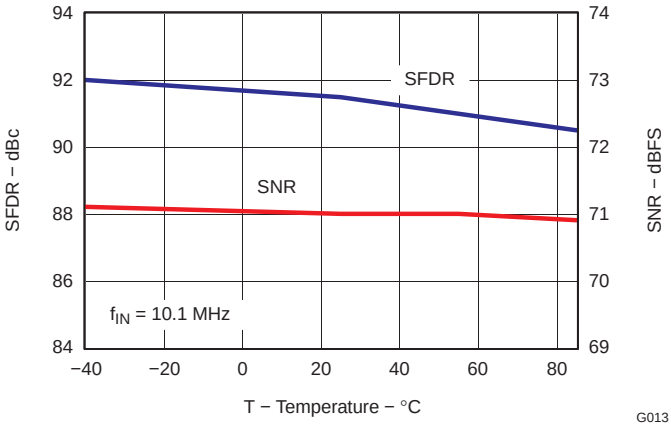

Figure 21.

PERFORMANCE vs INPUT AMPLITUDE

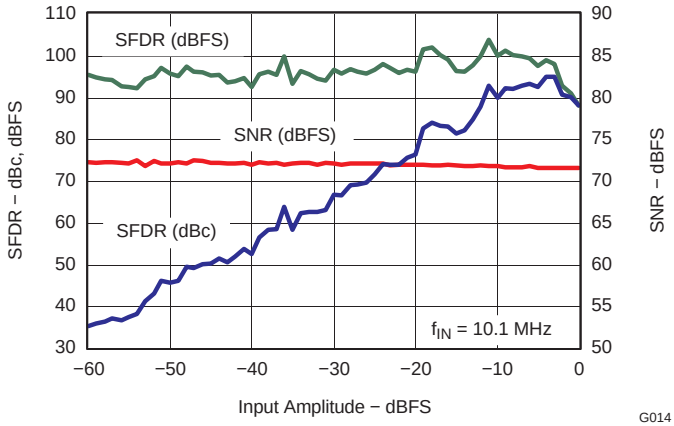

Figure 22.

PERFORMANCE vs CLOCK AMPLITUDE

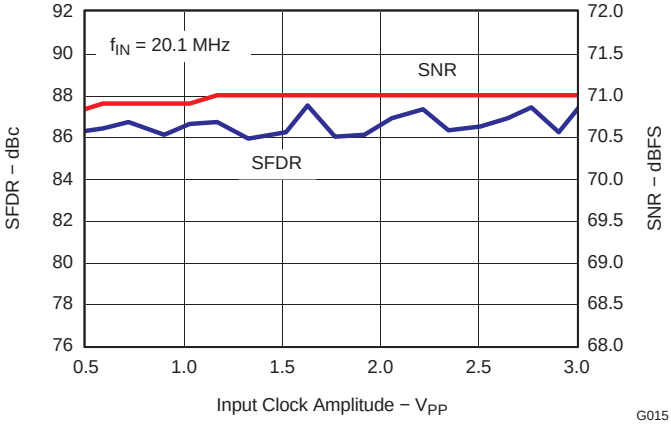

Figure 23.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

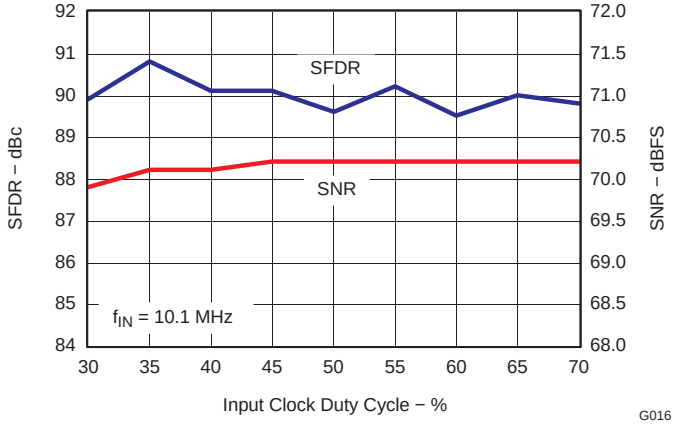

Figure 24.

OUTPUT NOISE HISTOGRAM (INPUTS TIED TO COMMON-MODE)

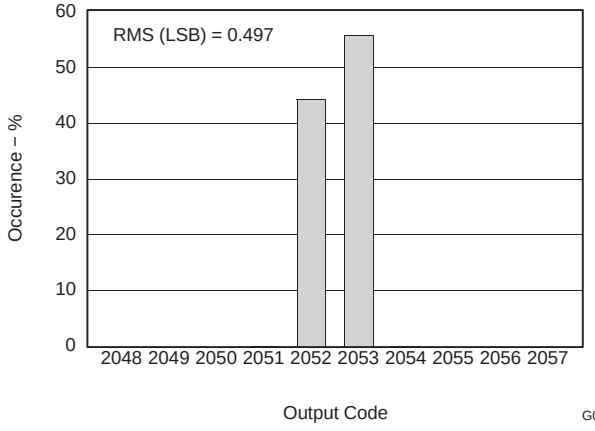

Figure 25.

PERFORMANCE IN EXTERNAL REFERENCE MODE

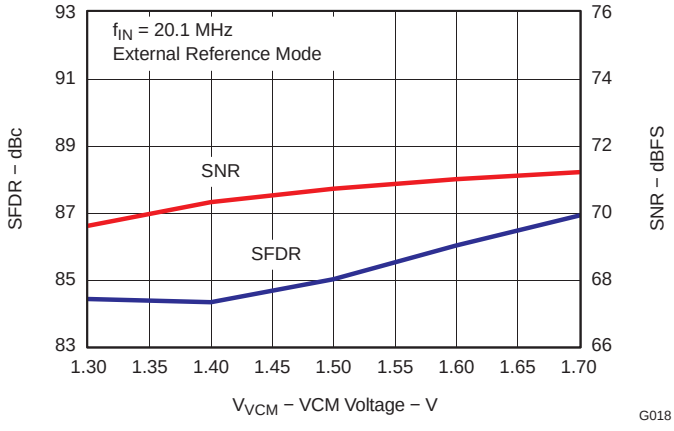

Figure 26.

TYPICAL CHARACTERISTICS - ADS6124 (F_S= 105 MSPS)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

FFT for 20 MHz INPUT SIGNAL

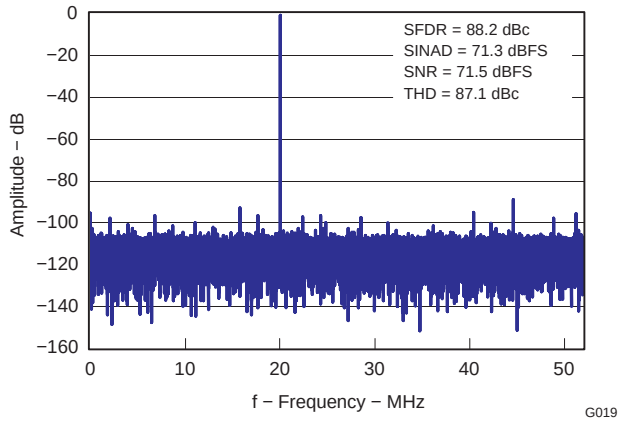

Figure 27.

FFT for 80 MHz INPUT SIGNAL

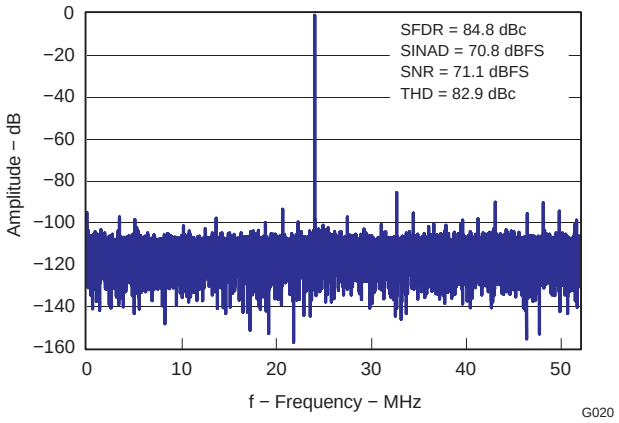

Figure 28.

FFT for 230 MHz INPUT SIGNAL

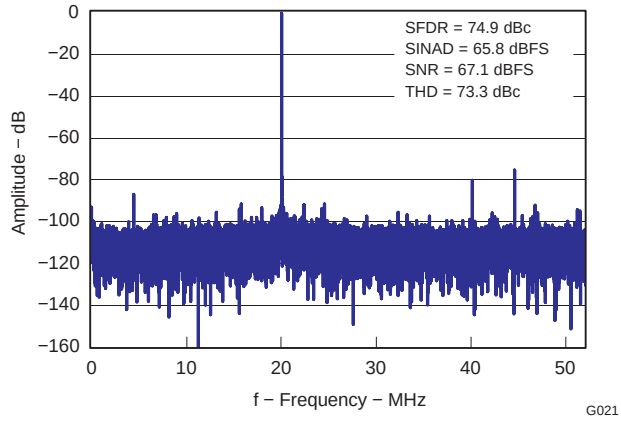

Figure 29.

INTERMODULATION DISTORTION (IMD) vs FREQUENCY

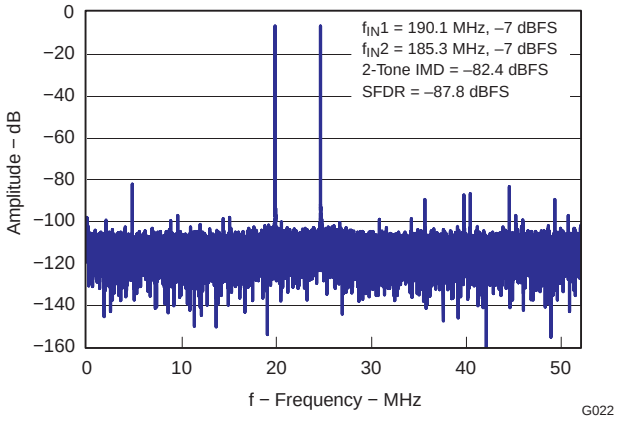

Figure 30.

SFDR vs INPUT FREQUENCY

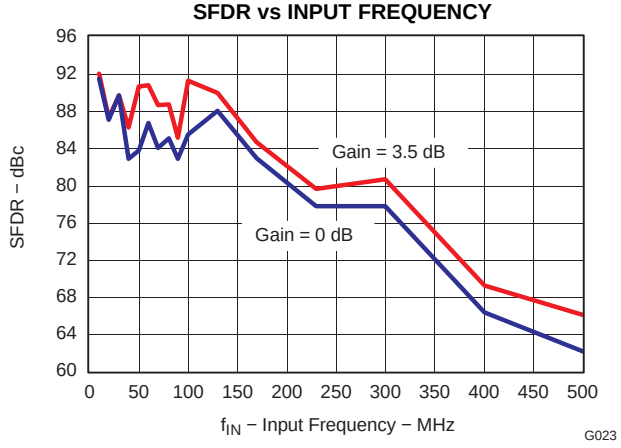

Figure 31.

SNR vs INPUT FREQUENCY

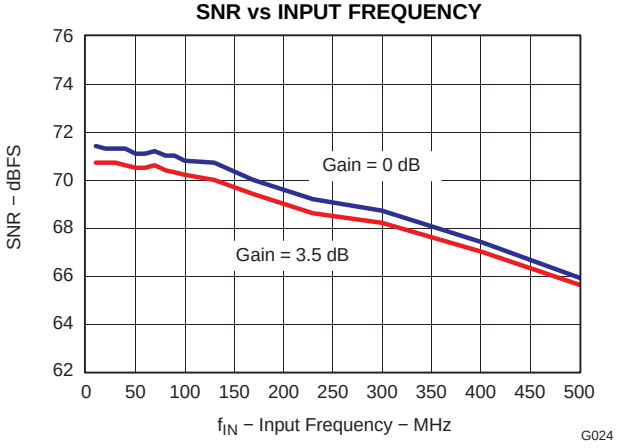

Figure 32.

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TYPICAL CHARACTERISTICS - ADS6124 (F_S= 105 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

SFDR vs INPUT FREQUENCY (LVDS interface)

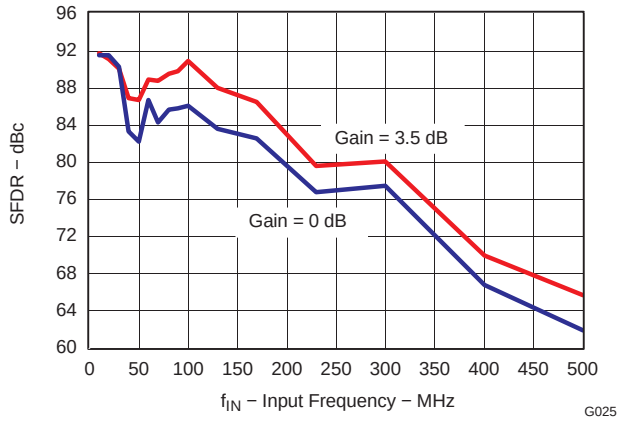

Figure 33.

SNR vs INPUT FREQUENCY (LVDS interface)

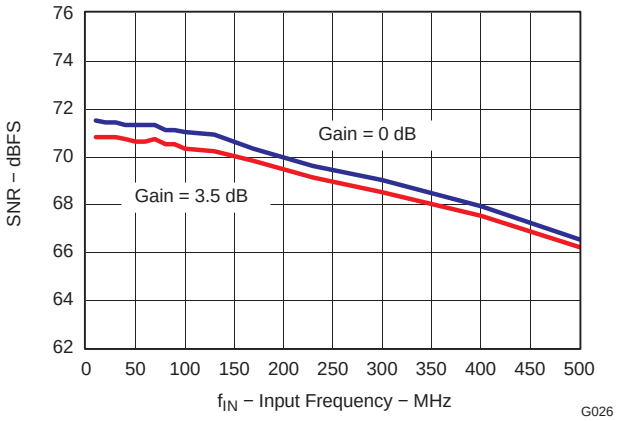

Figure 34.

SFDR vs INPUT FREQUENCY ACROSS GAINS

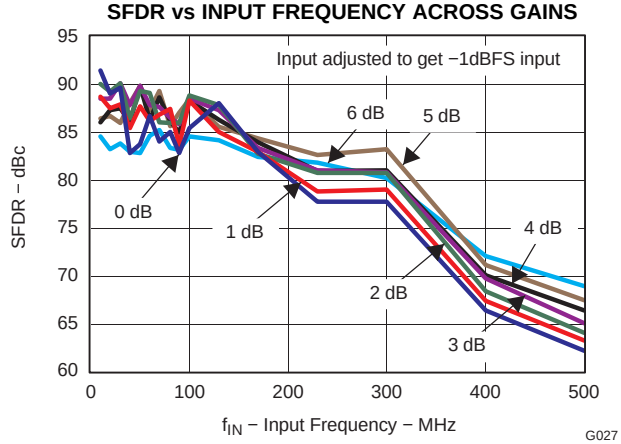

Figure 35.

SINAD vs INPUT FREQUENCY ACROSS GAINS

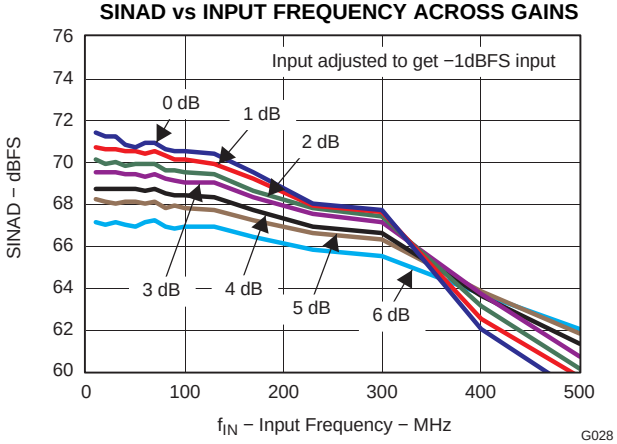

Figure 36.

PERFORMANCE vs AVDD

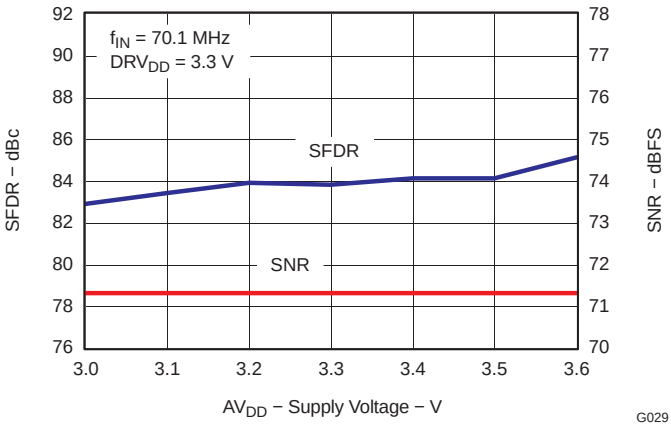

Figure 37.

PERFORMANCE vs DRVDD

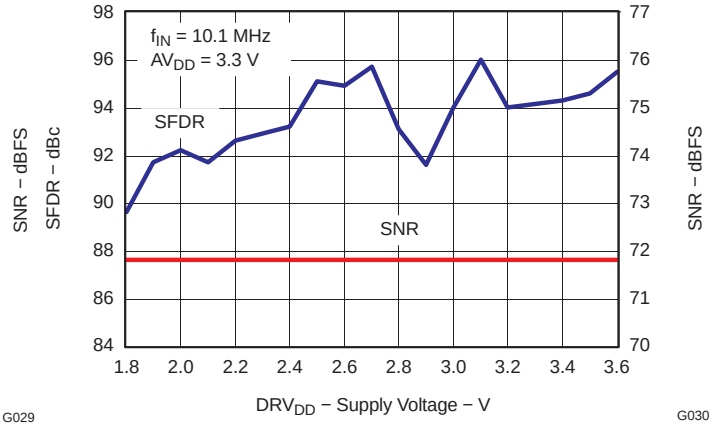

Figure 38.

TYPICAL CHARACTERISTICS - ADS6124 (F_S= 105 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

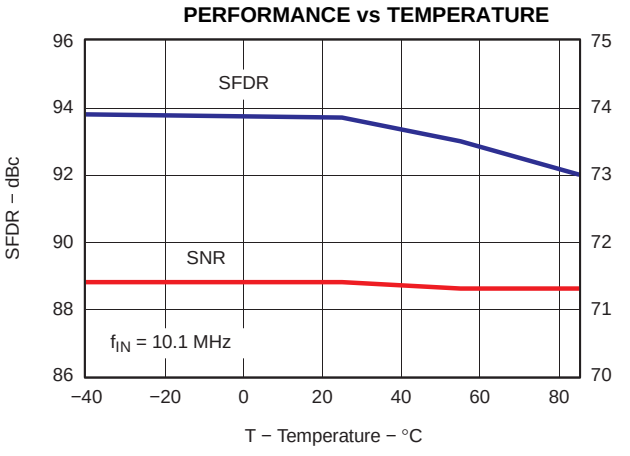

Figure 39.

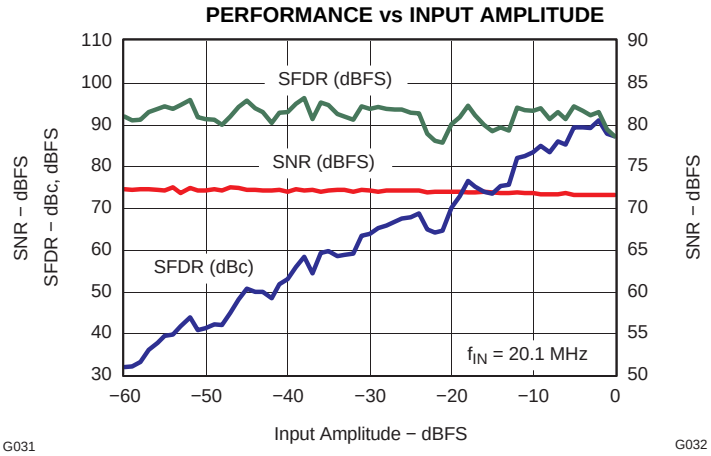

Figure 40.

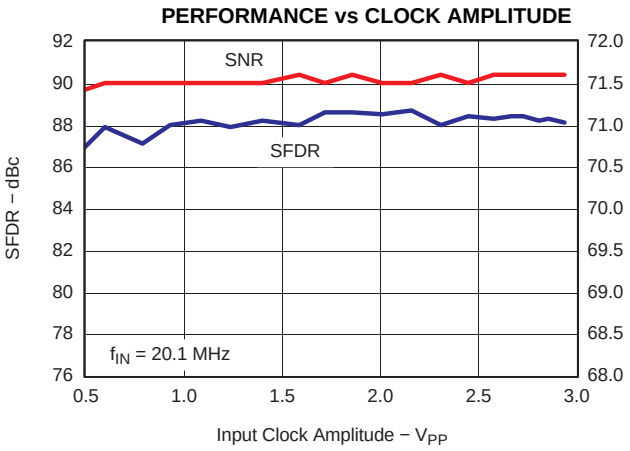

Figure 41.

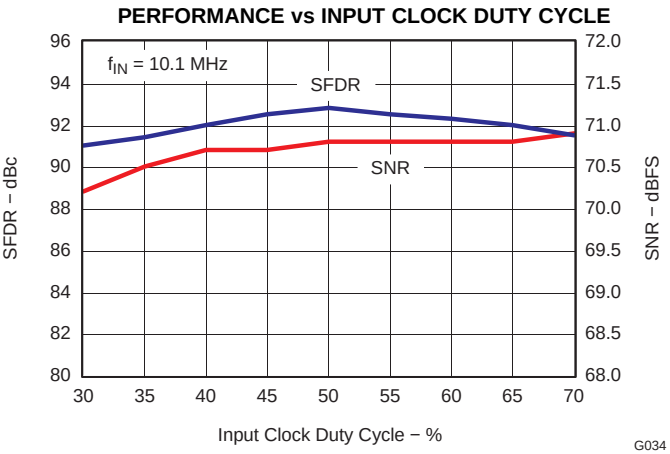

Figure 42.

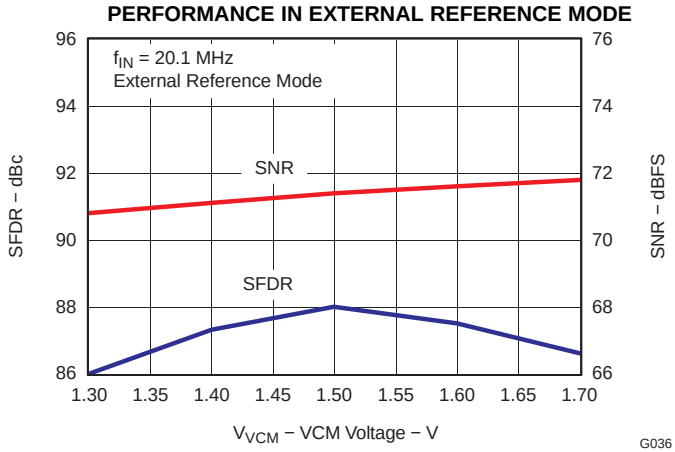

Figure 43.

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TYPICAL CHARACTERISTICS - ADS6123 (F_S= 80 MSPS)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

FFT for 20 MHz INPUT SIGNAL

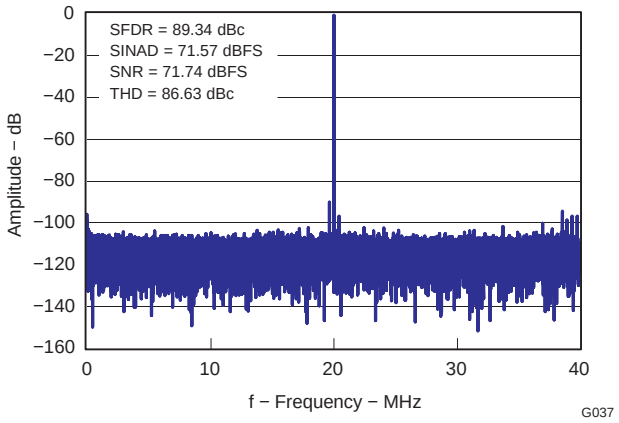

Figure 44.

FFT for 70 MHz INPUT SIGNAL

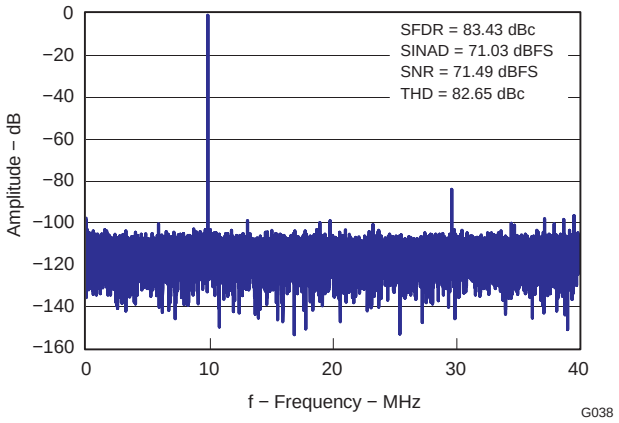

Figure 45.

FFT for 230 MHz INPUT SIGNAL

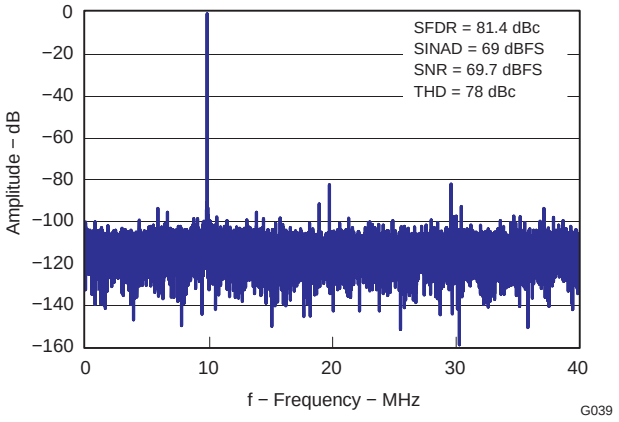

Figure 46.

INTERMODULATION DISTORTION (IMD) vs FREQUENCY

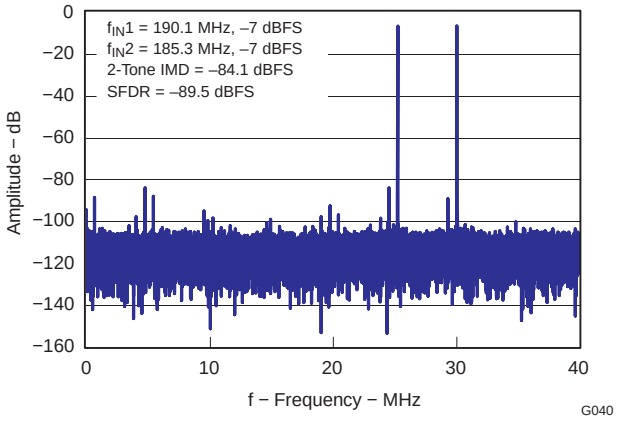

Figure 47.

SFDR vs INPUT FREQUENCY

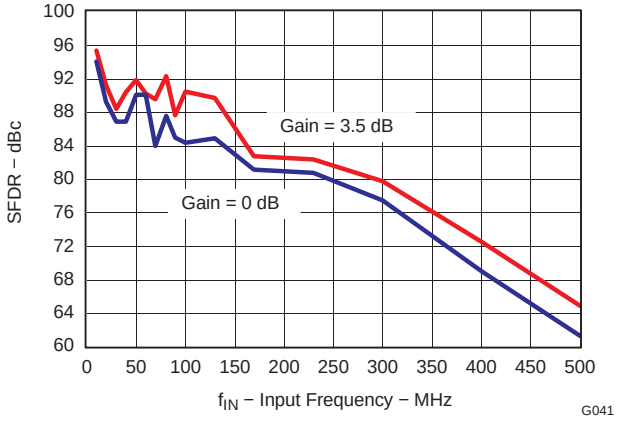

Figure 48.

SNR vs INPUT FREQUENCY

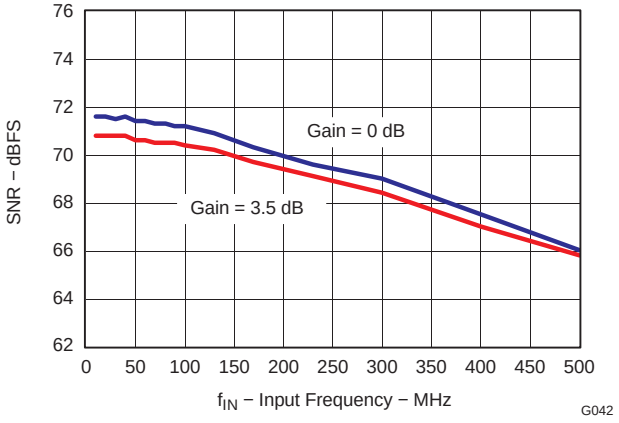

Figure 49.

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TYPICAL CHARACTERISTICS - ADS6123 (F_S= 80 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

SFDR vs INPUT FREQUENCY (LVDS interface)

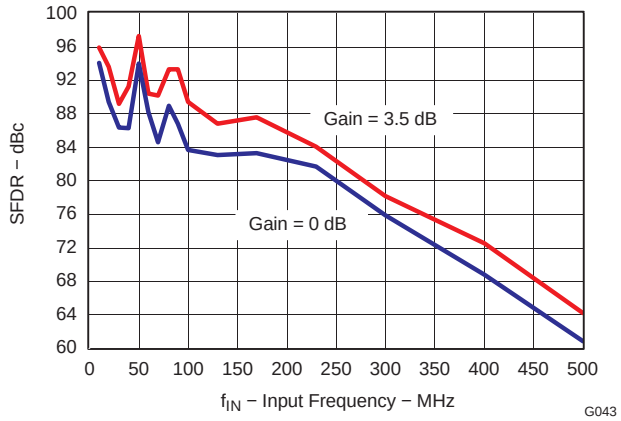

Figure 50.

SNR vs INPUT FREQUENCY (LVDS interface)

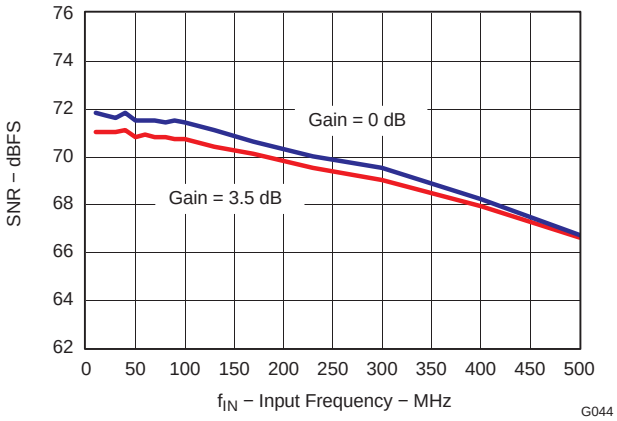

Figure 51.

SFDR vs INPUT FREQUENCY ACROSS GAINS

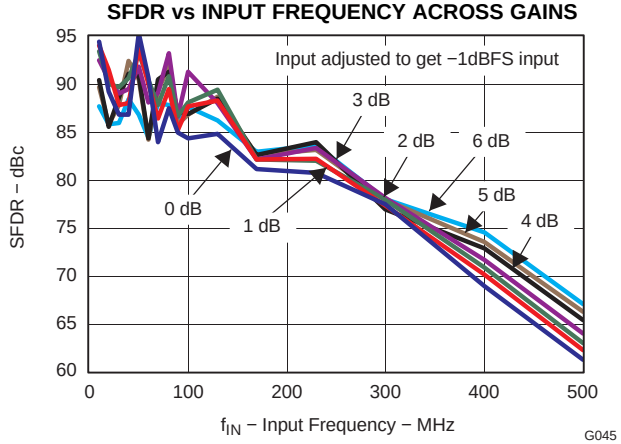

Figure 52.

SINAD vs INPUT FREQUENCY ACROSS GAINS

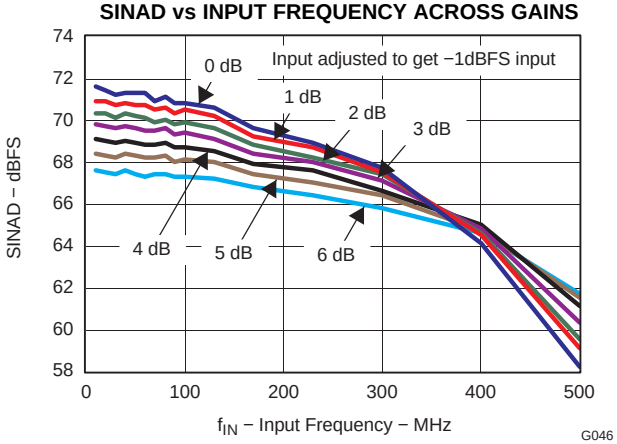

Figure 53.

PERFORMANCE vs AVDD

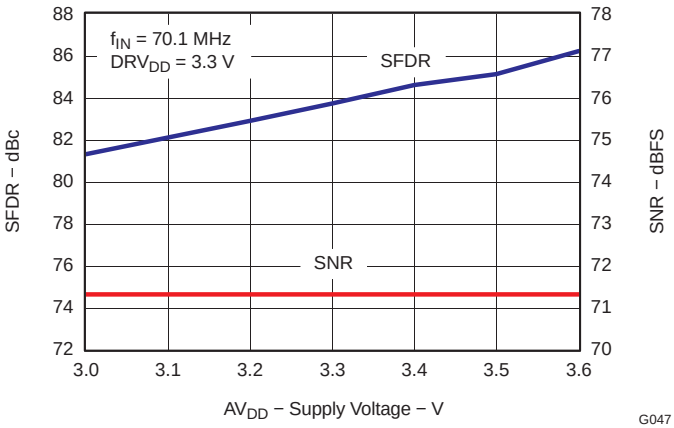

Figure 54.

PERFORMANCE vs DRVDD

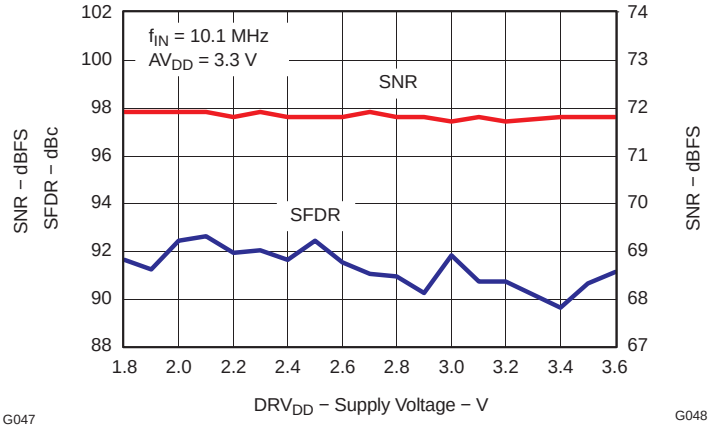

Figure 55.

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TYPICAL CHARACTERISTICS - ADS6123 (F_S= 80 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

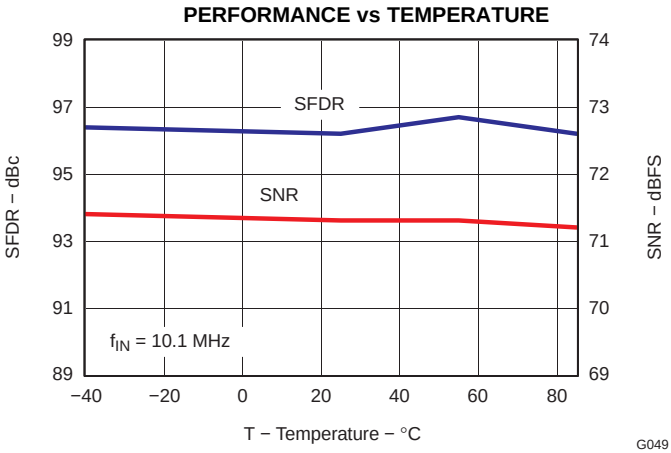

Figure 56.

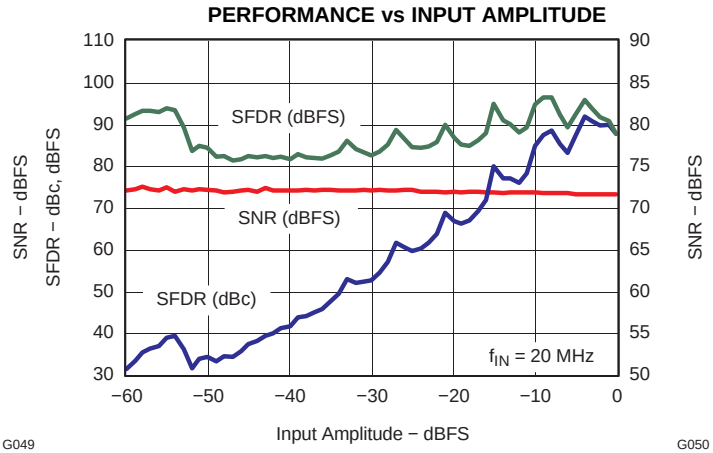

Figure 57.

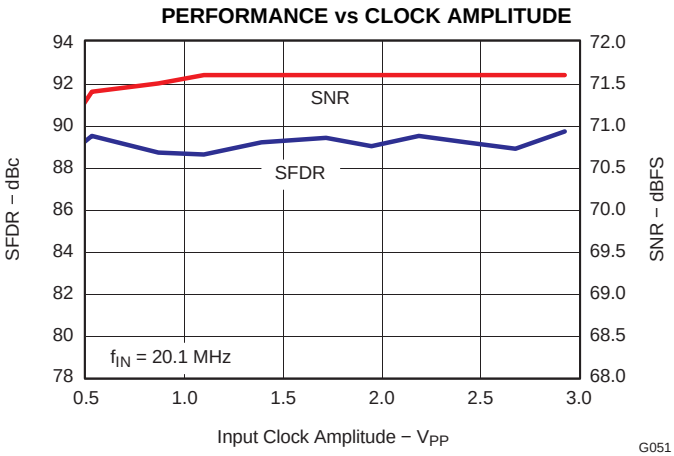

Figure 58.

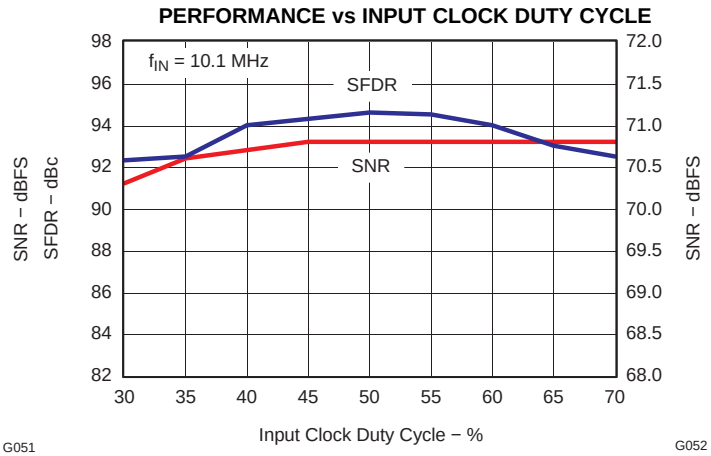

Figure 59.

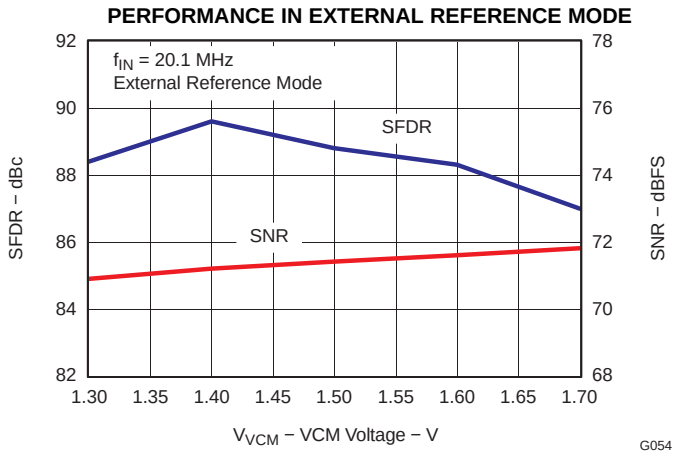

Figure 60.

TYPICAL CHARACTERISTICS - ADS6122 (F_S= 65 MSPS)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

FFT for 20 MHz INPUT SIGNAL

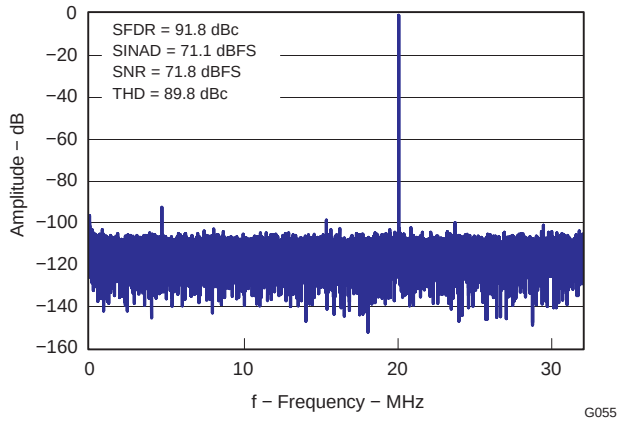

Figure 61.

FFT for 90 MHz INPUT SIGNAL

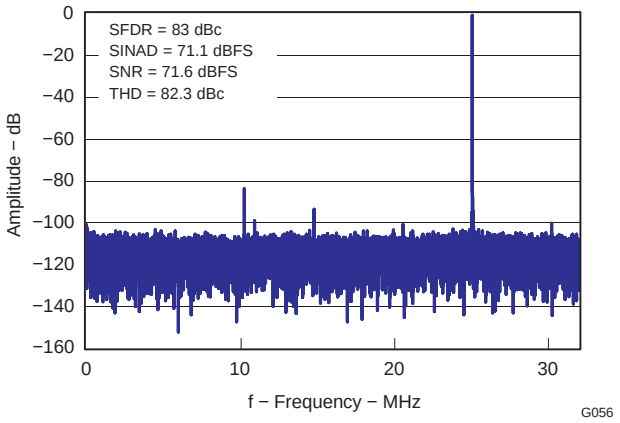

Figure 62.

FFT for 230 MHz INPUT SIGNAL

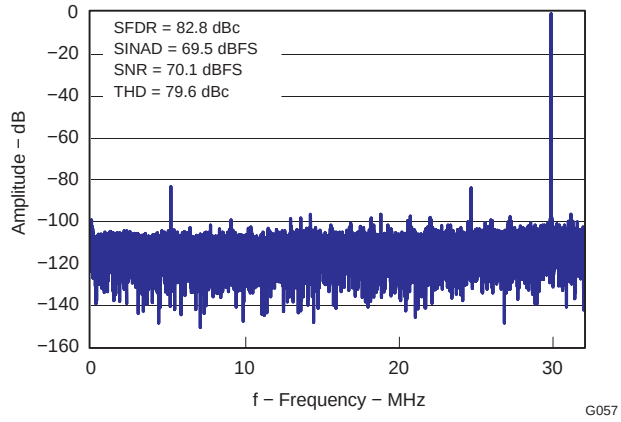

Figure 63.

INTERMODULATION DISTORTION (IMD) vs FREQUENCY

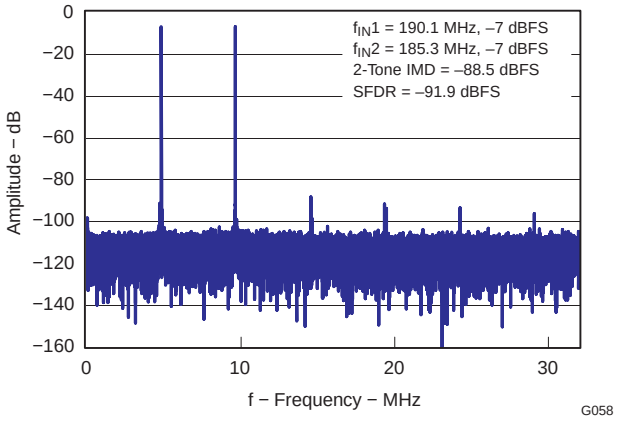

Figure 64.

SFDR vs INPUT FREQUENCY

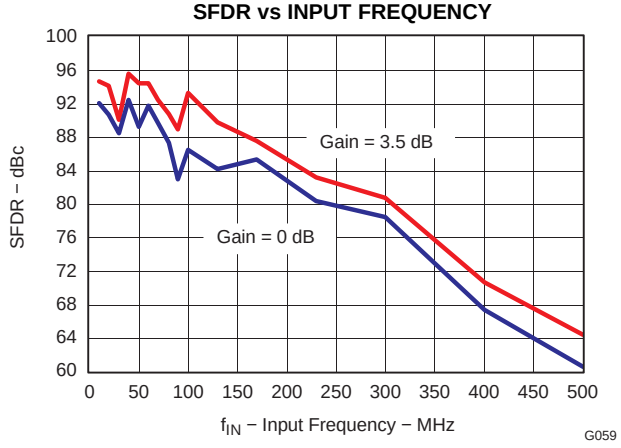

Figure 65.

SNR vs INPUT FREQUENCY

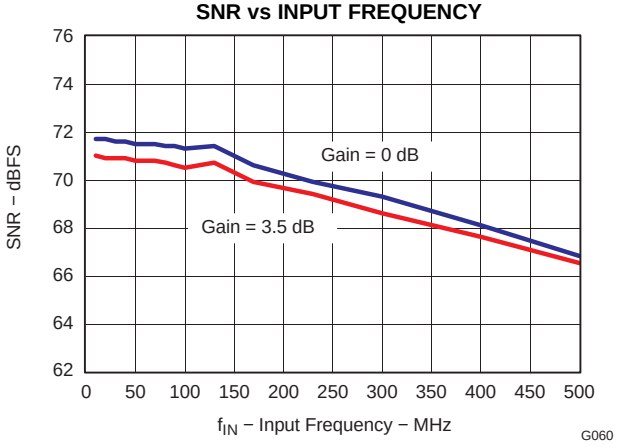

Figure 66.

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TYPICAL CHARACTERISTICS - ADS6122 (F_S= 65 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

SFDR vs INPUT FREQUENCY (LVDS interface)

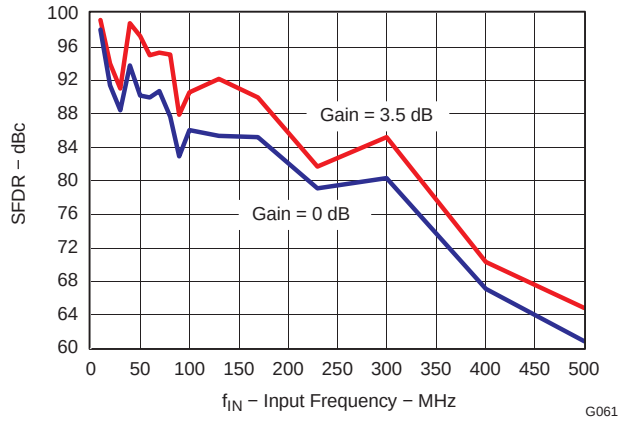

Figure 67.

SNR vs INPUT FREQUENCY (LVDS interface)

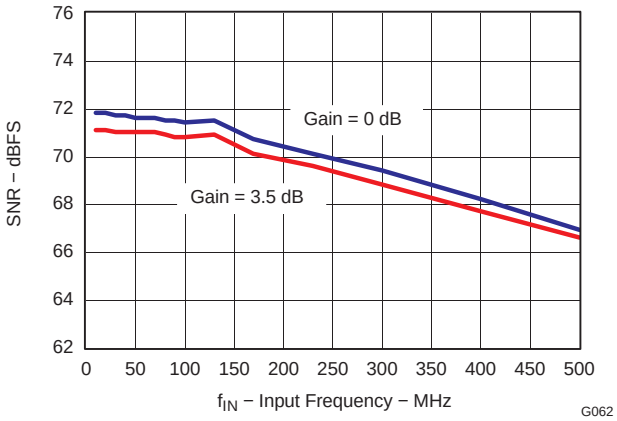

Figure 68.

SFDR vs INPUT FREQUENCY ACROSS GAINS

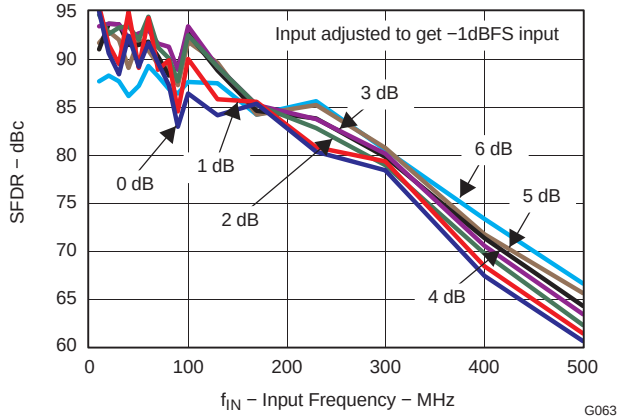

Figure 69.

SINAD vs INPUT FREQUENCY ACROSS GAINS

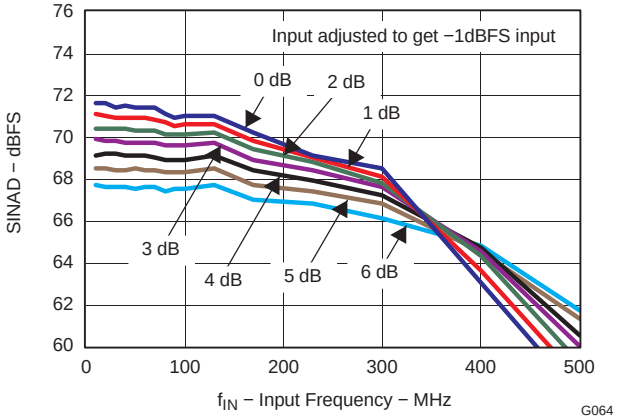

Figure 70.

PERFORMANCE vs AVDD

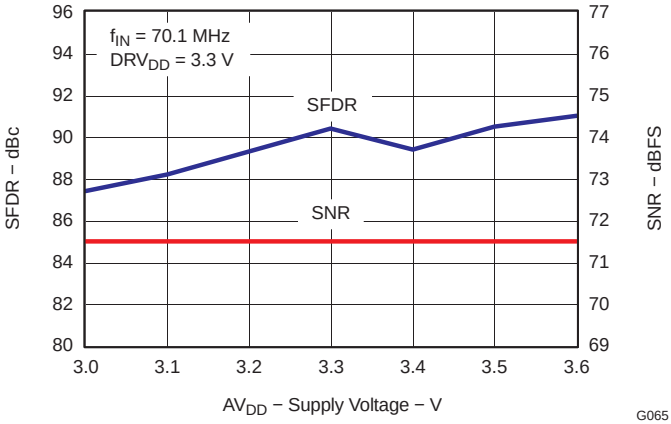

Figure 71.

PERFORMANCE vs DRVDD

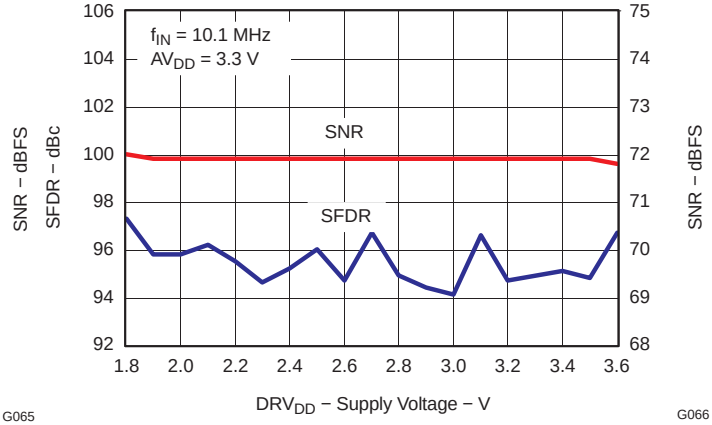

Figure 72.

TYPICAL CHARACTERISTICS - ADS6122 (F_S= 65 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

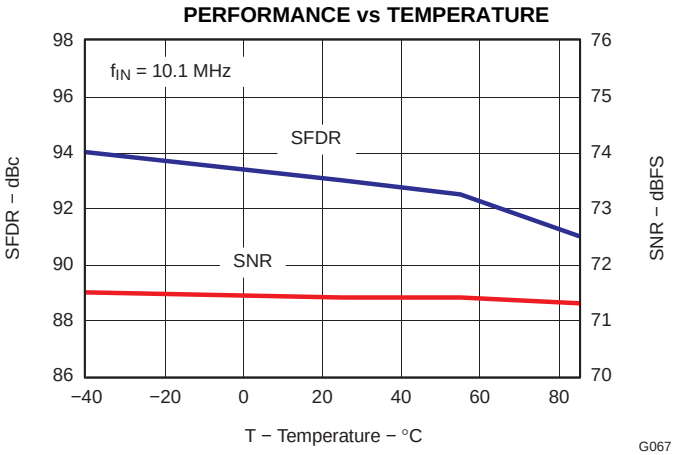

Figure 73.

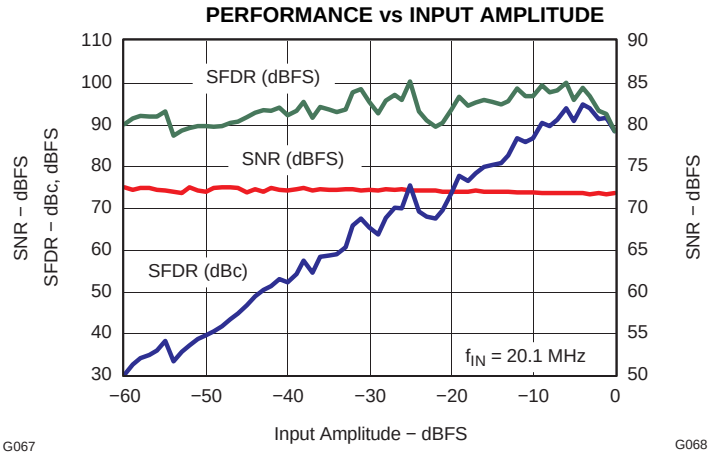

Figure 74.

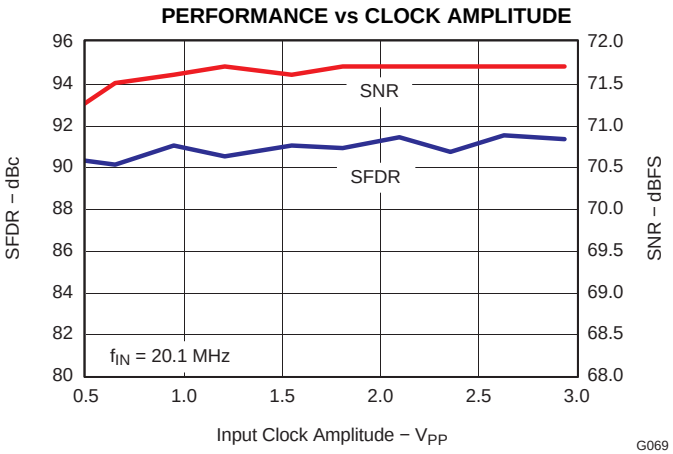

Figure 75.

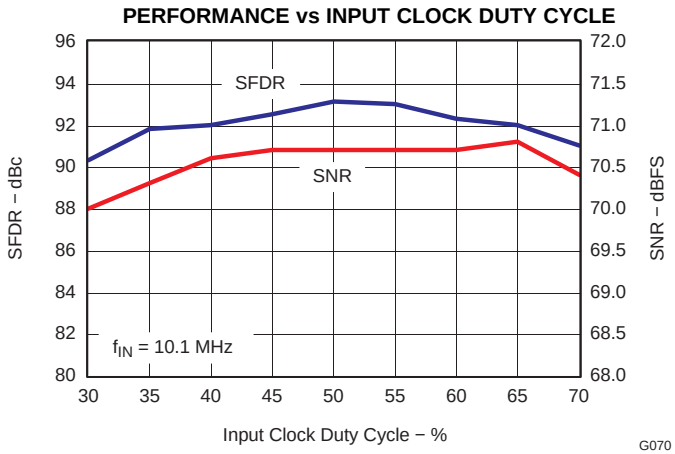

Figure 76.

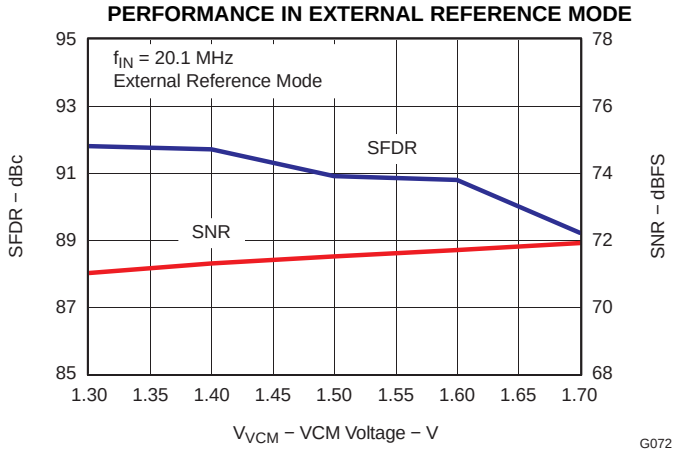

Figure 77.

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TYPICAL CHARACTERISTICS - LOW SAMPLING FREQUENCIES

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

F_S = 40 MSPS

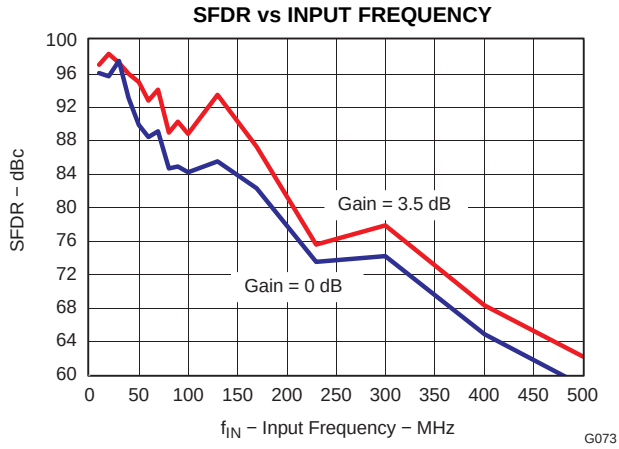

Figure 78.

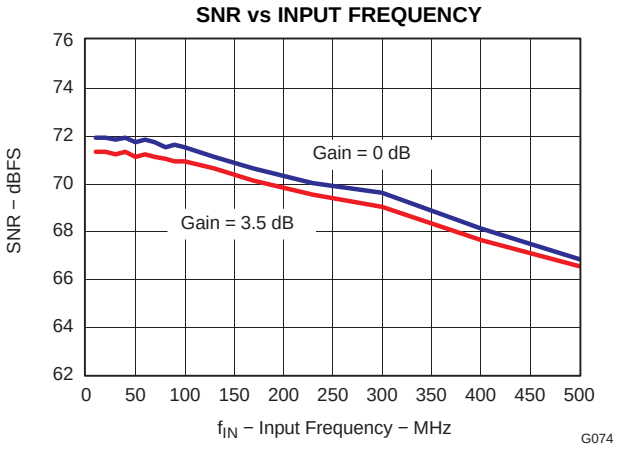

Figure 79.

F_S = 25 MSPS

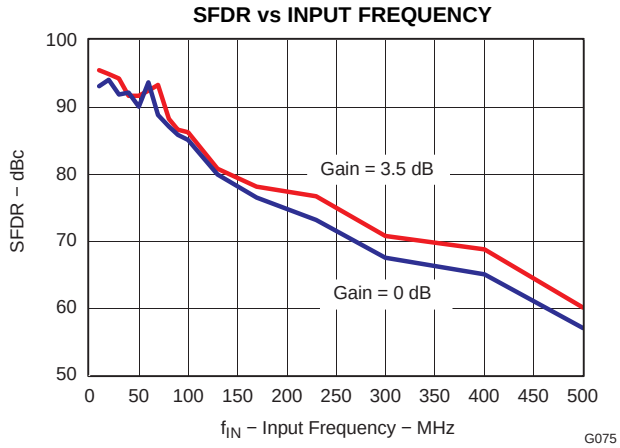

Figure 80.

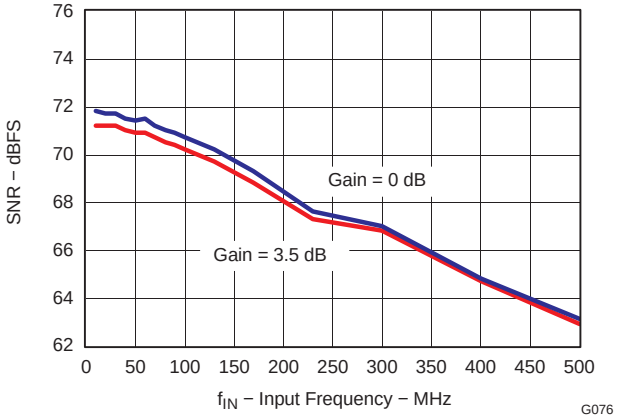

Figure 81.

COMMON PLOTS

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

COMMON-MODE REJECTION RATIO vs FREQUENCY

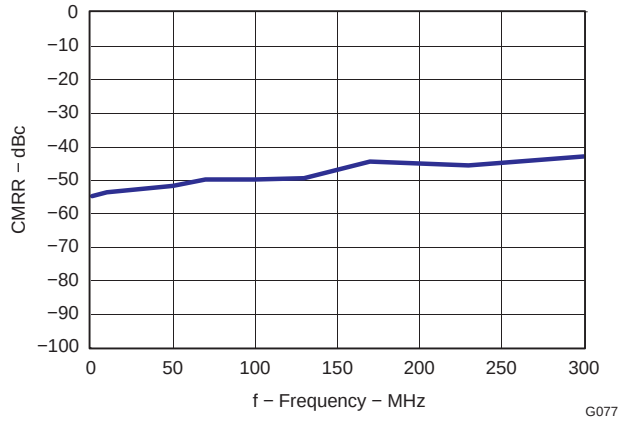

Figure 82.

POWER DISSIPATION vs SAMPLING FREQUENCY (DDR LVDS and CMOS)

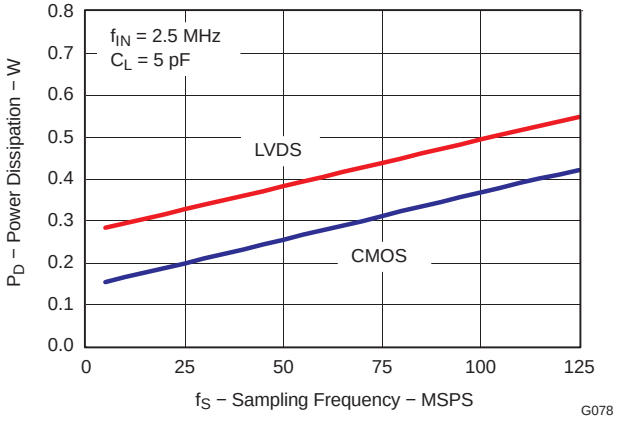

Figure 83.

DRVDD current vs SAMPLING FREQUENCY across load capacitance (CMOS)

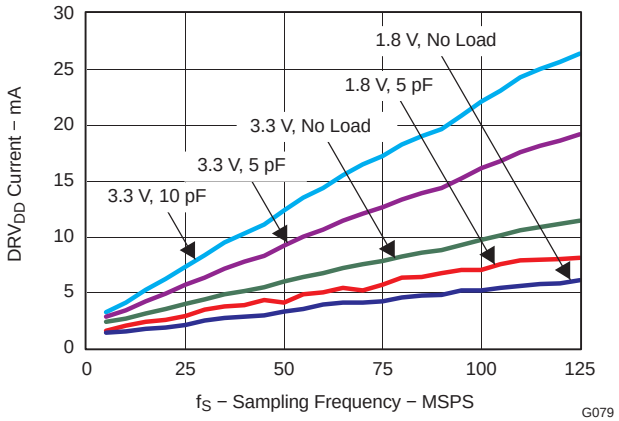

Figure 84.

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Contour Plots Across Input and Sampling Frequencies

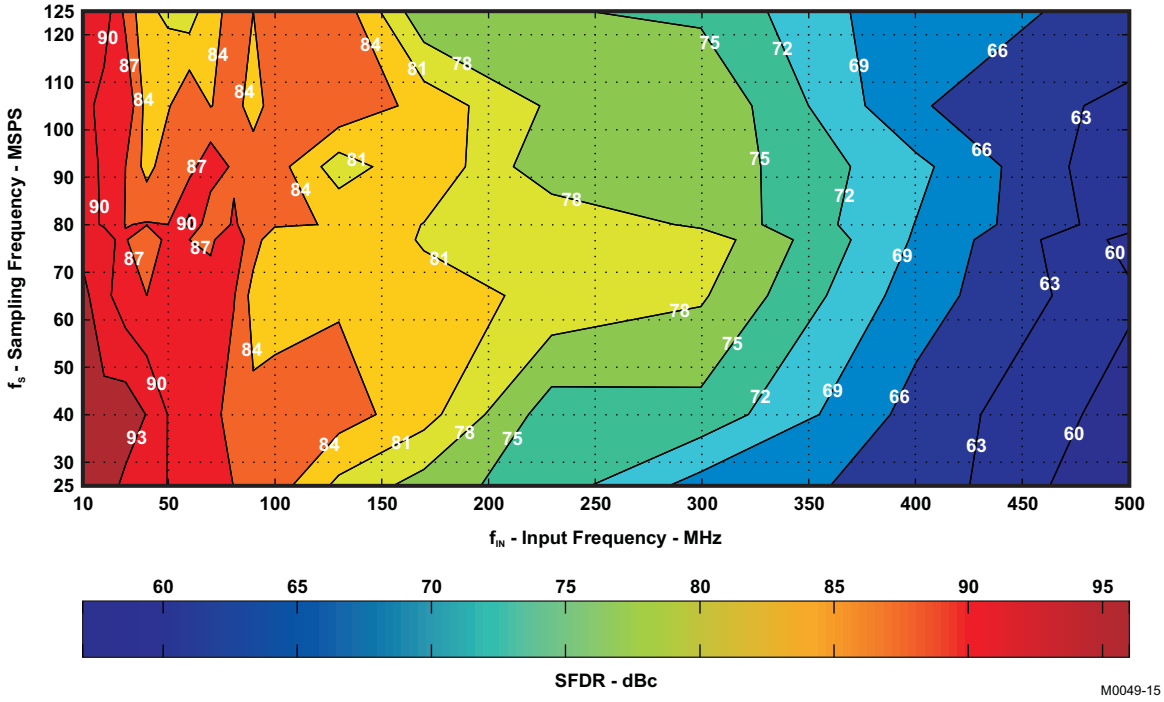

Figure 85. SFDR Contour (No gain, F_S = 2 V_{PP})

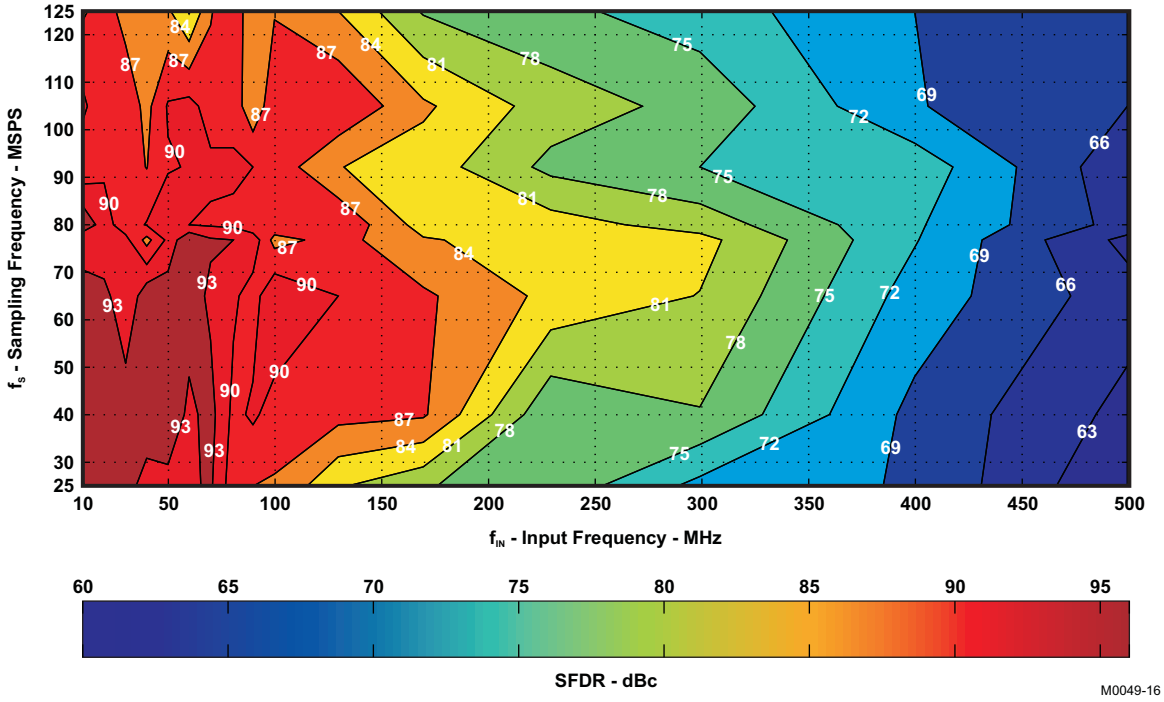

Figure 86. SFDR Contour (with 3.5 dB Coarse gain, F_S = 1.34 V_{PP})

Contour Plots Across Input and Sampling Frequencies (continued)

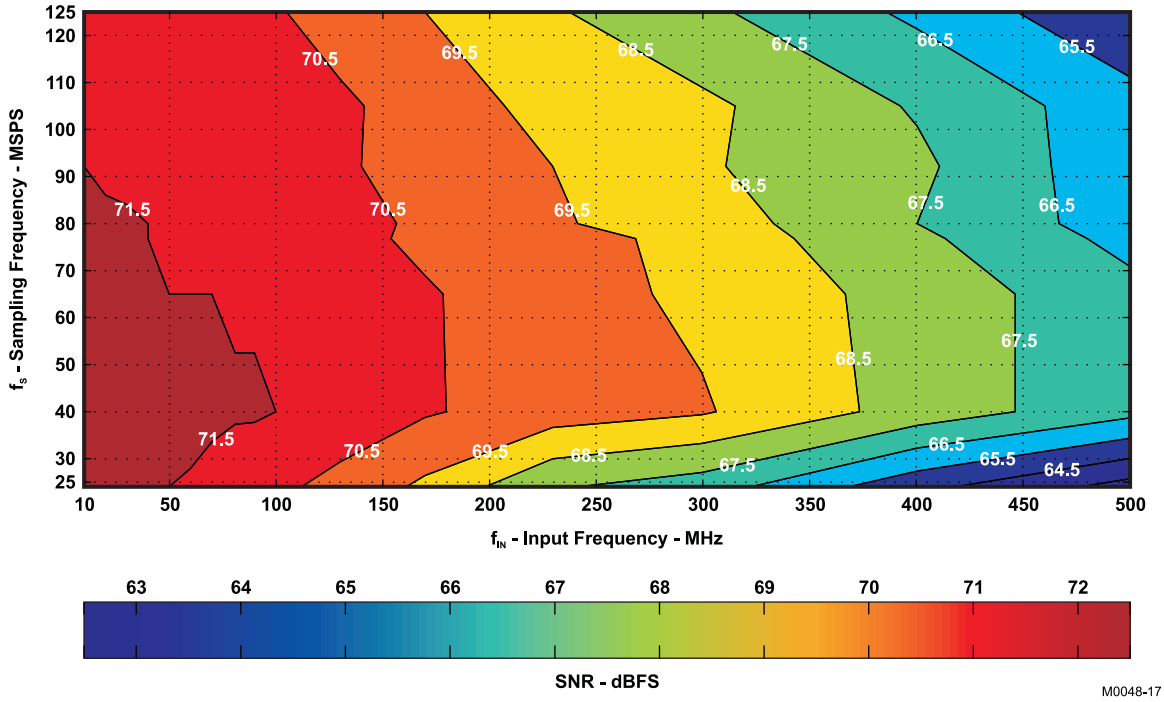

Figure 87. SNR Contour (No gain, F_S = 2 V_{PP})

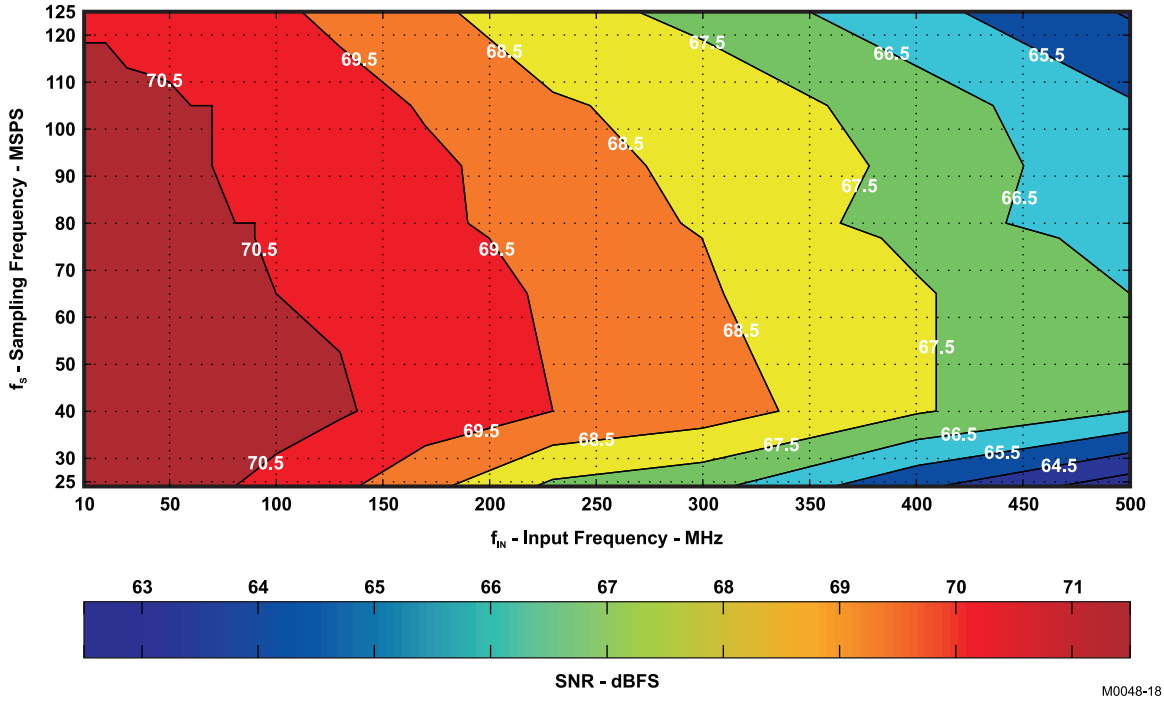

Figure 88. SNR Contour (with 3.5 dB Coarse gain, F_S = 1.34 V_{PP})

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APPLICATION INFORMATION

THEORY OF OPERATION

ADS612X is a family of low power 12-bit pipeline ADC in a CMOS process up to 125 MSPS sampling frequency. It is based on switched capacitor technology and runs off a single 3.3-V supply. The conversion process is initiated by a rising edge of the external input clock. Once the signal is captured by the input sample and hold, the input sample is sequentially converted by a series of lower resolution stages, with the outputs combined in a digital correction logic block. At every clock edge, the sample propagates through the pipeline resulting in a data latency of 9 clock cycles. The output is available as 12-bit data, in DDR LVDS or CMOS and coded in either straight offset binary or binary 2s complement format.

ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture, shown in Figure 89.

This differential topology results in good ac-performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5 V available on VCM pin. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V_{PP} differential input swing. The maximum swing is determined by the internal reference voltages REFP (2.5 V nominal) and REFM (0.5 V, nominal).

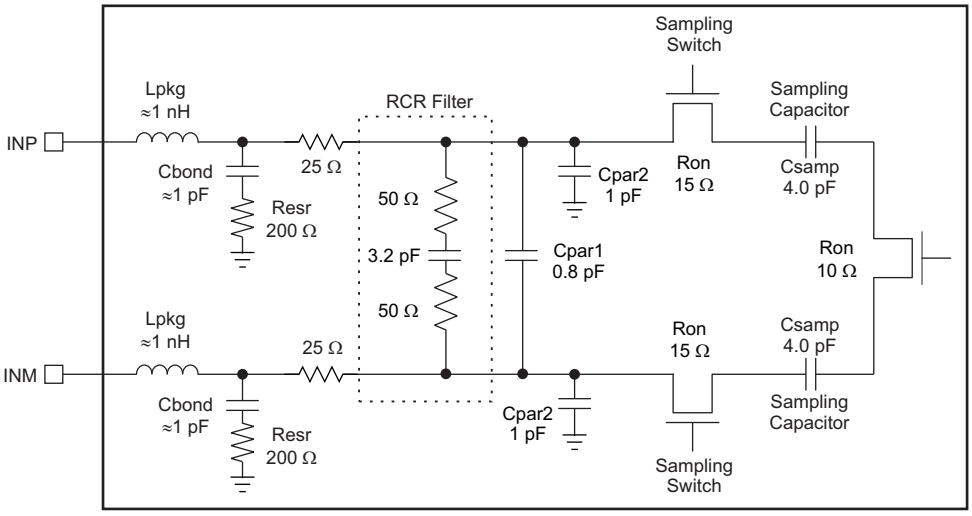

Figure 89. Input Stage

The input sampling circuit has a high 3-dB bandwidth that extends up to 450 MHz (measured from the input pins to the voltage across the sampling capacitors).

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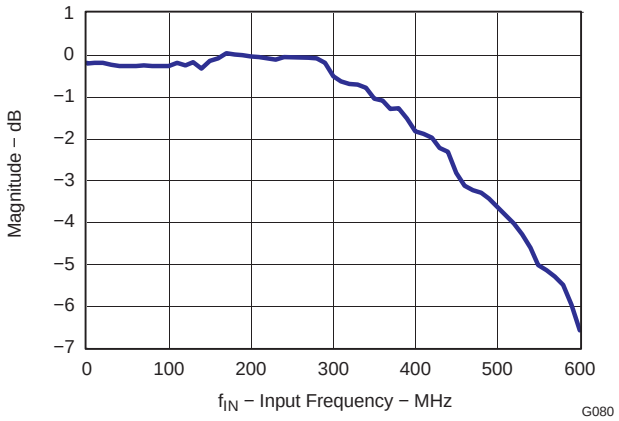

Figure 90. ADC Analog Input Bandwidth

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection.

A 5-Ω resistor in series with each input pin is recommended to damp out ringing caused by the package parasitics. It is also necessary to present low impedance (< 50 Ω) for the common mode switching currents. For example, this is achieved by using two resistors from each input terminated to the common mode voltage (VCM).

In addition to the above, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance must be considered. Over a wide frequency range, the input impedance can be approximated by a parallel combination of Rin and Cin (Zin = Rin || Cin).

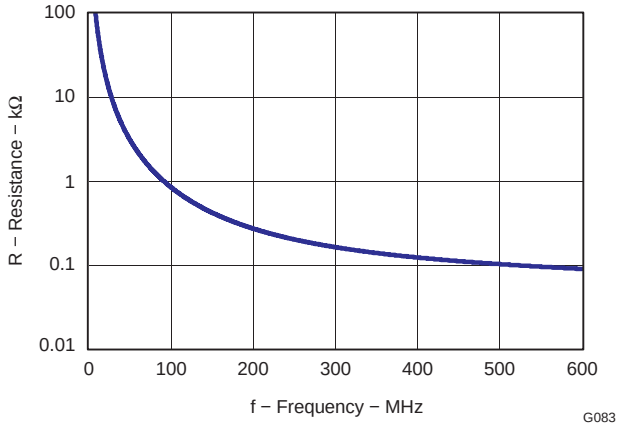

Figure 91. ADC Input Resistance, Rin

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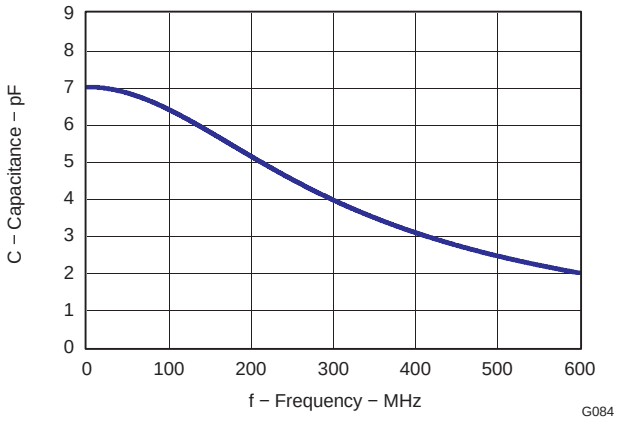

Figure 92. ADC Input Capacitance, Cin

Using RF-Transformer Based Drive Circuits

Figure 93 shows a configuration using a single 1:1 turns ratio transformer (for example, Coilcraft WBC1-1) that can be used for low input frequencies (about 100 MHz).

The single-ended signal is fed to the primary winding of the RF transformer. The transformer is terminated on the secondary side. Putting the termination on the secondary side helps to shield the kickbacks caused by the sampling circuit from the RF transformer's leakage inductances. The termination is accomplished by two resistors connected in series, with the center point connected to the 1.5 V common mode (VCM pin). The value of the termination resistors (connected to common mode) has to be low (< 100 Ω) to provide a low-impedance path for the ADC common-mode switching current.

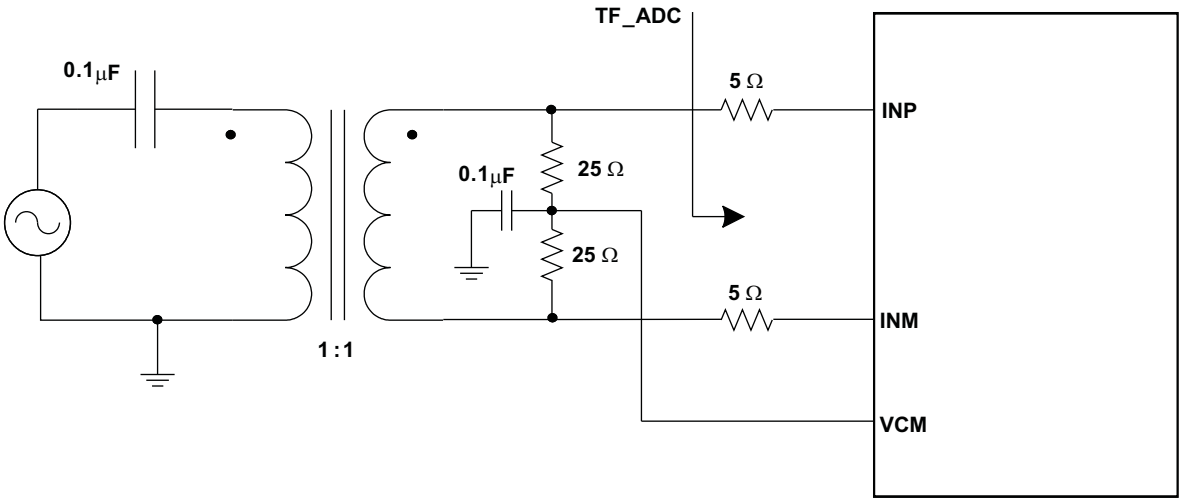

Figure 93. Single Transformer Drive Circuit

At high input frequencies, the mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch, and good performance is obtained for high frequency input signals. Figure 94 shows an example using two transformers (Coilcraft WBC1-1). An additional termination resistor pair (enclosed within the shaded box in Figure 94) may be required between the two transformers to improve the balance between the P and M sides. The center point of this termination must be connected to ground.

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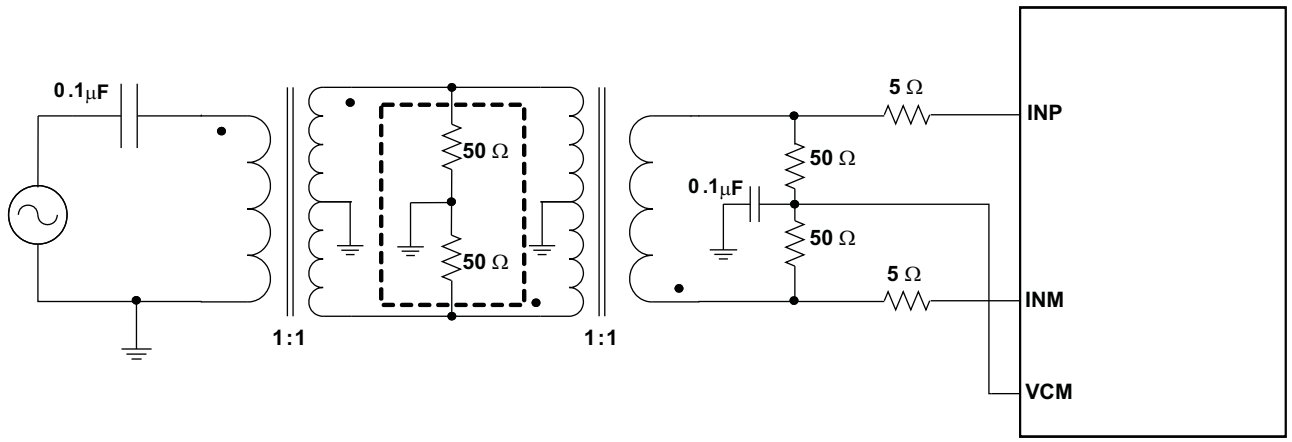

Figure 94. Two Transformer Drive Circuit

Using Differential Amplifier Drive Circuits

Figure 95 shows a drive circuit using a differential amplifier (TI's THS4509) to convert a single-ended input to differential output that can be interface to the ADC analog input pins. In addition to the single-ended to differential conversion, the amplifier also provides gain (10 dB in Figure 95). R_{FIL} helps to isolate the amplifier outputs from the switching input of the ADC. Together with C_{FIL} it also forms a low-pass filter that band-limits the noise (and signal) at the ADC input. As the amplifier output is ac-coupled, the common-mode voltage of the ADC input pins is set using two 200 Ω resistors connected to VCM.

The amplifier output can also be dc-coupled. Using the output common-mode control of the THS4509, the ADC input pins can be biased to 1.5 V. In this case, use +4 V and -1 V supplies for the THS4509 so that its output common-mode voltage (1.5 V) is at mid-supply.

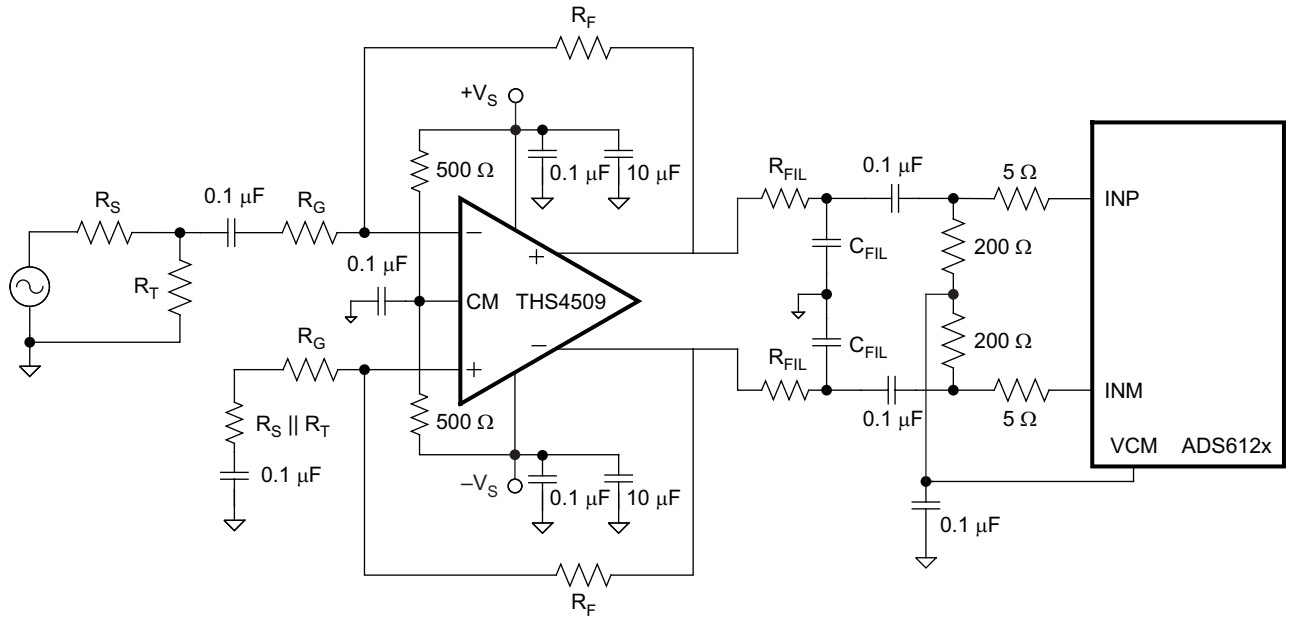

Figure 95. Drive Circuit Using the THS4509

See the EVM User Guide (SLWU028) for more information.

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Input Common-Mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1-µF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. The input stage of the ADC sinks a common-mode current in the order of 180 µA (at 125 MSPS). Equation 1 describes the dependency of the common-mode current and the sampling frequency.

$$180\ \mu A\ x\ \frac{Fs}{125\ MSPS} \quad (1)$$

Equation 1 helps to design the output capability and impedance of the CM driving circuit.

REFERENCE

ADS612X has built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the integration of the requisite reference capacitors on-chip eliminates the need for external decoupling. The full-scale input range of the converter is controlled in the external reference mode as explained below. The internal or external reference modes can be selected by programming the serial interface register bit **<REF>** (seeTable 5).

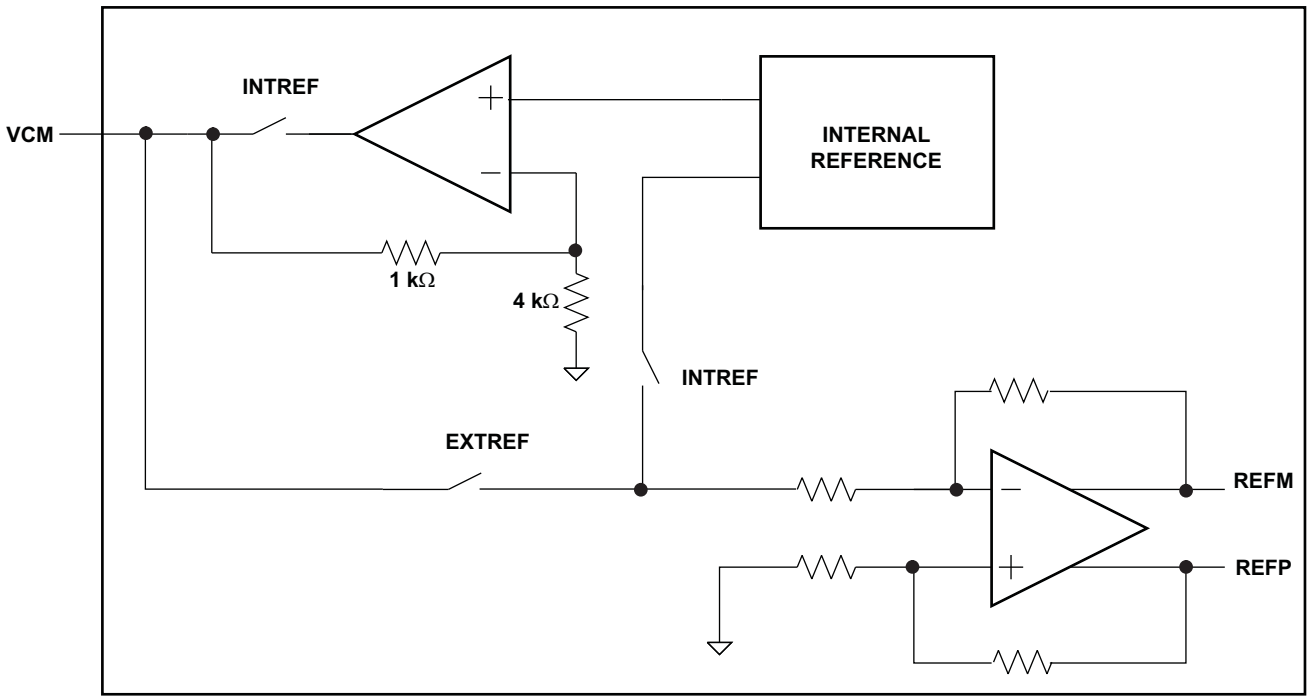

Figure 96. Reference Section

Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5 V nominal) is output on VCM pin, which can be used to externally bias the analog input pins.

External Reference

When the device is in external reference mode, the VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by Equation 2.

$$\text{Full–scale differential input pp} = (\text{Voltage forced on VCM}) \times 1.33 \quad (2)$$

In this mode, the 1.5 V common-mode voltage to bias the input pins has to be generated externally. There is no change in performance compared to internal reference mode.

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COARSE GAIN and PROGRAMMABLE FINE GAIN

ADS612X includes gain settings that can be used to get improved SFDR performance (compared to 0 dB gain mode). The gain settings are 3.5 dB coarse gain and programmable fine gain from 0 dB to 6 dB. For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 15.

The coarse gain is a fixed setting of 3.5 dB and is designed to improve SFDR with little degradation in SNR (as seen in Figure 13 and Figure 14). The fine gain is programmable in 1 dB steps from 0 to 6 dB. With fine gain also, SFDR improvement is achieved, but at the expense of SNR (there is about 1 dB SNR degradation for every 1 dB of fine gain).

So, the fine gain can be used to trade-off between SFDR and SNR. The coarse gain makes it possible to get best SFDR but without losing SNR significantly. At high input frequencies, the gains are especially useful as the SFDR improvement is significant with marginal degradation in SINAD. The gains can be programmed using the register bits **<COARSE GAIN>** (see Table 5) and **<FINE GAIN>** (see Table 10). Note that the default gain after reset is 0 dB.

Table 15. Full-Scale Range Across Gains

GAIN, dB	TYPE	FULL-SCALE RANGE, V_{PP}
0	Default after reset	2.00
3.5	Coarse setting (fixed)	1.34
1	Fine gain (programmable)	1.78
2		1.59
3		1.42
4		1.26
5		1.12
6		1.00

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CLOCK INPUT

The clock inputs of the ADS612X can be driven differentially (SINE, LVPECL or LVDS) or single-ended (LVCMOS), with little or no difference in performance between configurations. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors as shown in Figure 97. This allows the use of transformer-coupled drive circuits for sine wave clock, or ac-coupling for LVPECL, LVDS clock sources (Figure 99 and Figure 100).

For best performance, it is recommended to drive the clock inputs differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.1-µF capacitors, as shown in Figure 99. A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 100.

For high input frequency sampling, the use a clock source with very low jitter is recommended. Bandpass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input. Figure 24 shows the performance of the ADC versus clock duty cycle.

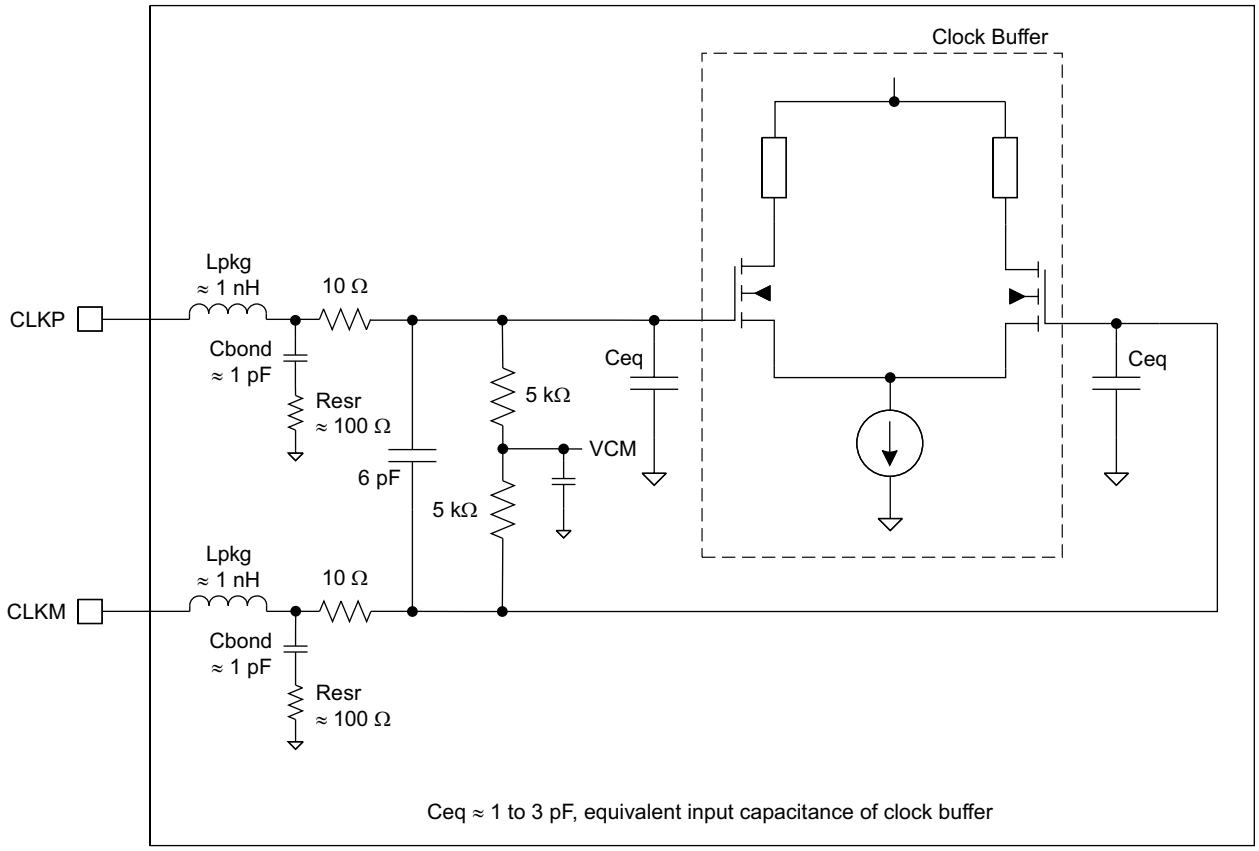

Figure 97. Internal Clock Buffer

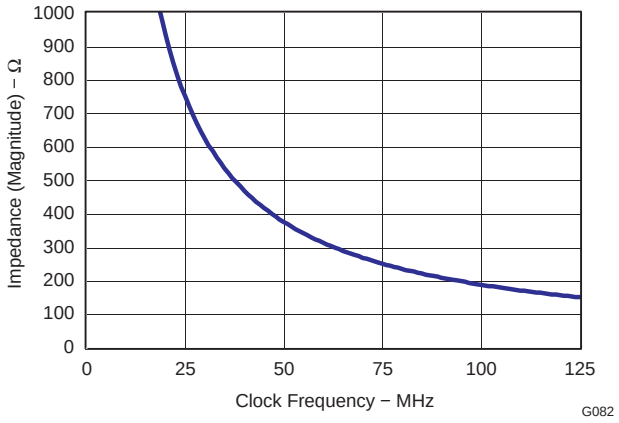

Figure 98. Clock Buffer Input Impedance

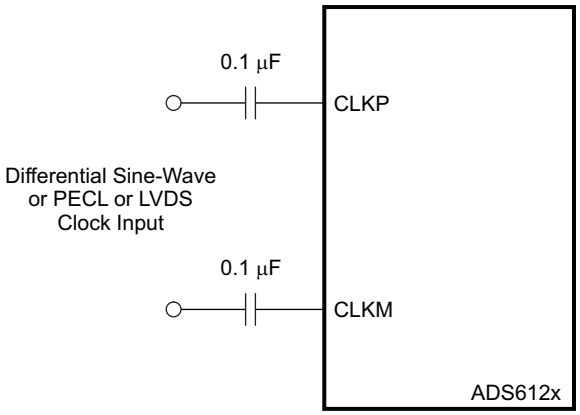

Figure 99. Differential Clock Driving Circuit

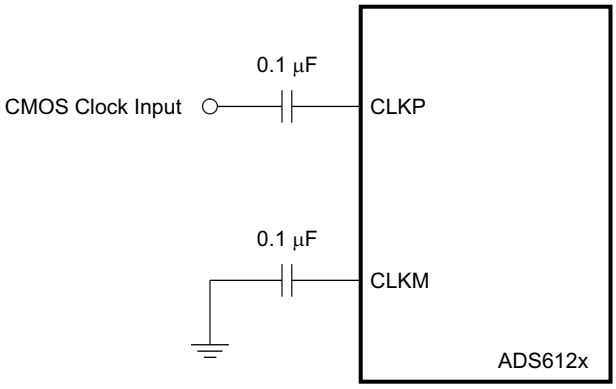

Figure 100. Single-Ended Clock Driving Circuit

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POWER DOWN MODES

ADS612X has four power-down modes – global power down, standby, output buffer disable and input clock stopped. These modes can be set using the serial interface or using the parallel interface (pins SDATA and PDN).

Table 16. Power Down Modes

POWER DOWN MODES	PARALLEL INTERFACE		SERIAL INTERFACE REGISTER BIT (Table 5)	TOTAL POWER, mW	WAKE-UP TIME (to valid data)
	SDATA	PDN			
Normal operation	Low	Low	**<PDN OBUF>**=0 and **<STBY>**=0	417	-
Standby	Low	High	**<PDN OBUF>**=0 and **<STBY>**=1	72	Slow (50 µs)
Output buffer disable	High	Low	**<PDN OBUF>**=1 and **<STBY>**=0	408	Fast (200 ns)
Global power down	High	High	**<PDN OBUF>**=1 and **<STBY>**=1	30	Slow (50 µs)

Global Powerdown

In this mode, the A/D converter, internal references and the output buffers are powered down and the total power dissipation reduces to about 30 mW. The output buffers are in high impedance state. The wake-up time from the global power down to output data becoming valid in the normal mode is maximum 50 µs. Note that after coming out of global power down, optimum performance will be achieved after the internal reference voltages have stabilized (about 1 ms).

Standby

Here, only the A/D converter is powered down and the total power dissipation is about 72 mW. The wake-up time from standby to output data becoming valid is maximum 50 µs.

Output Buffer Disable

The data output buffers can be disabled, reducing the total power to about 408 mW. With the buffers disabled, the outputs are in high impedance state. The wake-up time from this mode to data becoming valid in normal mode is maximum 500 ns in LVDS mode and 200 ns in CMOS mode.

Input Clock Stop

The converter enters this mode when the input clock frequency falls below 1 MSPS. The power dissipation is about 120 mW, and the wake-up time from this mode to data becoming valid in normal mode is maximum 50 µs.

Power Supply Sequence

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated inside the device. Externally, they can be driven from separate supplies or from a single supply.

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DIGITAL OUTPUT INTERFACE

ADS612X outputs 12 data bits together with an output clock. The output interface are either parallel CMOS or DDR LVDS voltage levels and can be selected using serial register bit **<LVDS CMOS>** or parallel pin SEN.

Parallel CMOS Interface

In the CMOS mode, the output buffer supply (DRVDD) can be operated over a wide range from 1.8 V to 3.3 V (typical). Each data bit is output on separate pin as CMOS voltage level, every clock cycle.

For DRVDD ≥ 2.2 V, it is recommended to use the CMOS output clock (CLKOUT) to latch data in the receiving chip. The rising edge of CLKOUT can be used to latch data in the receiver, even at the highest sampling speed (125 MSPS). It is recommended to minimize the load capacitance seen by data and clock output pins by using short traces to the receiver. Also, match the output data and clock traces to minimize the skew between them.

For DRVDD < 2.2 V, it is recommended to use external clock (for example, input clock delayed to get desired setup/hold times).

Output Clock Position Programmability

There exists an option to shift (delay) the output clock position so that the setup time increases by 400 ps (typical, with respect to the default timings specified). This may be useful if the receiver needs more setup time, especially at high sampling frequencies. This can be programmed using the serial interface register bit **<CLKOUT_POSN>** (see Table 6).

Output Buffer Strength Programmability

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs during the instant of sampling and degrade the SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this, the ADS612X CMOS output buffers are designed with controlled drive strength to get best SNR. The default drive strength also ensures wide data stable window for load capacitances upto 5 pF and DRVDD supply voltage ≥ 2.2 V.

To ensure wide data stable window for load capacitance > 5 pF, there is an option to increase the drive strength using the serial interface (**<DRIVE STRENGTH>**, see Table 12). Note that for DRVDD supply voltage < 2.2 V, it is recommended to use maximum drive strength (for any value of load capacitance).

CMOS Mode Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital current due to CMOS output switching = $C_L \times DRVDD \times (N \times F_{AVG})$

where C_L = load capacitance, $N \times F_{AVG}$ = average number of output bits switching

Figure 84 shows the current with various load capacitances across sampling frequencies at 2 MHz analog input frequency.

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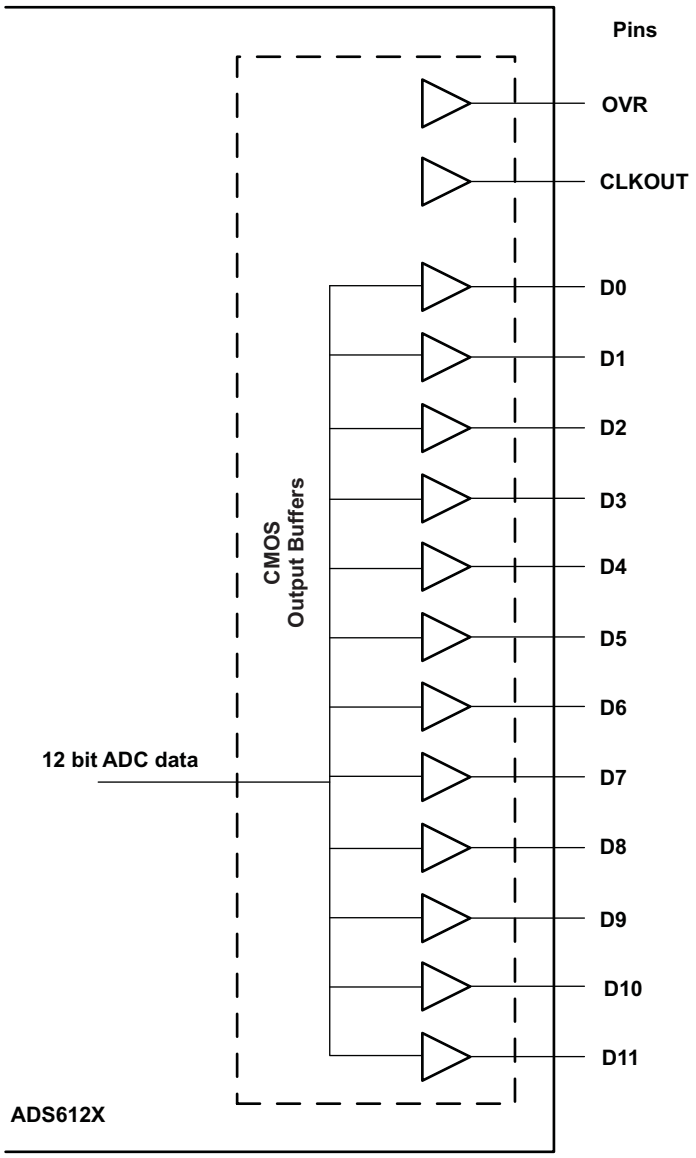

Figure 101. CMOS Output buffers

DDR LVDS Interface

The LVDS interface works only with 3.3 V DRVDD supply. In this mode, the 12 data bits and the output clock are available as LVDS (Low Voltage Differential Signal) levels. Two successive data bits are multiplexed and output on each LVDS differential pair every clock cycle (DDR - Double Data Rate, see Figure 102). So, there are 7 LVDS output pairs for the 12 data bits and 1 LVDS output pair for the output clock.

LVDS Buffer Current Programmability

The default LVDS buffer output current is 3.5 mA. When terminated by 100 Ω, this results in a 350-mV single-ended voltage swing (700-mV_{PP} differential swing). The LVDS buffer currents can also be programmed to 2.5 mA, 4.5 mA, and 1.75 mA (register bits **<LVDS CURRENT>**, see Table 11). In addition, there is a current double mode, where this current is doubled for the data and output clock buffers (register bits **<CURRENT DOUBLE>**, see Table 11).

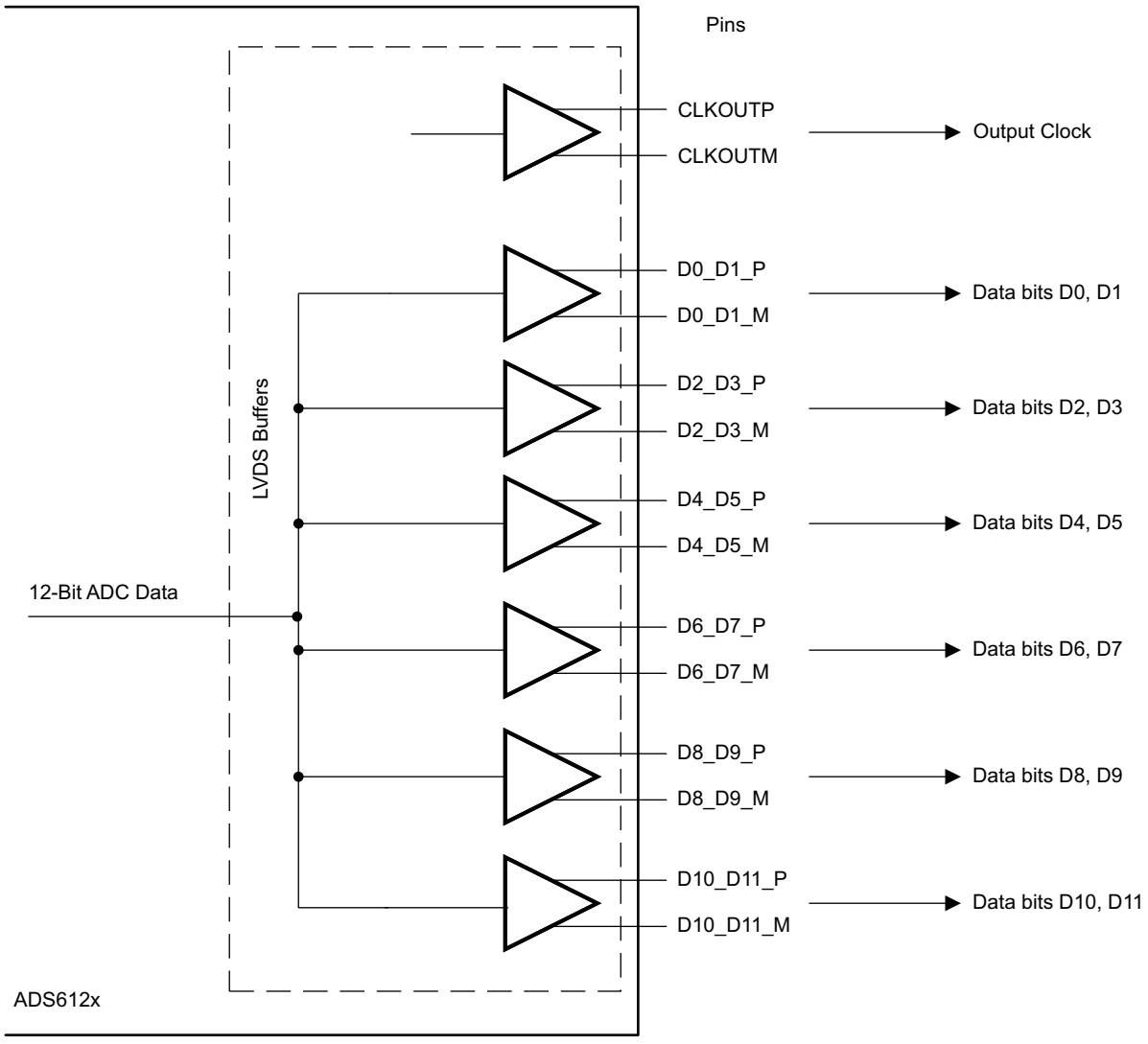

Figure 102. DDR LVDS Outputs

Even data bits D0, D2, D4, D6, D8, D10, and D12 are output at the rising edge of CLKOUTP and the odd data bits D1, D3, D5, D7, D9, D11, and D13 are output at the falling edge of CLKOUTP. Both the rising and falling edges of CLKOUTP must be used to capture all the 12 data bits (see Figure 103).

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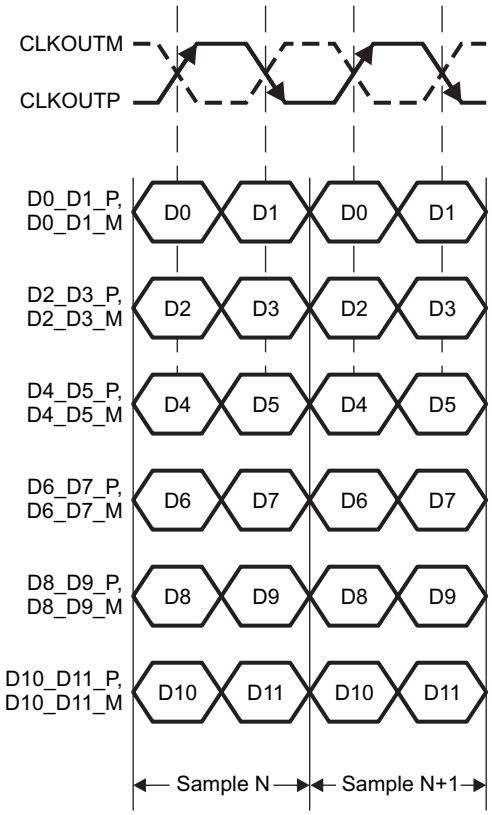

Figure 103. DDR LVDS Interface

LVDS Buffer Internal Termination

An internal termination option is available (using the serial interface), by which the LVDS buffers are differentially terminated inside the device. The termination resistances available are – 300 Ω, 185 Ω, and 150 Ω (nominal with ±20% variation). Any combination of these three terminations can be programmed; the effective termination is the parallel combination of the selected resistances. This results in eight effective terminations from open (no termination) to 65 Ω.

The internal termination helps to absorb any reflections coming from the receiver end, improving the signal integrity. With 100 Ω internal and 100 Ω external termination, the voltage swing at the receiver end is halved (compared to no internal termination). The voltage swing can be restored by using the LVDS current double mode. Figure 104 and Figure 105 compare the LVDS eye diagrams without and with internal termination (100 Ω). With internal termination, the eye looks clean even with 10 pF load capacitance (from each outpin to ground). The terminations is programmed using register bits **<DATA TERM>** and **<CLKOUT TERM>** (see Table 11).

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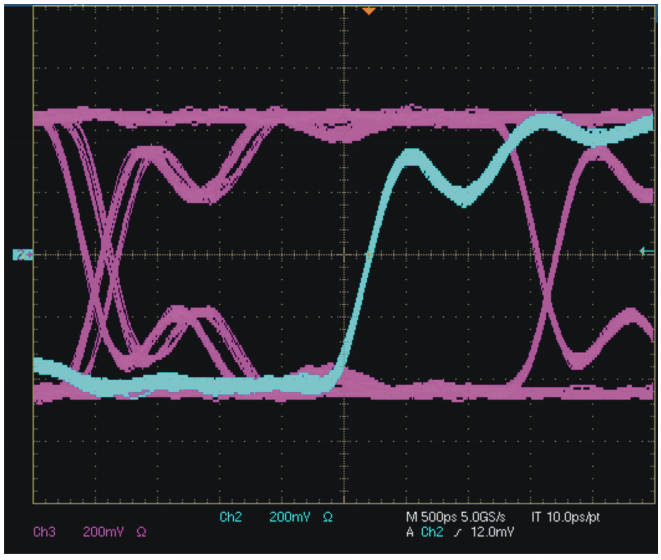

Figure 104. LVDS Eye Diagram - No Internal Termination
5-pF Load Capacitance
Blue Trace - Output Clock (CLKOUT)
Pink Trace - Output Data

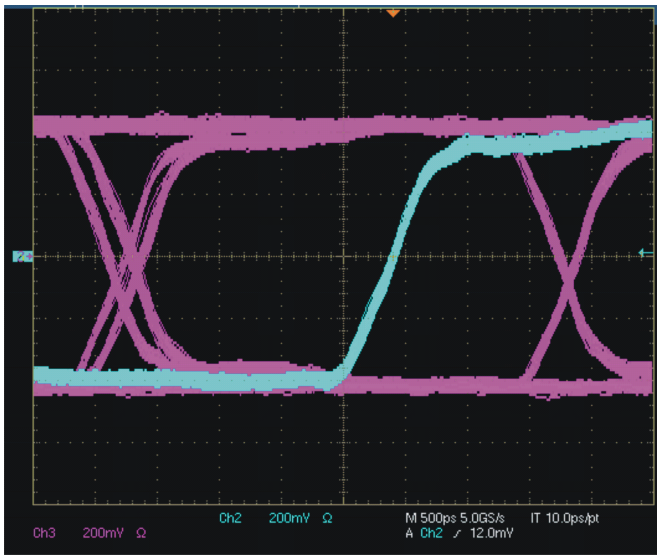

Figure 105. LVDS Eye Diagram with 100-Ω Internal Termination
10-pF Load Capacitance
Blue Trace - Output Clock (CLKOUT)
Pink Trace - Output Data

Output Data Format

Two output data formats are supported – 2s complement and offset binary. They can be selected using the parallel control pin SEN or the serial interface register bit **<DATA FORMAT>** (see Table 8).

Output Timings

The following table lists the timings at lower sampling frequencies.

Table 17. Timing Characteristics at Lower Sampling Frequencies (1)(2)

Fs, MSPS	t_{su} DATA SETUP TIME, ns			t_h DATA HOLD TIME, ns			t_{PDI} CLOCK PROPAGATION DELAY, ns		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
CMOS INTERFACE, DRVDD = 2.5 V to 3.3 V									
40	11.3	12.8		10	11.2		5	6.5	7.9
20	23	25		21	23				
10	48	50		46	48				
DDR LVDS INTERFACE, DRVDD = 3.3 V									
40	10.2	10.8		0.7	1.7		4.3	5.8	7.3
20	22	23		0.7	1.7		4.5	6.5	8.5
10	47	48		0.7	1.7		4.5	6.5	8.5

(1) Timing parameters are specified by design and characterization and not tested in production.
(2) Timings are specified with default output buffer drive strength and C_L= 5 pF

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BOARD DESIGN CONSIDERATIONS

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital and clock sections of the board are cleanly partitioned. See the EVM User Guide (SLWU028) for details on layout and grounding.

Supply Decoupling

As ADS612X already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help to filter external power supply noise, so the optimum number of capacitors would depend on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

It is recommended to use separate supplies for the analog and digital supply pins to isolate digital switching noise from sensitive analog circuitry. In case only a single 3.3-V supply is available, it should be routed first to AVDD. It can then be tapped and isolated with a ferrite bead (or inductor) with decoupling capacitor, before being routed to DRVDD.

Exposed Thermal Pad

It is necessary to solder the exposed pad at the bottom of the package to a ground plane for best thermal performance. For detailed information, see application notes ***QFN Layout Guidelines*** (SLOA122) and ***QFN/SON PCB Attachment*** (SLUA271).

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DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate

The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs

Integral Nonlinearity (INL)

The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error

The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}–T_{MIN}$.

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Signal-to-Noise Ratio

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10}\frac{P_S}{P_N} \quad (4)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10}\frac{P_S}{P_N + P_D} \quad (5)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB)

The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (6)$$

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$THD = 10Log^{10}\frac{P_S}{P_N} \quad (7)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1–f2 or 2f2–f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

DC Power Supply Rejection Ratio (DC PSRR)

The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

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AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR is the measure of rejection of variations in the supply voltage of the ADC. If ΔV_{SUP} is the change in the supply voltage and ΔV_{OUT} is the resultant change in the ADC output code (referred to the input), then

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (8)$$

Common Mode Rejection Ratio (CMRR)

CMRR is the measure of rejection of variations in the input common-mode voltage of the ADC. If ΔVcm is the change in the input common-mode voltage and ΔV_{OUT} is the resultant change in the ADC output code (referred to the input), then

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (9)$$

Voltage Overload Recovery

The number of clock cycles taken to recover to less than 1% error for a 6-dB overload on the analog inputs. A 6-dBFS sine wave at Nyquist frequency is used as the test stimulus.

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REVISION HISTORY

Changes from Original (October 2007) to Revision A	Page
• Changed DDR LVDS output data sequence in Figure 1	11
• Changed pin configuration (CMOS mode) information	21
• Changed pin configuration (LVDS mode) information	23

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS6122IRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6122	Samples
ADS6123IRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6123	Samples
ADS6124IRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ6124	Samples
ADS6124IRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ6124	Samples
ADS6125IRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ6125	Samples
ADS6125IRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ6125	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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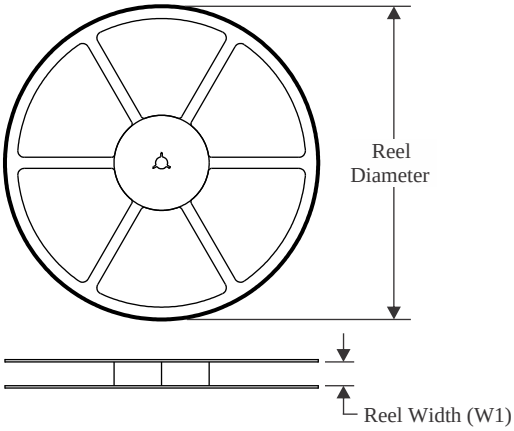
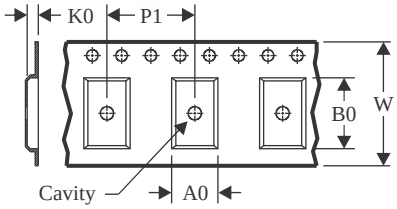
TAPE AND REEL INFORMATION

REEL DIMENSIONS

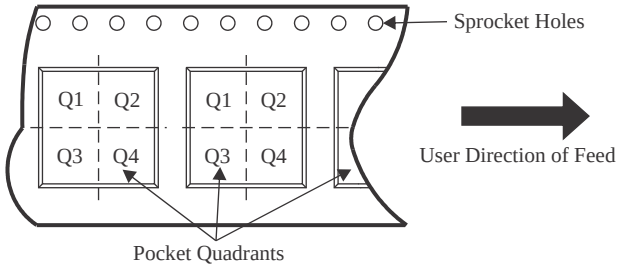


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

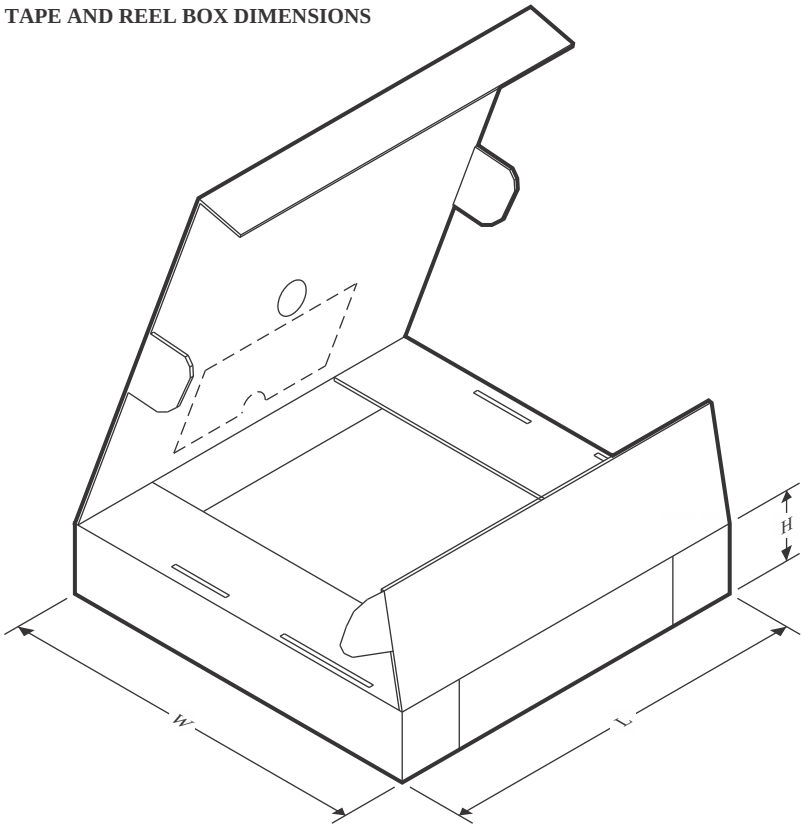
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS6124IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS6125IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS6124IRHBR	VQFN	RHB	32	3000	350.0	350.0	43.0
ADS6125IRHBR	VQFN	RHB	32	3000	350.0	350.0	43.0

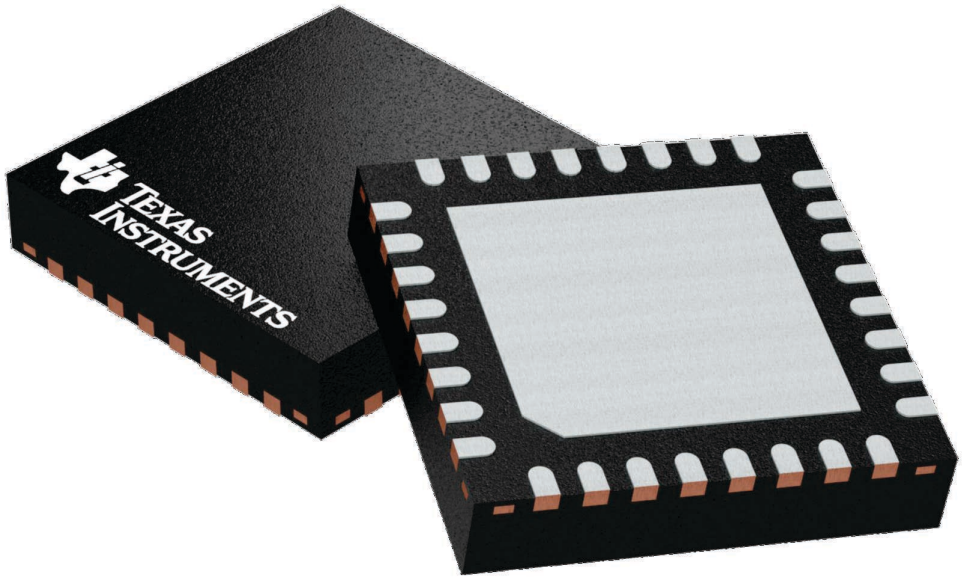
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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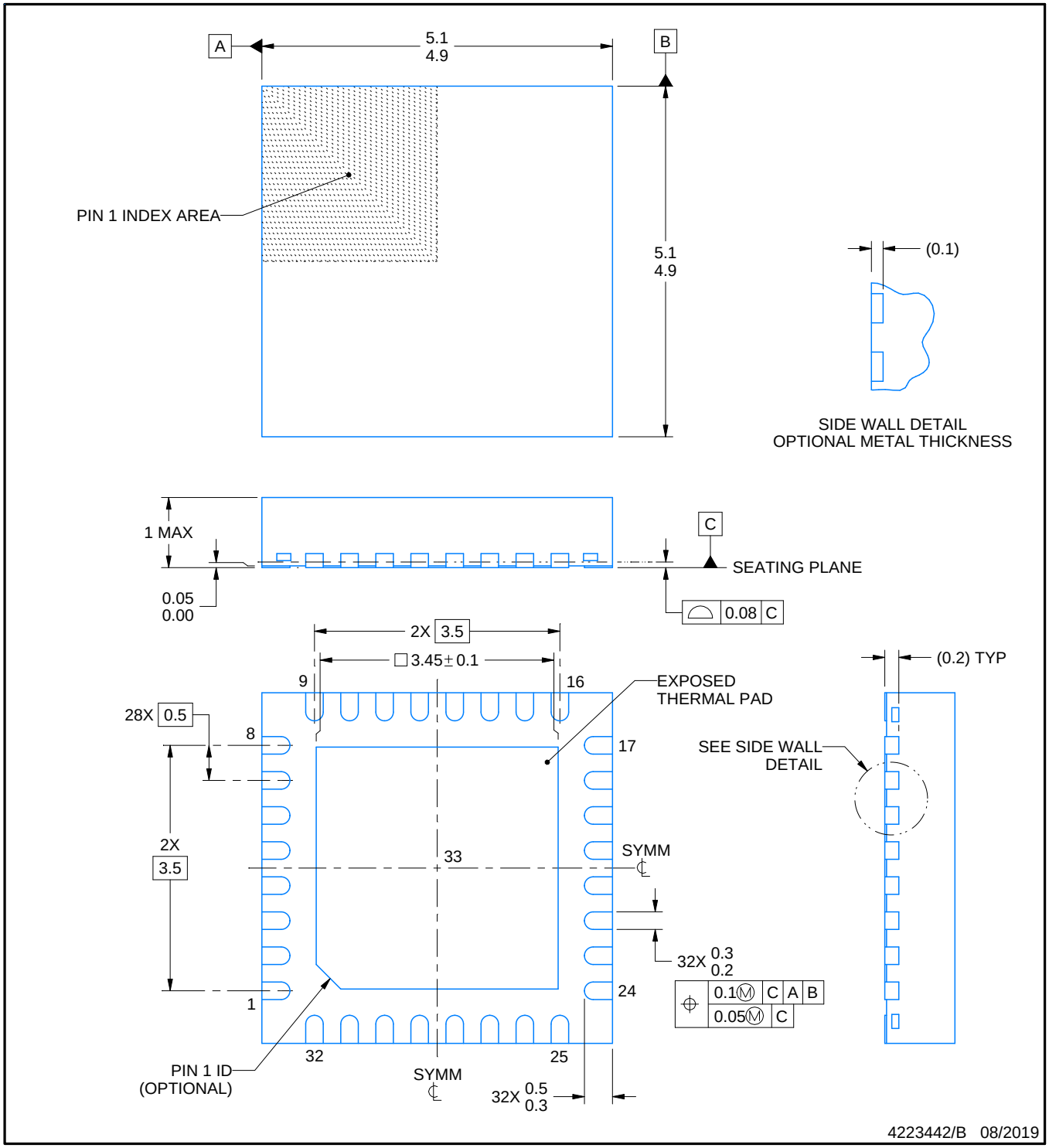
RHB0032E

PACKAGE OUTLINE

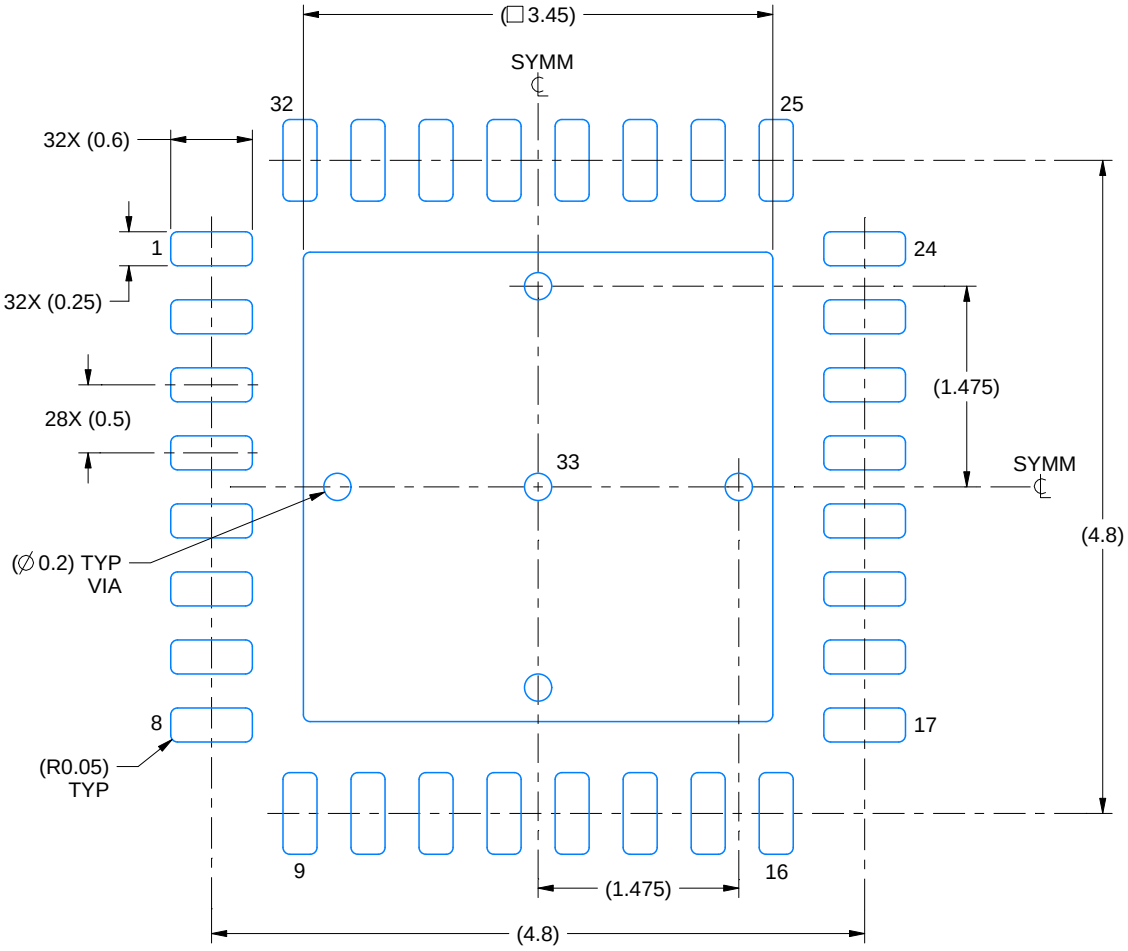
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

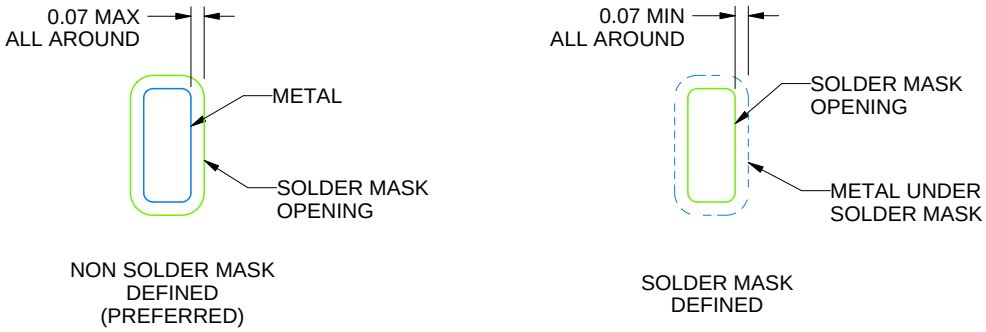


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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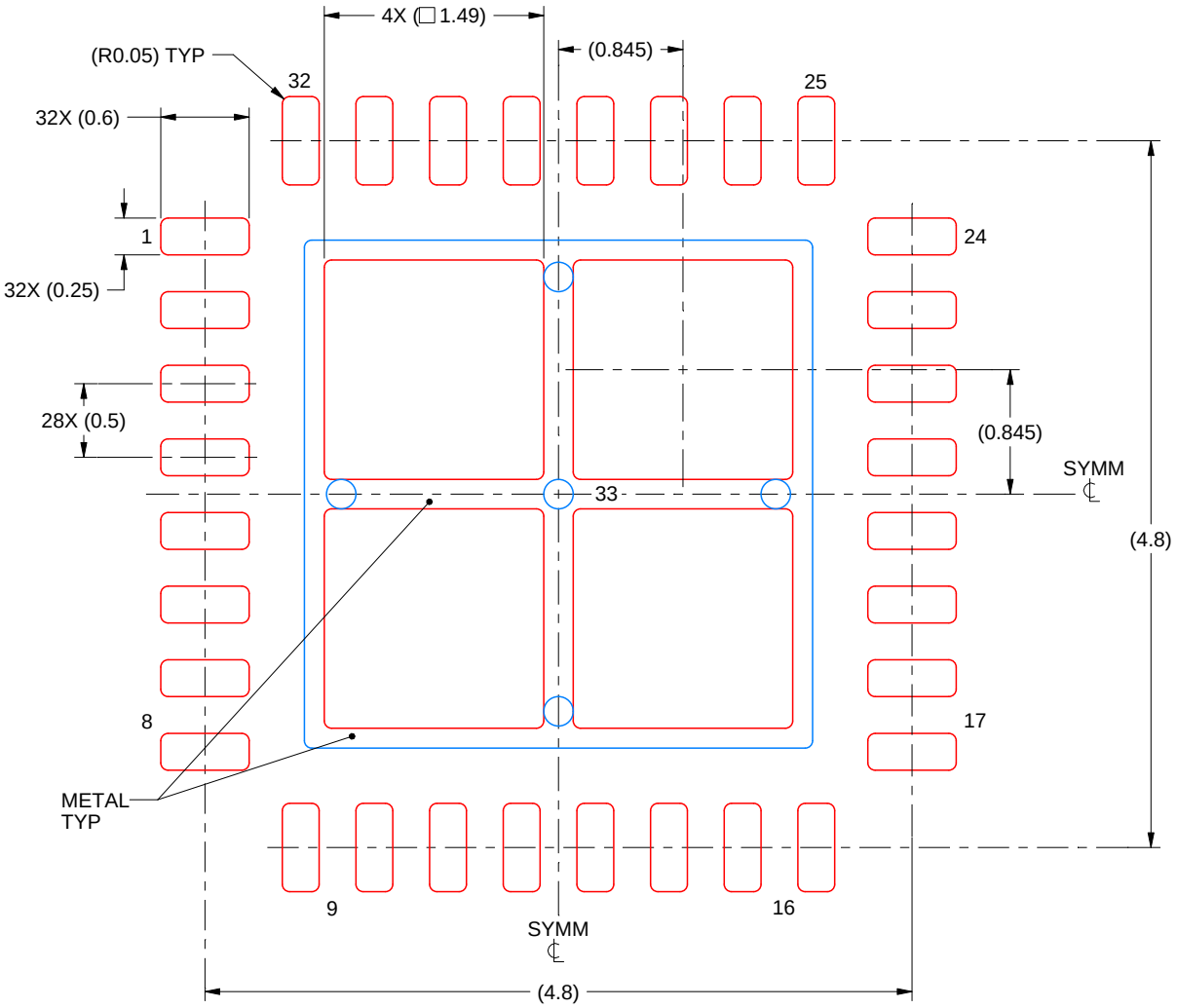
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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