



**THE DATASHEET OF  
74VCX1632245TTR**





# 74VCX1632245

## 16-BIT DUAL SUPPLY BUS TRANSCEIVER LEVEL TRANSLATOR WITH A SIDE SERIES RESISTOR

- HIGH SPEED:  $t_{PD} = 4.4ns$  (MAX.) at  $T_A=85^\circ C$   
 $V_{CCA} = 3.0V$   $V_{CCB} = 2.3V$
- LOW POWER DISSIPATION:  
 $I_{CCA} = I_{CCB} = 20\mu A$ (MAX.) at  $T_A=85^\circ C$
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OHA}| = I_{OLA} = 8mA$  MIN at  
 $V_{CCA} = 3.0V$   $V_{CCB} = 1.65V$  or  $2.3V$   
 $|I_{OHA}| = I_{OLA} = 18mA$  MIN at  
 $V_{CCA} = 2.3V$   $V_{CCB} = 1.65V$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- $26\Omega$  SERIES RESISTOR ON A SIDE OUTPUTS
- OPERATING VOLTAGE RANGE:  
 $V_{CCA}(OPR) = 2.3V$  to  $3.6V$  (1.2V Data Retention)  
 $V_{CCB}(OPR) = 1.65V$  to  $2.7V$  (1.2V Data Retention)
- MAX DATA RATES:  
380 Mbps (1.8V to 3.3V translation)  
260 Mbps (<1.8V to 3.3V translation)  
260 Mbps (Translate to 2.5V)  
210 Mbps (Translate to 1.5V)  
100 Mbps (Translate to 1.2V)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 16245
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE:  
HBM > 2000V (MIL STD 883 method 3015);  
MM > 200V

### DESCRIPTION

The 74VCX1632245 is a dual supply low voltage CMOS 16-BIT BUS TRANSCEIVER fabricated with sub-micron silicon gate and five-layer metal wiring C<sup>2</sup>MOS technology. Designed for use as an interface between a 3.3V bus and a 2.5V or 1.8V bus in a mixed 3.3V/1.8V, 3.3V/2.5V and 2.5V/1.8V supply systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This IC is intended for two-way asynchronous communication between data buses and the direction of data transmission is determined by nDIR inputs. The enable inputs nG can be used to disable the device so that the buses are effectively

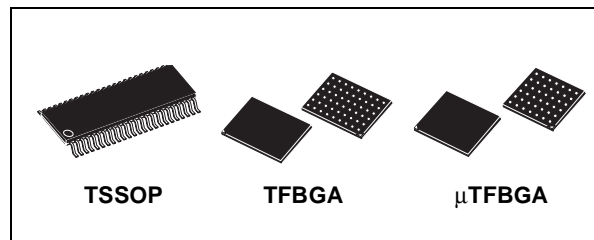


Table 1: Order Codes

PACKAGE	T & R
TSSOP48	74VCX1632245TTR
TFBGA54	74VCX1632245LBR
μTFBGA42	74VCX1632245TBR

isolated. The A-port interfaces with the 3V bus, the B-port with the 2.5V and 1.8V bus.

All inputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage. All floating bus terminals during High Z State must be held HIGH or LOW.

Figure 1: Logic Diagram

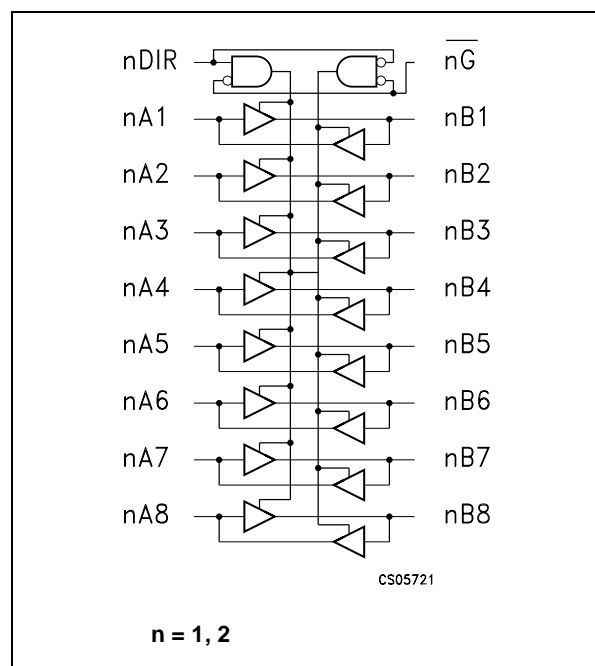


Figure 2: Input And Output Equivalent Circuit

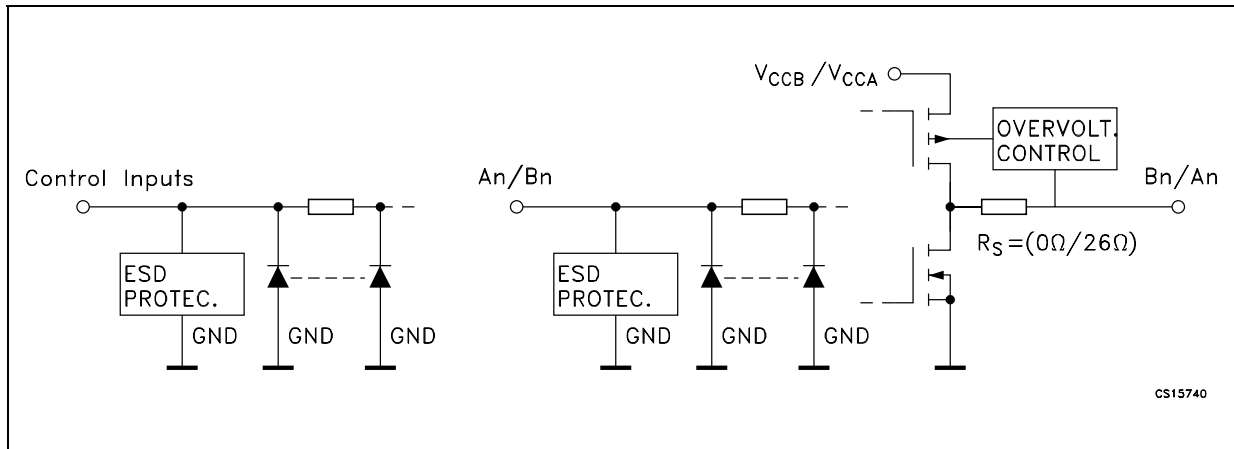


Table 2: Pin Description

TFBGA54 PIN°	μTFBGA42 PIN N°	TSSOP PIN N°	SYMBOL	NAME AND FUNCTION
A3	B3	1	1DIR	Directional Controls
J3	F3	24	2DIR	Directional Controls
A6, B5, B6, C5, C6, D5, D6, E5	A4, A5, A6, B5, B6, C5, C6, D5	47, 46, 44, 43, 41, 40, 38, 37	1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7, 1A8	Data Inputs/Outputs
E6, F5, F6, G5, G6, H5, H6, J6	D6, E5, E6, F5, F6, G4, G5, G6	36, 35, 33, 32, 30, 29, 27, 26	2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7, 2A8	Data Inputs/Outputs
A1, B2, B1, C2, C1, D2, D1, E2	A3, A2, A1, B2, B1, C2, C1, D2	2, 3, 5, 6, 8, 9, 11, 12	1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7, 1B8	Data Inputs/Outputs
E1, F2, F1, G2, G1, H2, H1, J1	D1, E2, E1, F2, F1, G3, G2, G1	13, 14, 16, 17, 19, 20, 22, 23	2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7, 2B8	Data Inputs/Outputs
J4	F4	25	G2	Output Enable Inputs
A4	B4	48	G1	Output Enable Inputs
D3, D4, E3, E4, F3, F4	C3, C4, E3, E4	4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
A2, A5, B3, B4, H3, H4, J2, J5	-	-	NC	No Connected
C4, G4	D4	42, 31	VCCA	Positive Supply Voltage
C3, G3	D3	7, 18	VCCB	Positive Supply Voltage

Figure 3: Pin Connection (top view for TSSOP, top through view for BGA)

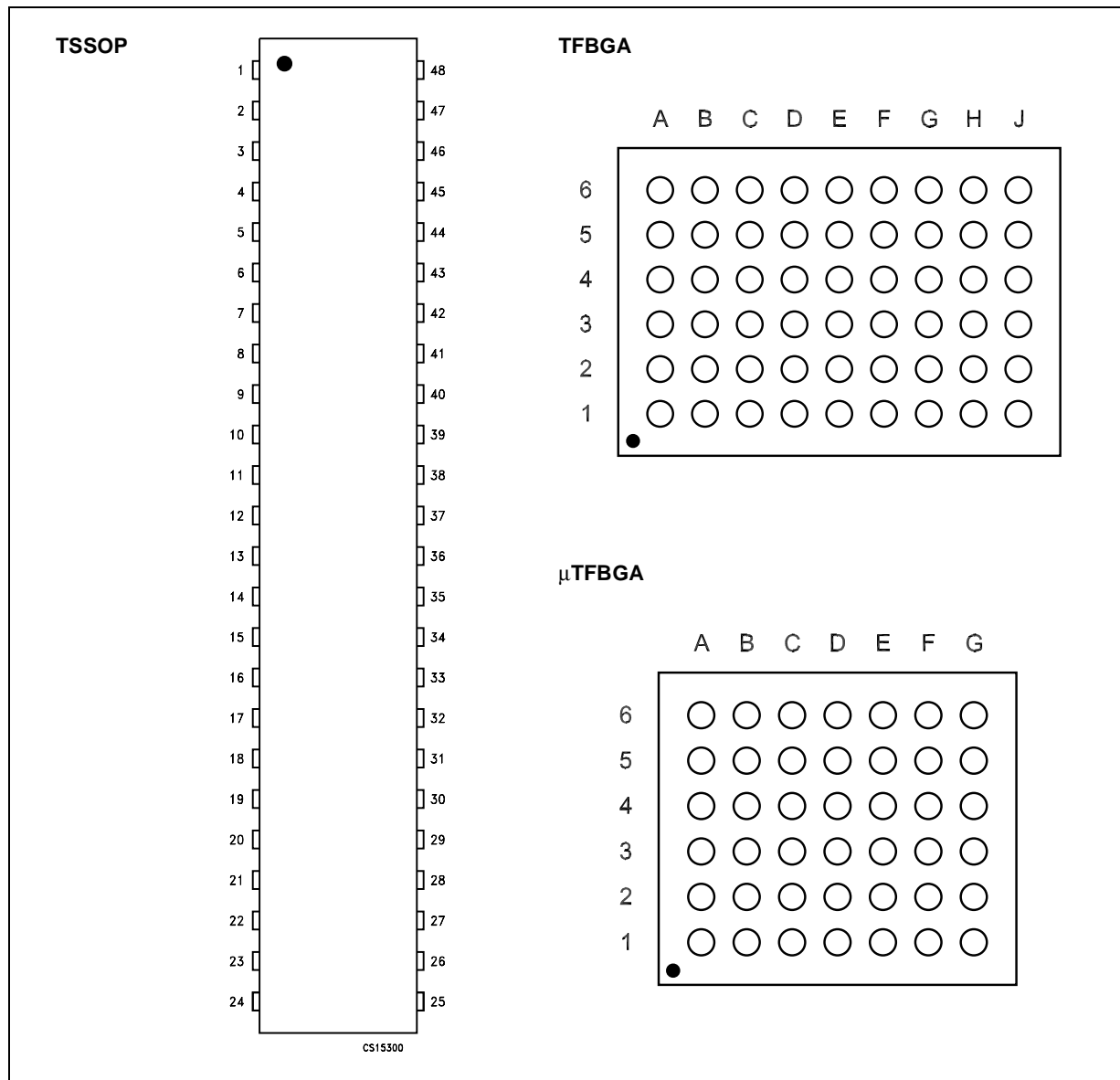


Table 3: Truth Table

INPUTS		FUNCTION		OUTPUT
$\overline{G}$	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	Z	Z	Z

X=Don't care; Z=High Impedance

**Table 4: Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$V_{CCA}$	Supply Voltage	-0.5 to +4.6	V
$V_{CCB}$	Supply Voltage	-0.5 to +4.6	V
$V_I$	DC Input Voltage	-0.5 to +4.6	V
$V_{I/OA}$	DC I/O Voltage (Output disabled)	-0.5 to +4.6	V
$V_{I/OB}$	DC I/O Voltage (Output disabled)	-0.5 to +4.6	V
$V_{I/OA}$	DC I/O Voltage	-0.5 to $V_{CCA} + 0.5$	V
$V_{I/OB}$	DC I/O Voltage	-0.5 to $V_{CCB} + 0.5$	V
$I_{IK}$	DC Input Diode Current	- 20	mA
$I_{OK}$	DC Output Diode Current	- 50	mA
$I_{OA}$	DC Output Current	$\pm 50$	mA
$I_{OB}$	DC Output Current	$\pm 50$	mA
$I_{CCA}$	DC $V_{CC}$ or Ground Current	$\pm 100$	mA
$I_{CCB}$	DC $V_{CC}$ or Ground Current	$\pm 100$	mA
$P_d$	Power Dissipation	400	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	260	°C

Absolute Maximum Ratings are those value beyond which damage to the device may occur. Functional operation under these conditions is not implied

**Table 5: Recommended Operating Conditions**

Symbol	Parameter	Value	Unit
$V_{CCA}$	Supply Voltage	2.3 to 3.6	V
$V_{CCB}$	Supply Voltage	1.65 to $V_{CCA}$	V
$V_I$	Input Voltage (Dir, $\bar{G}$ )	0 to $V_{CCB}$	V
$V_{I/OA}$	I/O Voltage	0 to $V_{CCA}$	V
$V_{I/OB}$	I/O Voltage	0 to $V_{CCB}$	V
$T_{op}$	Operating Temperature	-40 to 85	°C
dt/dv	Input Rise and Fall Time (note 1)	0 to 10	ns/V

1)  $V_I$  from 0.8V to 2.0V at  $V_{CC} = 3.0V$

Table 6: DC Specification For  $V_{CCA}$ 

Symbol	Parameter	Test Condition			Value					Unit
		$V_{CCB}$ (V)	$V_{CCA}$ (V)		$T_A = 25\text{ }^\circ\text{C}$			$-40\text{ to }85\text{ }^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	
$V_{IHA}$	High Level Input Voltage (An) (*)	1.8	2.5		1.6			1.6		V
		1.8	3.3		2.0			2.0		
		2.5	3.3		2.0			2.0		
$V_{ILA}$	Low Level Input Voltage (An) (*)	1.8	2.5				0.7		0.7	V
		1.8	3.3				0.8		0.8	
		2.5	3.3				0.8		0.8	
$V_{OHA}$	High Level Output Voltage	2.3	3.0	$I_O = -100\mu\text{A}$	2.8			2.8		V
		2.3	3.0	$I_O = -8\text{mA}$	2.4			2.4		
		1.65	3.0	$I_O = -8\text{mA}$	2.4			2.4		
		1.65	2.3	$I_O = -6\text{mA}$	1.8			1.8		
$V_{OLA}$	Low Level Output Voltage	2.3	3.0	$I_O = 100\mu\text{A}$			0.2		0.2	V
		2.3	3.0	$I_O = 8\text{mA}$			0.55		0.55	
		1.65	3.0	$I_O = 8\text{mA}$			0.55		0.55	
		1.65	2.3	$I_O = 6\text{mA}$			0.40		0.40	
$I_{IA}$	Input Leakage Current	2.7	3.6	$V_I = V_{CC}$ or GND			$\pm 0.5$		$\pm 5$	$\mu\text{A}$
$I_{OZA}$	High Impedance Output Leakage Current	2.7	3.6	$V_{IA} = \text{GND}$ or 3.6V $V_{IB} = V_{IHB}$ or $V_{ILB}$ $\bar{G} = V_{CCB}$			$\pm 1.0$		$\pm 10$	$\mu\text{A}$
$I_{OFF}$	Power Off Leakage Current	0	0	$V_{IA} = \text{GND}$ to 3.6V $V_{IB} = \text{GND}$ to 3.6V $\bar{G}$ , Dir = GND to 3.6V			$\pm 1.0$		$\pm 10$	$\mu\text{A}$
$I_{CCTA}$	Quiescent Supply Current	1.95	3.6	$V_{IA} = V_{CCA}$ or GND $V_{IB} = V_{CCB}$ or GND			2		20	$\mu\text{A}$
		1.95	2.7							
		2.7	3.6							
$\Delta I_{CCTA}$	Maximum Quiescent Supply Current / Input (An)	2.7	3.6	$V_{IA} = V_{CCA} - 0.6\text{V}$ $V_{IB} = V_{CCB}$ or GND					0.75	mA
		1.95	3.6							
		1.95	2.7							

(\*)  $V_{CC}$  range =  $3.3 \pm 0.3$ ;  $2.5 \pm 0.2\text{V}$ ;  $1.8 \pm 0.15\text{V}$

Table 7: DC Specification For  $V_{CCB}$ 

Symbol	Parameter	Test Condition			Value					Unit
		$V_{CCB}$ (V)	$V_{CCA}$ (V)		$T_A = 25\text{ }^\circ\text{C}$			$-40\text{ to }85\text{ }^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	
$V_{IHB}$	High Level Input Voltage (Bn, Dir, $\overline{G}$ ) (*)	1.8	2.5		0.65 $V_{CCB}$			0.65 $V_{CCB}$		V
		1.8	3.3		0.65 $V_{CCB}$			0.65 $V_{CCB}$		
		2.5	3.3		1.6			1.6		
$V_{ILB}$	Low Level Input Voltage (Bn, Dir, $\overline{G}$ ) (*)	1.8	2.5				0.35 $V_{CCB}$		0.35 $V_{CCB}$	V
		1.8	3.3				0.35 $V_{CCB}$		0.35 $V_{CCB}$	
		2.5	3.3				0.7		0.7	
$V_{OHB}$	High Level Output Voltage	2.3	3.0	$I_O = -100\mu\text{A}$	2.1			2.1		V
		2.3	3.0	$I_O = -18\text{mA}$	1.7			1.7		
		1.65	3.0	$I_O = -6\text{mA}$	1.25			1.25		
		1.65	2.3	$I_O = -6\text{mA}$	1.25			1.25		
$V_{OLB}$	Low Level Output Voltage	2.3	3.0	$I_O = 100\mu\text{A}$			0.2		0.2	V
		2.3	3.0	$I_O = 18\text{mA}$			0.60		0.60	
		1.65	3.0	$I_O = 6\text{mA}$			0.30		0.30	
		1.65	2.3	$I_O = 6\text{mA}$			0.30		0.30	
$I_{IB}$	Input Leakage Current	2.7	3.6	$V_I = V_{CC}$ or GND			$\pm 0.5$		$\pm 5$	$\mu\text{A}$
$I_{OZB}$	High Impedance Output Leakage Current	2.7	3.6	$V_{IA} = V_{IHA}$ or $V_{ILA}$ $V_{IB} = \text{GND}$ or $2.7\text{V}$ $\overline{G} = V_{CCB}$			$\pm 1.0$		$\pm 10$	$\mu\text{A}$
$I_{CCIB}$	Quiescent Supply Current	1.95	3.6	$V_{IA} = V_{CCA}$ or GND			2		20	$\mu\text{A}$
		1.95	2.7	$V_{IB} = V_{CCB}$ or GND						
		2.7	3.6	Dir or $\overline{G} = V_{CCB}$ or GND						
$\Delta I_{CCIB}$	Maximum Quiescent Supply Current / Input (Bn, DIR, $\overline{G}$ )	2.7	3.6	$V_{IB} = V_{CCB} - 0.6\text{V}$ $V_{IA} = V_{CCA}$ or GND					0.75	mA
		1.95	3.6							
		1.95	2.7							

(\*)  $V_{CC}$  range =  $3.3 \pm 0.3$ ;  $2.5 \pm 0.2\text{V}$ ;  $1.8 \pm 0.15\text{V}$

Table 8: Dynamic Switching Characteristics

Symbol	Parameter	Test Condition			Value					Unit
		V <sub>CCB</sub> (V)	V <sub>CCA</sub> (V)		T <sub>A</sub> = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V <sub>OLPA</sub>	Dynamic Low Level Quiet An Output	1.8	2.5	C <sub>L</sub> = 30pF V <sub>IL</sub> = 0V V <sub>IH</sub> = V <sub>CC</sub>		0.25				V
		1.8	3.3			0.35				
		2.5	3.3			0.35				
V <sub>OLPB</sub>	Dynamic Low Level Quiet Bn Output	1.8	2.5	C <sub>L</sub> = 30pF V <sub>IL</sub> = 0V V <sub>IH</sub> = V <sub>CC</sub>		0.25				V
		1.8	3.3			0.25				
		2.5	3.3			0.6				
V <sub>OLVA</sub>	Dynamic Low Level Quiet An Output	1.8	2.5	C <sub>L</sub> = 30pF V <sub>IL</sub> = 0V V <sub>IH</sub> = V <sub>CC</sub>		-0.25				V
		1.8	3.3			-0.35				
		2.5	3.3			-0.35				
V <sub>OLVB</sub>	Dynamic Low Level Quiet Bn Output	1.8	2.5	C <sub>L</sub> = 30pF V <sub>IL</sub> = 0V V <sub>IH</sub> = V <sub>CC</sub>		-0.25				V
		1.8	3.3			-0.25				
		2.5	3.3			-0.6				
V <sub>OHVA</sub>	Dynamic High Level Quiet An Output	1.8	2.5	C <sub>L</sub> = 30pF V <sub>IL</sub> = 0V V <sub>IH</sub> = V <sub>CC</sub>		2.1				V
		1.8	3.3			2.6				
		2.5	3.3			2.6				
V <sub>OHVB</sub>	Dynamic High Level Quiet Bn Output	1.8	2.5	C <sub>L</sub> = 30pF V <sub>IL</sub> = 0V V <sub>IH</sub> = V <sub>CC</sub>		1.7				V
		1.8	3.3			1.7				
		2.5	3.3			2.0				

Table 9: AC Electrical Characteristics

Symbol	Parameter	Test Condition			Value		Unit
		V <sub>CCB</sub> (V)	V <sub>CCA</sub> (V)		-40 to 85 °C		
					Min.	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time An to Bn	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω	1.0	5.8	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	6.2	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.4	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time Bn to An	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω	1.0	5.5	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	5.1	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.0	
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time G to An	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω	1.0	5.3	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	5.1	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.0	
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time G to Bn	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω	1.0	8.3	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	8.2	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.6	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time G to An	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω	1.0	5.2	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	5.6	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.8	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time G to Bn	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω	1.0	4.6	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	4.5	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.4	
t <sub>OSLH</sub> t <sub>OShL</sub>	Output To Output Skew Time (note1, 2)	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω		0.5	ns
		1.8 ± 0.15	3.3 ± 0.3			0.5	
		2.5 ± 0.2	3.3 ± 0.3			0.75	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|; t<sub>OShL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|)

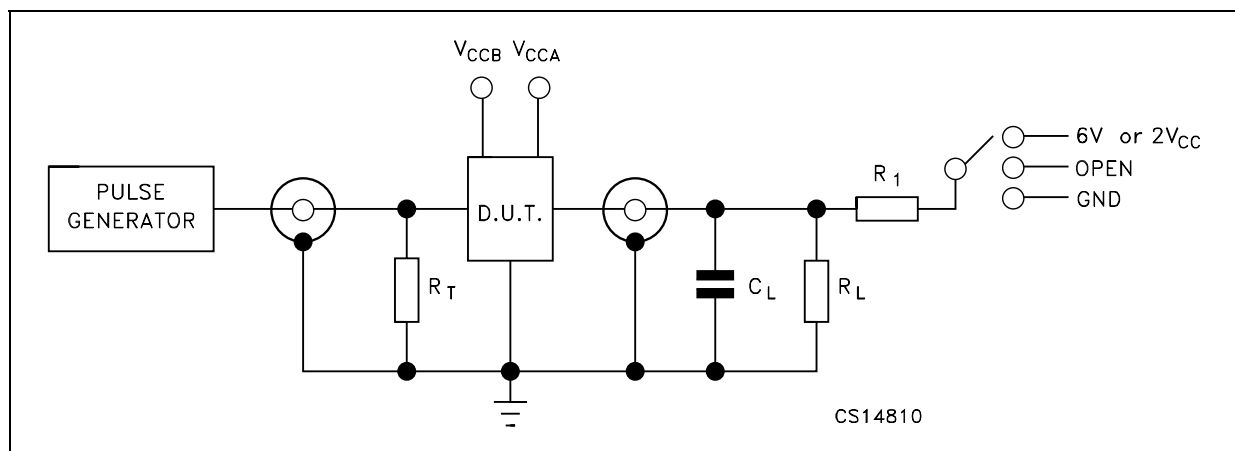
2) Parameter guaranteed by design

Table 10: Capacitance Characteristics

Symbol	Parameter	Test Condition			Value					Unit	
		V <sub>CCB</sub> (V)	V <sub>CCA</sub> (V)		T <sub>A</sub> = 25 °C			-40 to 85 °C			
					Min.	Typ.	Max.	Min.	Max.		
C <sub>INB</sub>	Input Capacitance	open	open			5					pF
C <sub>I/O</sub>	Input/Output Capacitance	2.5	3.3			6					pF
C <sub>PD</sub>	Power Dissipation Capacitance	2.5	3.3	f=10MHz		28					pF
		1.8	3.3			28					pF

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average current can be obtained by the following equation. I<sub>CC(opr)</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> + I<sub>CC</sub>/16 (per circuit)

Figure 4: Test Circuit



TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$ ( $V_{CC} = 3.0$ to $3.6V$ )	6V
$t_{PZL}$ , $t_{PLZ}$ ( $V_{CC} = 2.3$ to $2.7V$ or $V_{CC} = 1.65$ to $1.95V$ )	$2V_{CC}$
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 30pF$  or equivalent (includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

Table 11: Waveform Symbol Value

Symbol	$V_{CC}$		
	3.0 to 3.6V	2.3 to 2.7V	1.65 to 1.95V
$V_{IH}$	$V_{CC}$	$V_{CC}$	$V_{CC}$
$V_M$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_Y$	$V_{OL} - 0.3V$	$V_{OL} - 0.15V$	$V_{OL} - 0.15V$

Figure 5: Waveform - Propagation Delay (f=1MHz; 50% duty cycle)

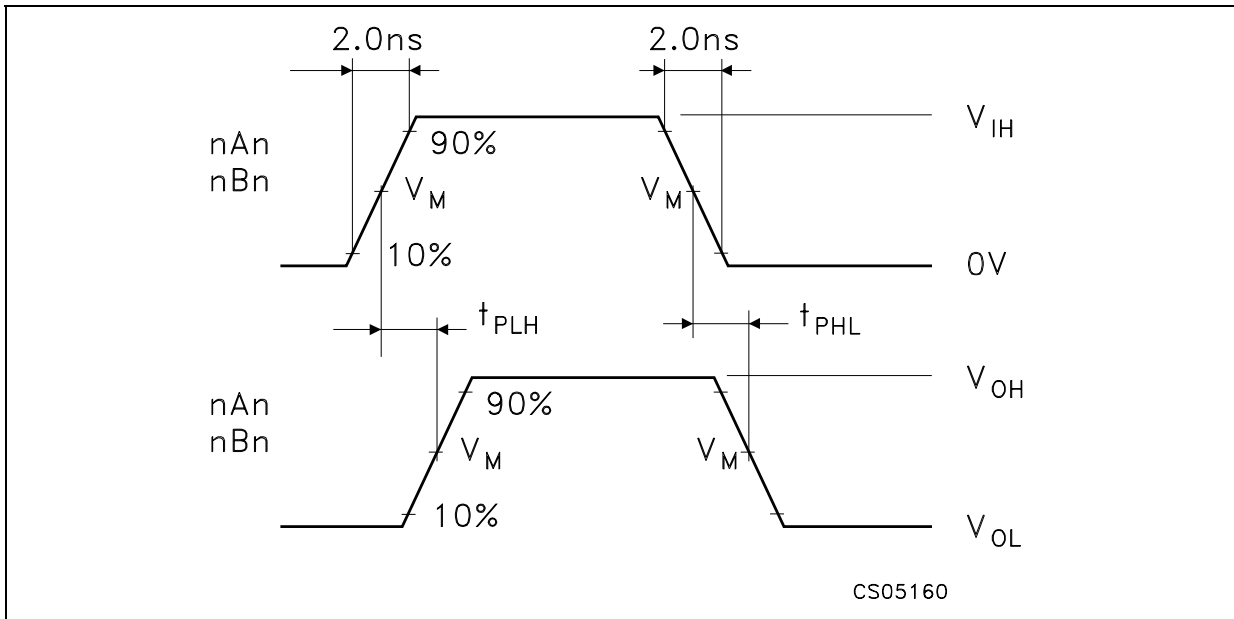
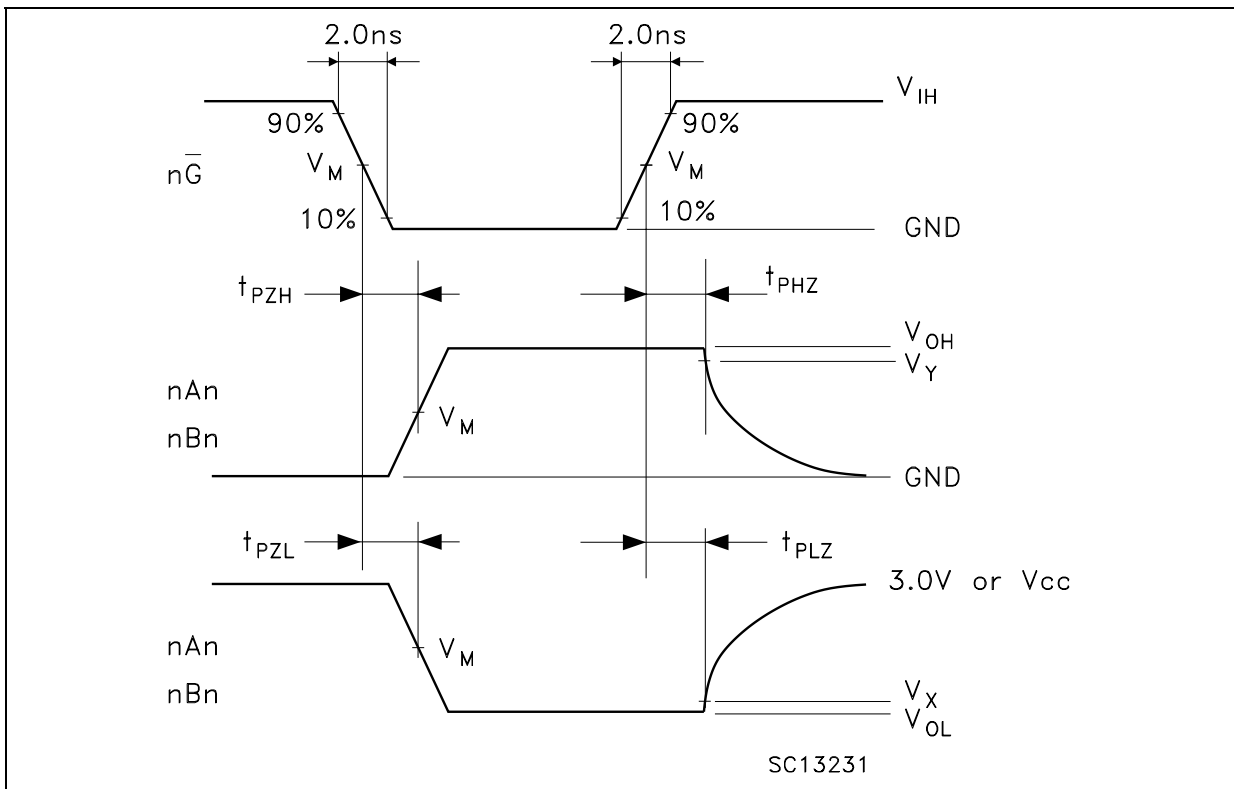
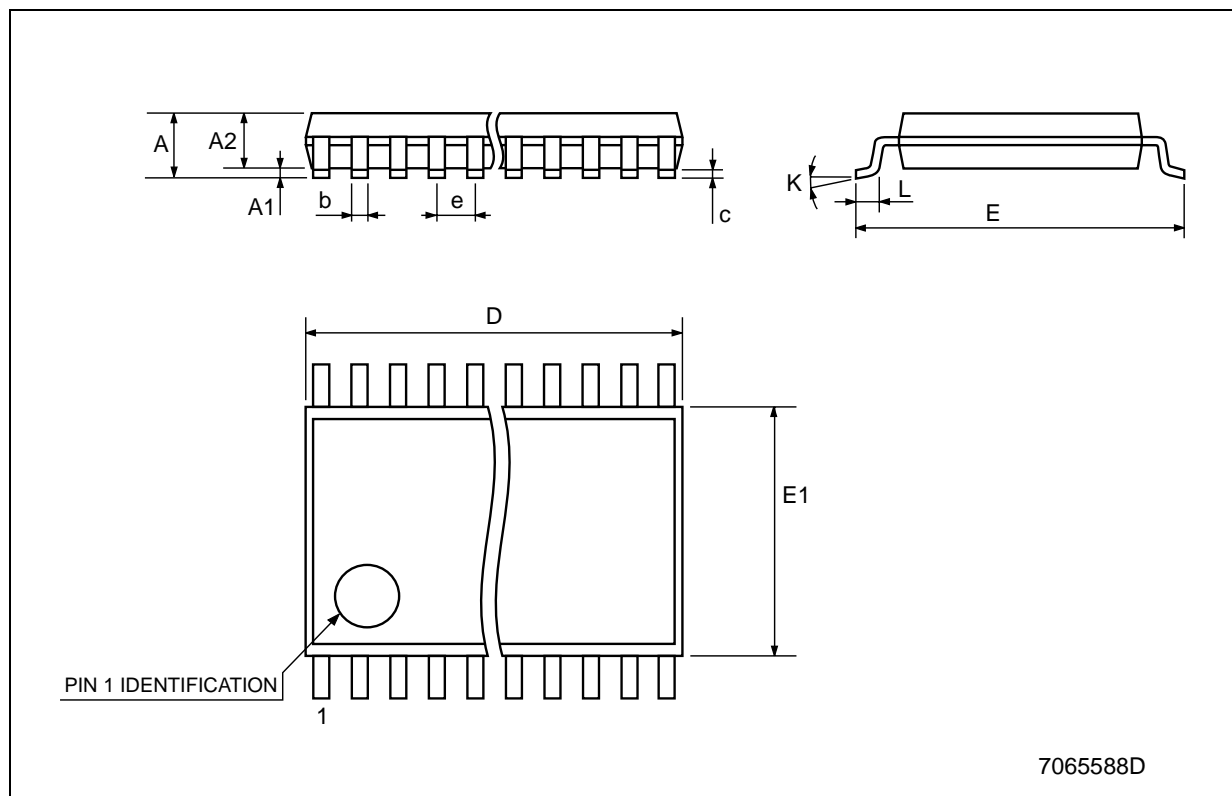


Figure 6: Waveform - Output Enable And Disable Time (f=1MHz; 50% duty cycle)



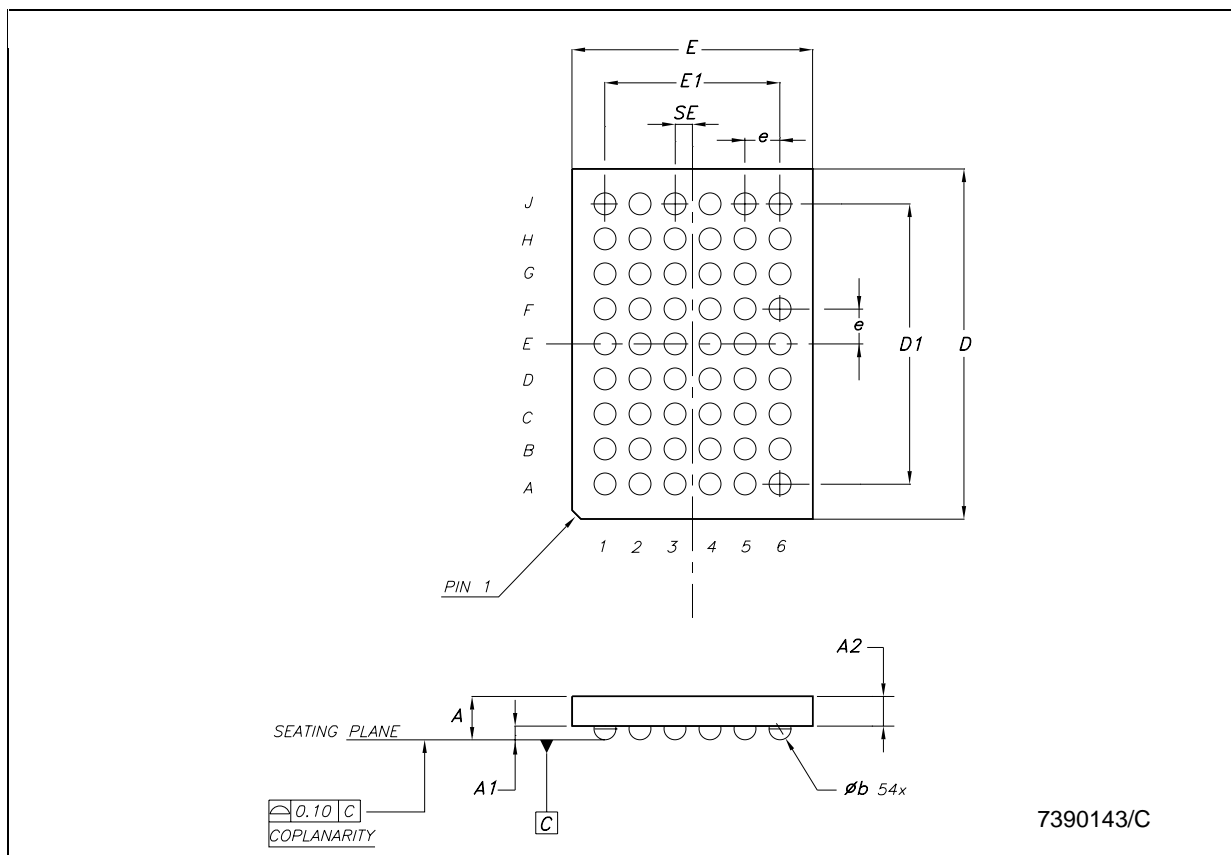
## TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.45		0.75	0.018		0.030



**TFBGA54 MECHANICAL DATA**

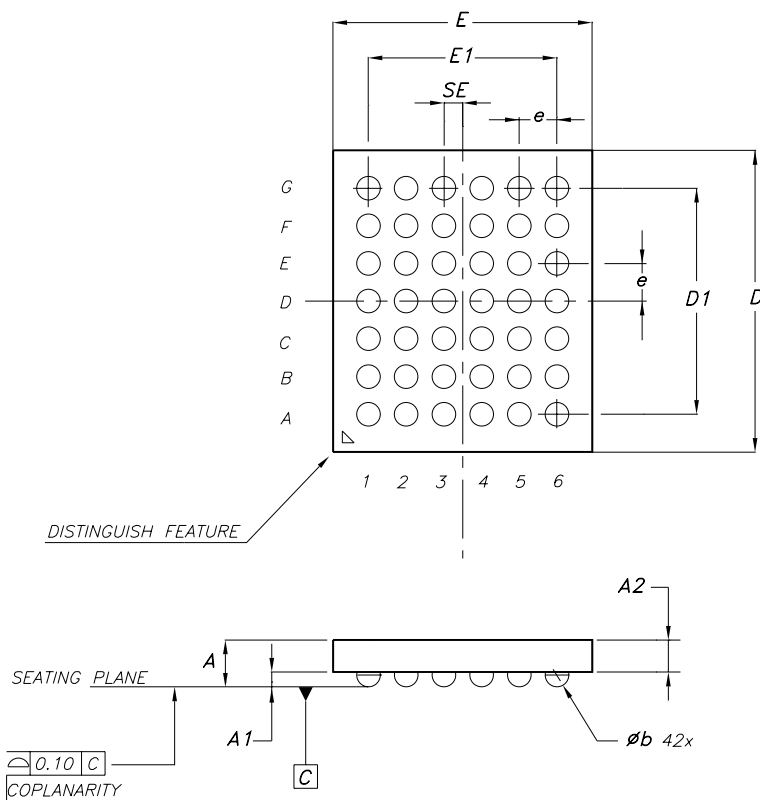
DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			47.2
A1	0.25			9.8		
A2	0.78		0.86	30.7		33.8
B	0.35	0.4	0.45	13.7	15.7	17.7
D	7.9		8.1	311.0		318.9
D1		6.4			252.0	
E	5.4	5.5	5.6	212.6	216.5	220.5
E1		4			157.5	
e		0.8			31.5	
SE		0.4			15.7	



7390143/C

**μTFBGA42 MECHANICAL DATA**

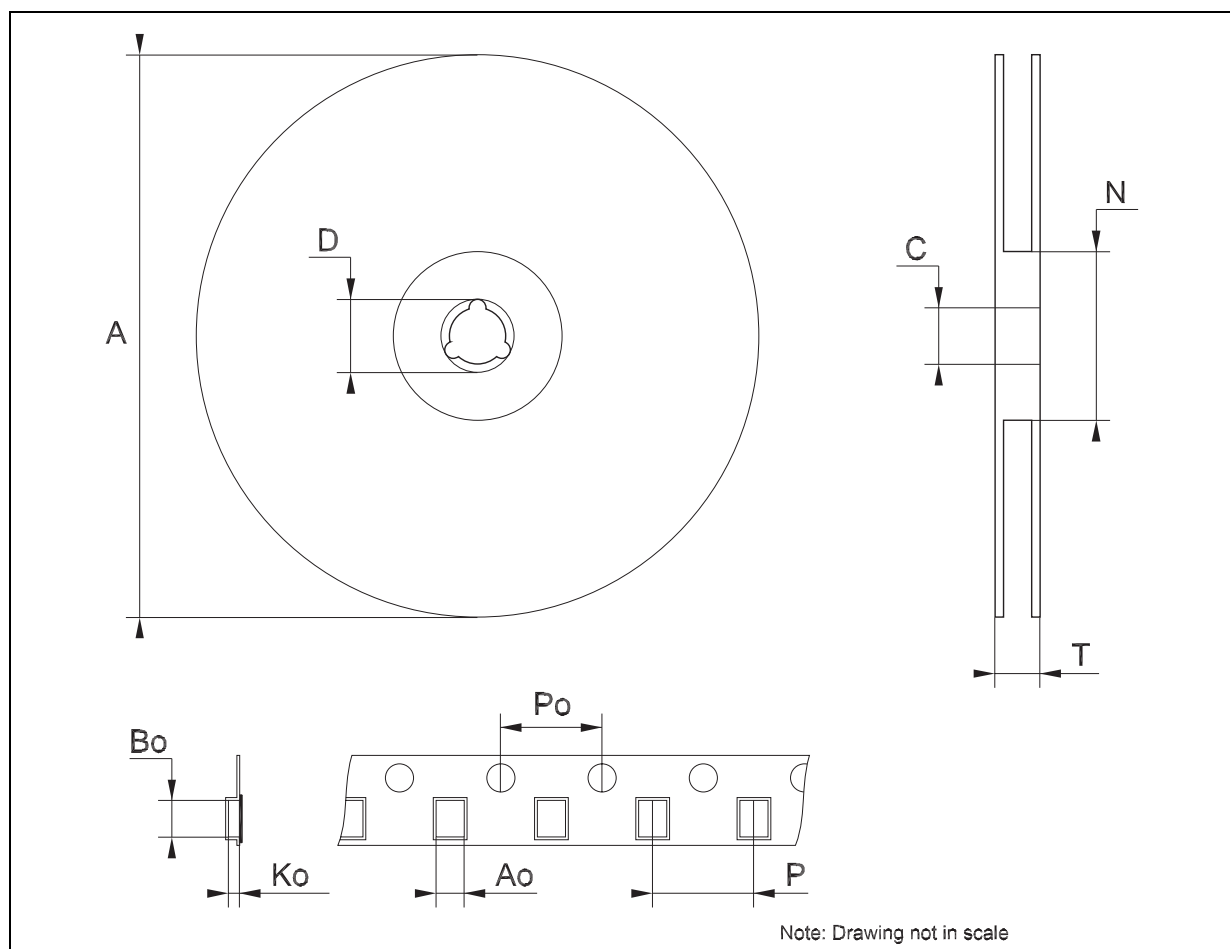
DIM.	mm.			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.0	1.1	1.16	39.4	43.3	45.7
A1			0.25			9.8
A2	0.78		0.86	30.7		33.9
b	0.25	0.30	0.35	9.8	11.8	13.8
D	3.9	4.0	4.1	153.5	157.5	161.4
D1		3			118.1	
E	3.4	3.5	3.6	133.9	137.8	141.7
E1		2.5			98.4	
e		0.5			19.7	
SE		0.25			9.8	



7513237/A

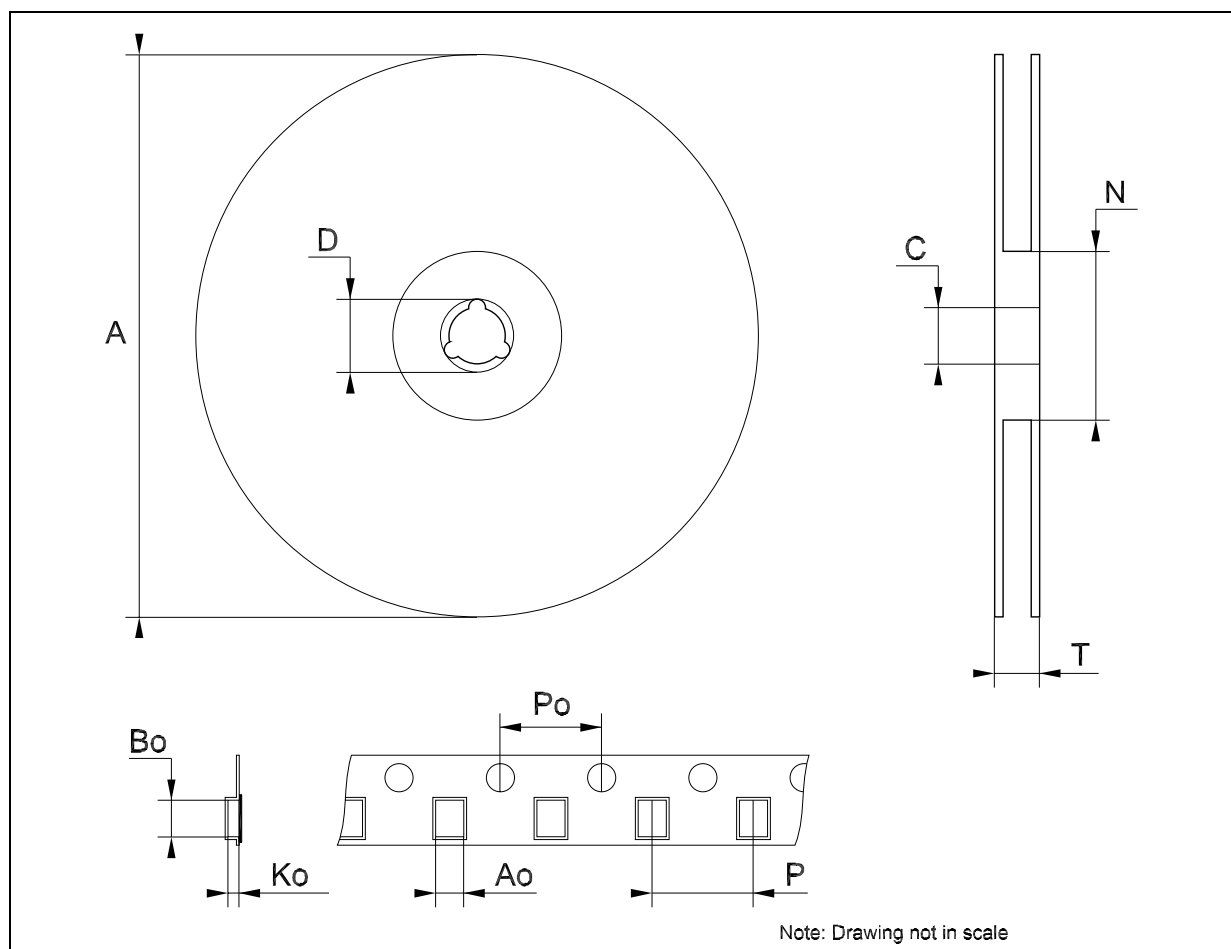
## Tape &amp; Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



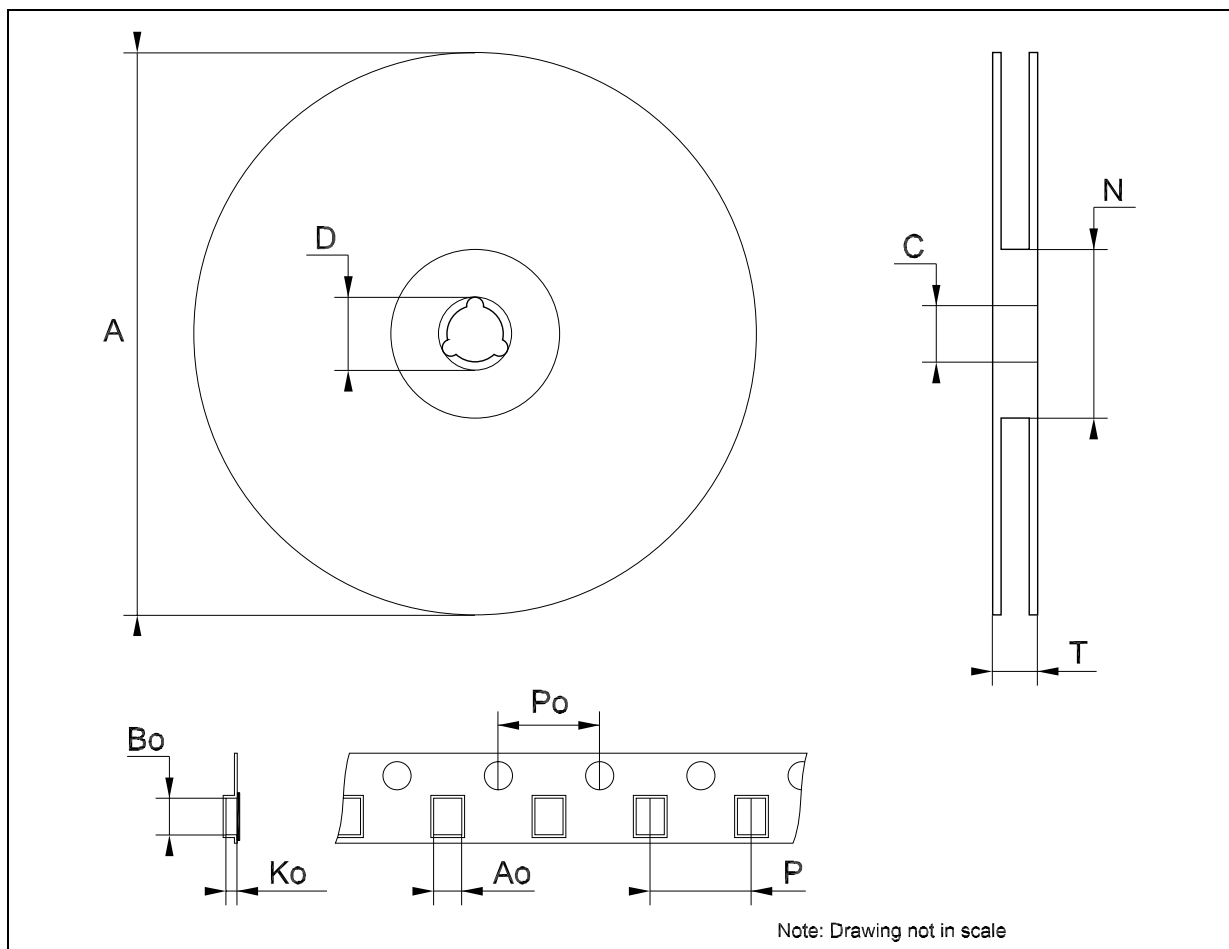
### Tape & Reel TFBGA42 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao		3.8		0.149		
Bo		4.3		0.169		
Ko		1.05		0.041		
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



### Tape & Reel TFBGA54 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao		6.1		0.240		
Bo		8.6		0.339		
Ko		1.8		0.071		
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



**Table 12: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
18-May-2004	12	TFBGA42 Reel Modified on page 15.
01-Sep-2004	13	$T_L$ on table 4 and $V_{CCB}$ on table 5: values changed.
16-Mar-2005	14	Add Features ==> Max Data Rates.

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