THE DATASHEET OF

ISL88731CHRTZ

ISL88731C

SMBus Level 2 Battery Charger

FN6978
Rev 3.00
June 8, 2011

The ISL88731C is a highly integrated Lithium-ion battery charger controller, programmable over the SMBus system management bus (SMBus). The ISL88731C is intended to be used in a smart battery charger (SBC) within a smart battery system (SBS) that throttles the charge power such that the current from the AC-adapter is automatically limited. High efficiency is achieved with a DC/DC synchronous-rectifier buck converter, equipped with diode emulation for enhanced light load efficiency and system bus boosting prevention. The ISL88731C charges one to four Lithium-ion series cells, and delivers up to 8A charge current. Integrated MOSFET drivers and bootstrap diode result in fewer components and smaller implementation area. Low offset current-sense amplifiers provide high accuracy with 10mΩ sense resistors. The ISL88731C provides 0.5% end-of-charge battery voltage accuracy.

The ISL88731C provides a digital output that indicates the presence of the AC adapter as well as an analog output which indicates the adapter current within 4% accuracy.

The ISL88731C is available in a small 5mmx5mm 28 Ld Thin (0.8mm) QFN package. An evaluation kit is available to reduce design time. The ISL88731C is available in Pb-Free packages.

Related Literature

- See AN1404 for "ISL88731EVAL2Z and ISL88731CEVAL2Z Evaluation Boards Setup Procedure"

Features

- 0.5% Battery Voltage Accuracy
- 3% Adapter Current Limit Accuracy
- 3% Charge Current Accuracy
- SMBus 2-Wire Serial Interface
- Battery Short Circuit Protection
- Fast Response for Pulse-Charging
- Fast System-Load Transient Response
- Monitor Outputs
  - Adapter Current (3% Accuracy)
  - AC-Adapter Detection
- 11-Bit Battery Voltage Setting
- 6 Bit Charge Current/Adapter Current Setting
- 8A Maximum Battery Charger Current
- 11A Maximum Adapter Current
- +8V to +26V Adapter Voltage Range
- Pb-Free (RoHS Compliant)

Applications

- Notebook Computers
- Tablet PCs
- Portable Equipment with Rechargeable Batteries

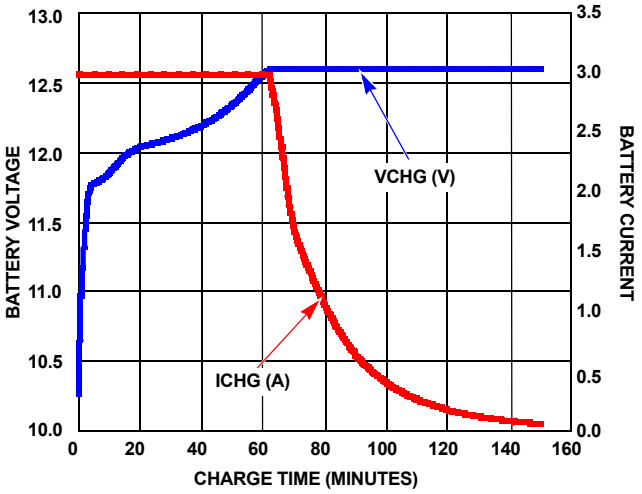


FIGURE 1. TYPICAL CHARGING VOLTAGE AND CURRENT

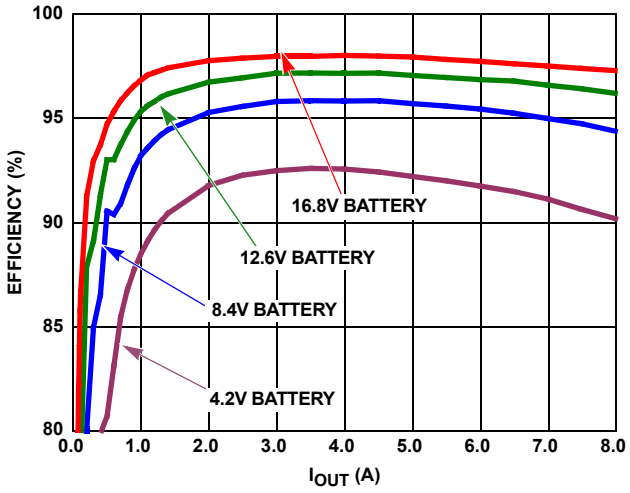


FIGURE 2. EFFICIENCY vs CHARGE CURRENT AND BATTERY VOLTAGE

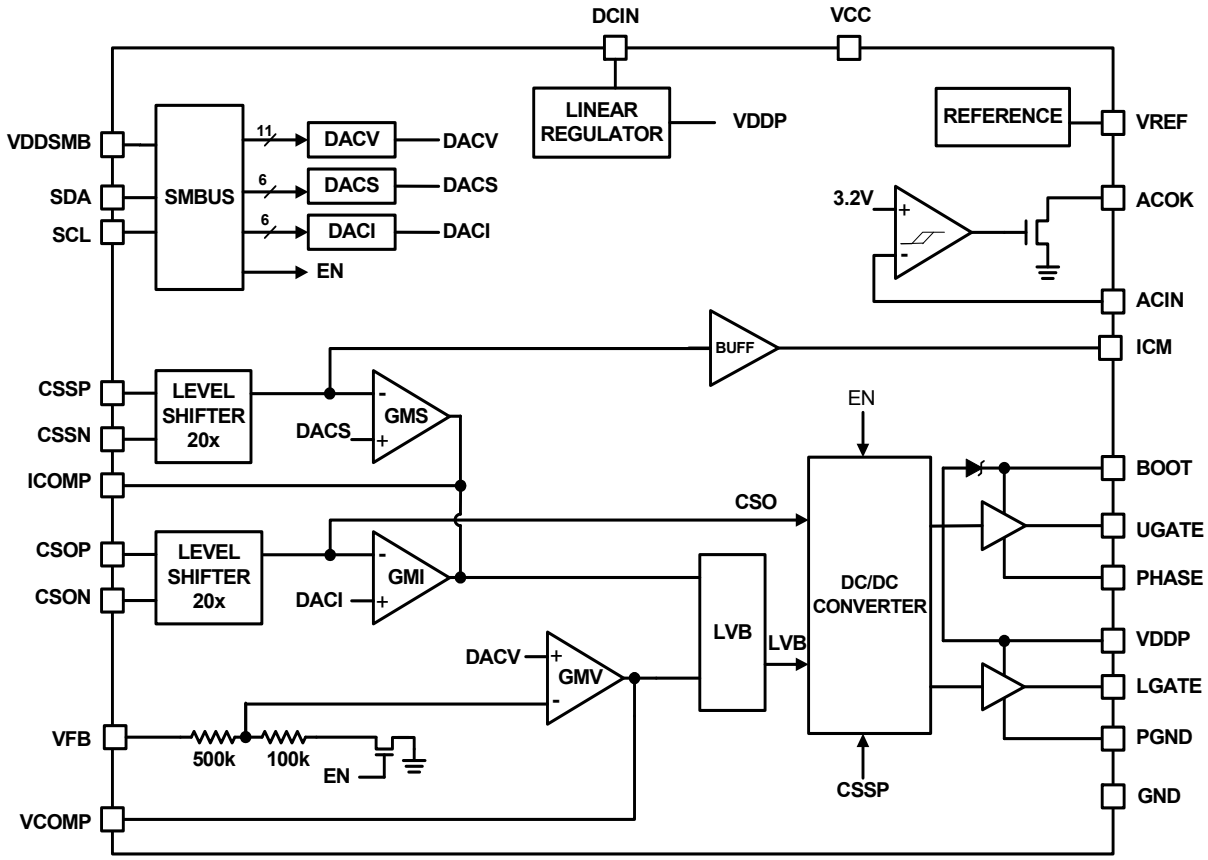


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

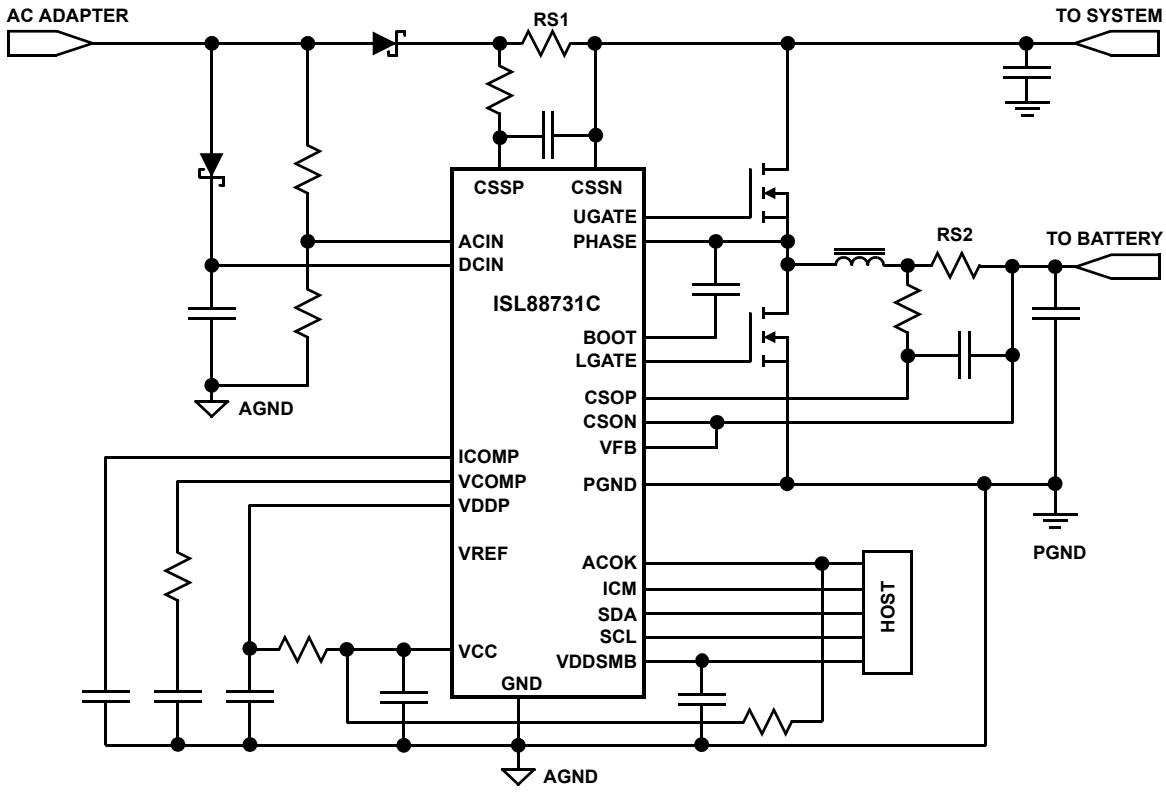
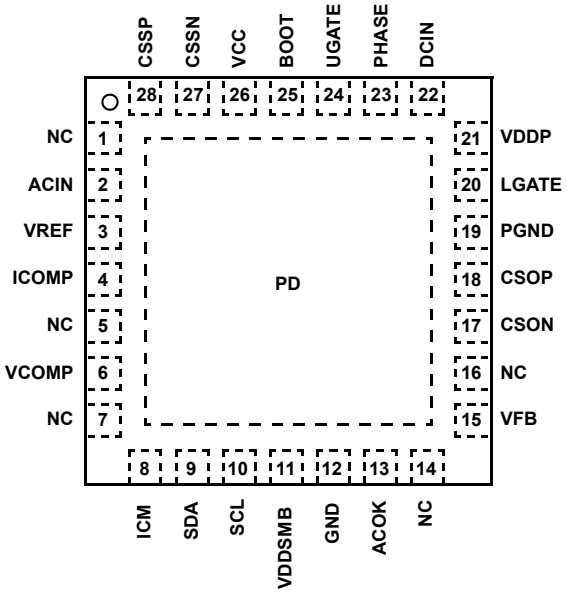


FIGURE 4. TYPICAL APPLICATION CIRCUIT

Pin Configuration

ISL88731C
(28 LD TQFN)
TOP VIEW



Functional Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
2	ACIN	AC Adapter Detection Input. Connect to a resistor divider from the AC adapter output. Range zero to 5.5V.
3	VREF	Reference Voltage output. Range 3.168V to 3.232V. It is internally compensated. Do not connect a decoupling capacitor.
4	ICOMP	Compensation Point for the charging current and adapter current regulation Loop. Connect 0.01µF to GND. See “Voltage Control Loop” on page 21 for details on selecting the ICOMP capacitor. Range zero to 5.5V.
6	VCOMP	Compensation Point for the voltage regulation loop. Connect 4.7kΩ in series with 0.01µF to GND. See “Voltage Control Loop” on page 21 for details on selecting VCOMP components. Range zero to 5.5V.
8	ICM	Input Current Monitor Output. ICM voltage equals 20 x (V_{CSSP} - V_{CSSN}). Range zero to 3V.
9	SDA	SMBus Data I/O. Open-drain Output. Connect an external pull-up resistor according to SMBus specifications. Range zero to 5.5V.
10	SCL	SMBus Clock Input. Connect an external pull-up resistor according to SMBus specifications. Range zero to 5.5V.
11	VDDSMB	SMBus interface Supply Voltage Input. Bypass with a 0.1µF capacitor to GND. Range 3.3V to 5.5V.
12	GND	Analog Ground. Connect directly to the backside paddle. Connect to the backside paddle and PGND at one point close to (under) the IC.
13	ACOK	AC Detect Output. This open drain output is high impedance when ACIN is greater than 3.2V. The ACOK output remains low when the ISL88731C is powered down. Connect a 10k pull-up resistor from ACOK to VDDSMB. Range 3.3V to 5.5V.
15	VFB	Feedback for the Battery Voltage. Range 1V to 19V.
17	CSON	Charge Current-Sense Negative Input. Range 1V to 19V.
18	CSOP	Charge Current-Sense Positive Input. Range 1V to 19V.
19	PGND	Power Ground. Connect PGND to the source of the low side MOSFET and the negative side of capacitors to the charger output and the drain of the upper switching FET. Connect this area to the Backside paddle at one location very near (under) the IC.
20	LGATE	Low-Side Power MOSFET Driver Output. Connect to low-side N channel MOSFET. LGATE drives between VDDP and PGND. Range is -0.3V to 5.23V.

Functional Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
21	VDDP	Linear Regulator Output. VDDP is the output of the 5.2V linear regulator supplied from DCIN. VDDP also directly supplies the LGATE driver and the BOOT strap diode. Bypass with a 1µF ceramic capacitor from VDDP to PGND. Range is 5.0V to 5.23V.
22	DCIN	Charger Bias Supply Input. Bypass DCIN with a 0.1µF capacitor to GND. Range 8V to +26V.
23	PHASE	High-Side Power MOSFET Driver Source Connection. Connect to the source of the high-side N-Channel MOSFET. Range -2V to +26V.
24	UGATE	High-Side Power MOSFET Driver Output. Connect to the high-side N-channel MOSFET gate. Range -2V to +33V.
25	BOOT	High-Side Power MOSFET Driver Power-Supply Connection. Connect a 0.1µF capacitor from BOOT-to-PHASE. Range -2V to +33V.
26	VCC	Power input for internal analog circuits. Connect a 4.7Ω resistor from VCC to VDDP and a 1µF ceramic capacitor from VCC to ground. Range 4V to 5.23V.
27	CSSN	Input Current-Sense Negative Input. Range 8V to 26V.
28	CSSP	Input Current-Sense Positive Input. Range 8V to 26V.
	PD	Connect the backside paddle to GND. This pad has the lowest thermal resistance to the die. It should be connected to a large area of ground with 3 to 5 vias for good thermal performance. The recommended potential of the thermal pad is zero (0) Volts.
1, 5, 7, 14, 16	NC	No Connect. Pins are not connected internally.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL88731CHRTZ	88731C HRTZ	-10 to +100	28 Ld 5x5 TQFN	L28.5x5B
ISL88731CEVAL2Z	Evaluation Board			

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL88731C. For more information on MSL please see tech brief TB363.

Table of Contents

Absolute Maximum Ratings

DCIN, CSSP, CSSN, CSOP, CSON, VFB . . . . . -0.3V to +28V
CSSP-CSSN, CSOP-CSON, PGND-GND . . . . . -0.3V to +0.3V
PHASE to GND . . . . . -6V to +30V
BOOT to GND . . . . . -0.3V to +33V
BOOT to PHASE . . . . . -0.3V to +6V
UGATE . . . . . PHASE - 0.3V to BOOT + 0.3V
LGATE . . . . . PGND - 0.3V to VDDP + 0.3V
ICOMP, VCOMP, VREF, to GND . . . . . -0.3V to VCC + 0.3V
VDDSMB, SCL, SDA, ACIN, ACOK . . . . . -0.3V to +6V
VDDP, ICM, VCC to GND, VDDP to PGND . . . . . -0.3V to +6V

Thermal Information

Thermal Resistance (Typical)	θJA (°C/W)	θJC (°C/W)
28 Ld TQFN Package (Notes 4, 5)	38	6.5

Junction Temperature Range . . . . . -55°C to +150°C
Operating Temperature Range . . . . . -10°C to +100°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

DCIN = CSSP = CSSN = 18V, CSOP = CSON = 12V, VDDP = 5V, BOOT-PHASE = 5.0V, GND = PGND = 0V, CVDDP = 1µF, IVDDP = 0mA, T_A = -10°C to +100°C. **Boldface limits apply over the operating temperature range, -10°C to +100°C.**

PARAMETER	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
CHARGE VOLTAGE REGULATION					
Battery Full Charge Voltage and Accuracy	ChargeVoltage = 0x41A0	**16.716**	16.8	**16.884**	V
		-0.5		**0.5**	%
	ChargeVoltage = 0x3130	**12.529**	12.592	**12.655**	V
		-0.5		**0.5**	%
	ChargeVoltage = 0x20D0	**8.350**	8.4	**8.450**	V
		-0.6		**0.6**	%
	ChargeVoltage = 0x1060	**4.163**	4.192	**4.221**	V
		-0.7		**0.7**	%
Battery Undervoltage Lockout Trip Point for Trickle Charge	VFB rising	**2.55**	2.7	**2.85**	V
Battery Undervoltage Lockout Trip Point Hysteresis		**100**	250	**400**	mV
CHARGE CURRENT REGULATION					
CSOP to CSON Full-Scale Current-Sense Voltage		**78.22**	80.64	**83.06**	mV
Charge Current and Accuracy	RS2 = 10mΩ (see Figure 4) ChargingCurrent = 0x1f80	**7.822**	8.064	**8.306**	A
		-3		**3**	%
	RS2 = 10mΩ (see Figure 4) ChargingCurrent = 0x0f80	**3.809**	3.968	**4.126**	A
		-4		**4**	%
	RS2 = 10mΩ (see Figure 4) ChargingCurrent = 0x0080	**64**	128	**220**	mA
Charge Current Gain Error	Based on charge current = 128mA and 8.064A	**-1.6**		**1.4**	%
CSOP/CSON Input Voltage Range		**0**		**19**	V

Electrical Specifications DCIN = CSSP = CSSN = 18V, CSOP = CSON = 12V, VDDP = 5V, BOOT-PHASE = 5.0V, GND = PGND = 0V, CVDDP = 1µF, IVDDP = 0mA, T_A = -10°C to +100°C. **Boldface limits apply over the operating temperature range, -10°C to +100°C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Battery Quiescent Current	Adapter present, not charging, $I_{CSOP} + I_{CSON} + I_{PHASE} + I_{CSSP} + I_{CSSN} + I_{FB}$ $V_{PHASE} = V_{CSON} = V_{CSOP} = V_{DCIN}$ = 19V, V_{ACIN} = 5V		135	**200**	µA
	Adapter Absent $I_{CSOP} + I_{CSON} + I_{PHASE} + I_{CSSP} + I_{CSSN} + I_{FB}$ $V_{PHASE} = V_{CSON} = V_{CSOP}$ = 19V, V_{DCIN} = 0V	**-1**	0.2	**2**	µA
Adapter Quiescent Current	$I_{DCIN} + I_{CSSP} + I_{CSSN}$ Vadapter = 8V to 26V, Vbattery 4V to 16.8V		3	**5**	mA
INPUT CURRENT REGULATION					
CSSP to CSSN Full-Scale Current-Sense Voltage	CSSP = 19V	**106.7**	110	**113.3**	mV
Input Current Accuracy	RS1 = 10mΩ (see Figure 4) Adapter Current = 11004mA or 3584mA	**-3**		**3**	%
	RS1 = 10mΩ (see Figure 4) Adapter Current = 2048mA	**-5**		**5**	%
Input Current Limit Gain Error	Based on InputCurrent = 1024mA and 11004mA	**-1.5**		**1.5**	%
Input Current Limit Offset		**-1**		**1**	mV
CSSP/CSSN Input Voltage Range		**8**		**26**	V
ICM Gain	$V_{CSSP-CSSN}$ = 110mV		20		V/V
ICM Accuracy	$V_{CSSP-CSSN}$ = 110mV	**-2.5**		**2.5**	%
	$V_{CSSP-CSSN}$ = 55mV or 35mV	**-4**		**4**	%
	$V_{CSSP-CSSN}$ = 20mV	**-8**		**8**	%
ICM Max Output Current	$V_{CSSP-CSSN}$ = 0.1V			**500**	µA
SUPPLY AND LINEAR REGULATOR					
DCIN, Input Voltage Range		**8**		**26**	V
VDDP Output Voltage	8.0V < V_{DCIN} < 28V, no load	**5.0**	5.1	**5.23**	V
VDDP Load Regulation	0 < I_{VDDP} < 30mA		35	**100**	mV
VDDSMB Range		**2.7**		**5.5**	V
VDDSMB UVLO Rising		**2.4**	2.5	**2.6**	V
VDDSMB UVLO Hysteresis		**40**	100	**150**	mV
VDDSMB Quiescent Current	VDDP = SCL = SDA = 5.5V		20	**27**	µA
V REFERENCE					
VREF Output Voltage	0 < I_{VREF} < 300µA	**3.168**	3.2	**3.232**	V
ACOK					
ACOK Sink Current	V_{ACOK} = 0.4V, ACIN = 1.5V	**2**	8		mA
ACOK Leakage Current	V_{ACOK} = 5.5V, ACIN = 3.7V			**1**	µA
ACIN					
ACIN rising Threshold		**3.15**	3.2	**3.25**	V
ACIN Threshold Hysteresis		**40**	60	**90**	mV
ACIN Input Bias Current		**-1**		**1**	µA

Electrical Specifications

DCIN = CSSP = CSSN = 18V, CSOP = CSON = 12V, VDDP = 5V, BOOT-PHASE = 5.0V, GND = PGND = 0V, CVDDP = 1µF, IVDDP = 0mA, T_A = -10°C to +100°C. **Boldface limits apply over the operating temperature range, -10°C to +100°C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SWITCHING REGULATOR					
Frequency		**330**	400	**440**	kHz
BOOT Supply Current	UGATE High	**170**	290	**400**	µA
PHASE Input Bias Current	V_{DCON} = 28V, V_{CSON} = V_{PHASE} = 20V		0	**2**	µA
UGATE On-Resistance Low	I_{UGATE} = -100mA		0.9	**1.6**	Ω
UGATE On-Resistance High	I_{UGATE} = 10mA		1.4	**2.5**	Ω
LGATE On-Resistance High	I_{LGATE} = +10mA		1.4	**2.5**	Ω
LGATE On-Resistance Low	I_{LGATE} = -100mA		0.9	**1.6**	Ω
Dead Time	Falling UGATE to rising LGATE or falling LGATE to rising UGATE	**35**	50	**80**	ns
ERROR AMPLIFIERS					
GMV Amplifier Transconductance		**200**	250	**300**	µA/V
GMI Amplifier Transconductance		**40**	50	**60**	µA/V
GMS Amplifier Transconductance		**40**	50	**60**	µA/V
GMI/GMS Saturation Current		**15**	21	**25**	µA
GMV Saturation Current		**10**	17	**30**	µA
ICOMP, VCOMP Clamp Voltage	0.25V < $V_{ICOMP, VCOMP}$ < 3.5V	**200**	300	**400**	mV
LOGIC LEVELS					
SDA/SCL Input Low Voltage	VDDSMB = 2.7V to 5.5V			**0.8**	V
SDA/SCL Input High Voltage	VDDSMB = 2.7V to 5.5V	**2**			V
SDA/SCL Input Bias Current	VDDSMB = 2.7V to 5.5V	**-1**		**1**	µA
SDA, Output Sink Current	V_{SDA} = 0.4V	**7**	15		mA

SMBus Timing Specifications

VDDSMB = 2.7V to 5.5V.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMBus Frequency	FSMB		10		100	kHz
Bus Free Time	t_{BUF}		4.7			µs
Start Condition Hold Time from SCL	$t_{HD:STA}$		4			µs
Start Condition Setup Time from SCL	$t_{SU:STA}$		4.7			µs
Stop Condition Setup Time from SCL	$t_{SU:STO}$		4			µs
SDA Hold Time from SCL	$t_{HD:DAT}$		300			ns
SDA Setup Time from SCL	$t_{SU:DAT}$		250			ns
SCL Low Timeout (Note 6)	$t_{TIMEOUT}$		22	25	30	ms
SCL Low Period	t_{LOW}		4.7			µs
SCL High Period	t_{HIGH}		4			µs
Maximum Charging Period without an SMBus Write to ChargeVoltage or ChargeCurrent Register			140	180	220	s

NOTES:

6. If SCL is low for longer than the specified time, the charger is disabled.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Operating Performance

DCIN = 20V, 3S2P Li-Battery, T_A = +25°C, unless otherwise noted.

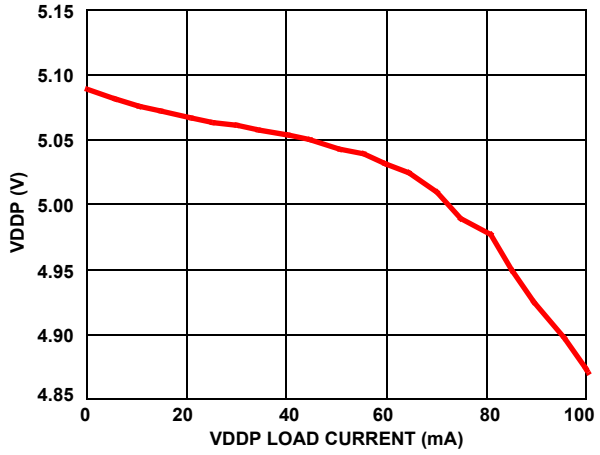


FIGURE 5. VDD LOAD REGULATION

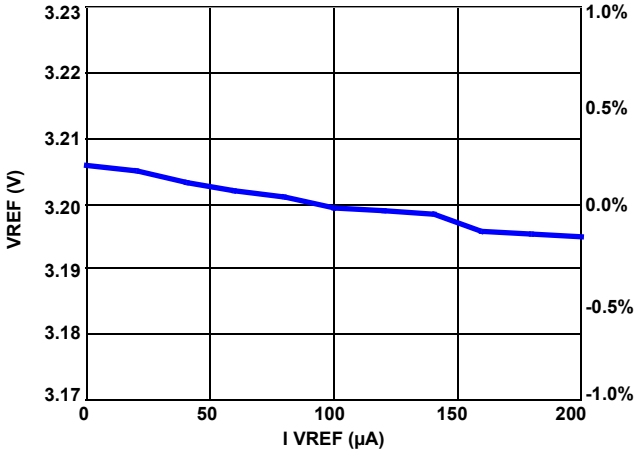


FIGURE 6. VREF LOAD REGULATION

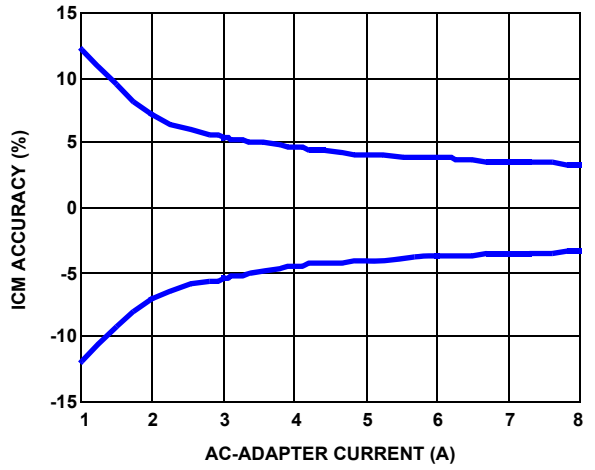


FIGURE 7. ICM ACCURACY vs AC-ADAPTER CURRENT

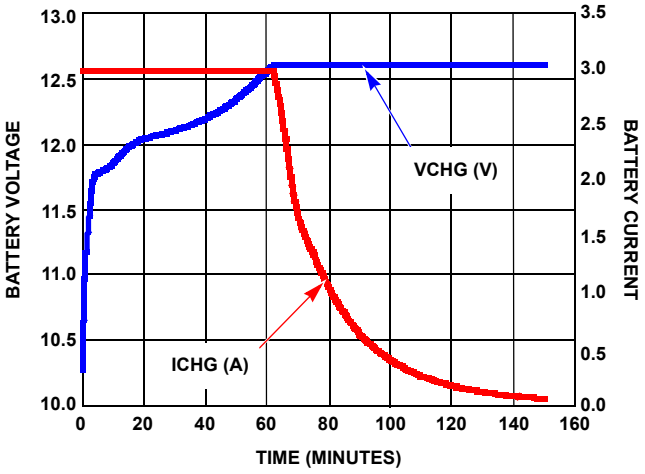


FIGURE 8. TYPICAL CHARGING VOLTAGE AND CURRENT

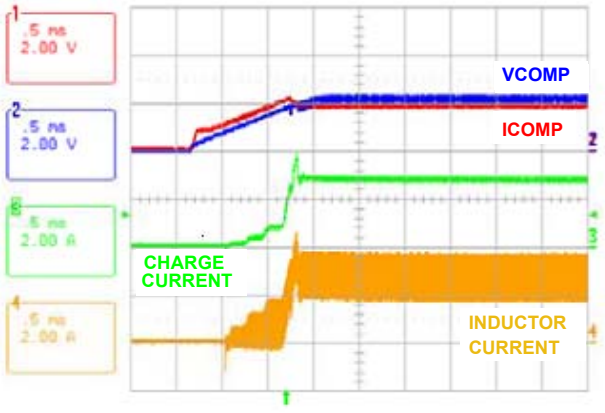


FIGURE 9. CHARGE ENABLE

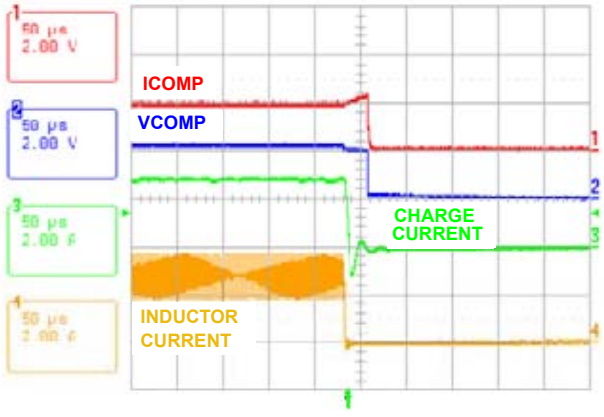


FIGURE 10. CHARGE DISABLE

Typical Operating Performance

DCIN = 20V, 3S2P Li-Battery, T_A = +25°C, unless otherwise noted. **(Continued)**

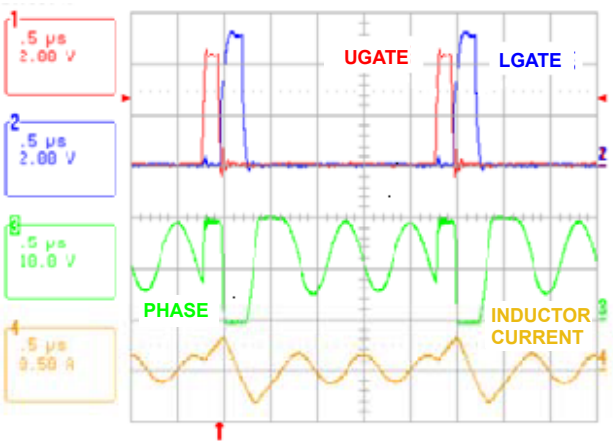


FIGURE 11. SWITCHING WAVEFORMS AT DIODE EMULATION

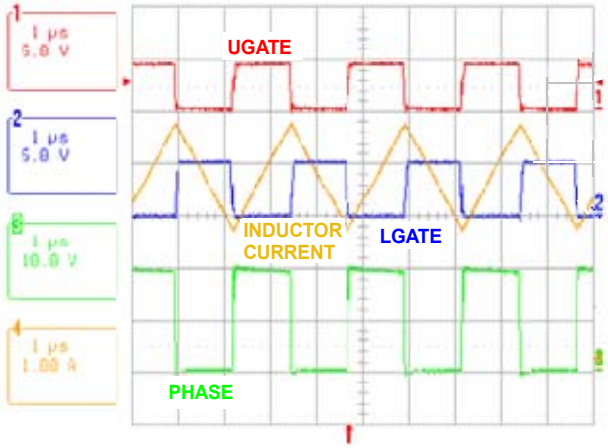


FIGURE 12. SWITCHING WAVEFORMS IN CC MODE

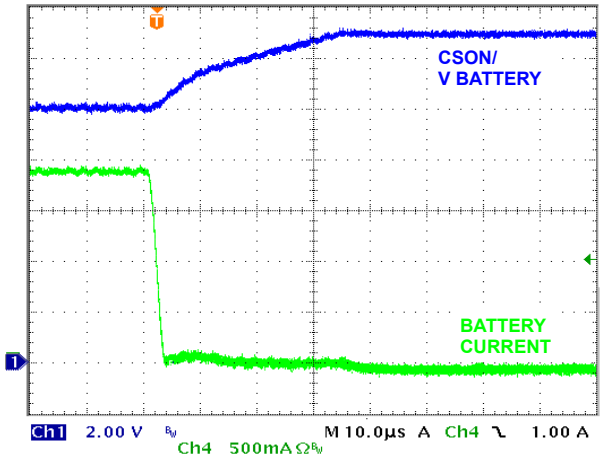


FIGURE 13. BATTERY REMOVAL

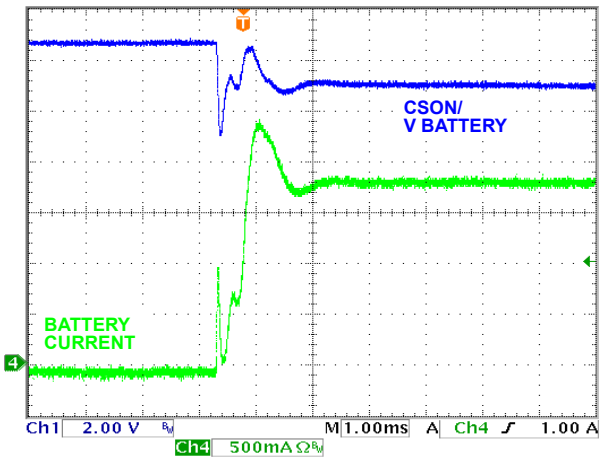


FIGURE 14. BATTERY INSERTION

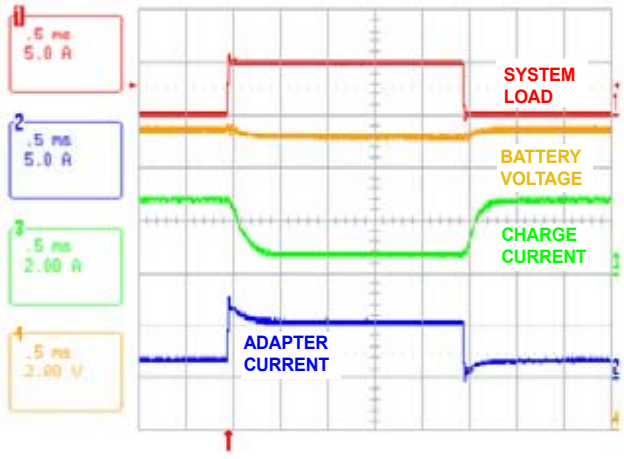


FIGURE 15. LOAD TRANSIENT RESPONSE

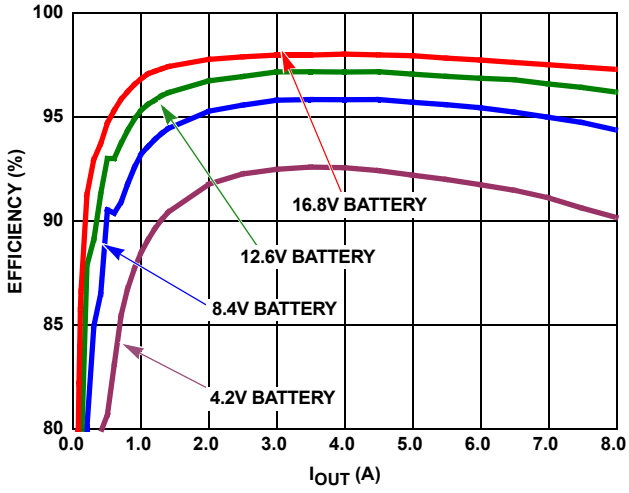


FIGURE 16. EFFICIENCY vs CHARGE CURRENT AND BATTERY VOLTAGE

Theory of Operation

Introduction

The ISL88731C includes all of the functions necessary to charge 1 to 4 cell Li-Ion and Li-polymer batteries. A high efficiency synchronous buck converter is used to control the charging voltage up to 19.2V and charging current up to 8A. The ISL88731C also has input current limiting up to 11A. The Input current limit, charge current limit and charge voltage limit are set by internal registers written with SMBus. The ISL88731C "Typical Application Circuit" is shown in Figure 4.

The ISL88731C charges the battery with constant charge current, set by the ChargeCurrent register, until the battery voltage rises to a voltage set by the ChargeVoltage register. The charger will then operate at a constant voltage. The adapter current is monitored and if the adapter current rises to the limit set by the InputCurrent register, battery charge current is reduced so the charger does not reduce the adapter current available to the system.

The ISL88731C features a voltage regulation loop (VCOMP) and 2 current regulation loops (ICOMP). The VCOMP voltage regulation loop monitors VFB to limit the battery charge voltage. The ICOMP current regulation loop limits the battery charging current delivered to the battery to ensure that it never exceeds the current set by the ChargeCurrent register. The ICOMP current regulation loop also limits the input current drawn from the AC-adapter to ensure that it never exceeds the limit set by the InputCurrent register, and to prevent a system crash and AC-adapter overload.

PWM Control

The ISL88731C employs a fixed frequency PWM control architecture with a feed-forward function. The feed-forward function maintains a constant modulator gain of 11 to achieve fast line regulation as the input voltage changes.

The duty cycle of the buck regulator is controlled by the lower of the voltages on ICOMP and VCOMP. The voltage on ICOMP and VCOMP are inputs to a Lower Voltage Buffer (LVB) who's output is the lower of the 2 inputs. The output of the LVB is compared to an internal 400kHz ramp to produce the Pulse Width Modulated signal that controls the UGATE and LGATE drivers. An internal clamp holds the higher of the 2 voltages (0.3V) above the lower voltage. This speeds the transition from voltage loop control to current loop control or vice versa.

The ISL88731C can operate up to 99.6% duty cycle if the input voltage drops close to or below the battery charge voltage (drop out mode). The DC/DC converter has a timer to prevent the frequency from dropping into the audible frequency range.

To prevent boosting of the system bus voltage, the battery charger drives the lower FET in a way that prevents negative inductor current.

An adaptive gate drive scheme is used to control the dead time between two switches. The dead time control circuit monitors the LGATE output and prevents the upper side MOSFET from turning on until 20ns after LGATE falls below 1V V_{GS}, preventing cross-conduction and shoot-through. The same occurs for LGATE turn on. In order for the deadtime circuit to work properly, there must be a low resistance, low inductance path from the LGATE driver to MOSFET gate, and from the source of MOSFET to PGND. An internal Schottky diode between the VDDP pin and BOOT pin keeps the bootstrap capacitor charged.

AC-Adapter Detection

Connect the AC-adapter voltage through a resistor divider to ACIN to detect when AC power is available, as shown in Figure 4. ACOK is an open-drain output and is active low when ACIN is less than $V_{th,fall}$, and high when ACIN is above $V_{th,rise}$. The ACIN rising threshold is 3.2V (typ) with 60mV hysteresis.

Current Measurement

Use ICM to monitor the adapter current being sensed across CSSP and CSSN. The output voltage range is 0V to 2.5V. The voltage of ICM is proportional to the voltage drop across CSSP and CSSN, and is given by Equation 1:

$$ICM = 20 \cdot I_{INPUT} \cdot R_{S1} \quad \text{(EQ. 1)}$$

where $I_{adapter}$ is the DC current drawn from the AC adapter. It is recommended to have an RC filter at the ICM output for minimizing the switching noise.

VDDP Regulator

VDDP provides a 5.1V supply voltage from the internal LDO regulator from DCIN and can deliver up to 30mA of continuous current. The MOSFET drivers are powered by VDDP. VDDP also supplies power to VCC through a low pass filter as shown in "TYPICAL APPLICATION CIRCUIT" on page 2. Bypass VDDP and VCC with a 1µF capacitor.

VDDSMB Supply

The VDDSMB input provides power to the SMBus interface. Connect VDDSMB to VCC, or apply an external supply to VDDSMB. Bypass VDDSMB to GND with a 0.1µF or greater ceramic capacitor.

The typical application connects VDDSMB to the same power source as the SMBus master. This supply should be active and greater than 2.5V when either the adapter or the battery is present.

ISL88731C does not function when VDDSMB is below its specified Under Voltage Lockout (UVLO) voltage. All of the SMBus registers in ISL88731C are powered by VDDSMB and are set to zero when it is below the UVLO threshold. Other functions are unpredictable when VDDSMB is below the UVLO threshold.

Short Circuit Protection and 0V Battery Charging

Since the battery charger will regulate the charge current to the limit set by the ChargeCurrent register, it automatically has short circuit protection and is able to provide the charge current to wake up an extremely discharged battery. Undervoltage trickle charge folds back current if there is a short circuit on the output.

Undervoltage Detect and Battery Trickle Charging

If the voltage at CSON falls below 2.5V ISL88731C reduces the charge current limit to 128mA to trickle charge the battery. When the voltage rises above 2.7V, the charge current reverts to the programmed value in the ChargeCurrent register.

Over-Temperature Protection

If the die temp exceeds +150°C, it stops charging. Once the die temp drops below +125°C, charging will start up again.

Overvoltage Protection

ISL88731C has an Overvoltage Protection circuit that limits the output voltage when the battery is removed or disconnected by a pulse charging circuit. If CSON exceeds the output voltage set point in the charge voltage register by more than 300mV, an internal comparator pulls VCOMP down and turns off both upper and lower FETs of the buck as in Figure 17. There is a delay of approximately 1µs between V_{OUT} exceeding the OVP trip point and pulling VCOMP, LGATE and UGATE low. After UGATE and LGATE are turned OFF, inductor current continues to flow through the body diode of the lower FET and V_{OUT} continues to rise until inductor current reaches zero.

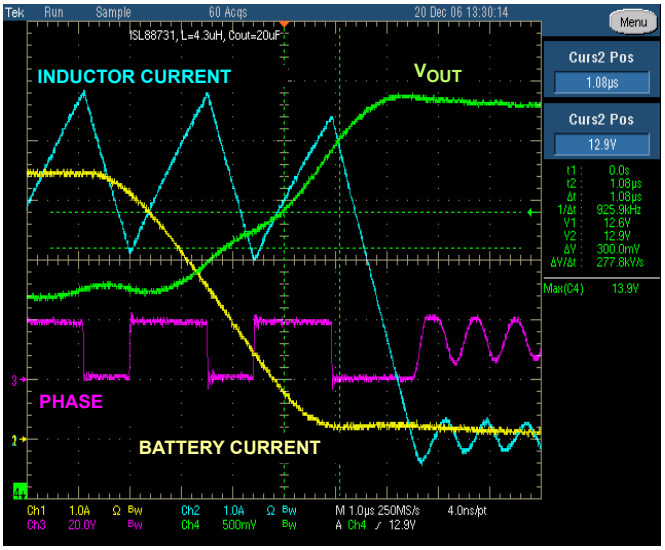
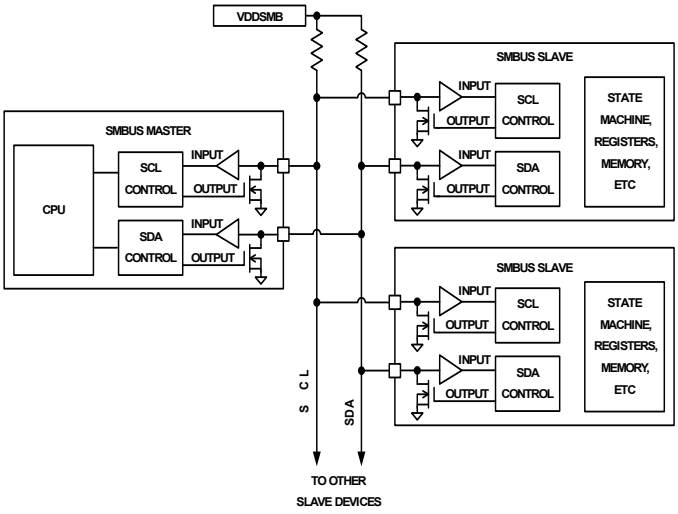


FIGURE 17. OVERVOLTAGE PROTECTION IN ISL88731C

The System Management Bus

The System Management Bus (SMBus) is a 2-wire bus that supports bidirectional communications. The protocol is described briefly here. More detail is available from www.smbus.org.

General SMBus Architecture



Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to Figure 18.

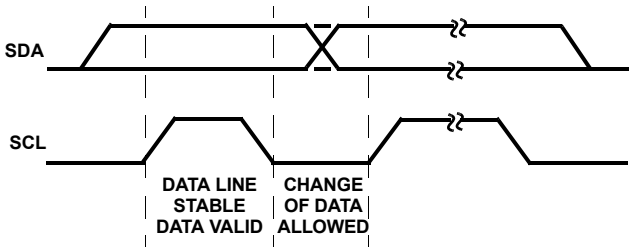


FIGURE 18. DATA VALIDITY

START and STOP Conditions

As shown in Figure 19, START condition is a HIGH-to-LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW-to-HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

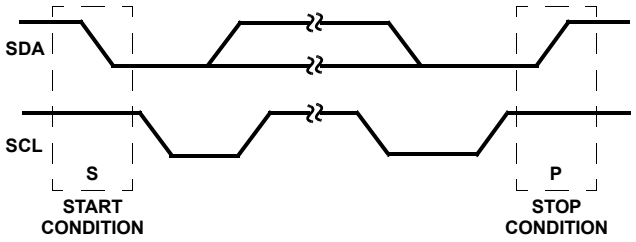


FIGURE 19. START AND STOP WAVEFORMS

Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the start condition, the master sends 7-slave address bits and a R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data (see Figure 20).

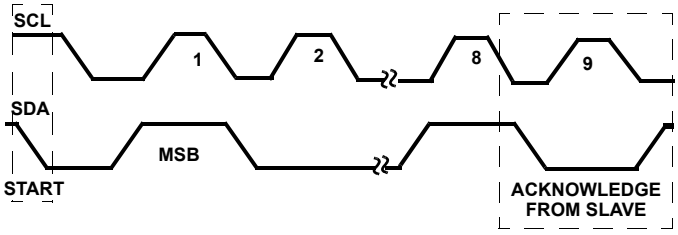


FIGURE 20. ACKNOWLEDGE ON THE I^2C BUS

SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a Start condition, followed by 7-bits of slave address (0001001 for the ISL88731C) followed by the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the SMBus bus recognize their address, they will Acknowledge by pulling the serial data (SDA) line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition.

Once the control byte is sent, and the ISL88731C acknowledges it, the 2nd byte sent by the master must be a register address byte such as 0x14 for the ChargeCurrent register. The register address byte tells the ISL88731C which register the master will write or read. See Table 1 for details of the registers. Once the ISL88731C receives a register address byte it responds with an acknowledge.

Byte Format

Every byte put on the SDA line must be eight bits long and must be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB) and the least significant bit last (LSB).

ISL88731C and SMBus

The ISL88731C receives control inputs from the SMBus interface. The serial interface complies with the SMBus protocols as documented in the System Management Bus Specification V1.1, which can be downloaded from www.smbus.org. The ISL88731C uses the SMBus Read-Word and Write-Word protocols (Figure 21) to communicate with the smart battery. The ISL88731C is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_ (0x12).

Read address = 0b00010011 and

Write address = 0b00010010.

In addition, the ISL88731C has two identification (ID) registers: a 16-bit device ID register and a 16-bit manufacturer ID register.

TABLE 1. BATTERY CHARGER REGISTER SUMMARY

REGISTER ADDRESS	REGISTER NAME	READ/WRITE	DESCRIPTION	POR STATE
0x14	ChargeCurrent	Read or Write	6-bit Charge Current Setting	0x0000
0x15	ChargeVoltage	Read or Write	11-bit Charge Voltage Setting	0x0000
0x3F	InputCurrent	Read or Write	6-bit Charge Current Setting	0x0080
0xFE	ManufacturerID	Read Only	Manufacturer ID	0x0049
0xFF	DeviceID	Read Only	Device ID	0x0001

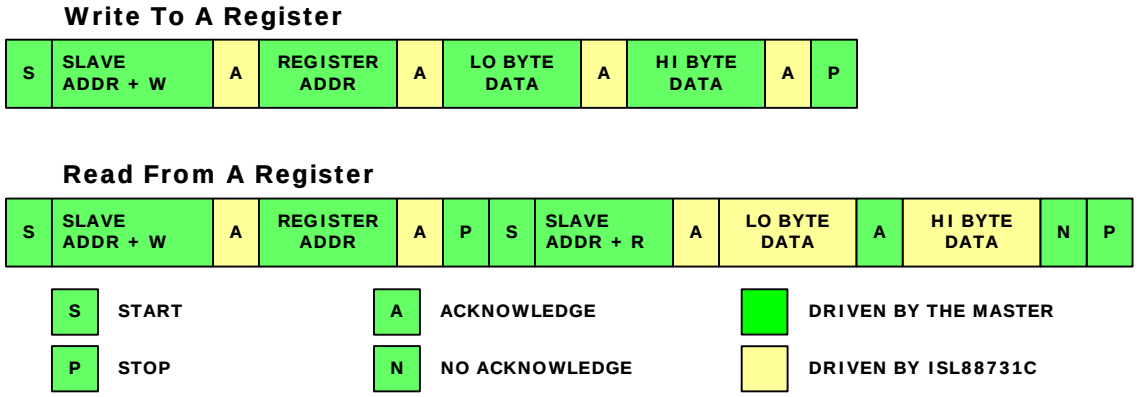


FIGURE 21. SMBus/ISL88731C READ AND WRITE PROTOCOL

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications. The ISL88731C is controlled by the data written to the registers described in Table 1.

Battery Charger Registers

The ISL88731C supports five battery-charger registers that use either Write-Word or Read-Word protocols, as summarized in Table 1. ManufacturerID and DeviceID are “read only” registers and can be used to identify the ISL88731C. On the ISL88731C, ManufacturerID always returns 0x0049 (ASCII code for “I” for Intersil) and DeviceID always returns 0x0001.

Enabling and Disabling Charging

After applying power to ISL88731C, the internal registers contain their POR values (see Table 1). The POR values for charge current and charge voltage are 0x0000. These values disable charging. To enable charging, the ChargeCurrent register must be written with a number >0x007F and the ChargeVoltage register must be written with a number >0x000F. Charging can be disabled by writing 0x0000 to either of these registers.

Setting Charge Voltage

Charge voltage is set by writing a valid 16-bit number to the ChargeVoltage register. This 16-bit number translates to a 65.535V full-scale voltage. The ISL88731C ignores the first 4 LSBs and uses the next 11 bits to set the voltage DAC. The charge voltage range of the ISL88731C is 1.024V to 19.200V. Numbers requesting charge voltage greater than 19.200V result in a ChargeVoltage of 19.200V. All numbers requesting charge voltage below 1.024V result in a voltage set point of zero, which terminates charging. Upon initial power-up or reset, the ChargeVoltage and ChargeCurrent registers are reset to 0 and the charger remains shut down until valid numbers are sent to the ChargeVoltage and ChargeCurrent registers. Use the Write-Word protocol (Figure 21) to write to the ChargeVoltage register. The register address for ChargeVoltage is 0x15. The 16-bit binary number formed by D15–D0 represents the charge voltage set point in mV. However, the resolution of the ISL88731C is 16mV because the D0–D3 bits are ignored as shown in Table 2. The D15 bit is also ignored because it is not needed to span the 1.024V to 19.2V range. Table 2 shows the mapping between the charge-voltage set point and the 16-bit number written to the ChargeVoltage register. The ChargeVoltage register can be read back to verify its contents.

TABLE 2. CHARGEVOLTAGE (REGISTER 0x15)

BIT	BIT NAME	DESCRIPTION
0		Not used.
1		Not used.
2		Not used.
3		Not used.
4	Charge Voltage, DACV 0	0 = Adds 0mV of charger voltage, 1024mV min. 1 = Adds 16mV of charger voltage.
5	Charge Voltage, DACV 1	0 = Adds 0mV of charger voltage, 1024mV min. 1 = Adds 32mV of charger voltage.
6	Charge Voltage, DACV 2	0 = Adds 0mV of charger voltage, 1024mV min. 1 = Adds 64mV of charger voltage.
7	Charge Voltage, DACV 3	0 = Adds 0mV of charger voltage, 1024mV min. 1 = Adds 128mV of charger voltage.
8	Charge Voltage, DACV 4	0 = Adds 0mV of charger voltage, 1024mV min. 1 = Adds 256mV of charger voltage.
9	Charge Voltage, DACV 5	0 = Adds 0mV of charger voltage, 1024mV min. 1 = Adds 512mV of charger voltage.
10	Charge Voltage, DACV 6	0 = Adds 0mA of charger voltage. 1 = Adds 1024mV of charger voltage.
11	Charge Voltage, DACV 7	0 = Adds 0mV of charger voltage. 1 = Adds 2048mV of charger voltage.
12	Charge Voltage, DACV 8	0 = Adds 0mV of charger voltage. 1 = Adds 4096mV of charger voltage.
13	Charge Voltage, DACV 9	0 = Adds 0mV of charger voltage. 1 = Adds 8192mV of charger voltage.
14	Charge Voltage, DACV 10	0 = Adds 0mV of charger voltage. 1 = Adds 16384mV of charger voltage, 19200mV max.
15		Not used. Normally a 32768mV weight.

Setting Charge Current

ISL88731C has a 16-bit ChargeCurrent register that sets the battery charging current. ISL88731C controls the charge current by controlling the CSOP-CSON voltage. The register's LSB translates to 10µV at CSON-CSOP. With a 10mΩ charge current R_{sense} resistor (RS2 in "Typical Application Circuit" on page 2), the LSB translates to 1mA charge current. The ISL88731C ignores the first 7 LSBs and uses the next 6 bits to control the current DAC. The charge-current range of the ISL88731C is 0A to 8.064A (using a 10mΩ current-sense resistor). All numbers requesting charge current above 8.064A result in a current setting of 8.064A. All numbers requesting charge current between 0mA to 128mA result in a current setting of 0mA. The default charge current setting at Power-On Reset (POR) is 0mA. To stop charging, set ChargeCurrent to 0. Upon initial power up, the ChargeVoltage and ChargeCurrent registers are reset to 0 and the charger is disabled. To start the charger, write valid numbers to the ChargeVoltage and ChargeCurrent registers. The ChargeCurrent register uses the Write-Word protocol (Figure 21). The register code for ChargeCurrent is 0x14 (0b00010100). Table 3 shows the mapping between the charge current set point and the ChargeCurrent number. The ChargeCurrent register can be read back to verify its contents.

The ISL88731C includes a fault limiter for low battery conditions. If the battery voltage is less than 2.5V, the charge current is temporarily set to 128mA. The ChargeCurrent register is preserved and becomes active again when the battery voltage is higher than 2.7V. This function effectively provides a foldback current limit, which protects the charger during short circuit and overload.

TABLE 3. CHARGE CURRENT (REGISTER 0x14) (10mΩ SENSE RESISTOR, RS2)

BIT	BIT NAME	DESCRIPTION
0		Not used.
1		Not used.
2		Not used.
3		Not used.
4		Not used.
5		Not used.
6		Not used.
7	Charge Current, DACI 0	0 = Adds 0mA of charger current. 1 = Adds 128mA of charger current.
8	Charge Current, DACI 1	0 = Adds 0mA of charger current. 1 = Adds 256mA of charger current.
9	Charge Current, DACI 2	0 = Adds 0mA of charger current. 1 = Adds 512mA of charger current.
10	Charge Current, DACI 3	0 = Adds 0mA of charger current. 1 = Adds 1024mA of charger current.
11	Charge Current, DACI 4	0 = Adds 0mA of charger current. 1 = Adds 2048mA of charger current.
12	Charge Current, DACI 5	0 = Adds 0mA of charger current. 1 = Adds 4096mA of charger current, 8064mA max.
13		Not used.
14		Not used.
15		Not used.

Setting Input-Current Limit

The total power from an AC adapter is the sum of the power supplied to the system and the power into the charger and battery. When the input current exceeds the set input current limit, the ISL88731C decreases the charge current to provide priority to system load current. As the system load rises, the available charge current drops linearly to zero. Thereafter, the total input current can increase to the limit of the AC adapter.

The internal amplifier compares the differential voltage between CSSP and CSSN to a scaled voltage set by the InputCurrent register. The total input current is the sum of the device supply current, the charger input current, and the system load current. The total input current can be estimated as shown in Equation 2.

$$I_{INPUT} = I_{SYSTEM} + [(I_{CHARGE} \times V_{BATTERY}) / (V_{IN} \times \eta)] \quad \text{(EQ. 2)}$$

Where η is the efficiency of the DC/DC converter (typically 85% to 95%).

The ISL88731C has a 16-bit InputCurrent register that translates to a 2mA LSB and a 131.071A full scale current using a 10mΩ current-sense resistor (RS1 in Figure 4). Equivalently, the 16-bit InputCurrent number sets the voltage across CSSP and CSSN inputs in 20µV per LSB increments. To set the input current limit use the SMBus to write a 16-bit InputCurrent register using the data format listed in Table 4. The InputCurrent register uses the Write-Word protocol (see Figure 21). The register code for InputCurrent is 0x3F (0b00111111). The InputCurrent register can be read back to verify its contents.

The ISL88731C ignores the first 7 LSBs and uses the next 6 bits to control the input-current DAC. The input-current range of the ISL88731C is from 256mA to 11.004A. All 16-bit numbers requesting input current above 11.004A result in an input-current setting of 11.004A. All 16-bit numbers requesting input current between 0mA to 256mA result in an input-current setting of 0mA. The default input-current-limit setting at POR is 256mA. When choosing the current-sense resistor RS1, carefully calculate its power rating. Take into account variations in the system's load current and the overall accuracy of the sense amplifier. Note that the voltage drop across RS1 contributes additional power loss, which reduces efficiency. System currents normally fluctuate as portions of the system are powered up or put to sleep. Without input current regulation, the input source must be able to deliver the maximum system current and the maximum charger-input current. By using the input-current-limit circuit, the output-current capability of the AC wall adapter can be lowered, reducing system cost.

TABLE 4. INPUT CURRENT (REGISTER 0x3F) (10mΩ SENSE RESISTOR, RS1)

BIT	BIT NAME	DESCRIPTION
0		Not used.
1		Not used.
2		Not used.
3		Not used.
4		Not used.
5		Not used.
6		Not used.
7	Input Current, DACS 0	0 = Adds 0mA of input current. 1 = Adds 256mA of input current.
8	Input Current, DACS 1	0 = Adds 0mA of input current. 1 = Adds 512mA of input current.
9	Input Current, DACS 2	0 = Adds 0mA of input current. 1 = Adds 1024mA of input current.
10	Input Current, DACS 3	0 = Adds 0mA of input current. 1 = Adds 2048mA of input current.
11	Input Current, DACS 4	0 = Adds 0mA of input current. 1 = Adds 4096mA of input current.
12	Input Current, DACS 5	0 = Adds 0mA of input current. 1 = Adds 8192mA of input current, 11004mA max.
13		Not used.
14		Not used.
15		Not used.

Charger Timeout

The ISL88731C includes 2 timers to insure the SMBus master is active and to prevent overcharging the battery. ISL88731C will terminate charging if the charger has not received a write to the ChargeVoltage or ChargeCurrent register within 175s or if the SCL line is low for more than 25ms. If a time-out occurs, either ChargeVoltage or ChargeCurrent registers must be written to re-enable charging.

ISL88731C Data Byte Order

Each register in ISL88731C contains 16-bits or 2, 8 bit bytes. All data sent on the SMBus is in 8-bit bytes and 2 bytes must be written or read from each register in ISL88731C. The order in which these bytes are transmitted appears reversed from the way they are normally written. The LOW byte is sent first and the HI byte is sent second. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is sent second.

Writing to the Internal Registers

In order to set the charge current, charge voltage or input current, valid 16-bit numbers must be written to ISL88731C's internal registers via the SMBus.

To write to a register in the ISL88731C, the master sends a control byte with the R/$\overline{W}$ bit set to 0, indicating a write. If it receives an Acknowledge from the ISL88731C it sends a register address byte setting the register to be written (i.e., 0x14 for the ChargeCurrent register). The ISL88731C will respond with an Acknowledge. The master then sends the lower data byte to be written into the desired register. The ISL88731C will respond with an Acknowledge. The master then sends the higher data byte to be written into the desired register. The ISL88731C will respond with an Acknowledge. The master then issues a Stop condition, indicating to the ISL88731C that the current transaction is complete. Once this transaction completes the ISL88731C will begin operating at the new current or voltage.

ISL88731C does not support writing more than one register per transaction.

Reading from the Internal Registers

The ISL88731C has the ability to read from 5 internal registers. Prior to reading from an internal register, the master must first select the desired register by writing to it and sending the registers address byte. This process begins by the master sending a control byte with the R/$\overline{W}$ bit set to 0, indicating a write. Once it receives an Acknowledge from the ISL88731C it sends a register address byte representing the internal register it wants to read. The ISL88731C will respond with an Acknowledge. The master must then respond with a Stop condition. After the Stop condition the master follows with a new Start condition, then sends a new control byte with the ISL88731C slave address and the R/$\overline{W}$ bit set to 1, indicating a read. The ISL88731C will Acknowledge then send the lower byte stored in that register. After receiving the byte, the master Acknowledges by holding SDA low during the 9th clock pulse. ISL88731C then sends the higher byte stored in the register. After the second byte neither device holds SDA low (No Acknowledge). The master will then produce a Stop condition to end the read transaction.

ISL88731C does not support reading more than 1 register per transaction.

Application Information

The following battery charger design refers to the "Typical Application Circuit" (see Figure 4), where typical battery configuration of 3S2P is used. This section describes how to select the external components including the inductor, input and output capacitors, switching MOSFETs and current sensing resistors.

Inductor Selection

The inductor selection has trade-offs between cost, size, crossover frequency and efficiency. For example, the lower the inductance, the smaller the size, but ripple current is higher. This also results in higher AC losses in the magnetic core and the windings, which decreases the system efficiency. On the other hand, the higher inductance results in lower ripple current and smaller output filter capacitors, but it has higher DCR (DC resistance of the inductor) loss, lower saturation current and has slower transient response. So, the practical inductor design is based on the inductor ripple current being ±15% to ±20% of the maximum operating DC current at maximum input voltage. Maximum ripple is at 50% duty cycle or $V_{BAT} = V_{IN,MAX}/2$. The required inductance for ±15% ripple current can be calculated from Equation 3:

$$L = \frac{V_{IN,\,MAX}}{4 \cdot F_{SW} \cdot 0.3 \cdot I_{L,\,MAX}} \quad \text{(EQ. 3)}$$

Where $V_{IN,MAX}$ is the maximum input voltage, F_{SW} is the switching frequency and $I_{L,MAX}$ is the max DC current in the inductor.

For $V_{IN,MAX}$ = 20V, V_{BAT} = 12.6V, $I_{BAT,MAX}$ = 4.5A, and f_s = 400kHz, the calculated inductance is 9.3µH. Choosing the closest standard value gives L = 10µH. Ferrite cores are often the best choice since they are optimized at 400kHz to 600kHz operation with low core loss. The core must be large enough not to saturate at the peak inductor current I_{Peak} in Equation 4:

$$I_{PEAK} = I_{L,\,MAX} + \frac{1}{2} \cdot I_{RIPPLE} \quad \text{(EQ. 4)}$$

Inductor saturation can lead to cascade failures due to very high currents. Conservative design limits the peak and RMS current in the inductor to less than 90% of the rated saturation current.

Crossover frequency is heavily dependent on the inductor value. F_{CO} should be less than 20% of the switching frequency and a conservative design has F_{CO} less than 10% of the switching frequency. The highest F_{CO} is in voltage control mode with the battery removed and may be calculated (approximately) from Equation 5:

$$F_{CO} = \frac{5 \cdot 11 \cdot RS2}{2\pi \cdot L} \quad \text{(EQ. 5)}$$

Output Capacitor Selection

The output capacitor in parallel with the battery is used to absorb the high frequency switching ripple current and smooth the output voltage. The RMS value of the output ripple current I_{RMS} is given by Equation 6:

$$(Cout)_{RMS} = \frac{V_{IN,MAX}}{\sqrt{12} \cdot L \cdot F_{SW}} \cdot D \cdot (1 - D) \quad \text{(EQ. 6}$$

Where the duty cycle D is the ratio of the output voltage (battery voltage) over the input voltage for continuous conduction mode which is typical operation for the battery charger. During the battery charge period, the output voltage varies from its initial battery voltage to the rated battery voltage. So, the duty cycle varies from 0.53 for the minimum battery voltage of 7.5V (2.5V/Cell) to 0.88 for the maximum battery voltage of 12.6V. The maximum RMS value of the output ripple current occurs at the duty cycle of 0.5 and is expressed as Equation 7:

$$I(Cout)_{RMS} = \frac{V_{IN,MAX}}{4 \cdot \sqrt{12} \cdot L \cdot F_{SW}} \quad \text{(EQ. 7)}$$

For $V_{IN,MAX}$ = 19V, VBAT = 16.8V, L = 10µH, and f_s = 400kHz, the maximum RMS current is 0.19A. A typical 20µF ceramic capacitor is a good choice to absorb this current and also has very small size. Organic polymer capacitors have high capacitance with small size and have a significant equivalent series resistance (ESR). Although ESR adds to ripple voltage, it also creates a high frequency zero that helps the closed loop operation of the buck regulator.

EMI considerations usually make it desirable to minimize ripple current in the battery leads. Beads may be added in series with the battery pack to increase the battery impedance at 400kHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and battery impedance. If the ESR of the output capacitor is 10mΩ and battery impedance is raised to 2Ω with a bead, then only 0.5% of the ripple current will flow in the battery.

MOSFET Selection

The Notebook battery charger synchronous buck converter has the input voltage from the AC-adapter output. The maximum AC-adapter output voltage does not exceed 25V. Therefore, 30V logic MOSFET should be used.

The high-side MOSFET must be able to dissipate the conduction losses plus the switching losses. For the battery charger application, the input voltage of the synchronous buck converter is equal to the AC-adapter output voltage, which is relatively constant. The maximum efficiency is achieved by selecting a high side MOSFET that has the conduction losses equal to the switching losses. Switching losses in the low-side FET are very small. The choice of low-side FET is a trade-off between conduction losses ($r_{DS(ON)}$) and cost. A good rule of thumb for the $r_{DS(ON)}$ of the low-side FET is 2x the $r_{DS(ON)}$ of the high-side FET.

The LGATE gate driver can drive sufficient gate current to switch most MOSFETs efficiently. However, some FETs may exhibit cross conduction (or shoot-through) due to current injected into the drain-to-source parasitic capacitor (C_{gd}) by the high dv/dt rising edge at the phase node when the high side MOSFET turns on. Although LGATE sink current (1.8A typical) is more than enough to switch the FET off quickly, voltage drops across parasitic impedances between LGATE and the MOSFET can allow the gate to rise during the fast rising edge of voltage on the drain. MOSFETs with low threshold voltage (<1.5V) and low ratio of C_{gs}/C_{gd} (<5) and high gate resistance (>4Ω) may be turned on for a few ns by the high dv/dt (rising edge) on their drain. This can be avoided with higher threshold voltage and C_{gs}/C_{gd} ratio. Another way to avoid cross conduction is slowing the turn-on speed of the high-side MOSFET by connecting a resistor between the BOOT pin and the bootstrap capacitor.

For the high-side MOSFET, the worst-case conduction losses occur at the minimum input voltage, as shown in Equation 8:

$$P_{Q1,\,conduction} = \frac{V_{OUT}}{V_{IN}} \cdot I_{BAT}^{2} \cdot r_{DS(ON)} \quad \text{(EQ. 8)}$$

The optimum efficiency occurs when the switching losses equal the conduction losses. However, it is difficult to calculate the switching losses in the high-side MOSFET since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the MOSFET internal gate resistance, gate charge, threshold voltage, stray inductance and the pull-up and pull-down resistance of the gate driver.

The following switching loss calculation (Equation 9) provides a rough estimate.

$$P_{Q1,\,Switching} = \frac{1}{2} V_{IN} I_{LV} f_{sw} \left(\frac{Q_{gd}}{I_{g,\,source}} \right) + \frac{1}{2} V_{IN} I_{LP} f_{sw} \left(\frac{Q_{gd}}{I_{g,\,sink}} \right) + Q_{rr} V_{IN} f_{sw} \quad \text{(EQ. 9)}$$

Where the following are the peak gate-drive source/sink current of Q_1, respectively:

- Q_{gd}: drain-to-gate charge,
- Q_{rr}: total reverse recovery charge of the body-diode in low-side MOSFET,
- I_{LV}: inductor valley current,
- I_{LP}: Inductor peak current,
- $I_{g,sink}$
- $I_{g,source}$

Low switching loss requires low drain-to-gate charge Q_{gd}. Generally, the lower the drain-to-gate charge, the higher the ON-resistance. Therefore, there is a trade-off between the ON-resistance and drain-to-gate charge. Good MOSFET selection is based on the Figure of Merit (FOM), which is a product of the total gate charge and on-resistance. Usually, the smaller the value of FOM, the higher the efficiency for the same application.

For the low-side MOSFET, the worst-case power dissipation occurs at minimum battery voltage and maximum input voltage as shown in Equation 10.

$$P_{Q2} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot I_{BAT}^{2} \cdot r_{DS(ON)} \quad \text{(EQ. 10)}$$

Choose a low-side MOSFET that has the lowest possible ON-resistance with a moderate-sized package (like the 8 Ld SOIC) and is reasonably priced. The switching losses are not an issue for the low-side MOSFET because it operates at zero-voltage-switching.

Ensure that the required total gate drive current for the selected MOSFETs should be less than 24mA. Thus, the total gate charge for the high-side and low-side MOSFETs is limited by Equation 11:

$$Q_{GATE} \leq \frac{I_{GATE}}{F_{SW}} \quad \text{(EQ. 11)}$$

Where I_{GATE} is the total gate drive current and should be less than 24mA. Substituting I_{GATE} = 24mA and f_s = 400kHz into Equation 11 yields that the total gate charge should be less than 80nC. Therefore, the ISL88731C easily drives the battery charge current up to 8A.

Snubber Design

ISL88731C's buck regulator operates in discontinuous current mode (DCM) when the load current is less than half the peak-to-peak current in the inductor. After the low-side FET turns off, the phase voltage rings due to the high impedance with both FETs off. This can be seen in Figure 11. Adding a snubber (resistor in series with a capacitor) from the phase node to ground can greatly reduce the ringing. In some situations, a snubber can improve output ripple and regulation.

The snubber capacitor should be approximately twice the parasitic capacitance on the phase node. This can be estimated by operating at very low load current (100mA) and measuring the ringing frequency.

C_{SNUB} and R_{SNUB} can be calculated from Equations 12 and 13:

$$C_{SNUB} = \frac{2}{(2\pi F_{ring})^2 \cdot L} \quad \text{(EQ. 12)}$$

$$R_{SNUB} = \sqrt{\frac{2 \cdot L}{C_{SNUB}}} \quad \text{(EQ. 13)}$$

Input Capacitor Selection

The input capacitor absorbs the ripple current from the synchronous buck converter, which is given by Equation 14:

$$I_{RMS} = I_{BAT} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \quad \text{(EQ. 14)}$$

This RMS ripple current must be smaller than the rated RMS current in the capacitor data sheet. Non-tantalum chemistries (ceramic, aluminum, or OSCON) are preferred due to their resistance to power-up surge currents when the AC-adapter is plugged into the battery charger. For Notebook battery charger applications, it is recommended that ceramic capacitors or polymer capacitors from Sanyo be used due to their small size and reasonable cost.

Loop Compensation Design

ISL88731C has three closed loop control modes. One controls the output voltage when the battery is fully charged or absent. A second controls the current into the battery when charging and the third limits current drawn from the adapter. The charge current and input current control loops are compensated by a single capacitor on the ICOMP pin. The voltage control loop is compensated by a network on the VCOMP pin. Descriptions of these control loops and guidelines for selecting compensation components will be given in the following sections. Which loop controls the output is determined by the minimum current buffer and the minimum voltage buffer shown in the "FUNCTIONAL BLOCK DIAGRAM" on page 2. These three loops will be described separately.

Transconductance Amplifiers GMV, GMI and GMS

ISL88731C uses several transconductance amplifiers (also known as gm amps). Most commercially available op amps are voltage controlled voltage sources with gain expressed as $A = V_{OUT}/V_{IN}$. gm amps are voltage controlled current sources with gain expressed as $gm = I_{OUT}/V_{IN}$. gm will appear in some of the equations for poles and zeros in the compensation.

PWM Gain F_m

The Pulse Width Modulator in the ISL88731C converts voltage at VCOMP to a duty cycle by comparing VCOMP to a triangle wave (duty = $VCOMP/V_{P-P\ RAMP}$). The low-pass filter formed by L and C_O convert the duty cycle to a DC output voltage ($Vo = V_{DCIN}$*duty). In ISL88731C, the triangle wave amplitude is proportional to V_{DCIN}. Making the ramp amplitude proportional to DCIN makes the gain from VCOMP to the PHASE output a constant 11 and is independent of DCIN. For small signal AC analysis, the battery is modeled by its internal resistance. The total output resistance is the sum of the sense resistor and the internal resistance of the MOSFETs, inductor and capacitor.

Figure 22 shows the small signal model of the pulse width modulator (PWM), power stage, output filter and battery.

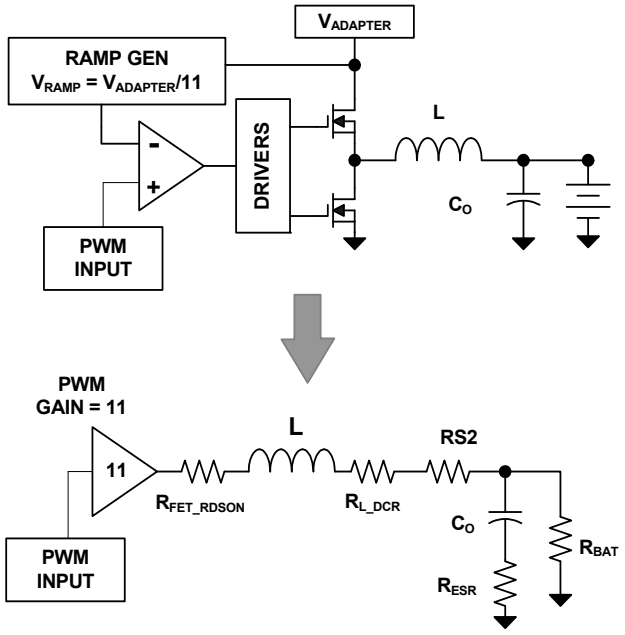


FIGURE 22. SMALL SIGNAL AC MODEL

In most cases the Battery resistance is very small (<200mΩ) resulting in a very low Q in the output filter. This results in a frequency response from the input of the PWM to the inductor current with a single pole at the frequency calculated in Equation 15:

$$F_{POLE1} = \frac{(RS2 + r_{DS(ON)} + R_{DCR} + R_{BAT})}{2\pi \cdot L} \quad \text{(EQ. 15)}$$

The output capacitor creates a pole at a very high frequency due to the small resistance in parallel with it. The frequency of this pole is calculated in Equation 16:

$$F_{POLE2} = \frac{1}{2\pi \cdot C_o \cdot R_{BAT}} \quad \text{(EQ. 16)}$$

Charge Current Control Loop

When the battery is less than the fully charged, the voltage error amplifier goes to it's maximum output (limited to 0.3V above ICOMP) and the ICOMP voltage controls the loop through the minimum voltage buffer. Figure 24 shows the charge current control loop.

The compensation capacitor (C_{ICOMP}) gives the error amplifier (GMI) a pole at a very low frequency (<<1Hz) and a zero at F_{Z1}. F_{Z1} is created by the 0.25*CA2 output added to ICOMP. The frequency can be calculated from Equation 17:

$$F_{ZERO} = \frac{4 \cdot gm2}{(2\pi \cdot C_{ICOMP})} \qquad gm2 = 50\mu A/V \quad \text{(EQ. 17)}$$

Placing this zero at a frequency equal to the pole calculated in Equation 16 will result in maximum gain at low frequencies and phase margin near 90°. If the zero is at a higher frequency (smaller C_{ICOMP}), the DC gain will be higher but the phase margin will be lower. Use a capacitor on ICOMP that is equal to or greater than the value calculated in Equation 18. The factor of 1.5 is to ensure the zero is at a frequency lower than the pole including tolerance variations.

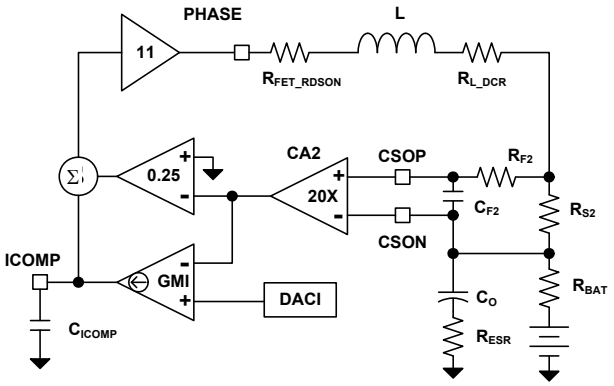


FIGURE 23. CHARGE CURRENT LIMIT LOOP

$$C_{ICOMP} = \frac{1.5 \cdot 4 \cdot (50\mu A/V) \cdot L}{(RS2 + r_{DS(ON)} + R_{DCR} + R_{BAT})} \quad \text{(EQ. 18)}$$

A filter should be added between R_{S2} and CSOP and CSON to reduce switching noise. The filter roll-off frequency should be between the crossover frequency and the switching frequency (~100kHz). R_{F2} should be small (<10Ω) to minimize offsets due to leakage current into CSOP. The filter cutoff frequency is calculated using Equation 19:

$$F_{FILTER} = \frac{1}{(2\pi \cdot C_{F2} \cdot R_{F2})} \quad \text{(EQ. 19)}$$

The crossover frequency is determined by the DC gain of the modulator and output filter and the pole in Equation 16. The DC gain is calculated in Equation 20 and the cross over frequency is calculated with Equation 21:

$$A_{DC} = \frac{11 \cdot RS2}{(RS2 + r_{DS(ON)} + R_{DCR} + R_{BAT})} \quad \text{(EQ. 20)}$$

$$F_{CO} = A_{DC} \cdot F_{POLE} = \frac{11 \cdot RS2}{2\pi \cdot L} \quad \text{(EQ. 21)}$$

The Bode plot of the loop gain, the compensator gain and the power stage gain is shown in Figure 24.

Adapter Current Limit Control Loop

If the combined battery charge current and system load current draws current that equals the adapter current limit set by the InputCurrent register, ISL88731C will reduce the current to the battery and/or reduce the output voltage to hold the adapter current at the limit. Above the adapter current limit the minimum current buffer equals the output of GMS and ICOMP controls the

charger output. Figure 25 shows the adapter current limit control loop.

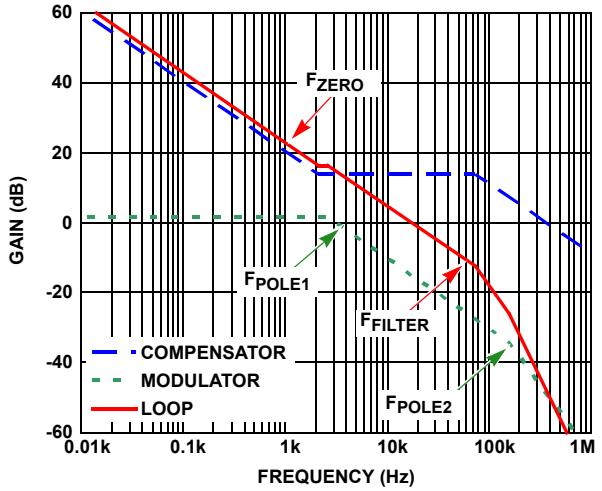


FIGURE 24. CHARGE CURRENT LOOP BODE PLOTS

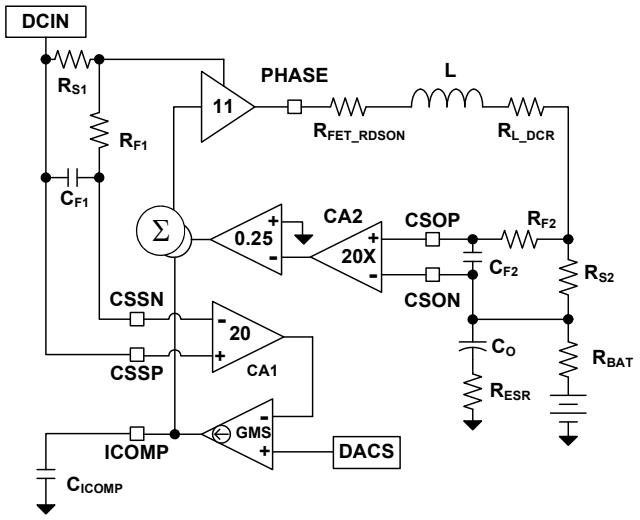


FIGURE 25. ADAPTER CURRENT LIMIT LOOP

The loop response equations, bode plots and the selection of C_{ICOMP} are the same as the charge current control loop with loop gain reduced by the duty cycle and the ratio of R_{S1}/R_{S2}. In other words, if $R_{S1} = R_{S2}$ and the duty cycle D = 50%, the loop gain will be 6dB lower than the loop gain in Figure 25. This gives lower crossover frequency and higher phase margin in this mode. If $R_{S1}/R_{S2} = 2$ and the duty cycle is 50% then the adapter current loop gain will be identical to the gain in Figure 25.

A filter should be added between R_{S1} and CSIP and CSIN to reduce switching noise. The filter roll off frequency should be between the cross over frequency and the switching frequency (~100kHz).

Voltage Control Loop

When the battery is charged to the voltage set by ChargeVoltage register, the voltage error amplifier (GMV) takes control of the output (assuming that the adapter current is below the limit set by ACLIM). The voltage error amplifier (GMV) discharges the cap on VCOMP to limit the output voltage. The current to the battery decreases as the cells charge to the fixed voltage and the voltage across the internal battery resistance decreases. As battery current decreases the 2 current error amplifiers (GMI and GMS) output their maximum current and charge the capacitor on ICOMP to its maximum voltage (limited to 0.3V above VCOMP). With high voltage on ICOMP, the minimum voltage buffer output equals the voltage on VCOMP.

The voltage control loop is shown in Figure 26.

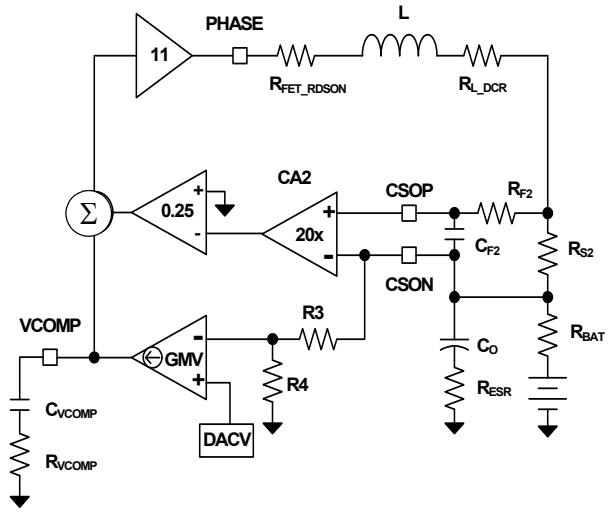


FIGURE 26. VOLTAGE CONTROL LOOP

Output LC Filter Transfer Functions

The gain from the phase node to the system output and battery depend entirely on external components. Typical output LC filter response is shown in Figure 27. Transfer function $A_{LC}(s)$ is shown in Equation 22:

$$A_{LC} = \frac{\left(1 - \frac{s}{\omega_{ESR}}\right)}{\left(\frac{s^2}{\omega_{DP}} + \frac{s}{(\omega_{LC} \cdot Q)} + 1\right)}$$

$$\omega_{ESR} = \frac{1}{(R_{ESR} \cdot C_o)} \quad \omega_{LC} = \frac{1}{(\sqrt{L \cdot C_o})} \quad Q = R_o \cdot \sqrt{\frac{L}{C_o}} \qquad \text{(EQ. 22)}$$

The resistance R_o is a combination of MOSFET $r_{DS(ON)}$, inductor DCR, R_{SENSE} and the internal resistance of the battery (normally between 50mΩ and 200mΩ) The worst case for voltage mode control is when the battery is absent. This results in the highest Q of the LC filter and the lowest phase margin.

The compensation network consists of the voltage error amplifier GMV and the compensation network R_{VCOMP}, C_{VCOMP} which give the loop very high DC gain, a very low frequency pole and a zero at F_{ZERO1}. Inductor current information is added to the feedback to create a second zero F_{ZERO2}. The low pass filter R_{F2}, C_{F2} between R_{S2} and ISL88731C add a pole at F_{FILTER}. R_3 and R_4 are internal divider resistors that set the DC output voltage. For a 3-cell battery, R_3 = 500kΩ and R_4 = 100kΩ. The following equations relate the compensation network's poles, zeros and

gain to the components in Figure 26. Figure shows an asymptotic Bode plot of the DC/DC converter's gain vs. frequency. It is strongly recommended that F_{ZERO1} is approximately 30% of F_{LC} and F_{ZERO2} is approximately 70% of F_{LC}.

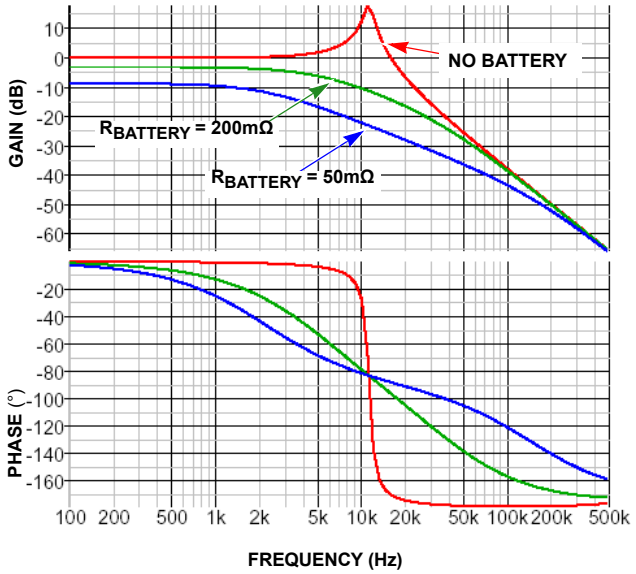


FIGURE 27. FREQUENCY RESPONSE OF THE LC OUTPUT FILTER

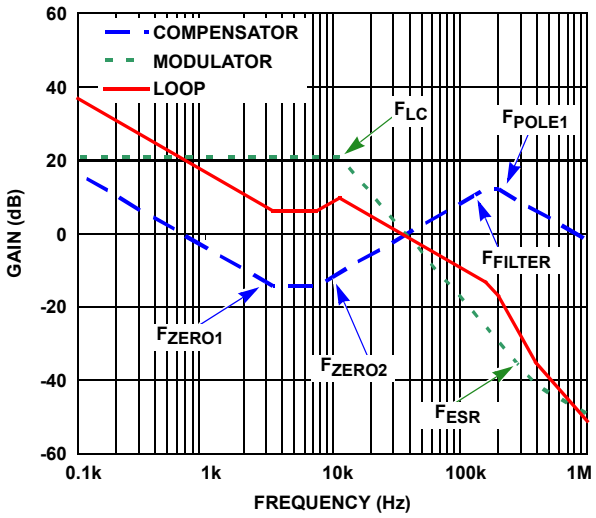


FIGURE 28. ASYMPTOTIC BODE PLOT OF THE VOLTAGE CONTROL LOOP GAIN

Compensation Break Frequency Equations

$$F_{ZERO1} = \frac{1}{(2\pi \cdot C_{VCOMP} \cdot R_{VCOMP})} \quad \text{(EQ. 23)}$$

$$F_{ZERO2} = \left(\frac{R_{VCOMP}}{2\pi \cdot RS2 \cdot C_o}\right) \cdot \left(\frac{R_4}{R_4 + R_3}\right) \cdot \left(\frac{gm1}{5}\right) \quad \text{(EQ. 24)}$$

$$F_{LC} = \frac{1}{(2\pi \sqrt{L \cdot C_o})} \quad \text{(EQ. 25)}$$

$$F_{FILTER} = \frac{1}{(2\pi \cdot R_{F2} \cdot C_{F2})} \quad \text{(EQ. 26)}$$

$$F_{POLE1} = \frac{1}{(2\pi \cdot RS2 \cdot C_o)} \quad \text{(EQ. 27)}$$

$$F_{ESR} = \frac{1}{(2\pi \cdot C_o \cdot R_{ESR})} \quad \text{(EQ. 28)}$$

Choose R_{VCOMP} equal or lower than the value calculated from Equation 29.

$$R_{VCOMP} = (0.7 \cdot F_{LC}) \cdot (2\pi \cdot C_o \cdot RS2) \cdot \left(\frac{5}{gm1}\right) \cdot \left(\frac{R_3 + R_4}{R_4}\right) \quad \text{(EQ. 29)}$$

Next, choose C_{VCOMP} equal or higher than the value calculated from Equation 30.

$$C_{VCOMP} = \frac{1}{(0.3 \cdot F_{LC}) \cdot (2\pi \cdot R_{VCOMP})} \quad \text{(EQ. 30)}$$

PCB Layout Considerations

Power and Signal Layers Placement on the PCB

As a general rule, power layers should be close together, either on the top or bottom of the board, with signal layers on the opposite side of the board. As an example, layer arrangement on a 4-layer board is shown in the following:

1. Top Layer: signal lines, or half board for signal lines and the other half board for power lines
2. Signal Ground
3. Power Layers: Power Ground
4. Bottom Layer: Power MOSFET, Inductors and other Power traces

Separate the power voltage and current flowing path from the control and logic level signal path. The controller IC will stay on the signal layer, which is isolated by the signal ground to the power signal traces.

Component Placement

The power MOSFET should be close to the IC so that the gate drive signal, the LGATE, UGATE, PHASE, and BOOT, traces can be short.

Place the components in such a way that the area under the IC has less noise traces with high dv/dt and di/dt, such as gate signals and phase node signals.

Signal Ground and Power Ground Connection

At minimum, a reasonably large area of copper, which will shield other noise couplings through the IC, should be used as signal ground beneath the IC. The best tie-point between the signal ground and the power ground is at the negative side of the output

capacitor on each side, where there is little noise; a noisy trace beneath the IC is not recommended.

GND and VCC Pin

At least one high quality ceramic decoupling capacitor should be used to cross these two pins. The decoupling capacitor can be put close to the IC.

LGATE Pin

This is the gate drive signal for the bottom MOSFET of the buck converter. The signal going through this trace has both high dv/dt and high di/dt, and the peak charging and discharging current is very high. These two traces should be short, wide, and away from other traces. There should be no other traces in parallel with these traces on any layer.

PGND Pin

PGND pin should be laid out to the negative side of the relevant output capacitor with separate traces. The negative side of the output capacitor must be close to the source node of the bottom MOSFET. This trace is the return path of LGATE.

PHASE Pin

This trace should be short, and positioned away from other weak signal traces. This node has a very high dv/dt with a voltage swing from the input voltage to ground. No trace should be in parallel with it. This trace is also the return path for UGATE. Connect this pin to the high-side MOSFET source.

UGATE Pin

This pin has a square shape waveform with high dv/dt. It provides the gate drive current to charge and discharge the top MOSFET with high di/dt. This trace should be wide, short, and away from other traces, similar to the LGATE.

BOOT Pin

This pin's di/dt is as high as the UGATE; therefore, this trace should be as short as possible.

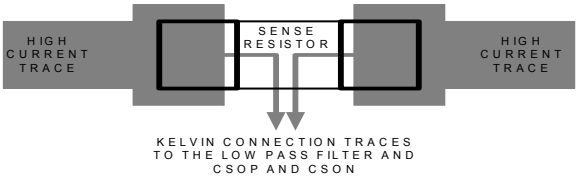


FIGURE 29. CURRENT SENSE RESISTOR LAYOUT

CSOP, CSON, CSSP and CSSN Pins

Accurate charge current and adapter current sensing is critical for good performance. The current sense resistor connects to the CSON and the CSOP pins through a low pass filter with the filter capacitor very near the IC (see Figure 4). Traces from the sense resistor should start at the pads of the sense resistor and should be routed close together, through the low pass filter and to the CSOP and CSON pins (see Figure 29). The CSON pin is also used as the battery voltage feedback. The traces should be routed away from the high dv/dt and di/dt pins like PHASE, BOOT pins. In general, the current sense resistor should be close to the IC. These guidelines should also be followed for the adapter current sense resistor and CSSP and CSSN. Other layout arrangements should be adjusted accordingly.

DCIN Pin

This pin connects to AC-adapter output voltage, and should be less noise sensitive.

Copper Size for the Phase Node

The capacitance of PHASE should be kept very low to minimize ringing. It would be best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application.

Identify the Power and Signal Ground

The input and output capacitors of the converters, the source terminal of the bottom switching MOSFET PGND should connect to the power ground. The other components should connect to signal ground. Signal and power ground are tied together at one point.

Clamping Capacitor for Switching MOSFET

It is recommended that ceramic capacitors be used closely connected to the drain of the high-side MOSFET, and the source of the low-side MOSFET. This capacitor reduces the noise and the power loss of the MOSFET.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
5/25/11	FN6978.3	Removed ICM OFFSET spec line from EC table Removed upper and lower ICM gain limits Changed Elect Specs Note 7, from: "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design" to: Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
1/14/11	FN6978.2	Revised "VDDSMB Supply" on page 11 from: "The VDDSMB input provides power to the SMBus interface. Connect VDDSMB to VCC, or apply an external supply to VDDSMB to keep the SMBus interface active while the supply to DCIN is removed. When VDDSMB is biased the internal registers are maintained. Bypass VDDSMB to GND with a 0.1µF or greater ceramic capacitor." to: "The VDDSMB input provides power to the SMBus interface. Connect VDDSMB to VCC, or apply an external supply to VDDSMB. Bypass VDDSMB to GND with a 0.1µF or greater ceramic capacitor. The typical application connects VDDSMB to the same power source as the SMBus master. This supply should be active and greater than 2.5V when either the adapter or the battery is present. ISL88731C does not function when VDDSMB is below its specified Under Voltage Lockout (UVLO) voltage. All of the SMBus registers in ISL88731C are powered by VDDSMB and are set to zero when it is below the UVLO threshold. Other functions are unpredictable when VDDSMB is below the UVLO threshold."
12/9/10		VDDSMB UVLO Hysteresis limits updated to reflect actual test results From (100, 150, 200 mV) to (40, 100, 150mV) Added to Pin 3 VREF Pin Description on page 3 "It is internally compensated. Do not connect a decoupling capacitor."
12/3/10		-Converted to New Intersil Template -Updated Related Literature's Application Note's Title to match application note -Changed copyright to legal's suggested verbiage -On page 2, Figure 3, Functional Block Diagram, ACOK comparator input changed from REF to 3.2V. "REF" was a typo. -Added Eval board to ordering information -ACOK Leakage Current Test condition in Electrical Spec Table on page 7 changed from ACIN = 2.5V to 3.7V. 3.7V has always been the test condition on this part. -Removed Note: Limits established by characterization and are not production tested (no longer an Intersil standard) and all references to it in switching regulators UGate and Lgate -Changed Note: Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. to new standard note: Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8/23/10	FN6978.1	Added "Overvoltage Protection" on page 12 and Figure 17"OVERVOLTAGE PROTECTION IN ISL88731C" to page 12.
3/8/10	FN6978.0	Initial release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL88731C

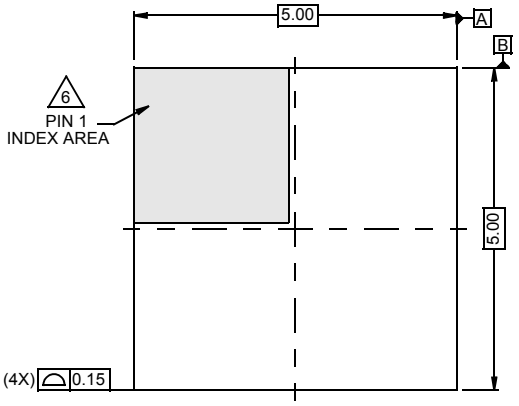
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

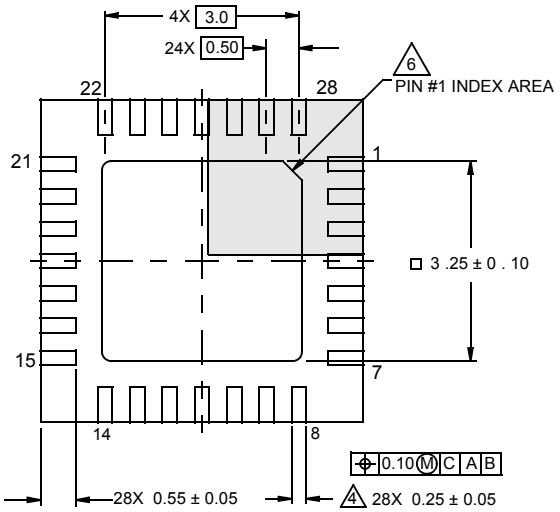
Package Outline Drawing

L28.5x5B

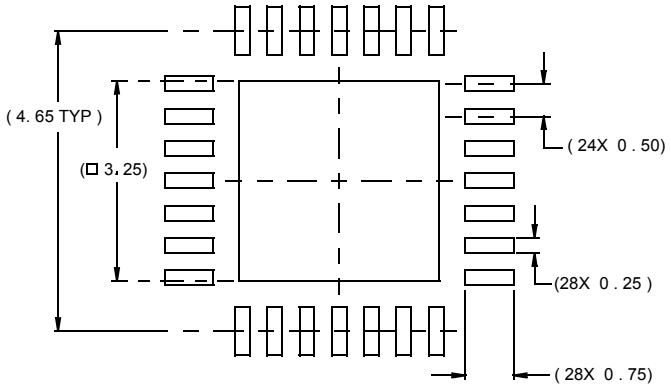
28 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 10/07



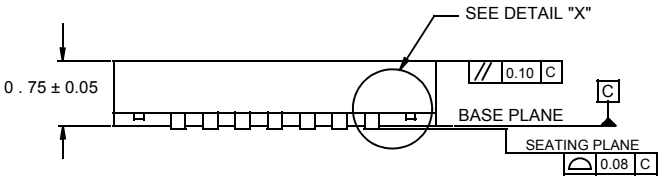
TOP VIEW



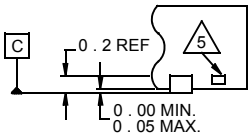
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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