



TRUTH TABLE (positive logic)		
LED	ENABLE	OUTPUT
On	H	L
Off	H	H
On	L	H
Off	L	H
On	NC	L
Off	NC	H

ABSOLUTE MAXIMUM RATINGS (T _{amb} = 25 °C, unless otherwise specified)				
PARAMETER	CONDITIONS	SYMBOL	VALUE	UNIT
INPUT				
Average forward current (single channel)		I _F	20	mA
Average forward current (per channel for dual channel)		I _F	15	mA
Reverse input voltage		V _R	5	V
Enable input voltage		V _E	V _{CC} + 0.5 V	V
Enable input current		I _E	5	mA
Surge current	t = 100 μs	I _{FSM}	200	mA
Output power dissipation (single channel)		P _{diss}	35	mW
Output power dissipation (per channel for dual channel)		P _{diss}	25	mW
OUTPUT				
Supply voltage	1 min maximum	V _{CC}	7	V
Output current		I _O	50	mA
Output voltage		V _O	7	V
Output power dissipation (single channel)		P _{diss}	85	mW
Output power dissipation (per channel for dual channel)		P _{diss}	60	mW
COUPLER				
Storage temperature		T _{stg}	-55 to +150	°C
Operating temperature		T _{amb}	-40 to +100	°C
Lead solder temperature	for 10 s		260	°C
Solder reflow temperature			260	°C

Note

- Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability.

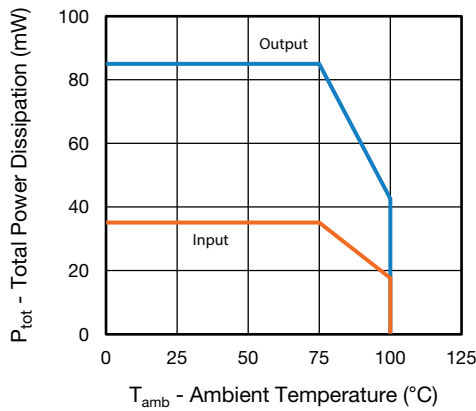


Fig. 1 - Total Power Dissipation vs. Ambient Temperature (single channel)

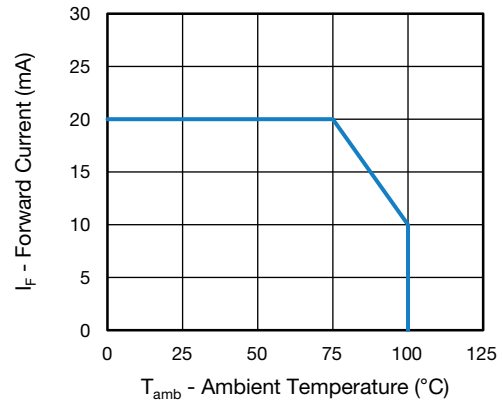


Fig. 3 - Forward Current vs. Ambient Temperature (single channel)

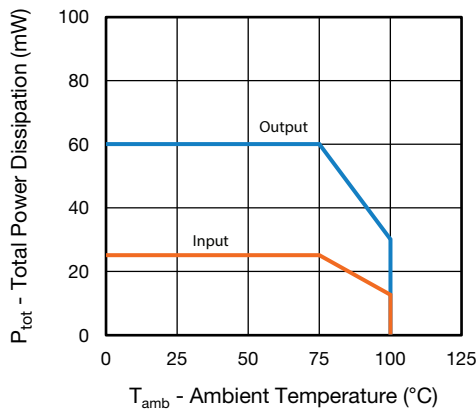


Fig. 2 - Total Power Dissipation vs. Ambient Temperature (dual channel)

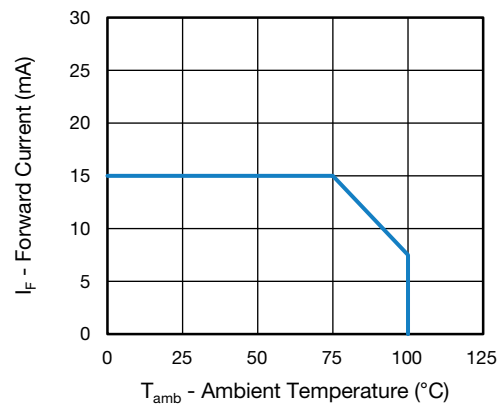


Fig. 4 - Forward Current vs. Ambient Temperature (dual channel)

RECOMMENDED OPERATING CONDITIONS					
PARAMETER	TEST CONDITION	SYMBOL	MIN.	MAX.	UNIT
Operating temperature		T _{amb}	-40	100	°C
Supply voltage		V _{CC}	4.5	5.5	V
Input current low level		I _{FL}	0	250	μA
Input current high level		I _{FH}	5	15	mA
Logic high enable voltage		V _{EH}	2	V _{CC}	V
Logic low enable voltage		V _{EL}	0	0.8	V
Output pull up resistor		R _L	330	4K	Ω
Fanout	R _L = 1 kΩ	N	-	5	-



ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
INPUT						
Input forward voltage	$I_F = 10\text{ mA}$	V_F	1.1	1.4	1.7	V
Reverse current	$V_R = 5\text{ V}$	I_R	-	0.01	10	μA
Input capacitance	$f = 1\text{ MHz}, V_F = 0\text{ V}$	C_I	-	55	-	pF
OUTPUT						
High level supply current (single channel)	$V_E = 0.5\text{ V}, I_F = 0\text{ mA}$	I_{CCH}	-	4.1	7	mA
	$V_E = V_{CC}, I_F = 0\text{ mA}$	I_{CCH}	-	3.3	6	mA
High level supply current (dual channel)	$I_F = 0\text{ mA}$	I_{CCH}	-	6.5	12	mA
Low level supply current (single channel)	$V_E = 0.5\text{ V}, I_F = 10\text{ mA}$	I_{CCL}	-	4	7	mA
	$V_E = V_{CC}, I_F = 10\text{ mA}$	I_{CCL}	-	3.3	6	mA
Low level supply current (dual channel)	$I_F = 10\text{ mA}$	I_{CCL}	-	6.5	12	mA
High level output current	$V_E = 2\text{ V}, V_{CC} = 5.5\text{ V}, I_F = 250\text{ }\mu\text{A}$	I_{OH}	-	0.002	1	μA
Low level output voltage	$V_E = 2\text{ V}, I_F = 5\text{ mA}, I_{OL}(\text{sinking}) = 13\text{ mA}$	V_{OL}	-	0.2	0.6	V
Input threshold current	$V_E = 2\text{ V}, V_{CC} = 5.5\text{ V}, I_{OL}(\text{sinking}) = 13\text{ mA}$	I_{TH}	-	2.4	5	mA
High level enable current	$V_E = 2\text{ V}$	I_{EH}	-	-0.6	-1.6	mA
Low level enable current	$V_E = 0.5\text{ V}$	I_{EL}	-	-0.8	-1.6	mA
High level enable voltage		V_{EH}	2	-	-	V
Low level enable voltage		V_{EL}	-	-	0.8	V

Note

- Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

SWITCHING CHARACTERISTICS						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Propagation delay time to high output level	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$	t_{PLH}	20	48	75 ⁽¹⁾	ns
		t_{PLH}	-	-	100	ns
Propagation delay time to low output level	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$	t_{PHL}	25	50	75 ⁽¹⁾	ns
		t_{PHL}	-	-	100	ns
Pulse width distortion	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$	$ t_{PHL} - t_{PLH} $	-	2.9	35	ns
Propagation delay skew	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$	t_{PSK}	-	8	40	ns
Output rise time (10 % to 90 %)	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$	t_r	-	23	-	ns
Output fall time (90 % to 10 %)	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$	t_f	-	7	-	ns
Propagation delay time of enable from V_{EH} to V_{EL}	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}, V_{EL} = 0\text{ V}, V_{EH} = 3\text{ V}$	t_{ELH}	-	12	-	ns
Propagation delay time of enable from V_{EL} to V_{EH}	$R_L = 350\text{ }\Omega, C_L = 15\text{ pF}, V_{EL} = 0\text{ V}, V_{EH} = 3\text{ V}$	t_{EHL}	-	11	-	ns

Notes

- Over recommended temperature ($T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+100\text{ }^{\circ}\text{C}$), $V_{CC} = 5\text{ V}, I_F = 7.5\text{ mA}$ unless otherwise specified. All typicals at $T_{amb} = 25\text{ }^{\circ}\text{C}, V_{CC} = 5\text{ V}$.
- (1) 75 ns applies to the 6N137 only, a JEDEC® registered specification

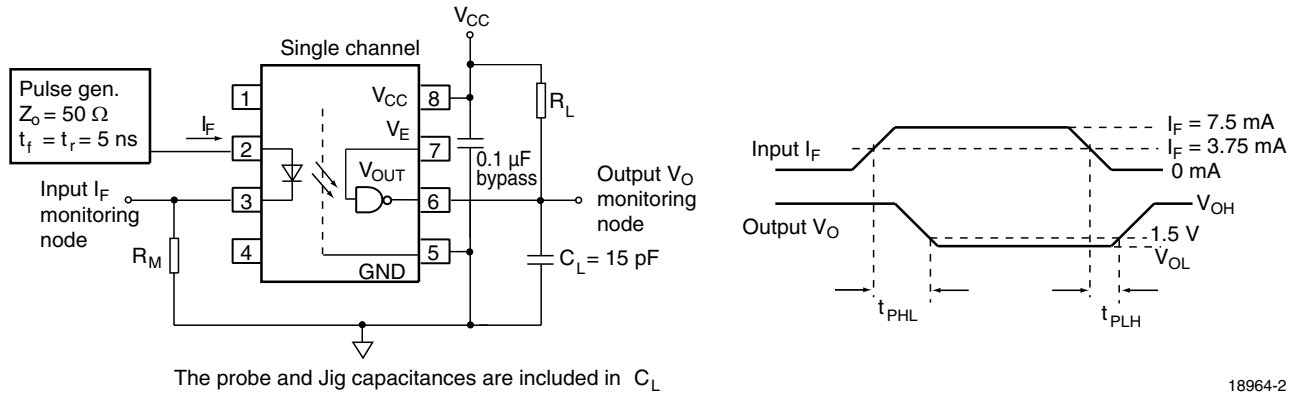


Fig. 5 - Single Channel Test Circuit for t_{PLH} , t_{PHL} , t_r and t_f

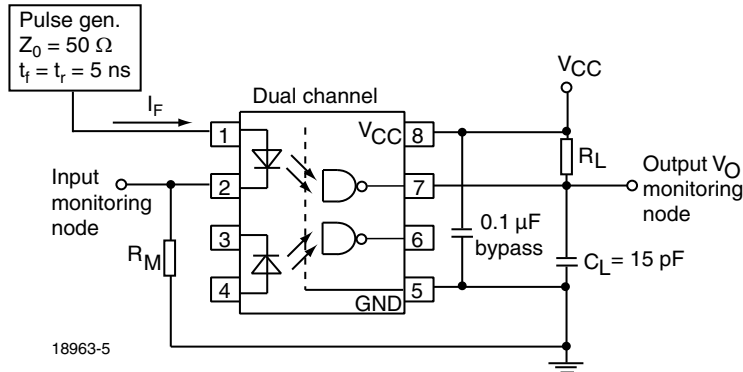


Fig. 6 - Dual Channel Test Circuit for t_{PLH} , t_{PHL} , t_r and t_f

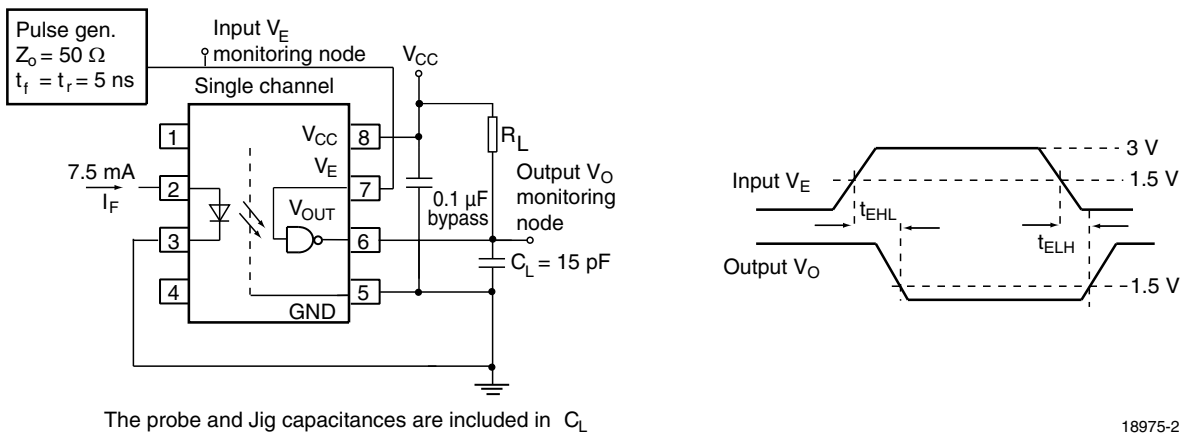


Fig. 7 - Single Channel Test Circuit for t_{EHL} and t_{ELH}

COMMON MODE TRANSIENT IMMUNITY ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Common mode transient immunity	$ V_{CM} = 10\text{ V}$, $V_{CC} = 5\text{ V}$, $I_F = 0\text{ mA}$, $V_{O(min.)} = 2\text{ V}$, $R_L = 350\text{ }\Omega$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ (1)	$ CM_H $	1000	-	-	$\text{V}/\mu\text{s}$
	$ V_{CM} = 50\text{ V}$, $V_{CC} = 5\text{ V}$, $I_F = 0\text{ mA}$, $V_{O(min.)} = 2\text{ V}$, $R_L = 350\text{ }\Omega$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ (2)	$ CM_H $	5000	10 000	-	$\text{V}/\mu\text{s}$
	$ V_{CM} = 1\text{ kV}$, $V_{CC} = 5\text{ V}$, $I_F = 0\text{ mA}$, $V_{O(min.)} = 2\text{ V}$, $R_L = 350\text{ }\Omega$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ (3)	$ CM_H $	15 000	25 000	-	$\text{V}/\mu\text{s}$
	$ V_{CM} = 10\text{ V}$, $V_{CC} = 5\text{ V}$, $I_F = 7.5\text{ mA}$, $V_{O(max.)} = 0.8\text{ V}$, $R_L = 350\text{ }\Omega$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ (1)	$ CM_L $	1000	-	-	$\text{V}/\mu\text{s}$
	$ V_{CM} = 50\text{ V}$, $V_{CC} = 5\text{ V}$, $I_F = 7.5\text{ mA}$, $V_{O(max.)} = 0.8\text{ V}$, $R_L = 350\text{ }\Omega$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ (2)	$ CM_L $	5000	10 000	-	$\text{V}/\mu\text{s}$
	$ V_{CM} = 1\text{ kV}$, $V_{CC} = 5\text{ V}$, $I_F = 7.5\text{ mA}$, $V_{O(max.)} = 0.8\text{ V}$, $R_L = 350\text{ }\Omega$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ (3)	$ CM_L $	15 000	25 000	-	$\text{V}/\mu\text{s}$

Notes

- (1) For 6N137 and VO2630
 (2) For VO2601 and VO2631
 (3) For VO2611 and VO4661

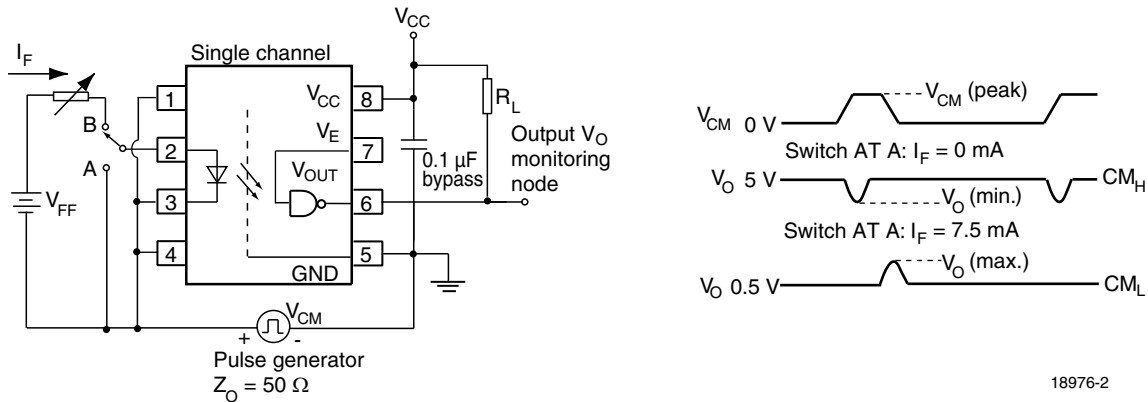


Fig. 8 - Single Channel Test Circuit for Common Mode Transient Immunity

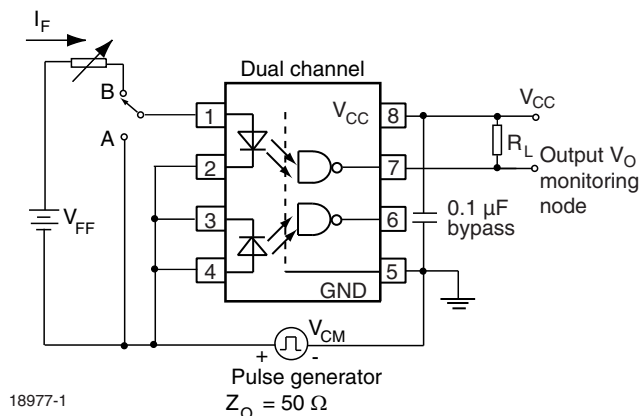


Fig. 9 - Dual Channel Test Circuit for Common Mode Transient Immunity

SAFETY AND INSULATION RATINGS				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Climatic classification	According to IEC 68 part 1		40 / 100 / 21	
Pollution degree	According to DIN VDE 0109		2	
Comparative tracking index	Insulation group IIIa	CTI	175	
Maximum rated withstanding isolation voltage	According to UL1577, t = 1 min	V_{ISO}	5300	V_{RMS}
Maximum transient isolation voltage	According to DIN EN 60747-5-5	V_{IOTM}	8000	V_{peak}
Maximum repetitive peak isolation voltage	According to DIN EN 60747-5-5	V_{IORM}	890	V_{peak}
Isolation resistance	$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{IO} = 500\text{ V}$	R_{IO}	$\geq 10^{12}$	Ω
	$T_{amb} = 100\text{ }^{\circ}\text{C}$, $V_{IO} = 500\text{ V}$	R_{IO}	$\geq 10^{11}$	Ω
Output safety power		P_{SO}	500	mW
Input safety current		I_{SI}	300	mA
Input safety temperature		T_S	175	$^{\circ}\text{C}$
Creepage distance	DIP-8		≥ 7	mm
Clearance distance			≥ 7	mm
Creepage distance	DIP-8, 400 mil (option 6)		≥ 8	mm
Clearance distance			≥ 8	mm
Creepage distance	SMD-8 (option 7)		≥ 8	mm
Clearance distance			≥ 8	mm
Creepage distance	SMD-8 (option 9)		≥ 8	mm
Clearance distance			≥ 8	mm
Insulation thickness		DTI	≥ 0.4	mm

Note

- As per IEC 60747-5-5, § 7.4.3.8.2, this optocoupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of protective circuits.

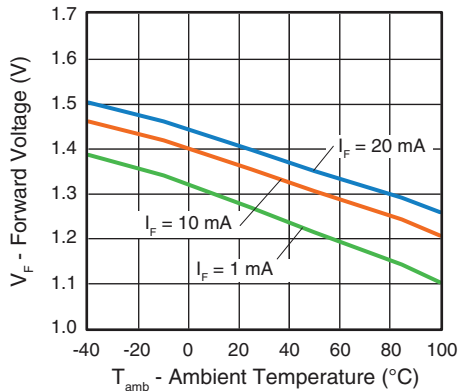
TYPICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)


Fig. 10 - Forward Voltage vs. Ambient Temperature

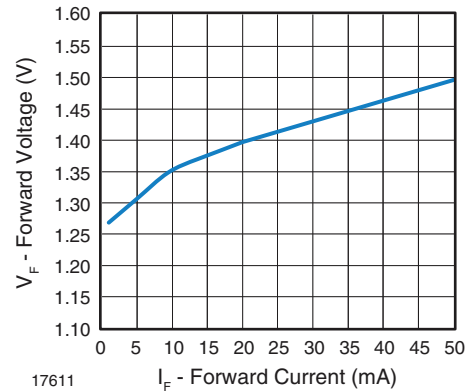


Fig. 11 - Forward Voltage vs. Forward Current

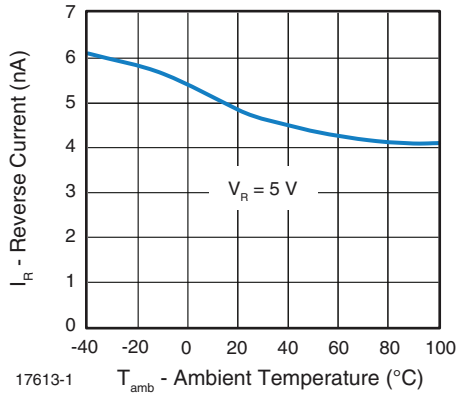


Fig. 12 - Reverse Current vs. Ambient Temperature

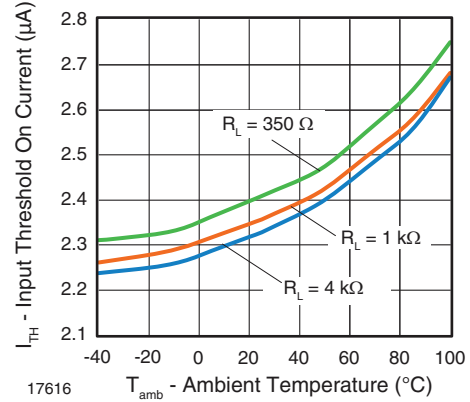


Fig. 15 - Input Threshold On Current vs. Ambient Temperature

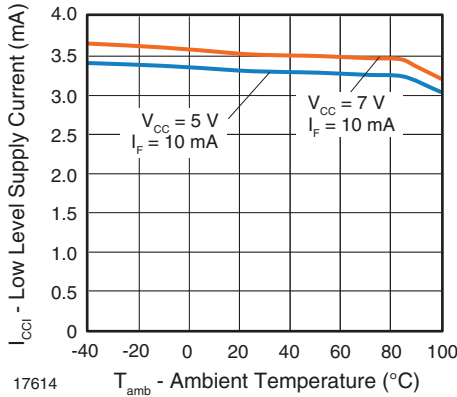


Fig. 13 - Low Level Supply Current vs. Ambient Temperature

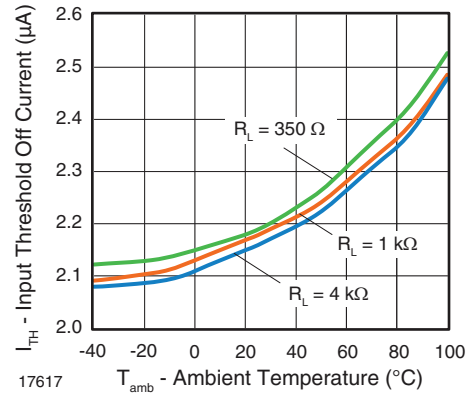


Fig. 16 - Input Threshold Off Current vs. Ambient Temperature

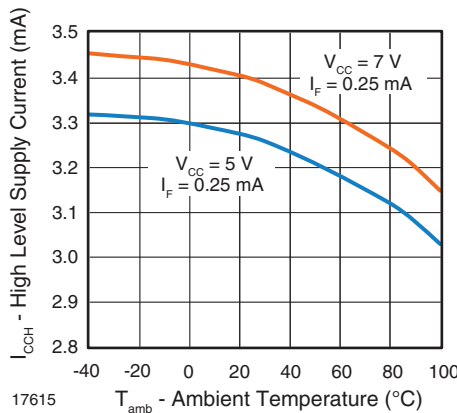


Fig. 14 - High Level Supply Current vs. Ambient Temperature

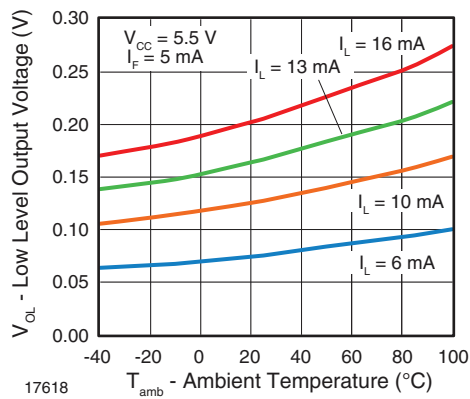


Fig. 17 - Low Level Output Voltage vs. Ambient Temperature

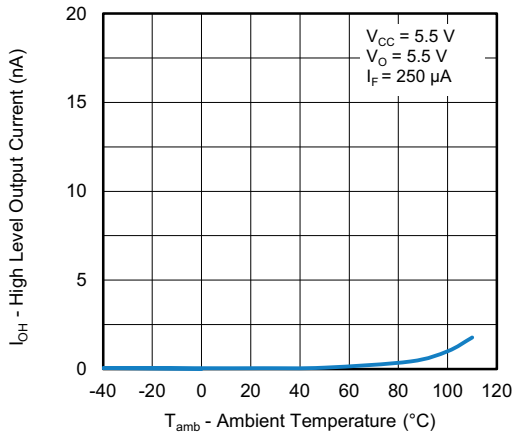


Fig. 18 - Low Level Output Current vs. Ambient Temperature

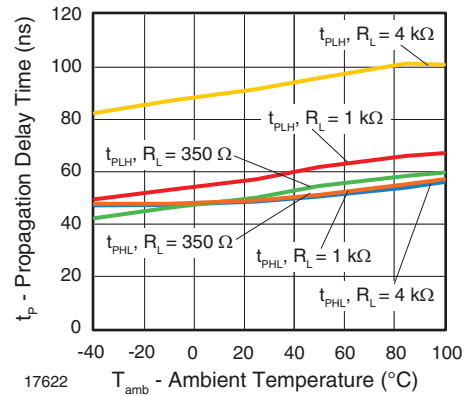


Fig. 21 - Propagation Delay vs. Ambient Temperature

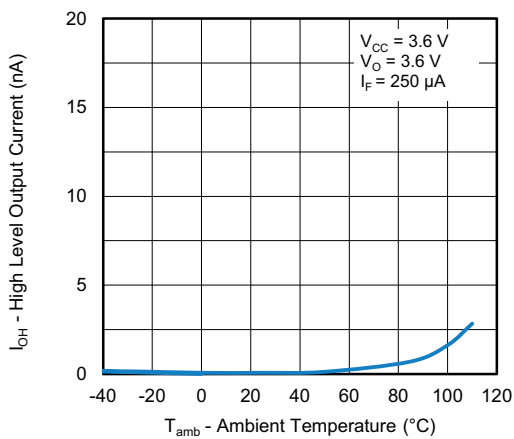


Fig. 19 - High Level Output Current vs. Ambient Temperature

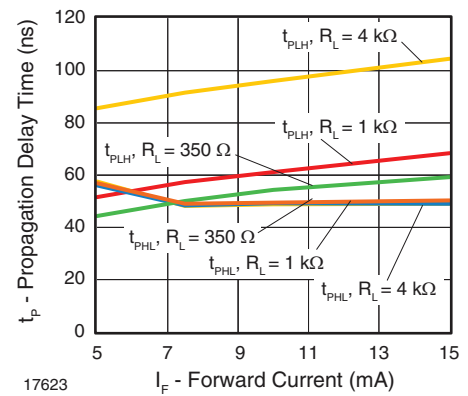


Fig. 22 - Propagation Delay vs. Forward Current

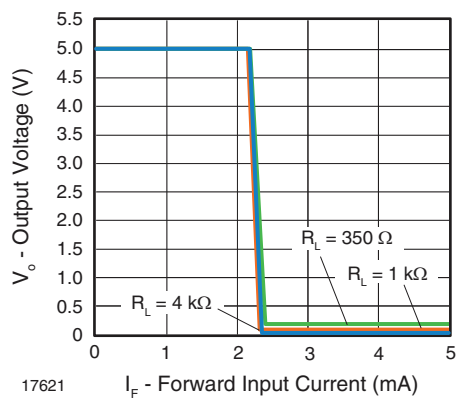


Fig. 20 - Output Voltage vs. Forward Input Current

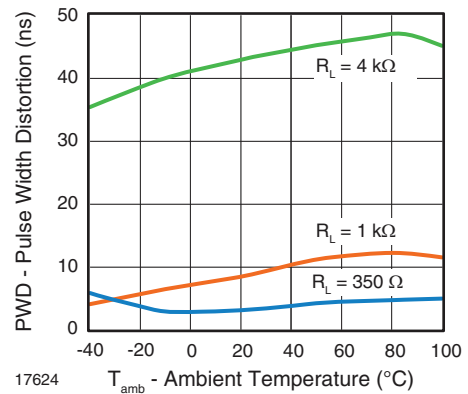


Fig. 23 - Pulse Width Distortion vs. Ambient Temperature

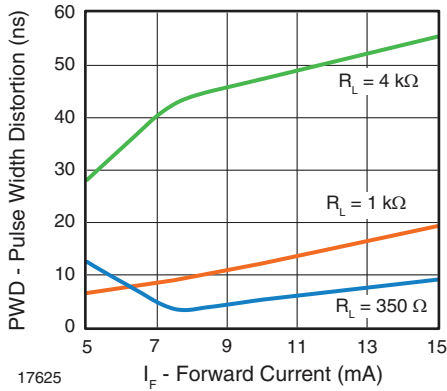


Fig. 24 - Pulse Width Distortion vs. Forward Current

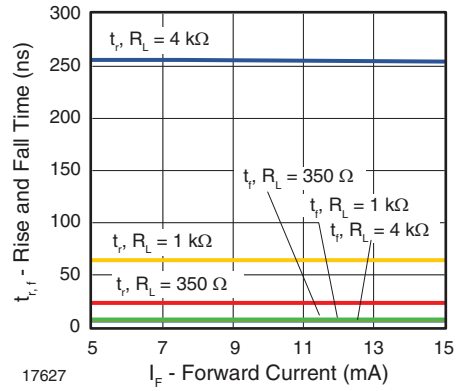


Fig. 26 - Rise and Fall Time vs. Forward Current

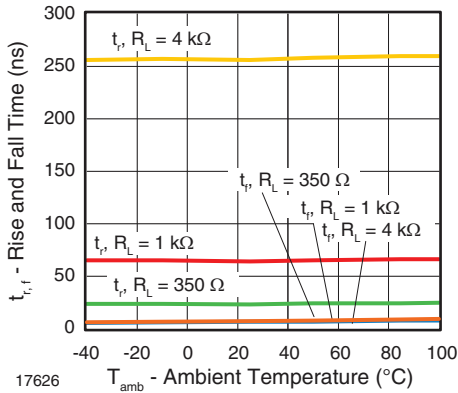


Fig. 25 - Rise and Fall Time vs. Ambient Temperature

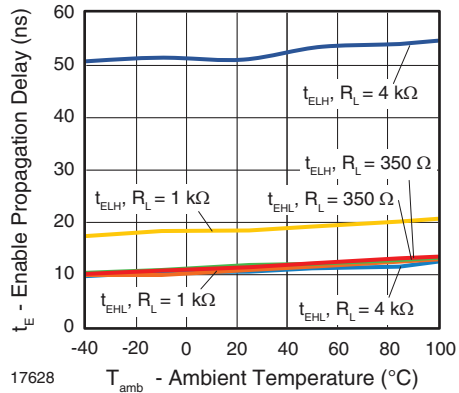
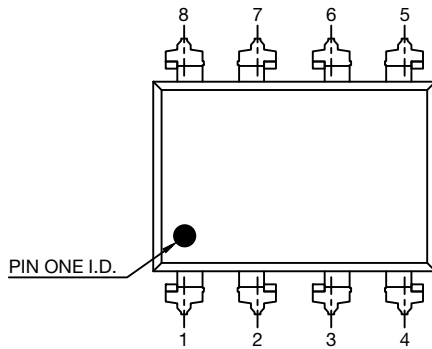
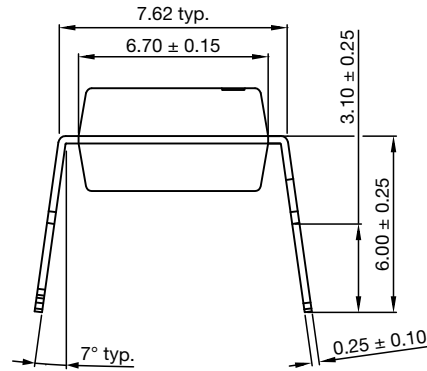
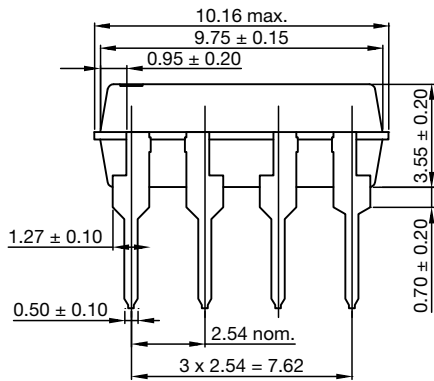


Fig. 27 - Enable Propagation Delay vs. Ambient Temperature

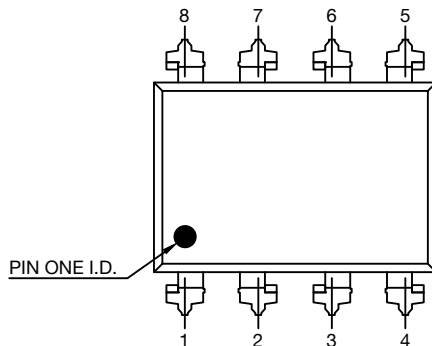
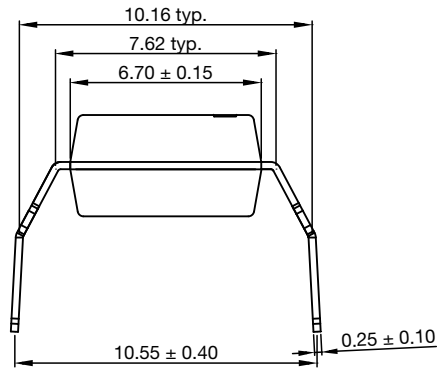
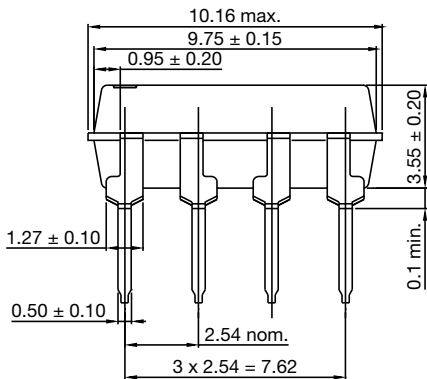


PACKAGE DIMENSIONS (in millimeters)

DIP-8

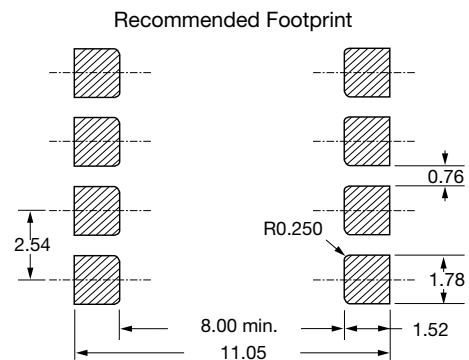
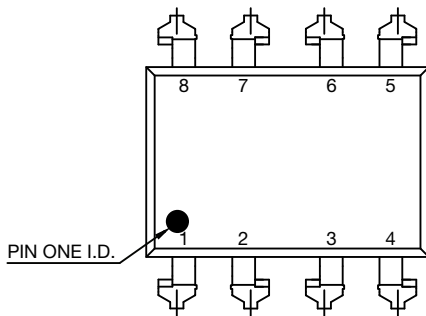
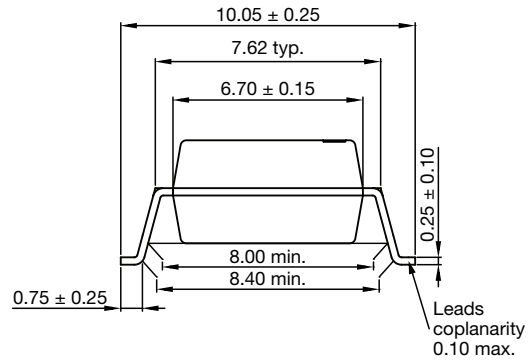
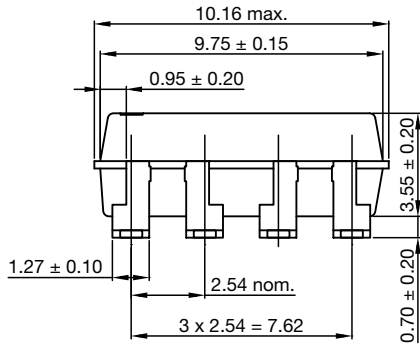


DIP-8, 400 mil (option 6)

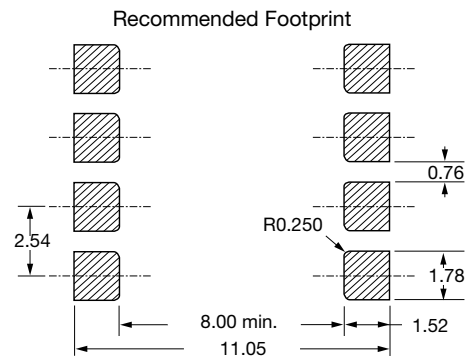
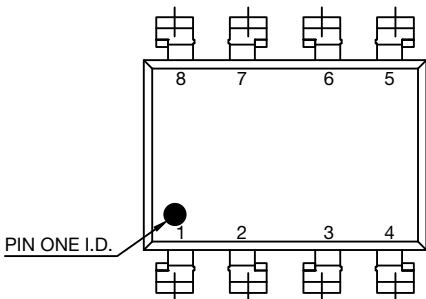
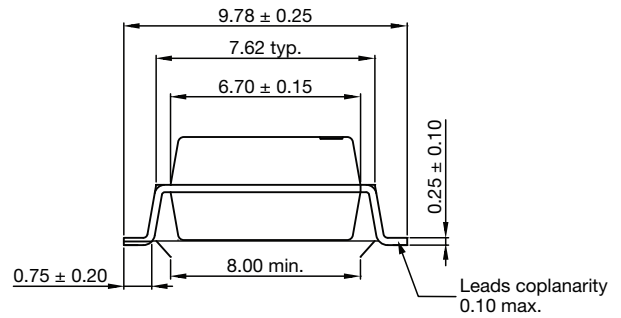
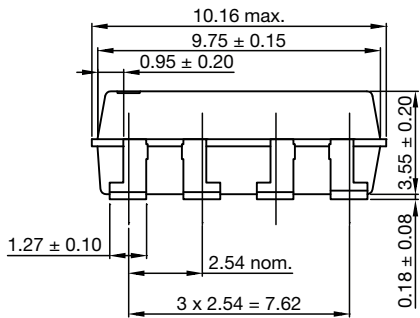




SMD-8 (option 7)



SMD-8 (option 9)



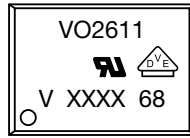
PACKAGE MARKING


Fig. 28 - Example of VO2611-X017T

Notes

- XXXX = LMC (lot marking code)
- VDE logo is only marked on option 1 parts
- Tape and reel suffix (T) is not part of the package marking

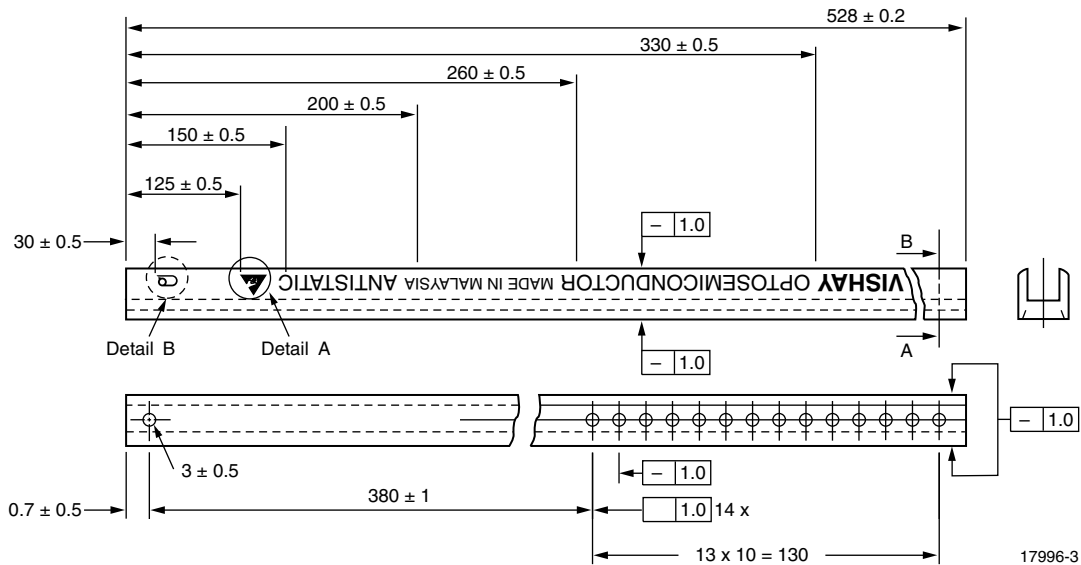
PACKING INFORMATION (in millimeters)
Tube


Fig. 29 - Shipping Tube Specifications for DIP-8 Packages

DEVICES PER TUBS			
TYPE	UNITS/TUBE	TUBES/BOX	UNITS/BOX
DIP-8	50	40	2000

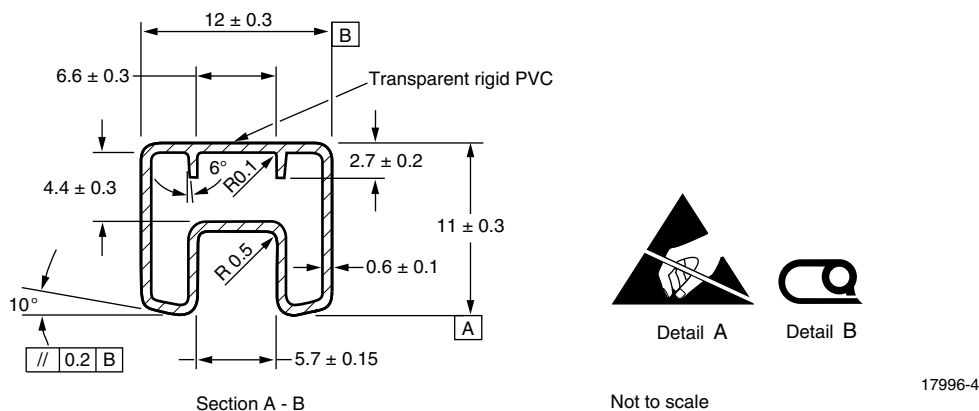
DIP-8


Fig. 30 - Tube Shipping Medium

DIP-8, 400 mil (option 6)

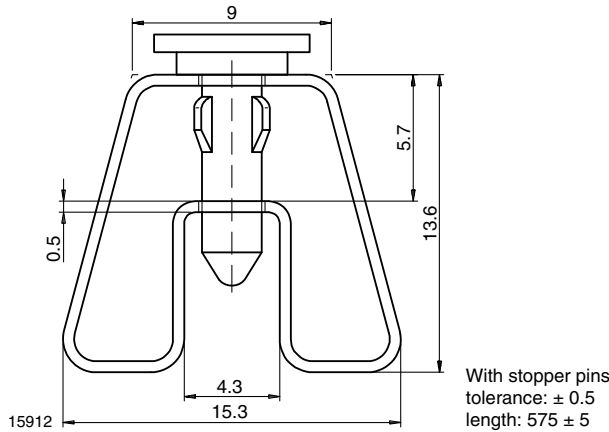


Fig. 31 - Tube Shipping Medium

Tape and Reel

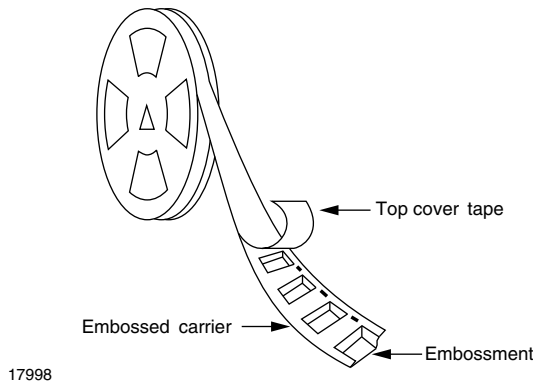


Fig. 32 - Tape and Reel Shipping Medium

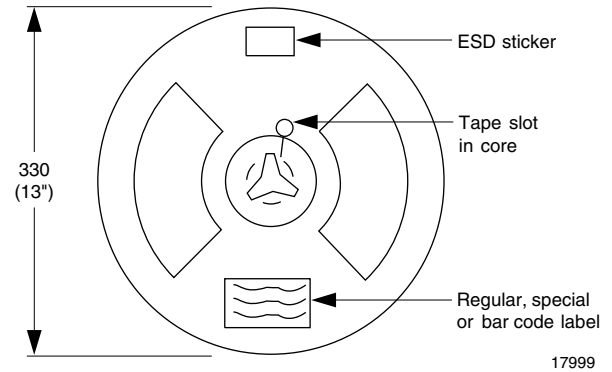


Fig. 33 - Tape and Reel Shipping Medium

SMD-8 (option 7)

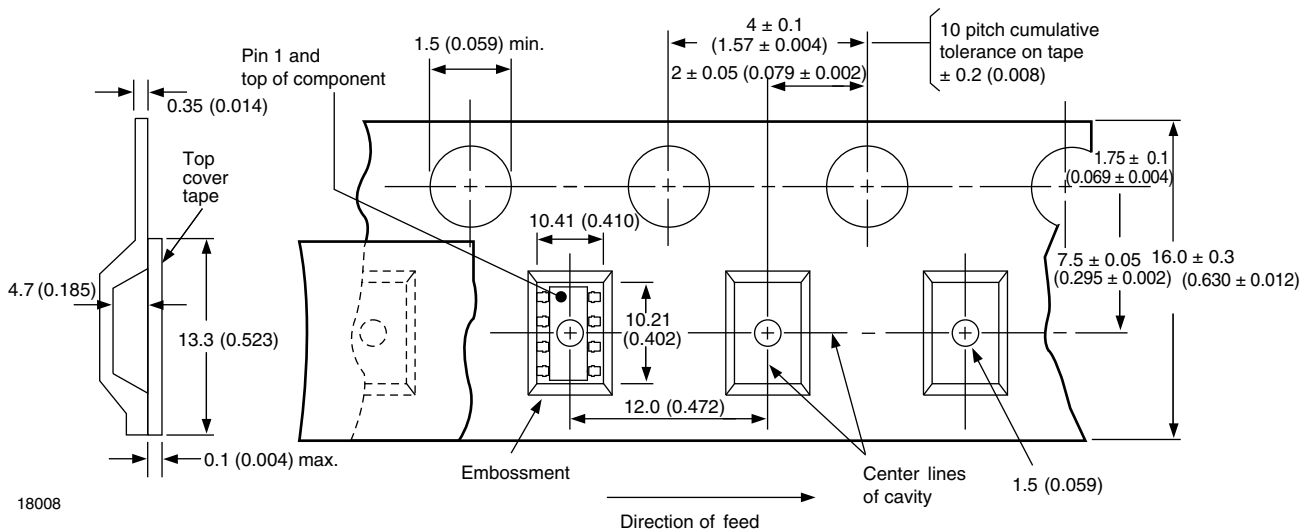


Fig. 34 - Tape and Reel Packing (1000 pieces on Reel)

SMD-8 (option 9)

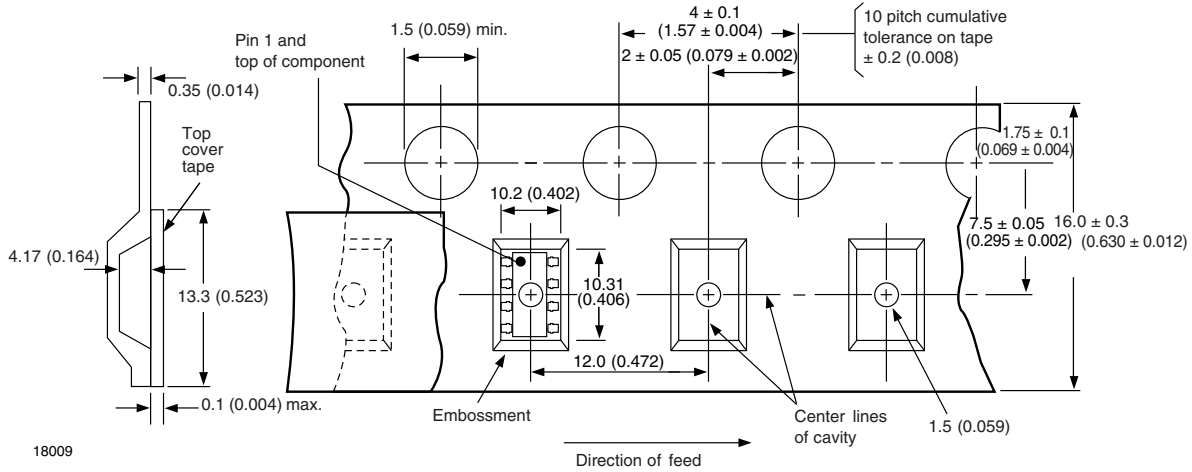


Fig. 35 - Tape and Reel Shipping Medium

SOLDER PROFILES

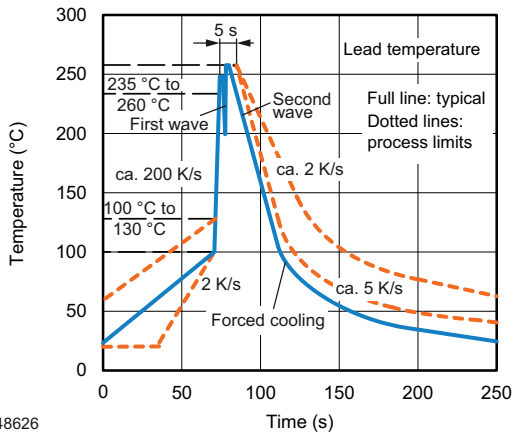


Fig. 36 - Wave Soldering Double Wave Profile According to J-STD-020 for DIP Devices

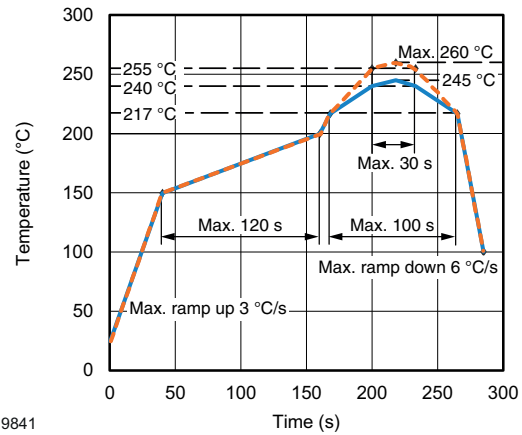


Fig. 37 - Lead (Pb)-free Reflow Solder Profile According to J-STD-020 for SMD Devices

HANDLING AND STORAGE CONDITIONS

ESD level: HBM class 2

Floor life: unlimited

Conditions: $T_{amb} < 30\text{ °C}$, RH < 85 %

Moisture sensitivity level 1, according to J-STD-020



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