AsahiKASEI
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AK4682

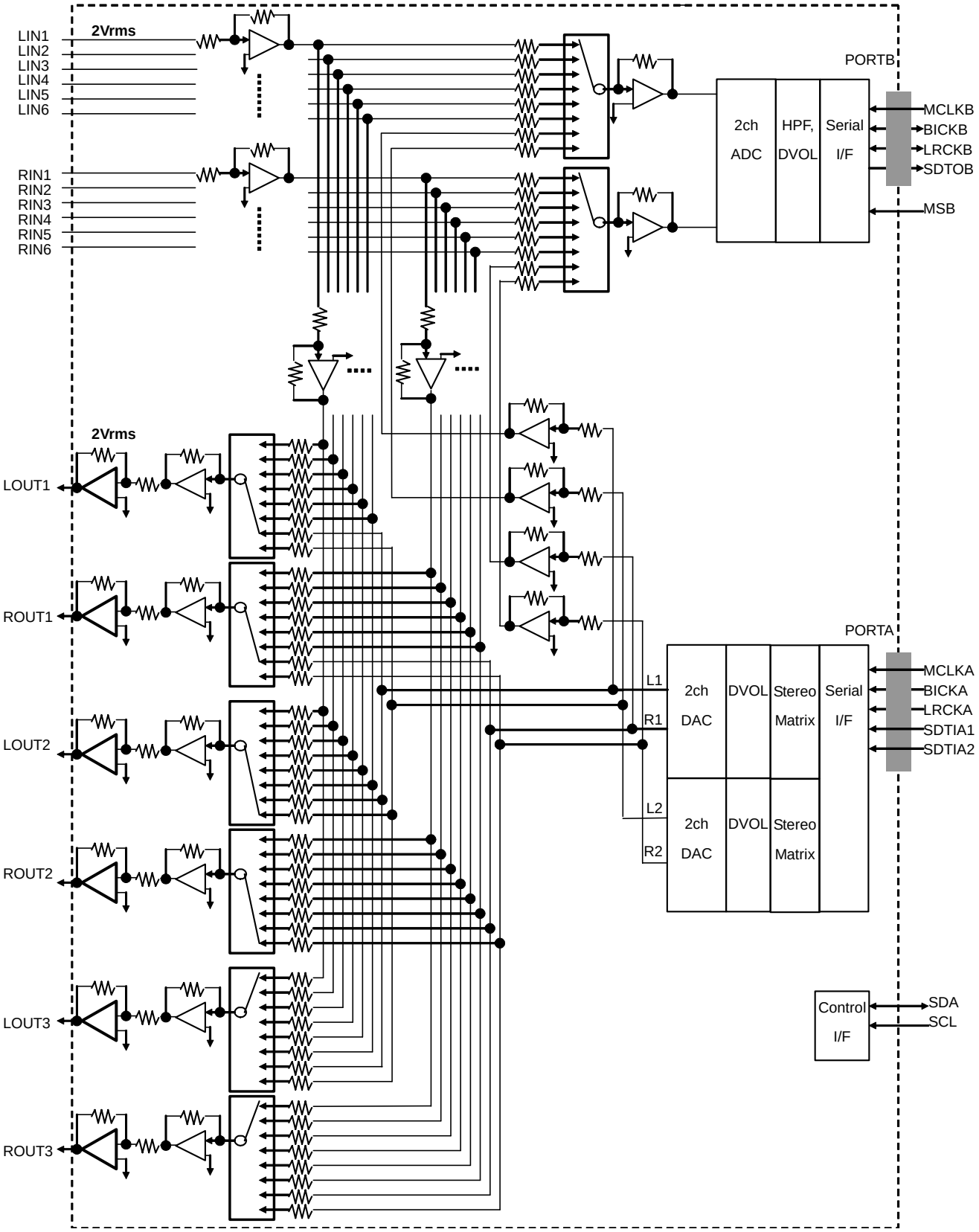
Multi-channel CODEC with 2Vrms Stereo Selector

GENERAL DESCRIPTION

The AK4682 is a single chip CODEC that includes two channels of ADC and four channels of DAC. The ADC outputs 24bit data and the DAC accepts up to 24bit input data. The ADC has the Enhanced Dual Bit architecture with wide dynamic range. The DAC introduces the new developed Advanced Multi-Bit architecture, and achieves wider dynamic range and lower outband noise. The AK4682 integrates stereo selector supporting 2Vrms I/O. The AK4682 has a dynamic range of 96dB for ADC, 102dB for DAC and is well suited for digital TV and home theater system.

FEATURES

- ☐ **ADC/DAC part**
  - ☐ **Asynchronous ADC/DAC Operation**
  - ☐ **8:1 Stereo Selector for ADC Input**
  - ☐ **8:3 Stereo Selector with 2Vrms Output Buffer**
  - ☐ **2-channel 24bit ADC**
    - **64x Oversampling**
    - **Sampling Rate up to 48kHz**
    - **Linear Phase Digital Anti-Alias Filter**
    - **Single-Ended Input**
    - **S/(N+D): 88dB**
    - **Dynamic Range, S/N: 96dB**
    - **Digital HPF for Offset Cancellation**
    - **Channel Independent Digital Volume (+24/-103dB, 0.5dB/step)**
    - **Soft Mute**
  - ☐ **4-channel 24bit DAC**
    - **128x Oversampling**
    - **Sampling Rate up to 192kHz**
    - **24bit 8 times Digital Filter**
    - **S/(N+D): 86dB**
    - **Dynamic Range, S/N: 102dB**
    - **Channel Independent Digital Volume (+12/-115dB, 0.5dB/step)**
    - **Soft Mute**
    - **De-emphasis Filter**
    - **Output Mode: Stereo, Mono, Reverse, Mute**
  - ☐ **High Jitter Tolerance**
- ☐ **TTL Level Digital I/F**
- ☐ **External Master Clock Input:**
  - **256fs, 384fs, 512fs 768fs (fs=32kHz ~ 48kHz)**
  - **128fs, 192fs, 256fs 384fs (fs=64kHz ~ 96kHz)**
  - **128fs, 192fs (fs=120kHz ~ 192kHz)**
- ☐ **2 Audio Serial I/F (PORTA, PORTB)**
  - **Master/Slave mode (for PORTB)**
  - **I/F format**
    - **PORTA: Left(24 bit)/Right(20/24 bit) justified, I^2S, TDM**
    - **PORTB: Left justified, I^2S**
- ☐ **I^2C Bus μP I/F for mode setting**
- ☐ **Operating Voltage:**
  - **Digital I/O: 2.7V ~ 5.25V,**
  - **Analog: 4.75V ~ 5.25V and 8.5V ~ 12.6V**
- ☐ **Package: 48pin LQFP (0.5mm pitch)**

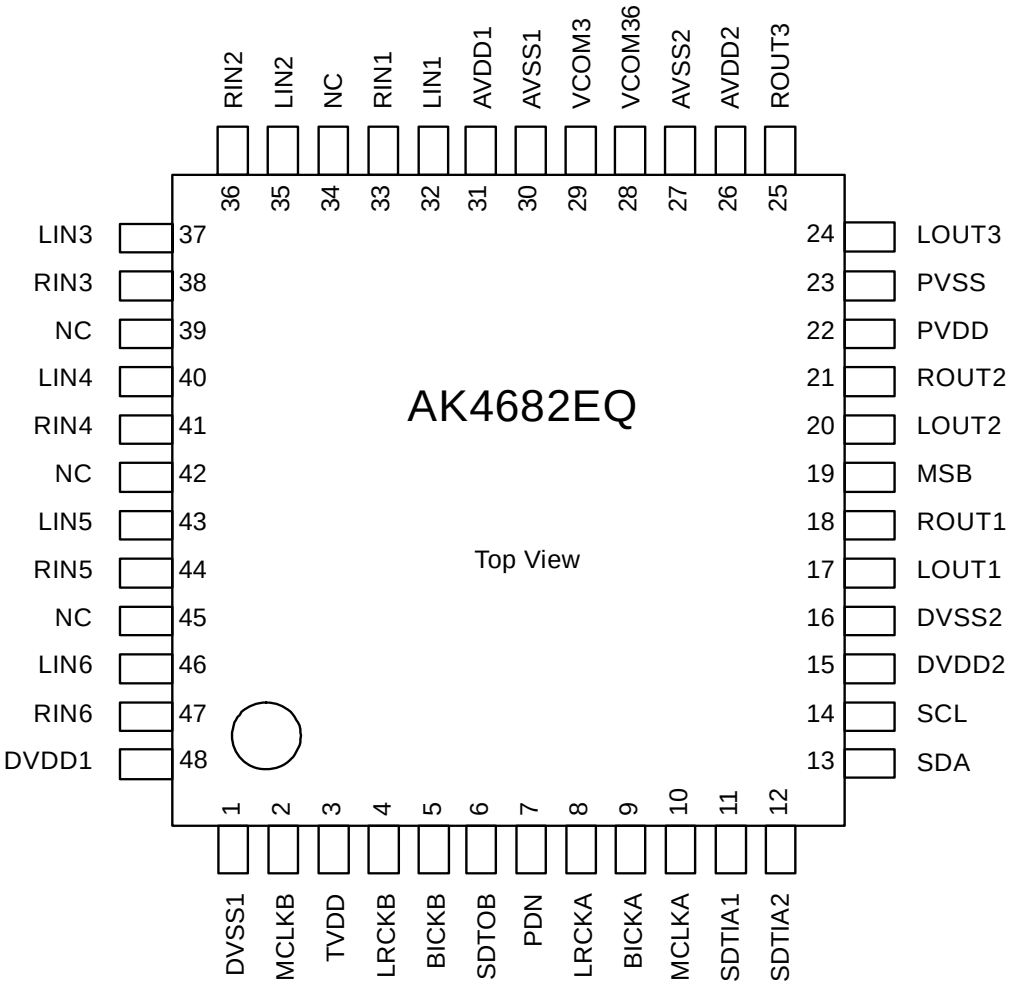


AK4682 Block Diagram

■ Ordering Guide

AK4682EQ	-20 ~ +85°C	48pin LQFP (0.5mm pitch)
AKD4682	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DVSS1	-	ADC Digital Ground Pin, 0V
2	MCLKB	I	ADC Master Clock Input Pin
3	TVDD	-	Output Buffer Power Supply Pin, 2.7V~5.25V
4	LRCKB	I/O	Channel Clock B Pin
5	BICKB	I/O	Audio Serial Data Clock B Pin
6	SDTOB	O	Audio Serial Data Output B Pin
7	PDN	I	Power-Down Mode & Reset Pin When "L", the AK4682 is powered-down, all registers are reset. And then all digital output pins go "L". The AK4682 must be reset once upon power-up.
8	LRCKA	I	Input Channel Clock A Pin
9	BICKA	I	Audio Serial Data Clock A Pin
10	MCLKA	I	DAC Master Clock Input Pin
11	SDTIA1	I	Audio Serial Data Input A1 Pin
12	SDTIA2	I	Audio Serial Data Input A2 Pin
13	SDA	I/O	Control Data Pin
14	SCL	I	Control Data Clock Pin
15	DVDD2	-	DAC Digital Power Supply Pin, 4.75V~5.25V
16	DVSS2	-	DAC Digital Ground Pin, 0V
17	LOUT1	O	Lch Analog Output Pin1
18	ROUT1	O	Rch Analog Output Pin1
19	MSB	I	PORTB Master Mode Select Pin. "L"(connected to the ground): Master/Slave mode. ORed with MSB bit. "H"(connected to DVDD2) : Master mode.
20	LOUT2	O	Lch Analog Output Pin2
21	ROUT2	O	Rch Analog Output Pin2
22	PVDD	-	Output Buffer Power Supply Pin, 8.5V ~ 12.6V.
23	PVSS	-	Output Buffer Ground Pin, 0V.
24	LOUT3	O	Lch Analog Output Pin 3
25	ROUT3	O	Rch Analog Output Pin 3
26	AVDD2	-	DAC Analog Power Supply Pin, 4.75V~5.25V
27	AVSS2	-	DAC Analog Ground Pin, 0V
28	VCOM36	-	Common Voltage Output Pin for Output Buffer. AVDD2 x 0.734(typ). 10μF capacitor should be connected to AVSS2 externally.
29	VCOM3	-	DAC/ADC Common Voltage Output Pin. AVDD2 x 0.6(typ). 10μF capacitor should be connected to AVSS2 externally.
30	AVSS1	-	ADC Analog Ground Pin, 0V
31	AVDD1	-	ADC Analog Power Supply Pin, 4.75V~5.25V
32	LIN1	I	Lch Input 1 Pin
33	RIN1	I	Rch Input 1 Pin
34	NC	-	No Connection. No internal bonding. This pin should be connected to the ground.
35	LIN2	I	Lch Input 2 Pin
36	RIN2	I	Rch Input 2 Pin
37	LIN3	I	Lch Input 3 Pin
38	RIN3	I	Rch Input 3 Pin
39	NC	-	No Connection. No internal bonding. This pin should be connected to the ground.
40	LIN4	I	Lch Input 4 Pin
41	RIN4	I	Rch Input 4 Pin
42	NC	-	No Connection. No internal bonding. This pin should be connected to the ground.

PIN/FUNCTION (continued)

No.	Pin Name	I/O	Function
43	LIN5	I	Lch Input 5 Pin
44	RIN5	I	Rch Input 5 Pin
45	NC	-	No Connection. No internal bonding. This pin should be connected to the ground.
46	LIN6	I	Lch Input 6 Pin
47	RIN6	I	Rch Input 6 Pin
48	DVDD1	-	ADC Digital Power Supply Pin, 4.75V~5.25V

Note: All digital input pins must not be left floating.
Note: Analog input pins (LIN1, RIN1, LIN2, RIN2, LIN3, RIN3, LIN4, RIN4, LIN5, RIN5, LIN6, RIN6 pin) must use the AC-coupling capacitor for signal input.
Note: Analog output pins (LOUT1, ROUT1, LOUT2, ROUT2, LOUT3, ROUT3 pins) must use the AC-coupling capacitor for signal output.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LOUT1-3, ROUT1-3, LIN1-6, RIN1-6	These pins should be open.
Digital	SDTOB, LRCKB(Master), BICKB(Master)	These pins should be open.
	MCLKA, LRCKA, BICKA, SDTIA1-2, MCLKB, LRCKB(Slave), BICKB(Slave), MSB	These pins should be connected to DVSS.
	SDA, SCL	These pins should be pulled-up to DVDD2.

ABSOLUTE MAXIMUM RATINGS

(AVSS1, AVSS2, DVSS1, DVSS2, PVSS=0V; Note: 1)

Parameter	Symbol	min	max	Units
Power Supply	TVDD	-0.3	6.0	V
	DVDD1	-0.3	6.0	V
	DVDD2	-0.3	6.0	V
	AVDD1	-0.3	6.0	V
	AVDD2	-0.3	6.0	V
	PVDD	-0.3	14.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Digital Input Voltage 1 (MCLKB pin)	VIND1	-0.3	DVDD1+0.3	V
Digital Input Voltage 2 (PDN, LRCKA, BICKA, MCLKA, SDTIA1-2, SDA, SCL, MSB pins)	VIND2	-0.3	DVDD2+0.3	V
Digital Input Voltage 3 (LRCKB, BICKB pins)	VIND3	-0.3	TVDD+0.3	V
Analog Input Voltage 1 (LIN1-6, RIN1-6 pins)	VINA1	-0.3	PVDD+0.3	V
Ambient Operating Temperature	Ta	-20	85	°C
Storage Temperature	Tstg	-65	150	°C

Note: 1. AVSS1, DVSS1, AVSS2, DVSS2 and PVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS1, AVSS2, DVSS1, DVSS2, PVSS=0V; Note: 1)

Parameter	Symbol	min	typ	max	Units
Power Supply (Note: 2)	TVDD	2.7	3.3	5.25	V
	DVDD1	4.75	5.0	5.25	V
	DVDD2	4.75	5.0	5.25	V
	AVDD1	4.75	5.0	5.25	V
	AVDD2	4.75	5.0	5.25	V
	PVDD	8.5	9.0	12.6	V

Note: 2. The AVDD1, AVDD2, DVDD1 and DVDD2 must be the same voltage.
The TVDD must not exceed any of AVDD1, AVDD2, DVDD1 and DVDD2 voltage.

*AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; TVDD = 3.3V; DVDD1, DVDD2, AVDD1, AVDD2= 5.0V; PVDD = 9V; AVSS1, AVSS2, DVSS1, DVSS2, PVSS = 0V; fs=48kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Frequency = 20Hz~20kHz at fs=48kHz, 20Hz~40kHz at fs=96kHz; 20Hz~40kHz at fs=192kHz, all blocks are synchronized, unless otherwise specified)

Parameter		min	typ	max	Units
Analog Input to Analog Output Characteristics (LIN1-6, RIN1-6 pin to LOUT1-3, ROUT1-3 pin)					
S/(N+D)	Input=2Vrms	-	92		dB
S/N	Input=0ff, A-weighted	-	96		dB
Input Impedance		40			kΩ
Maximum Input Voltage	(Note: 4)	2	-	-	Vrms
Gain		-	0	-	dB
Analog Input (LIN1-6, RIN1-6 pin) to ADC Analog Input Characteristics					
Resolution				24	Bits
S/(N+D) (-1dBFS)	fs=48kHz	80	88		dB
DR (-60dBFS)	fs=48kHz, A-weighted	88	96		dB
S/N (input off)	fs=48kHz, A-weighted	88	96		dB
Interchannel Isolation	(Note: 3)	90	100		dB
Interchannel Gain Mismatch			0.2	0.6	dB
Gain Drift			50	-	ppm/°C
Input Voltage	AIN= 2.2 x AVDD1/5	2	2.2	2.4	Vrms
Power Supply Rejection	(Note: 5)		60		dB
DAC to Analog Output (LOUT1-3, ROUT1-3 pin) Characteristics					
Resolution				24	Bits
S/(N+D) (0dBFS)	fs=48kHz	76	86		dB
	fs=96kHz	-	84		dB
	fs=192kHz	-	84		dB
DR (-60dBFS)	fs=48kHz, A-weighted	94	102		dB
	fs=96kHz	-	96		dB
	fs=96kHz, A-weighted	-	102		dB
	fs=192kHz	-	96		dB
	fs=192kHz, A-weighted	-	102		dB
S/N ("0" data)	fs=48kHz, A-weighted	94	102		dB
	fs=96kHz	-	96		dB
	fs=96kHz, A-weighted	-	102		dB
	fs=192kHz	-	96		dB
	fs=192kHz, A-weighted	-	102		dB
Interchannel Isolation		90	100		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			50	-	ppm/°C
Output Voltage	AOUT= 2 x AVDD2/5	1.85	2	2.15	Vrms
Load Resistance	(AC Load)	5			kΩ
Load Capacitance				30	pF
Power Supply Rejection	(Note: 5)		50		dB

Note: 3. This value is the interchannel isolation between all the channels of the LIN1-6 and RIN1-6.
Note: 4. Maximum input level that satisfy S/(N+D)>80dB.
Note: 5. PSR is applied to AVDD1, AVDD2, DVDD1, DVDD2 and PVDD with 1kHz, 50mVpp.

Power Supplies				
Parameter	**min**	**typ**	**max**	**Units**
Power Supply Current				
Normal Operation (PDN pin = "H")				
TVDD		1	3	mA
DVDD1+AVDD1		37	55	mA
DVDD2+AVDD2		33	50	mA
PVDD		15	25	mA
Power-Down Mode (PDN pin = "L"; Note: 6)				
TVDD		10	100	μA
DVDD1+AVDD1		10	100	μA
DVDD2+AVDD2		10	100	μA
PVDD		10	100	μA

Note: 6. All digital inputs including clock pins (MCLKA, MCLKB, BICKA, BICKB, LRCKA, LRCKB and SDTIA1-0) are held at DVDD1, DVDD2, DVSS1 or DVSS2.

FILTER CHARACTERISTICS

(Ta=-20°C ~+85°C; TVDD=2.7 ~ 5.25V; DVDD1, DVDD2, AVDD1, AVDD2=4.75 ~ 5.25V; PVDD=8.5 ~ 12.6V; fs=48kHz)

Parameter		**Symbol**	**min**	**typ**	**max**	**Units**
ADC Digital Filter (Decimation LPF):						
Passband (Note: 7)	±0.1dB	PB	0		18.9	kHz
	-0.2dB		-	20.0	-	kHz
	-3.0dB		-	23.0	-	kHz
Stopband		SB	28.0			kHz
Passband Ripple		PR			±0.04	dB
Stopband Attenuation		SA	68			dB
Group Delay (Note: 8)		GD		16		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note: 7)	-3dB	FR		1.0		Hz
	-0.1dB			6.5		Hz
DAC Digital Filter:						
Passband (Note: 7)	-0.1dB	PB	0		21.8	kHz
	-6.0dB		-	24.0	-	kHz
Stopband		SB	26.2			kHz
Passband Ripple		PR			±0.02	dB
Stopband Attenuation		SA	54			dB
Group Delay (Note: 8)		GD		20		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 20.0kHz		FR		±0.2		dB
40.0kHz (Note: 9)		FR		±0.3		dB
80.0kHz (Note: 9)		FR		±1.0		dB

Note: 7. The passband and stopband frequencies scale with fs.
For example, 21.8kHz at –0.1dB is 0.454 x fs (DAC). The reference frequency of these responses is 1kHz.
Note: 8. The calculating delay time occurred at digital filtering. This time is from setting the input of analog s signal to setting the 24bit data of both channels to the output register of PORTB.
For DAC, this time is from setting the 20/24bit data of both channels on input register of PORTA to the output of analog signal.
Note: 9. 40.0kHz@fs=96kHz, 80.0kHz@fs=192kHz.

DC CHARACTERISTICS

(Ta=-20°C ~+85°C; TVDD=2.7 ~ 5.25V; DVDD1, DVDD2, AVDD1, AVDD2=4.75 ~ 5.25V; PVDD=8.5~12.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
High-Level Output Voltage (Iout=-400μA)	VOH	TVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= -400μA(except SDA pin), 3mA(SDA pin))	VOL	-		0.4	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=-20°C ~+85°C; TVDD=2.7 ~ 5.25V; DVDD1, DVDD2, AVDD1, AVDD2=4.75 ~ 5.25V; PVDD=8.5~12.6V; C_L= 20pF (except for SDA pin), Cb=400pF(SDA pin))

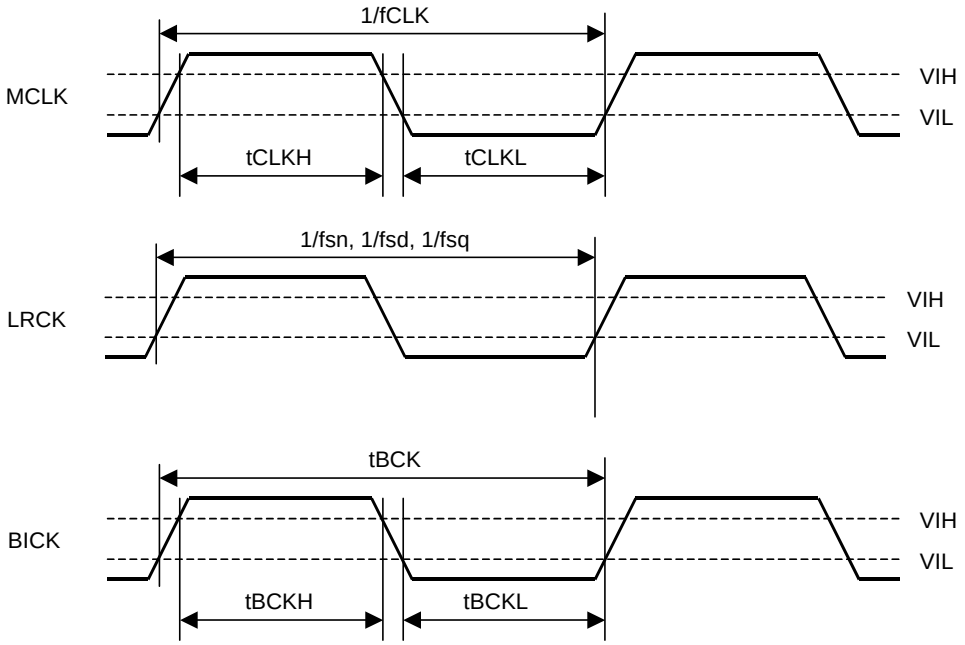
Parameter	Symbol	min	typ	max	Units
Master Clock Timing					
Frequency	fECLK	8.192		36.864	MHz
Duty	dECLK	40	50	60	%
Master Clock (Note: 10)					
256fsn, 128fsd:	fCLK	8.192		12.288	MHz
Pulse Width Low	tCLKL	27			ns
Pulse Width High	tCLKH	27			ns
384fsn, 192fsd:	fCLK	12.288		18.432	MHz
Pulse Width Low	tCLKL	20			ns
Pulse Width High	tCLKH	20			ns
512fsn, 256fsd, 128fsq:	fCLK	16.384		24.576	MHz
Pulse Width Low	tCLKL	15			ns
Pulse Width High	tCLKH	15			ns
768fsn, 384fsd, 192fsq:	fCLK	24.576		36.864	MHz
Pulse Width Low	tCLKL	10			ns
Pulse Width High	tCLKH	10			ns
LRCKA (LRCKB) Timing (Slave Mode)					
Normal mode					
Normal Speed Mode	fsn	32		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	120		192	kHz
Duty Cycle	Duty	45		55	%
TDM 128 mode					
LRCKA frequency	fs	32		96	kHz
"H" time	tLRH	1/128fs			ns
"L" time	tLRL	1/128fs			ns
LRCKB Timing (Master Mode)					
Normal mode					
LRCKB frequency	fs	32		48	kHz
Duty Cycle	Duty		50		%
Power-down & Reset Timing					
PDN Pulse Width (Note: 11)	tPD	150			ns
PDN "↑" to SDTOB valid (Note: 12)	tPDV		522		1/fs

Note: 10 MCLKB supports only the normal mode (256fsn, 384fsn, 512fsn, 768fsn).
Note: 11 The AK4682 can be reset by bringing the PDN pin = "L".
Note: 12 These cycles are the number of LRCKB rising from PDN rising.

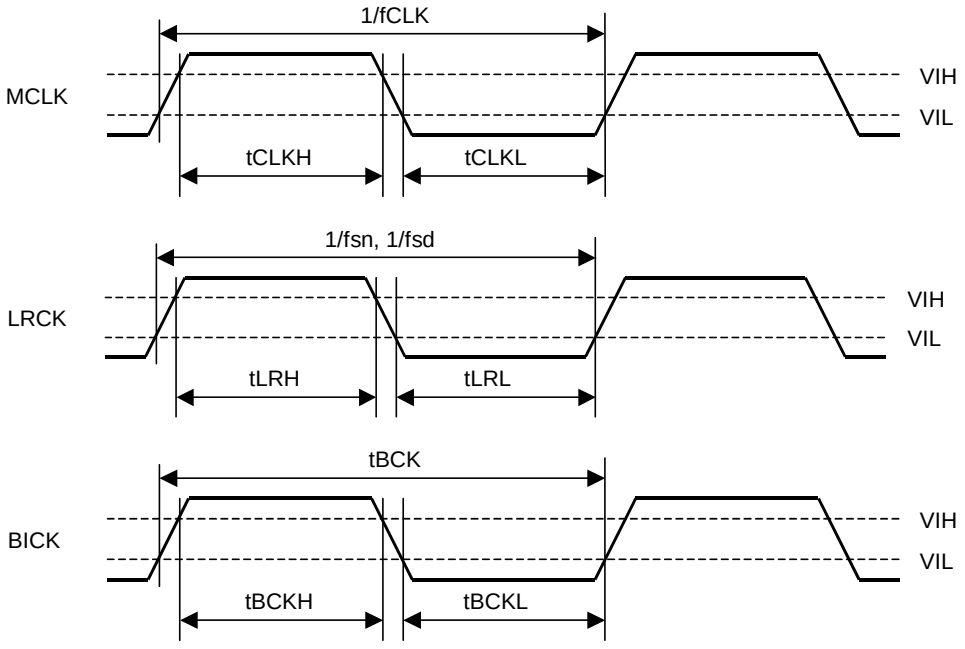
Parameter	Symbol	min	typ	max	Units
Audio Interface Timing (Slave Mode)					
Normal mode(PORTA)					
BICKA Period	tBCK	81			ns
BICKA Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCKA Edge to BICKA "↑" (Note: 13)	tLRB	20			ns
BICKA "↑" to LRCKA Edge (Note: 13)	tBLR	20			ns
SDTIA1-2 Hold Time	tSDH	10			ns
SDTIA1-2 Setup Time	tSDS	10			ns
Normal mode(PORTB)					
BICKB Period	tBCK	324			ns
BICKB Pulse Width Low	tBCKL	128			ns
Pulse Width High	tBCKH	128			ns
LRCKB Edge to BICKB "↑" (Note: 13)	tLRB	80			ns
BICKB "↑" to LRCKB Edge (Note: 13)	tBLR	80			ns
LRCKB to SDTOB (MSB)	tLRS			80	ns
BICKB "↓" to SDTOB	tBSD			80	ns
TDM 128 mode					
BICKA Period	tBCK	81			ns
BICKA Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCKA Edge to BICKA "↑" (Note: 13)	tLRB	20			ns
BICKA "↑" to LRCKA Edge (Note: 13)	tBLR	20			ns
SDTIA1-2 Hold Time	tSDH	10			ns
SDTIA1-2 Setup Time	tSDS	10			ns
Audio Interface Timing (Master Mode)					
Normal mode					
BICKB Frequency	fBCK		64fs		Hz
BICKB Duty	dBCK		50		%
BICKB "↓" to LRCKB Edge	tMBLR	-40		40	ns
BICKB "↓" to SDTO	tBSD			20	ns
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	μs
Clock Low Time	tLOW	1.3		-	μs
Clock High Time	tHIGH	0.6		-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	μs
SDA Hold Time from SCL Falling (Note: 14)	tHD:DAT	0		-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	μs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6		-	μs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	-		50	ns
Capacitive load on bus	Cb	0		400	pF

Note: 13 BICK rising edge must not occur at the same time as LRCK edge.
Note: 14 Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note: 15 I^2C is a registered trademark of Philips Semiconductors.

■ Timing Diagram

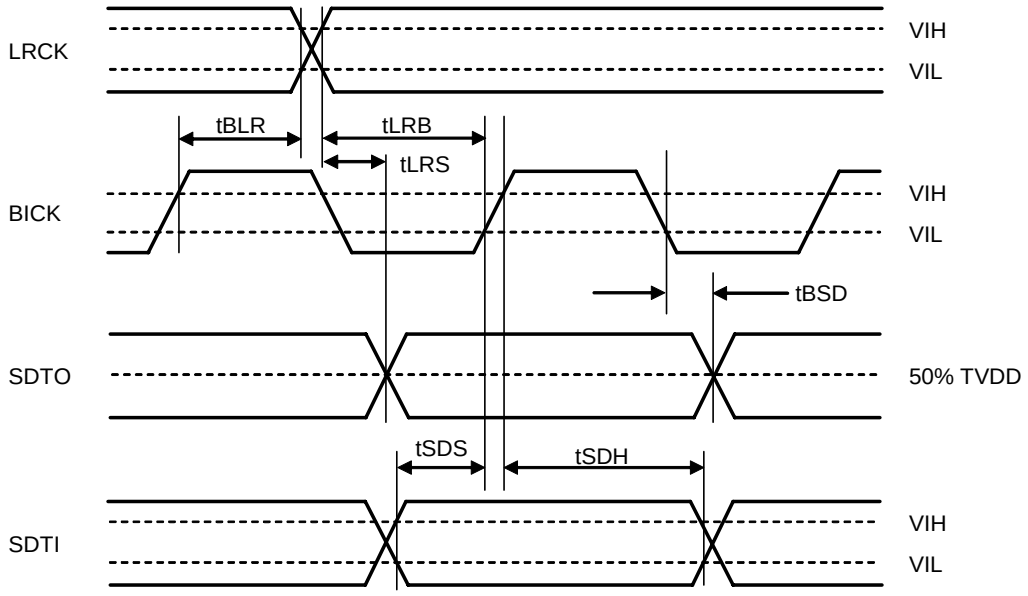


Clock Timing (Normal mode)

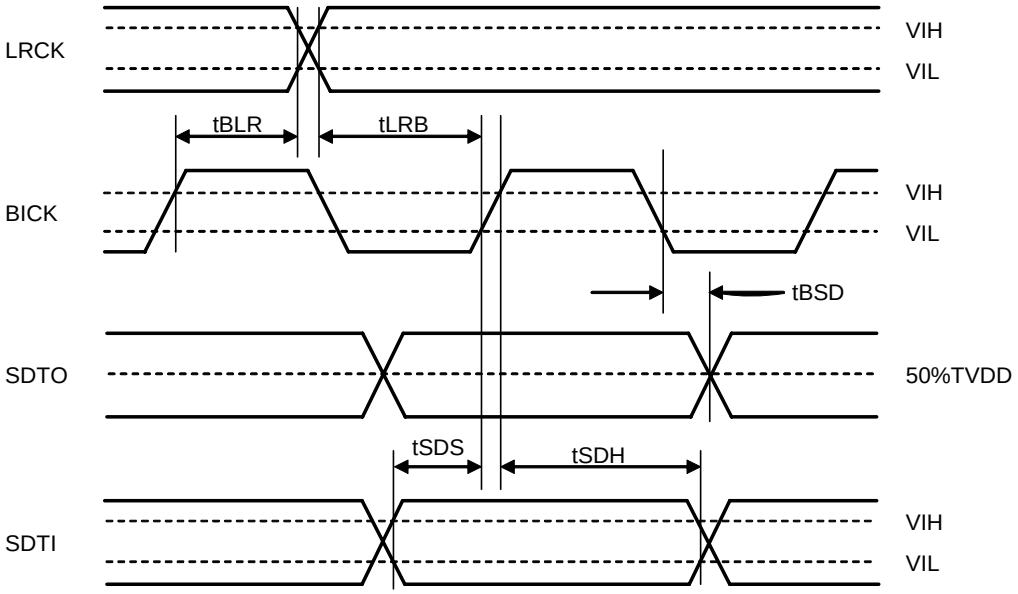


Clock Timing (TDM 128 mode)

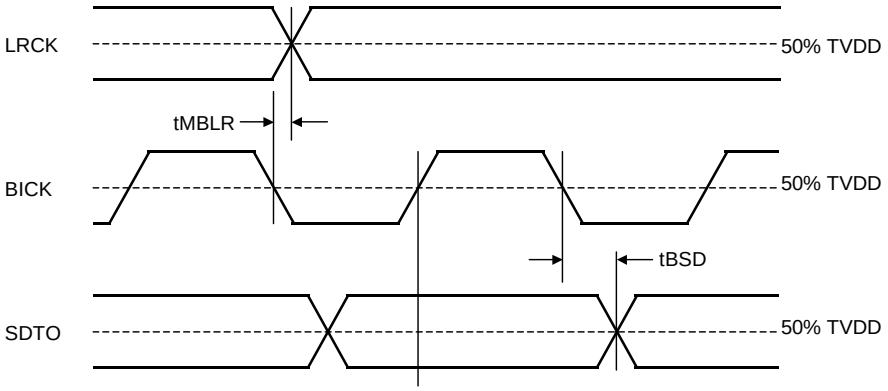
LRCK= LRCKB, LRCKA,
BICK= BICKA, BICKB,
SDTI= SDTIA,
SDTO= SDTOB.



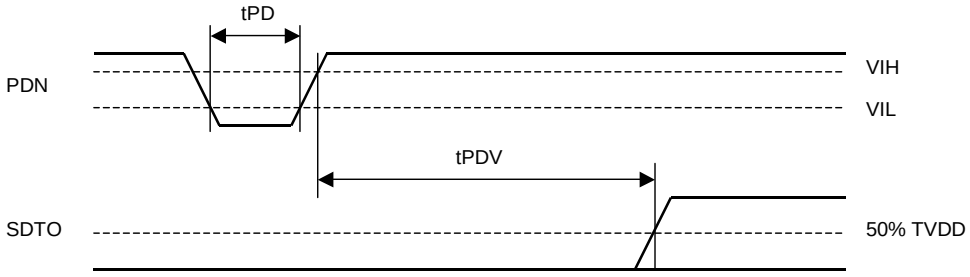
Audio Interface Timing (Normal mode)



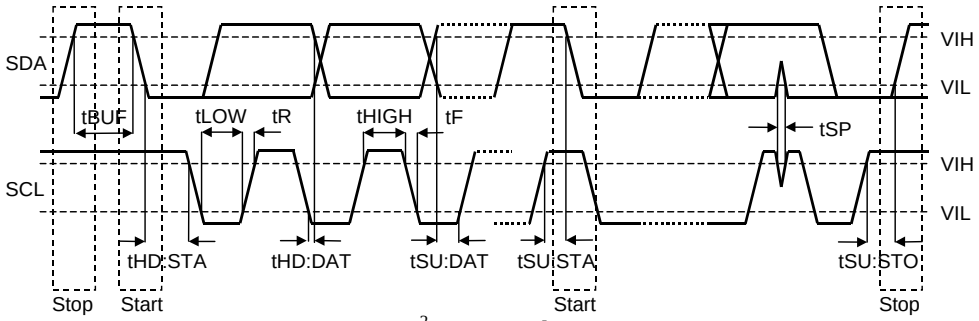
Audio Interface Timing (TDM 128 mode)



Audio Interface timing (Master Mode)



Power Down & Reset Timing



I^2C Bus mode Timing

OPERATION OVERVIEW

■ System Clock

The AK4682 has two audio serial interface (PORTA, PORTB) can operate asynchronously. At each PORT, the external clocks, which are required to operate the AK4682, are MCLKA (MCLKB), LRCKA (LRCKB) and BICKA (BICKB). The MCLKA (MCLKB) must be synchronized with LRCKA (LRCKB) but the phase is not critical. The PORT A is the audio data interface for DAC and the PORTB is for ADC.

■ Master/Slave Mode

The MSB pin and MSB bit are internally ORed and select the master/slave mode of PORTB. PORTA is slave mode only. In master mode, LRCKB pin and BICKB pin are output pins. In slave mode, LRCKA (LRCKB) pin and BICKA (BICKB) pin are input (Table 1).

The AK4682 is slave mode at power-down (PDN pin = "L"). To change to the master mode, set MSB pin "H" or write "1" to MSB bit. Until when setting MSB pin "H" or writing "1" to MSB bit, LRCKB and BICKB pins are input pins. Pull-up (or down) resistor with around 100kohm is required to prevent the floating of these input pins.

PDN pin	MSB pin	MSB bit (default: "0")	PORTB (ADC) BICKB, LRCKB	PORTA (DAC) BICKA, LRCKA
L	L	x	Input (slave mode)	Input (slave mode)
	H	x	Output "L"(master mode)	Input (slave mode)
H	L	0	Input (slave mode)	Input (slave mode)
	L	1	Output (master mode)	Input (slave mode)
	H	x	Output (master mode)	Input (slave mode)

(x: Don't care)

Table 1. Master/Salve Mode

■ ADC Clock Control

In master mode (MSB bit = "1"), the CKSB1-0 bits select the clock frequency (Table 2). The external clock (MCLKB) must always be supplied except in the power-down mode. The ADC is in power-down mode until MCLKB is supplied.

CKSB1	CKSB0	Clock Speed	
0	0	256fs	(default)
0	1	384fs	
1	0	512fs	
1	1	768fs	

Table 2. PORTB Master Clock Control (ADC Master Mode)

In slave mode (MSB bit = "0". default), external clocks (MCLKB, BICKB, LRCKB) must always be present whenever the ADC is in normal operation mode (PDN pin = "H" and PWAD = "1"). The master clock (MCLKB) must be synchronized with LRCKB but the phase is not critical. If these clocks are not provided, the ADC may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC must be in the power-down mode (PDN pin = "L" or PWAD = "0") or in the reset mode (RSTN bit = "0"). After exiting reset at power-up etc., the ADC is in the power-down mode until MCLKB and LRCKB are input.

LRCKB	MCLKB (MHz)						Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	
32.0kHz	-	-	8.1920	12.2880	16.3840	24.5760	Normal
44.1kHz	-	-	11.2896	16.9344	22.5792	33.8688	
48.0kHz	-	-	12.2880	18.4320	24.5760	36.8640	

Table 3. System clock example (ADC Slave Mode)

■ DAC Clock Control

External clocks (MCLKA, BICKA, LRCKA) must always be present whenever the DAC is in normal operation mode (PDN pin = "H" and PWDA = "1"). The master clock (MCLKA) must be synchronized with LRCKA but the phase is not critical. If these clocks are not provided, the DAC may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the DAC must be in the power-down mode (PDN pin = "L" or PWDA = "0") or in the reset mode (RSTN bit = "0"). After exiting reset at power-up etc., the DAC is in the power-down mode until MCLKA and LRCKA are input.

There are two modes for controlling the sampling speed of DAC. One is the Manual Setting Mode (ACKS bit = "0") using the DFS1-0 bits, and the other is Auto Setting Mode (ACKS bit = "1").

1. Manual Setting Mode (ACKS bit = "0")

When the ACKS bit = "0", DAC is in Manual Setting Mode and the sampling speed is selected by DFS1-0 bits (Table 4).

DFS1	DFS0	DAC Sampling Speed (fs)		
0	0	Normal Speed Mode	32kHz~48kHz	(default)
0	1	Double Speed Mode	64kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	
1	1	Not Available	-	

(Note: ADC is always in Normal Speed Mode)

Table 4.DAC sampling speed (ACKS bit = "0", Manual Setting Mode)

LRCKA	MCLKA (MHz)				BICKA (MHz)
fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920	12.2880	16.3840	24.5760	2.0480
44.1kHz	11.2896	16.9344	22.5792	33.8688	2.8224
48.0kHz	12.2880	18.4320	24.5760	36.8640	3.0720

Table 5. DAC system clock example (DAC Normal Speed Mode @Manual Setting Mode)

LRCKA	MCLKA (MHz)				BICKA (MHz)
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896	16.9344	22.5792	33.8688	5.6448
96.0kHz	12.2880	18.4320	24.5760	36.8640	6.1440

Table 6. DAC system clock example(DAC Double Speed Mode @Manual Setting Mode)

LRCKA	MCLKA (MHz)				BICKA (MHz)
Fs	128fs	192fs	256fs	384fs	64fs
176.4kHz	22.5792	33.8688	-	-	11.2896
192.0kHz	24.5760	36.8640	-	-	12.2880

Table 7. DAC system clock example (DAC Quad Speed Mode @Manual Setting Mode)

2. Auto Setting Mode (ACKS bit = "1")

When the ACKS bit = "1", DAC is in Auto Setting Mode and the sampling speed is selected automatically by the ratio MCLKA/LRCKA as shown in the Table 8. and the internal master clock is set to the appropriate frequency (Table 9). In this mode, the setting of DFS1-0 bits are ignored.

MCLKA	DAC Sampling Speed (fs) LRCKA	
512fs, 768fs	Normal Speed Mode	32kHz~48kHz
256fs, 384fs	Double Speed Mode	64kHz~96kHz
128fs, 192fs	Quad Speed Mode	120kHz~192kHz

(Note: ADC is always in Normal Speed Mode)

Table 8. DAC Sampling Speed (ACKS bit = "1", Auto Setting Mode)

LRCKA	MCLKA (MHz)						Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	
32.0kHz	-	-	-	-	16.3840	24.5760	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	
48.0kHz	-	-	-	-	24.5760	36.8640	
88.2kHz	-	-	22.5792	33.8688	-	-	Double
96.0kHz	-	-	24.5760	36.8640	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	

Table 9. DAC System clock example (Auto Setting Mode)

■ DAC Audio Data Control

The DAC1, DAC2 bits select the output data for each DAC.

DAC1 bit	DAC1 Source		
	Normal Mode TDMA bit = "0"	TDM Mode TDMA bit = "1"	
0	SDTIA1	L1, R1	(default)
1	SDTIA2	L2, R2	

Table 10. DAC1 Source Control

DAC2 bit	DAC2 Source		
	Normal Mode TDMA bit = "0"	TDM Mode TDMA bit = "1"	
0	SDTIA1	L1, R1	
1	SDTIA2	L2, R2	(default)

Table 11. DAC2 Source Control

■ De-emphasis Filter

The AK4682 includes the digital de-emphasis filter (tc=50/15μs) by IIR filter. This filter corresponds to three sampling frequencies (32kHz, 44.1kHz, 48kHz). De-emphasis filter is off in Double speed mode and Quad speed mode. De-emphasis of each DAC can be set individually by register.

Mode	DEM11 (DEM21)	DEM10 (DEM20)	DEM	
0	0	0	44.1kHz	
1	0	1	OFF	(default)
2	1	0	48kHz	
3	1	1	32kHz	

Table 12. De-emphasis control

■ ADC Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 1.0Hz at fs=48kHz and scales with sampling rate (fs).

■ Audio Serial Interface Format

Each PORTA/B can select independent audio interface format. The TDMA, DIFA1-0 bits control the audio format for PORTA and support normal mode and TDM128 mode. The DIFB1-0 bits control the audio format for PORTB and support only normal mode. The default is mode 2. In all modes the serial data is MSB-first, 2's complement format. The SDTOB pins are clocked out on the falling edge of BICKB pins and the SDTIA1-0 pins are latched on the rising edge of BICKA pins.

1. Setting for the PORTA

1-1. Normal mode: TDMA bit = "0" (default)

The TDMA bit = "0" sets the AK4682 audio serial interface format to the normal mode. The DIFA1-0 bits select following eight serial data format (Table 13).

Mode	DIFA1 bit	DIFA0 bit	SDTIA1-2	LRCKA		BICKA		
				L/R	I/O	speed	I/O	
0	0	0	20bit, Right justified	H/L	I	≥ 48fs	I	
1	0	1	24bit, Right justified	H/L	I	≥ 48fs	I	
2	1	0	24bit, Left justified	H/L	I	≥ 48fs	I	
3	1	1	24bit, I^2S	L/H	I	≥ 48fs	I	(default)

Table 13 Audio Interface Format (Normal mode.)

1-2. TDM 128 mode: TDMA bit = "1"

The TDMA bits = "1" set the AK4682 audio serial interface format to the TDM 128 mode. The four channel serial data (SDTIA1, 2) is input to the SDTIA1 pin. The data of SDTIA2 pin is not used. The TDM 128 mode is not available in Quad Speed Mode.

Mode	DIFA1 bit	DIFA0 bit	SDTIA1-2	LRCKA		BICKA		
				start	I/O	speed	I/O	
8	0	0	20bit, Right justified	↑	I	128fs	I	
9	0	1	24bit, Right justified	↑	I	128fs	I	
10	1	0	24bit, Left justified	↑	I	128fs	I	
11	1	1	24bit, I^2S	↓	I	128fs	I	(default)

Table 14. Audio Interface Format (TDM 128 mode.)

2. Setting for the PORTB

2-1: Normal mode:

The PORTB supports only the normal mode. The DIFB1-0 bits select following eight serial data format (Table 15).

Mode	MSB pin	MSB bit	DIFB1	DIFB0	SDTOB	LRCKB		BICKB		
						L/R	I/O	speed	I/O	
0	0	0	0	0	24bit, L J	H/L	I	≥ 48fs	I	
1	0	0	0	1	24bit, L J	H/L	I	≥ 48fs	I	
2	0	0	1	0	24bit, L J	H/L	I	≥ 48fs	I	
3	0	0	1	1	24bit, I^2S	L/H	I	≥ 48fs	I	(default)
4	0	1	0	0	24bit, L J	H/L	O	64fs	O	
5	0	1	0	1	24bit, L J	H/L	O	64fs	O	
6	0	1	1	0	24bit, L J	H/L	O	64fs	O	
7	0	1	1	1	24bit, I^2S	L/H	O	64fs	O	
8	1	x	0	0	24bit, L J	H/L	O	64fs	O	
9	1	x	0	1	24bit, L J	H/L	O	64fs	O	
10	1	x	1	0	24bit, L J	H/L	O	64fs	O	
11	1	x	1	1	24bit, I^2S	L/H	O	64fs	O	

Table 15. Audio Interface Format (Normal mode, x: Don't care. L J: Left justified.)

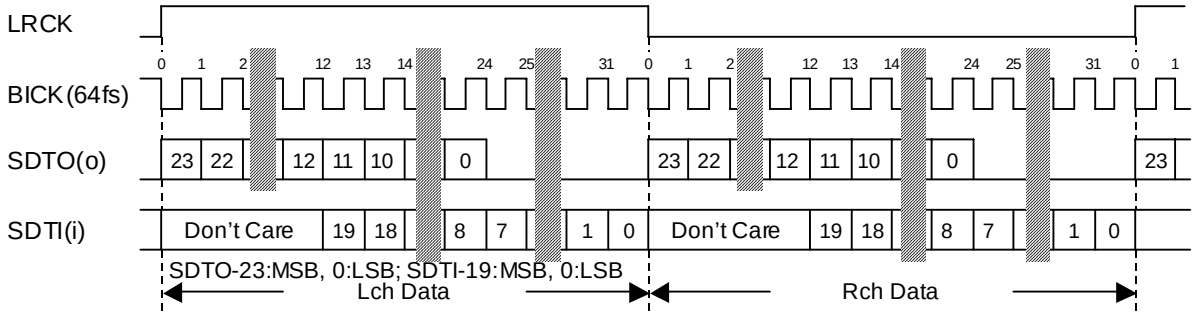


Figure 1. Mode 0, 4 Timing

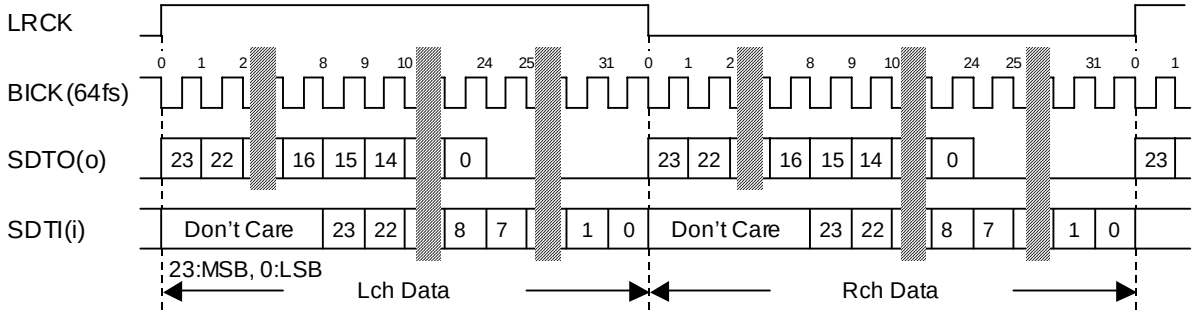


Figure 2. Mode 1, 5 Timing

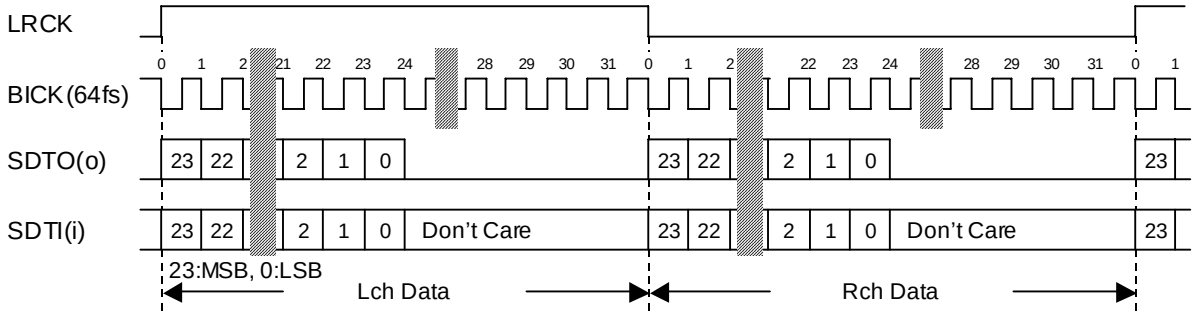


Figure 3.Mode 2, 6 Timing

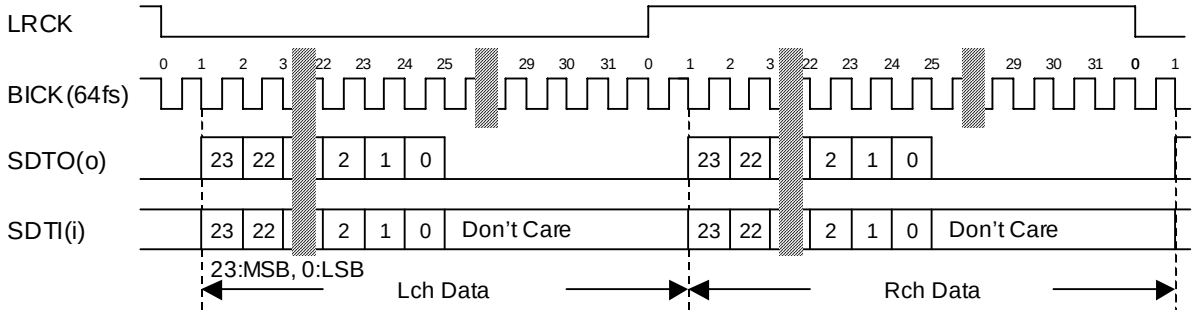


Figure 4. Mode 3, 7 Timing

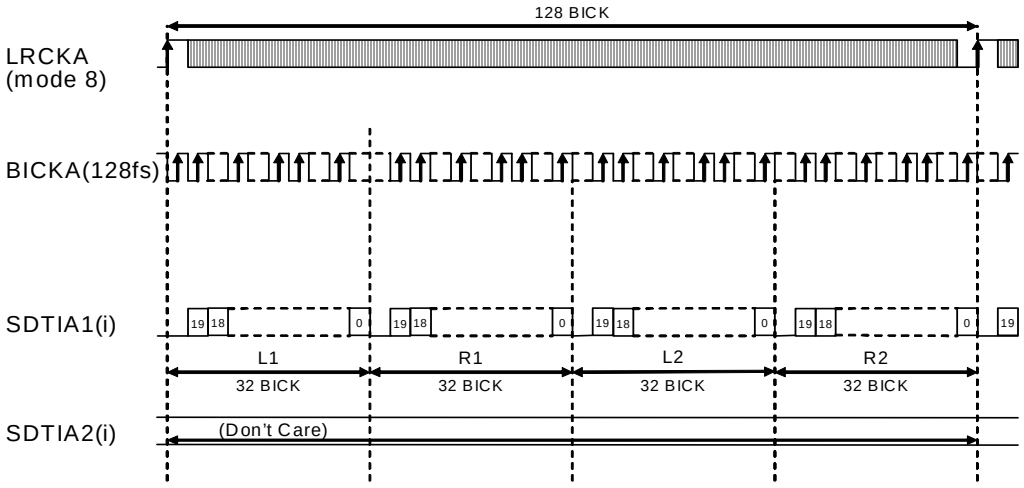


Figure 5. Mode 8 Timing

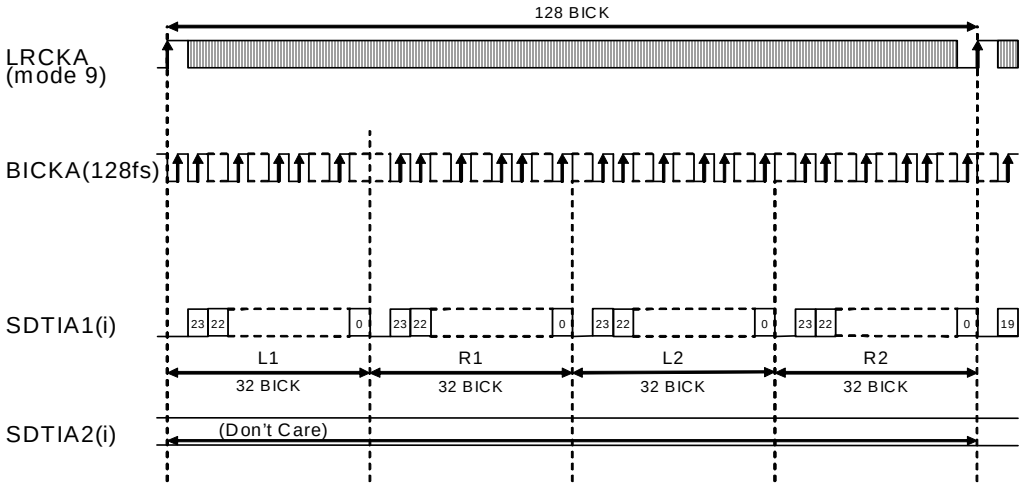


Figure 6. Mode 9 Timing

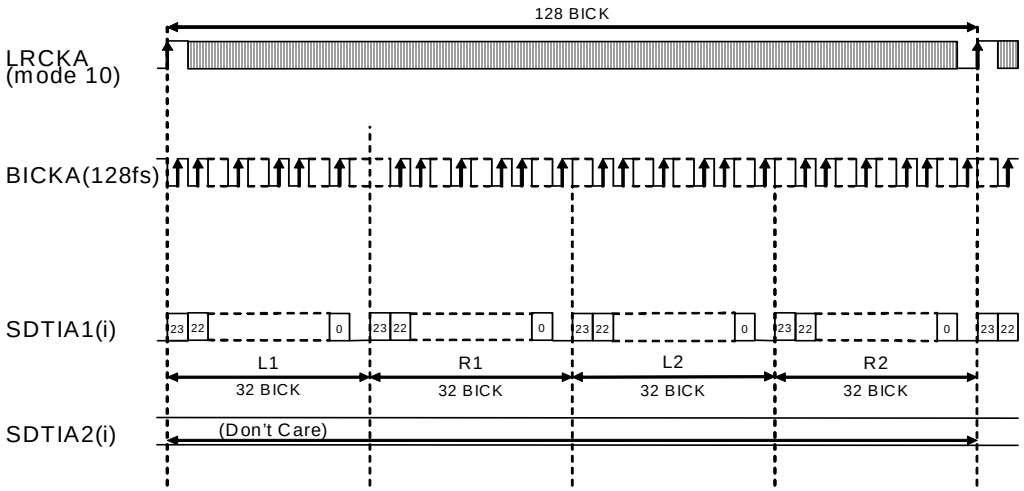


Figure 7. Mode 10 Timing

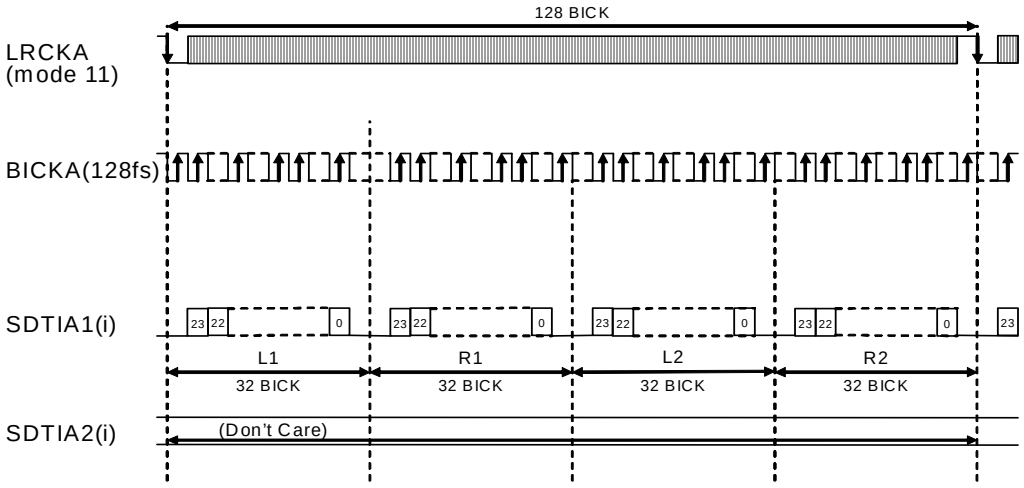


Figure 8. Mode 11 Timing

■ Digital Volume Control

The AK4682 has channel-independent digital volume control (256 levels, 0.5dB step). The IATL7-0, IATR7-0 bits set the volume level of each ADC channel (Table 16). The OAT1L7-0, OAT1R7-0, OAT2L7-0 and OAT2R7-0 bits set each DAC channel (Table 17).

IATL7-0, IATR7-0	Attenuation Level	
00H	+24dB	
01H	+23.5dB	
02H	+22.0dB	
:	:	
2FH	+0.5dB	
30H	0dB	(default)
31H	-0.5dB	
	:	
FEH	-103dB	
FFH	MUTE (-∞)	

Table 16.ADC Digital Volume (IATT)

OAT1L7-0, OAT1R7-0, OAT2L7-0, OAT2R7-0	Attenuation Level	
00H	+12dB	
01H	+11.5dB	
02H	+11.0dB	
:	:	
17H	+0.5dB	
18H	0dB	(default)
19H	-0.5dB	
	:	
FEH	-115dB	
FFH	MUTE (-∞)	

Table 17.DAC Digital Volume (OATT)

ATSAD (ATSDA) bits (Table 18, Table 19) control the transition time of attenuation. The transition between each attenuation level is the soft transition. Therefore, the switching noise does not occur in the transition.

Mode	ATSAD	ATT speed	
0	0	1061/fs	(default)
1	1	256/fs	

Table 18. Transition time of attenuation (ADC)

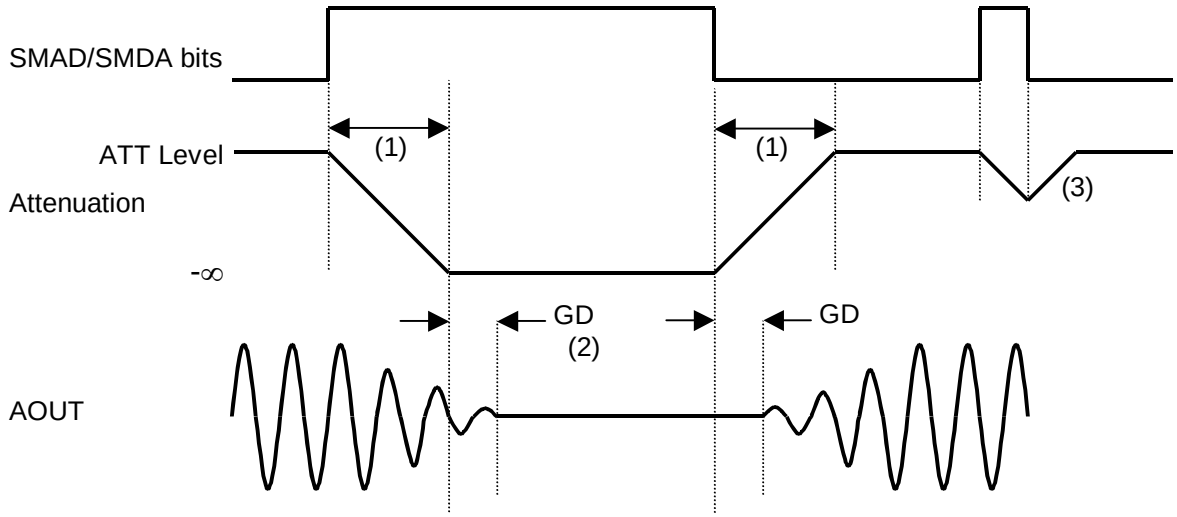
Mode	ATSDA	ATT speed	
0	0	1061/fs	(default)
1	1	256/fs	

Table 19. Transition time of attenuation (DAC)

The transition between set values is soft transition of 1061 levels in Mode 0. It takes 1061/fs (22ms@fs=48kHz) from 00H to FFH(MUTE) in mode 0. If PDN pin goes to "L", the IATL7-0, IATR7-0 (OAT1L7-0, OAT1R7-0, OAT2L7-0, OAT2R7-0) bits are initialized to 30H(18H). The ATTs goes to their default value when RSTN bit = "0". When RSTN bit return to "1", the ATTs fade to their current value.

■ Soft mute operation

The ADC and DAC have the soft mute function. The soft mute operation is performed at digital domain. When the SMAD/SMDA bits go to "1", the output signal is attenuated by -∞ during ATT_DATA×ATT transition time (Table 18, Table 19) from the current ATT level. When the SMAD/SMDA bits are returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA×ATT transition time (Table 18, Table 19). For example, in Normal Speed Mode, this time is 1061/fs cycles (256/fs) at ATT_DATA=00H. ATT transition of the soft-mute is from 00H to FFH

(2) The analog output corresponding to the digital input has a group delay, GD.

(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

Figure 9. Soft Mute Function

■ Stereo Matrix Control

The AK4682 has independent stereo matrix control for DAC1 and DAC2. The PL23-20 and PL13-10 bits control each matrix.

PL13	PL12	PL11	PL10	DAC1 Lch Output	DAC1 Rch Output	Note	
0	0	0	0	MUTE	MUTE	MUTE	
0	0	0	1	MUTE	R		
0	0	1	0	MUTE	L		
0	0	1	1	MUTE	(L+R)/2		
0	1	0	0	R	MUTE		
0	1	0	1	R	R		
0	1	1	0	R	L	REVERSE	
0	1	1	1	R	(L+R)/2		
1	0	0	0	L	MUTE		
1	0	0	1	L	R	STEREO	(default)
1	0	1	0	L	L		
1	0	1	1	L	(L+R)/2		
1	1	0	0	(L+R)/2	MUTE		
1	1	0	1	(L+R)/2	R		
1	1	1	0	(L+R)/2	L		
1	1	1	1	(L+R)/2	(L+R)/2	MONO	

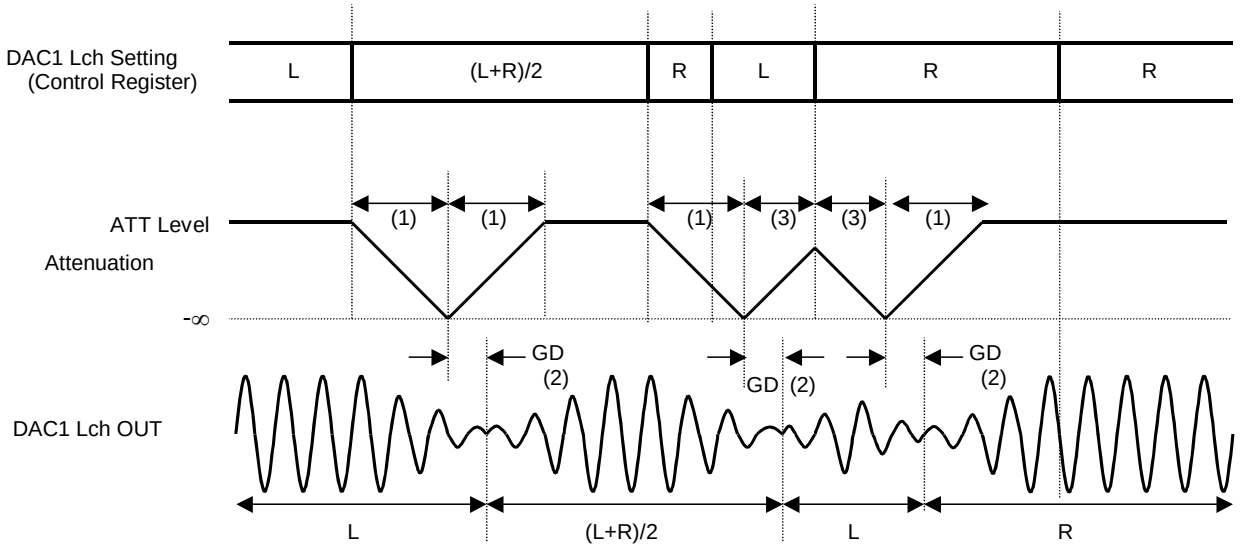
Table 20. PL13-10: DAC1 Stereo Matrix Control

PL23	PL22	PL21	PL20	DAC2 Lch Output	DAC2 Rch Output	Note	
0	0	0	0	MUTE	MUTE	MUTE	
0	0	0	1	MUTE	R		
0	0	1	0	MUTE	L		
0	0	1	1	MUTE	(L+R)/2		
0	1	0	0	R	MUTE		
0	1	0	1	R	R		
0	1	1	0	R	L	REVERSE	
0	1	1	1	R	(L+R)/2		
1	0	0	0	L	MUTE		
1	0	0	1	L	R	STEREO	(default)
1	0	1	0	L	L		
1	0	1	1	L	(L+R)/2		
1	1	0	0	(L+R)/2	MUTE		
1	1	0	1	(L+R)/2	R		
1	1	1	0	(L+R)/2	L		
1	1	1	1	(L+R)/2	(L+R)/2	MONO	

Table 21. PL23-20: DAC2 Stereo Matrix Control

STEREO: Normal stereo output
REVERSE: L/R Reverse output
MONO: Monaural output
MUTE: Mute operation

The stereo matrix control has the four channel independent soft transition using soft muting function.



Notes:

(1) ATT_DATA×ATT transition time (Table 18, Table 19). For example, in Normal Speed Mode, this time is 1061/fs cycles (256/fs) at ATT_DATA=00H. ATT transition of the soft-mute is from 00H to FFH

(2) The analog output corresponding to the digital input has a group delay, GD.

(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

Figure 10. Soft Mute Function for Stereo Matrix Control

■ Input Selector, Input Attenuator

The AK4682 includes 8:4 stereo input/output selectors. The AIN2-0, AOUT12-10, AOUT22-20, AOUT32-30 bits set each input channel (Table 22, Table 23, Table 24, Table 25). To select the DAC1 or DAC2, set PWAD bit = PWDA bit = PWANA bit = "1".

AIN3 bit	AIN2 bit	AIN1 bit	AIN0 bit	Input Selector	
0	0	0	0	LIN1 / RIN1	(default)
0	0	0	1	LIN2 / RIN2	
0	0	1	0	LIN3 / RIN3	
0	0	1	1	LIN4 / RIN4	
0	1	0	0	LIN5 / RIN5	
0	1	0	1	LIN6 / RIN6	
0	1	1	0	DAC1L/DAC1R	
0	1	1	1	DAC2L/DAC2R	
1	x	x	x	Mute	

Table 22. Input Selector (for ADC, x: Don't care)

AOUT13 bit	AOUT12 bit	AOUT11 bit	AOUT10 bit	Input Selector	
0	0	0	0	LIN1 / RIN1	
0	0	0	1	LIN2 / RIN2	
0	0	1	0	LIN3 / RIN3	
0	0	1	1	LIN4 / RIN4	
0	1	0	0	LIN5 / RIN5	
0	1	0	1	LIN6 / RIN6	
0	1	1	0	DAC1L/DAC1R	(default)
0	1	1	1	DAC2L/DAC2R	
1	x	x	x	Mute	

Table 23. Input Selector (for L/ROUT1, x: Don't care)

AOUT23 bit	AOUT22 bit	AOUT21 bit	AOUT20 bit	Input Selector	
0	0	0	0	LIN1 / RIN1	
0	0	0	1	LIN2 / RIN2	
0	0	1	0	LIN3 / RIN3	
0	0	1	1	LIN4 / RIN4	
0	1	0	0	LIN5 / RIN5	
0	1	0	1	LIN6 / RIN6	
0	1	1	0	DAC1L/DAC1R	
0	1	1	1	DAC2L/DAC2R	(default)
1	x	x	x	Mute	

Table 24. Input Selector (for L/ROUT2, x: Don't care)

AOUT33 bit	AOUT32 bit	AOUT31 bit	AOUT30 bit	Input Selector	
0	0	0	0	LIN1 / RIN1	(default)
0	0	0	1	LIN2 / RIN2	
0	0	1	0	LIN3 / RIN3	
0	0	1	1	LIN4 / RIN4	
0	1	0	0	LIN5 / RIN5	
0	1	0	1	LIN6 / RIN6	
0	1	1	0	DAC1L/DAC1R	
0	1	1	1	DAC2L/DAC2R	
1	x	x	x	Mute	

Table 25. Input Selector (for L/ROUT3, x: Don't care)

[Input selector switching sequence]

The input selector should be changed after soft mute to avoid the switching noise of the input selector (Figure 11).

1. Enable the soft mute before changing channel.
2. Change channel.
3. Disable the soft mute.

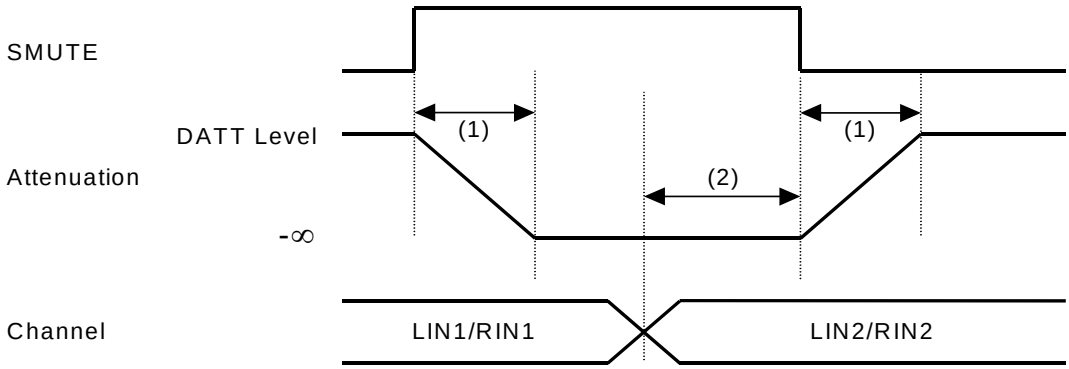


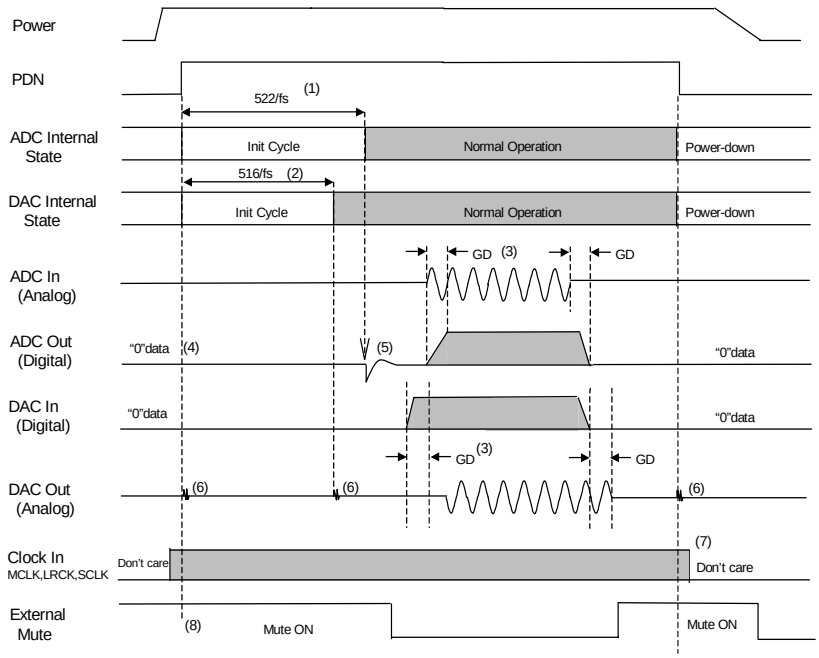
Figure 11. Input channel switching sequence example

The period of (1) varies in the setting value of DATT. It takes 1028/fs to mute when DATT value is +24dB.

When changing channels, the input channel should be changed during (2). The period of (2) should be around 200ms because there is some DC difference between the channels.

■ Power ON/OFF Sequence

The each block of the AK4682 are placed in the power-down mode by bringing PDN pin "L" and both digital filters are reset at the same time. PDN pin "L" also reset the control registers to their default values. In the power-down mode, the DAC outputs go to AVDD2 voltage and SDTOB pin goes to "L". This reset must always be done after power-up.
In slave mode, after exiting reset at power-up etc., the DAC (ADC) starts to operate from the rising edge of LRCKA (LRCKB) after MLCKA (MCLKB), and then the device is in the power-down mode until MCLKA (MCLKB) and LRCKA (LRCKB) are input. In slave mode, the DAC (ADC) starts to operate by the input of MLCKA (MCLKB) after exiting reset.
The analog initialization cycle of ADC starts after exiting the power-down mode. Therefore, the output data, SDTOB becomes available after 522/fs cycles of LRCKB clock. In case of the DAC, an analog initialization cycle starts after exiting the power-down mode. The analog outputs are AVDD2 voltage during the initialization. Figure 12 shows the sequences of the power-down and the power-up.
The ADC and all DACs can be powered-down individually by PWAD and PWDA bits. These bits don't initialize the internal register values. When PWAD bit = "0", the SDTOB pin goes to "L". When PWDA bit = "0", the DAC outputs go to AVDD2 voltage. Since some click noise may occur, the analog output should muted externally if the click noise influences system application.

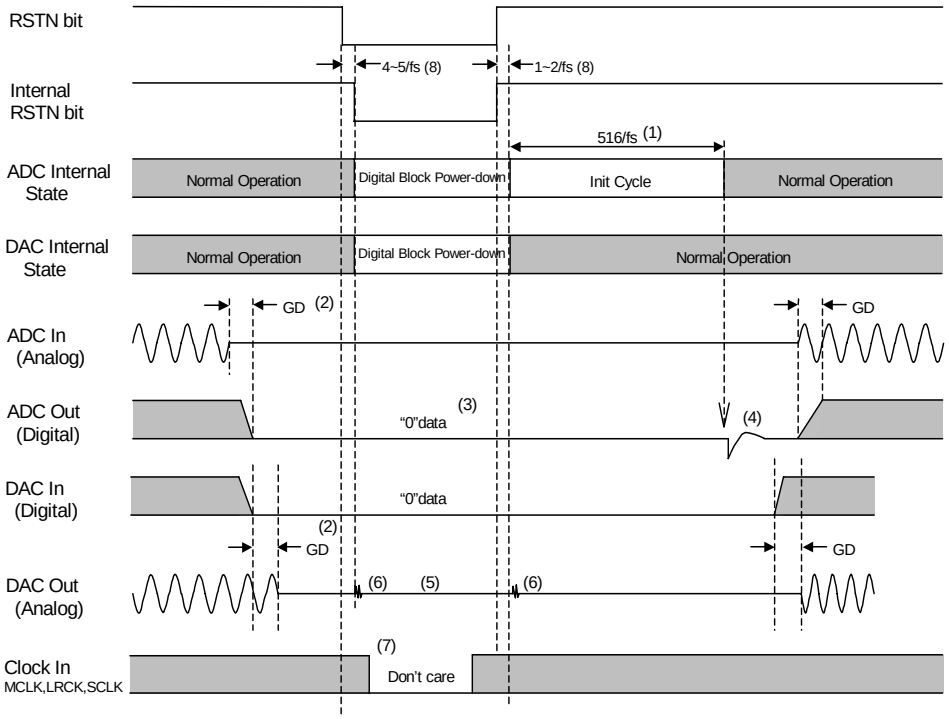


Notes:
(1) The analog part of ADC is initialized after exiting the power-down state.
(2) The analog part of DAC is initialized after exiting the power-down state.
(3) Digital output corresponding to analog input and analog output corresponding to digital input have the group delay (GD).
(4) ADC output is "0" data at the power-down state.
(5) Click noise occurs at the end of initialization of the analog part. Please mute the digital output externally if the click noise influences system application.
(6) Click noise occurs at the rising/falling edge of PDN and at 512/fs after the rising edge of PDN.
(7) When the external clocks (MCLKA (MCLKB), BICKA (BICKB), and LRCKA (LRCKB)) are stopped, the AK4682 must be in the power-down mode.
(8) Please mute the analog output externally if the click noise (6) influences system application.

Figure 12. Power-down/up sequence example

■ Reset Function

When RSTN bit = "0", ADC and DACs are powered-down but the internal register are not initialized. The DAC outputs go to AVDD2 voltage and SDTOB pins go to "L". Because some click noise occurs, the analog output should muted externally if the click noise influences system application. The Figure 13 shows the power-up sequence.



Notes:

(1) The analog part of ADC is initialized after exiting the reset state.

(2) Digital output corresponding to analog input and analog output corresponding to digital input have the group delay (GD).

(3) ADC output is "0" data at the power-down state.

(4) Click noise occurs when the internal RSTN bit becomes "1". Please mute the digital output externally if the click noise influences system application.

(5) When RSTN bit = "0", the analog outputs go to AVDD2 voltage.

(6) Click noise occurs at 4~5/fs after RSTN bit becomes "0", and occurs at 1~2/fs after RSTN bit becomes "1". This noise is output even if "0" data is input.

(7) The external clocks (MCLKA (MCLKB), BICKA (BICKB), LRCKA (LRCKB)) can be stopped in the reset mode. When exiting the reset mode, "1" should be written to RSTN bit after the external clocks (MCLKA (MCLKB), BICKA (BICKB), LRCKA (LRCKB)) are fed.

(8) There is a delay about 4~5/fs from RSTN bit "0" to the internal RSTN bit "0".

Figure 13. Reset sequence example

■ Serial Control Interface

AK4682 supports the fast-mode I^2C-bus system (max: 400kHz).

1. Data transfer

All commands are preceded by a START condition. After the START condition, a slave address is sent. After the AK4682 recognizes the START condition, the device interfaced to the bus waits for the slave address to be transmitted over the SDA line. If the transmitted slave address matches an address for one of the devices, the designated slave device pulls the SDA line to LOW (ACKNOWLEDGE). The data transfer is always terminated by a STOP condition generated by the master device.

1-1. Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW except for the START and the STOP condition.

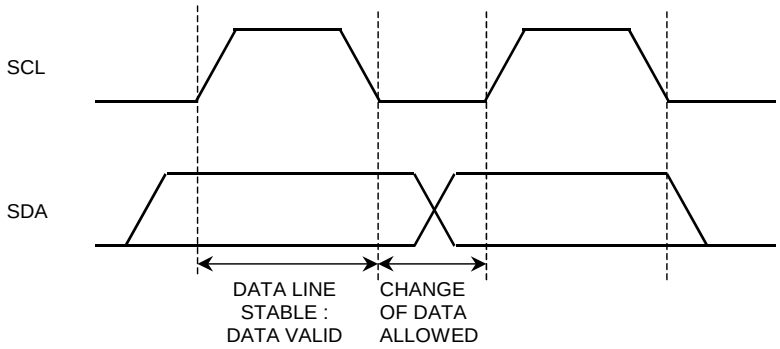


Figure 14. Data transfer

1-2. START and STOP condition

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. All sequences start from the START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. All sequences end by the STOP condition.

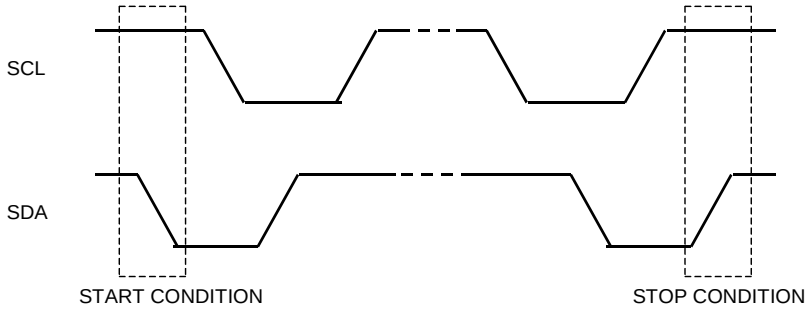


Figure 15. START and STOP conditions

1-3. ACKNOWLEDGE

ACKNOWLEDGE is a software convention used to indicate successful data transfers. The transmitting device will release the SDA line (HIGH) after transmitting eight bits. The receiver must pull down the SDA line during the acknowledge clock pulse so that that it remains stable "L" during "H" period of this clock pulse. The AK4682 will generates an acknowledge after each byte has been received.
In the read mode, the slave, the AK4682 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no STOP condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the STOP condition.

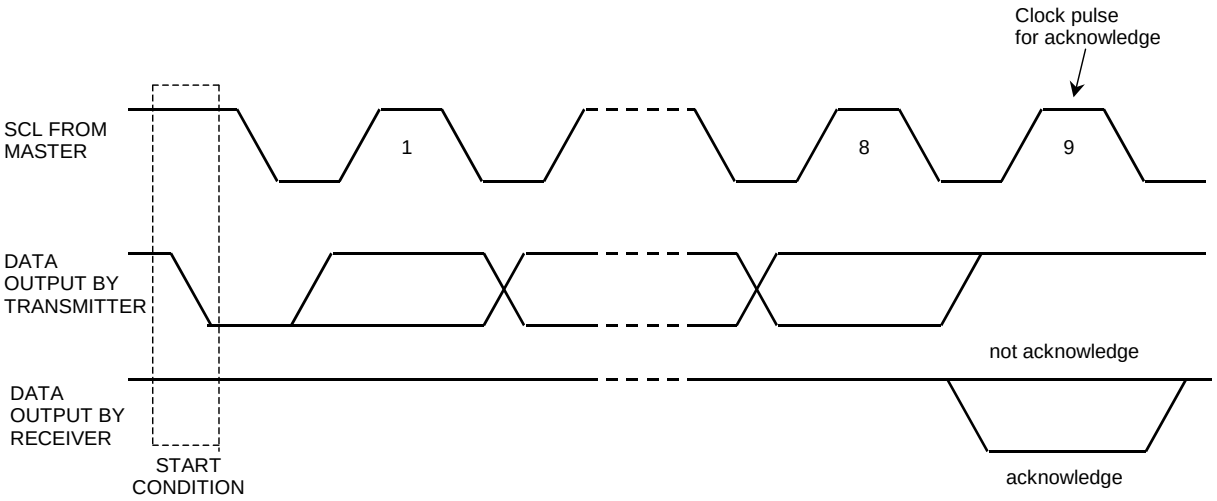


Figure 16. Acknowledge on the I^2C-bus

1-4. FIRST BYTE

The first byte, which includes seven bits of slave address and one bit of R/W bit, is sent after the START condition. If the transmitted slave address matches an address for one of the device, the receiver who has been addressed pulls down the SDA line.
The most significant five bits of the slave address are fixed as "00100". The next two bits are "10". These two bits identify the specific device on the bus. The eighth bit (LSB) of the first byte (R/W bit) defines whether a write or read condition which the master requests. A "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

0	0	1	0	0	1	0	R/W

Figure 17. The First Byte

2. WRITE Operations

Set R/W bit = "0" for the WRITE operation of the AK4682.
After receipt of the start condition and the first byte, the AK4682 generates an acknowledge, and awaits the second byte (register address). The second byte consists of the address for control registers of AK4682. The format is MSB first, and those most significant 3-bits are "Don't care".

*	*	*	A4	A3	A2	A1	A0

(*: Don't care)

Figure 18. The Second Byte

After receipt of the second byte, the AK4682 generates an acknowledge, and awaits the third byte. Those data after the second byte contain control data. The format is MSB first, 8bits.

D7	D6	D5	D4	D3	D2	D1	D0

Figure 19. Byte structure after the second byte

The AK4682 is capable of more than one byte write operation by one sequence.
After receipt of the third byte, the AK4682 generates an acknowledge, and awaits the next data again. The master can transmit more than one words instead of terminating the write cycle after the first data word is transferred. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 0DH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

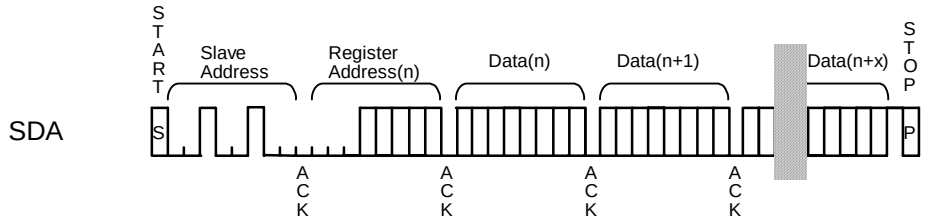


Figure 20. WRITE Operation

3. READ Operations

Set R/W bit = "1" for the READ operation of the AK4682.
After transmission of a data, the master can read next address's data by generating the acknowledge instead of terminating the write cycle after the receipt of the first data word. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 0DH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.
The AK4682 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

3-1. CURRENT ADDRESS READ

The AK4682 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1".
After receipt of the slave address with R/W bit set to "1", the AK4682 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4682 discontinues transmission

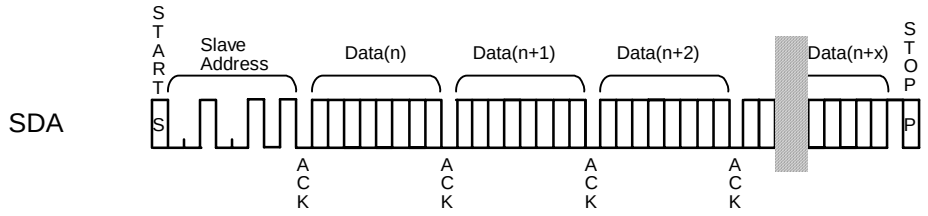


Figure 21. CURRENT ADDRESS READ

3-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation.
The master issues the start condition, slave address(R/W="0") and then the register address to read. After the register address's acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4682 generates an acknowledge, 1byte data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4682 discontinues transmission.

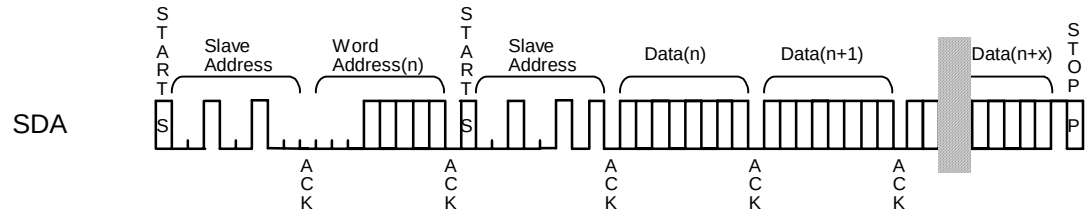


Figure 22. RANDOM READ

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Powerdown 1	0	0	PWANA	0	0	SMAD	SMDA	RSTN
01H	Powerdown 2	0	0	PWDA	PWAD	0	0	0	0
02H	Audio Data Format	0	0	DIFB1	DIFB0	0	TDMA	DIFA1	DIFA0
03H	De-emphasis/ ATT speed	DEM21	DEM20	DEM11	DEM10	DAC2	DAC1	ATSAD	ATSDA
04H	Clock Control	0	ACKS	DFS1	DFS0	0	CKSB1	CKSB0	MSB
05H	Stereo Matrix Control	PL23	PL22	PL21	PL20	PL13	PL12	PL11	PL10
06H	Input Selector Control 1	AOUT13	AOUT12	AOUT11	AOUT10	AIN3	AIN2	AIN1	AIN0
07H	Input Selector Control 2	AOUT33	AOUT32	AOUT31	AOUT30	AOUT23	AOUT22	AOUT21	AOUT20
08H	ADC Lch Volume	IATL7	IATL6	IATL5	IATL4	IATL3	IATL2	IATL1	IATL0
09H	ADC Rch Volume	IATR7	IATR6	IATR5	IATR4	IATR3	IATR2	IATR1	IATR0
0AH	DAC1 Lch Volume	OAT1L7	OAT1L6	OAT1L5	OAT1L4	OAT1L3	OAT1L2	OAT1L1	OAT1L0
0BH	DAC1 Rch Volume	OAT1R7	OAT1R6	OAT1R5	OAT1R4	OAT1R3	OAT1R2	OAT1R1	OAT1R0
0CH	DAC2 Lch Volume	OAT2L7	OAT2L6	OAT2L5	OAT2L4	OAT2L3	OAT2L2	OAT2L1	OAT2L0
0DH	DAC2 Rch Volume	OAT2R7	OAT2R6	OAT2R5	OAT2R4	OAT2R3	OAT2R2	OAT2R1	OAT2R0

Note: For addresses from 0EH to 1FH, data must not be written.
When PDN pin goes to “L”, the registers are initialized to their default values.
When RSTN bit goes to “0”, the internal timing is reset, but registers are not initialized to their default values.
Unused bits must contain a “0” data.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Powerdown 1	0	0	PWANA	0	0	SMAD	SMDA	RSTN
Default		0	0	1	0	0	0	0	1

RSTN: Internal timing reset
0: Reset. Registers are not initialized.
1: Normal operation (default)

SMDA: DAC Soft Mute Enable
0: Normal operation (default)
1: All DAC outputs soft-muted

SMAD: ADC Soft Mute Enable
0: Normal operation (default)
1: ADC outputs soft-muted

PWANA: Power management for 2Vrms analog I/O
0: Power OFF
1: Power ON (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Powerdown 2	0	0	PWDA	PWAD	0	0	0	0
Default		0	0	1	1	0	0	0	0

PWAD: Power-down control of ADC
0: Power-down
1: Normal operation (default)

PWDA: Full-Power-down control of DAC1-2
0: Power-down
1: Normal operation (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Audio Data Format	0	0	DIFB1	DIFB0	0	TDMA	DIFA1	DIFA0
Default		0	0	1	1	0	0	1	1

DIFA1-0, TDMA: Audio format control for PORTA
Refer Table 13, Table 14.
DIFB1-0: Audio format control for PORTB
Refer Table 15.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	De-emphasis/ ATT speed	DEM21	DEM20	DEM11	DEM10	DAC2	DAC1	ATSAD	ATSDA
Default		0	1	0	1	1	0	0	0

ATSDA: DAC digital Attenuator transition time control
ATSAD: ADC digital Attenuator transition time control
Refer Table 18, Table 19.

DAC2-1: DAC Data control
Refer Table 10, Table 11

DEM11-10: DAC1 De-emphasis filter control
DEM21-20: DAC2 De-emphasis filter control
Refer Table 12.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Clock Control	0	ACKS	DFS1	DFS0	0	CKSB1	CKSB0	MSB
Default		0	0	0	0	0	0	0	0

MSB: ADC Master/Slave control
Refer Table 1.

CKSB1-0: ADC Clock control for Master mode.
Refer Table 2.

DFS1-0: DAC Sampling Speed Control
These settings are ignored in Auto Setting Mode. Refer Table 4.

ACKS: DAC Auto Setting Mode
0: Disable, Manual Setting Mode (default)
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKS bit “1”. In this case, the DFS1-0 bits are ignored. When this bit is “0”, DFS1-0 bits set the sampling speed mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Stereo Matrix Control	PL23	PL22	PL21	PL20	PL13	PL12	PL11	PL10
Default		1	0	0	1	1	0	0	1

PL13-10: DAC1 Stereo Matrix Control.
Refer Table 20.

PL23-20: DAC2 Stereo Matrix Control.
Refer Table 21.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Input Selector Control 1	AOUT13	AOUT12	AOUT11	AOUT10	AIN3	AIN2	AIN1	AIN0
Default		0	1	1	0	0	0	0	0

AIN3-0: ADC input selector control
0000: LIN1/RIN1 (default)
0001: LIN2/RIN2
0010: LIN3/RIN3
0011: LIN4/RIN4
0100: LIN5/RIN5
0101: LIN6/RIN6
0110: DAC1L/DAC1R
0111: DAC2L/DAC2R
1xxx: Mute (x: don't care)

AOUT13-10: L/ROUT1 input selector control
0000: LIN1/RIN1
0001: LIN2/RIN2
0010: LIN3/RIN3
0011: LIN4/RIN4
0100: LIN5/RIN5
0101: LIN6/RIN6
0110: DAC1L/DAC1R (default)
0111: DAC2L/DAC2R
1xxx: Mute (x: don't care)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Input Selector Control 2	AOUT33	AOUT32	AOUT31	AOUT30	AOUT23	AOUT22	AOUT21	AOUT20
Default		0	0	0	0	0	1	1	1

AOUT23-20: L/ROUT2 input selector control
0000: LIN1/RIN1
0001: LIN2/RIN2
0010: LIN3/RIN3
0011: LIN4/RIN4
0100: LIN5/RIN5
0101: LIN6/RIN6
0110: DAC1L/DAC1R
0111: DAC2L/DAC2R (default)
1xxx: Mute (x: don't care)

AOUT33-30: L/ROUT3 input selector control
0000: LIN1/RIN1 (default)
0001: LIN2/RIN2
0010: LIN3/RIN3
0011: LIN4/RIN4
0100: LIN5/RIN5
0101: LIN6/RIN6
0110: DAC1L/DAC1R
0111: DAC2L/DAC2R
1xxx: Mute (x: don't care)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	ADC Lch Volume	IATL7	IATL6	IATL5	IATL4	IATL3	IATL2	IATL1	IATL0
09H	ADC Rch Volume	IATR7	IATR6	IATR5	IATR4	IATR3	IATR2	IATR1	IATR0
Default		0	0	1	1	0	0	0	0

IATL7-0, IATR7-0: ADC Volume level control
Refer Table 16.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	DAC1 Lch Volume	OAT1L7	OAT1L6	OAT1L5	OAT1L4	OAT1L3	OAT1L2	OAT1L1	OAT1L0
0BH	DAC1 Rch Volume	OAT1R7	OAT1R6	OAT1R5	OAT1R4	OAT1R3	OAT1R2	OAT1R1	OAT1R0
0CH	DAC2 Lch Volume	OAT2L7	OAT2L6	OAT2L5	OAT2L4	OAT2L3	OAT2L2	OAT2L1	OAT2L0
0DH	DAC2 Rch Volume	OAT2R7	OAT2R6	OAT2R5	OAT2R4	OAT2R3	OAT2R2	OAT2R1	OAT2R0
Default		0	0	0	1	1	0	0	0

OAT1L7-0, OAT1R7-0, OAT2L7-0, OAT2R7-0: DAC Volume level control
Refer Table 17.

SYSTEM DESIGN

Figure 23 shows the system connection diagram. The evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

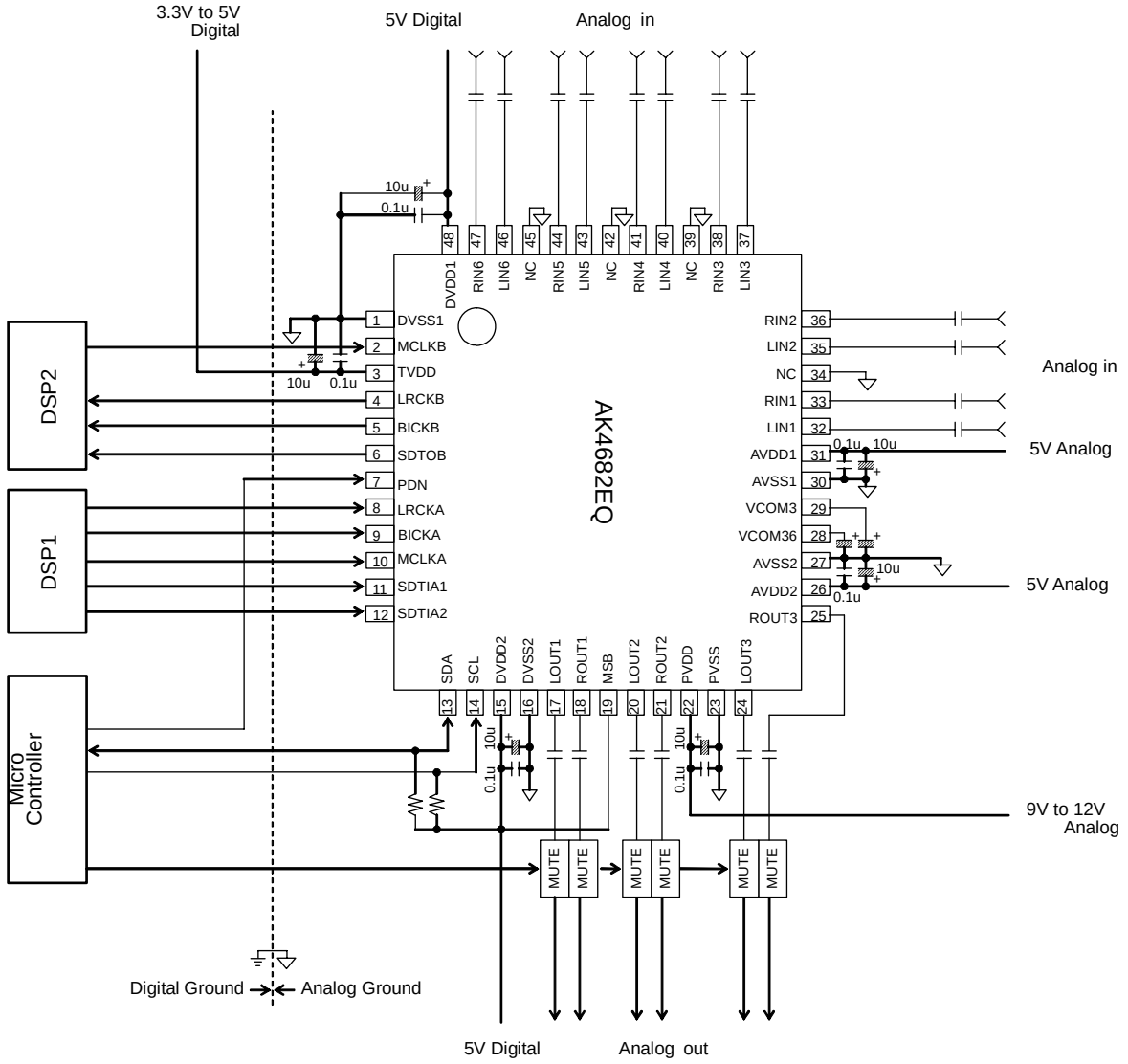


Figure 23. Typical Connection Diagram (Master Mode)

Notes:

- DVSS1, AVSS1, DVSS2, AVSS2 and PVSS must be connected the same analog ground plane.

1. Grounding and Power Supply Decoupling

The AK4682 requires careful attention to power supply and grounding arrangements. AVDD1, AVDD2, DVDD1, DVDD2, TVDD and PVDD are usually supplied from analog supply in system. If AVDD1, AVDD2, DVDD1, DVDD2 and TVDD are supplied separately, the power up sequence is not critical. **AVSS1, DVSS1, AVSS2, DVSS2 and PVSS of the AK4682 must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4682 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference Inputs

The voltage of AVDD1 sets the ADC input range, AVDD2 sets the DAC analog output range. VCOM3 and VCOM36 are signal grounds of this chip. An electrolytic capacitor 10μF parallel with a 0.1μF ceramic capacitor attached between these VCOM pins and AVSS1 pin eliminates the effects of high frequency noise. No load current may be drawn from these VCOM pins. All signals, especially clocks, should be kept away from the AVDD1, AVDD2, VCOM3 and VCOM36 pins in order to avoid unwanted coupling into the AK4682.

3. Analog Inputs

The AK4682 receives the analog input through the single-ended Pre-amp using external resistors. The input range is 2.2 x AVDD1/5 Vrms (typ. fs=48kHz) at each analog input pins. Each input pins are biased internally. The ADC output data format is 2's complement. The internal digital HPF removes the DC offset.

The AK4682 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK4682 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

4. Analog Outputs

The analog outputs are also single-ended and centered on around the AVDD2 voltage. The output signal range scales with the supply voltage and nominally 2 x AVDD2/5 Vrms at each analog output pins. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal output is AVDD2 voltage for 000000H(@24bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband.

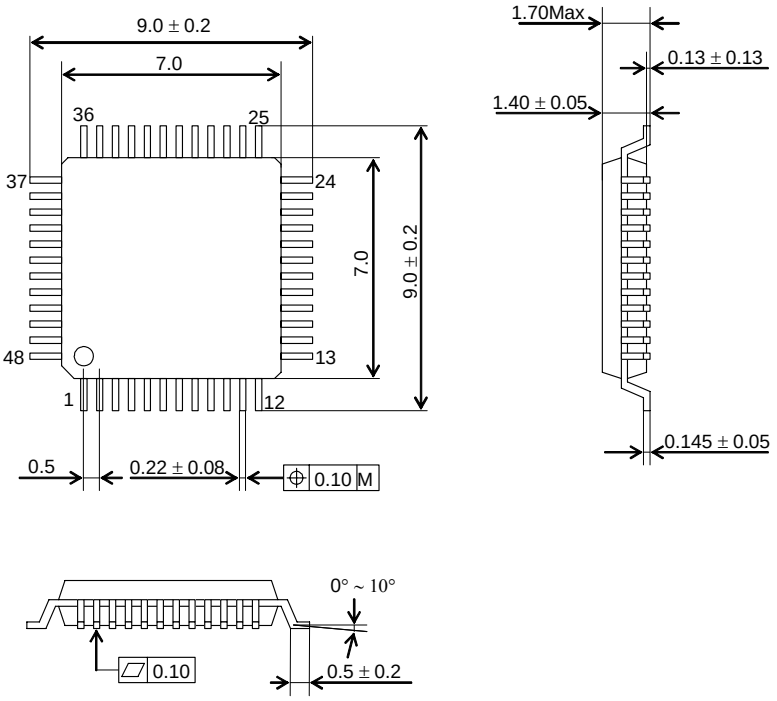
DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets a few mV.

5. Attention to the PCB Wiring

Attention should be given to avoid coupling with other signals on each analog input/output pins. Unused input pins among LIN1-6 and RIN1-6 pins should be left open.

PACKAGE

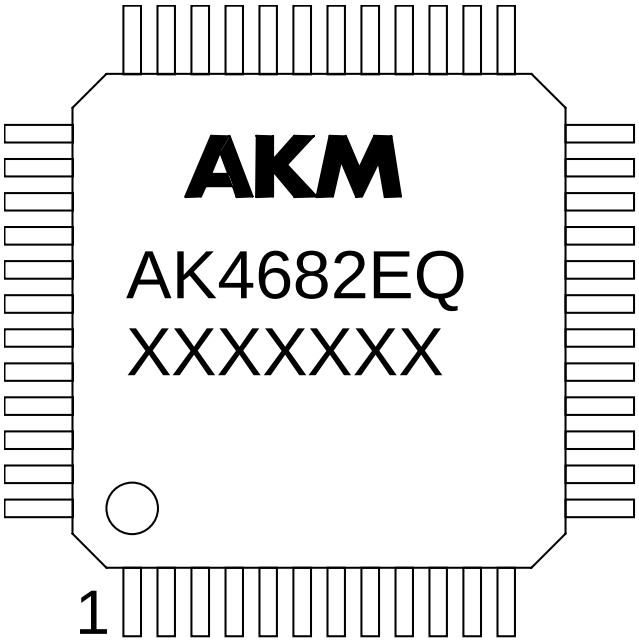
48pin LQFP(Unit: mm)



■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Asahi Kasei Logo
3) Marking Code: AK4682EQ
4) Date Code: XXXXXXX (7 digits)

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
07/04/24	00	First Edition		
07/07/02	01	Error Correct	12	Audio Interface Timing (Normal and TDM128 mode) were changed.

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